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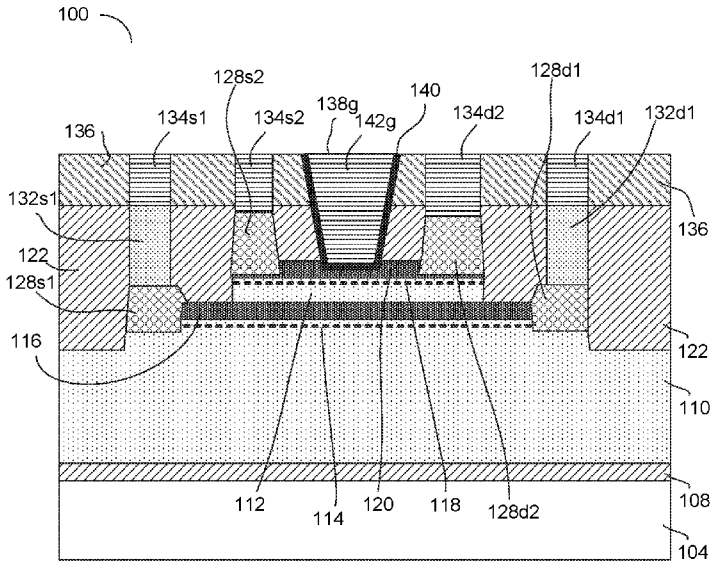


Fig. 1

(57) Abstract: A variable capacitance III-N device having multiple two-dimensional electron gas (2DEG) layers are described. In some embodiments, the device comprises a first source and a first drain; a first polarization layer adjacent to the first source and the first drain; a first channel layer coupled to the first source and the first drain and adjacent to the first polarization layer, the first channel layer comprising a first 2DEG region; a second source and a second drain; a second polarization layer adjacent to the second source and the second drain; and a second channel layer coupled to the second source and the second drain and adjacent to the second polarization layer, the second channel layer comprising a second 2DEG region, wherein the second channel layer is over the first polarization layer.

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VARIABLE CAPACITANCE DEVICE WITH MULTIPLE TWO-DIMENSIONAL ELECTRON GAS (2DEG) LAYERS

BACKGROUND

[0001] In various computing system applications, a variable capacitance device (e.g., a varactor) may be used. In a basic, cost optimized Gallium nitride (GaN) technology based device, there may not be a p-doping device available (e.g., due to relative complexity of activating p dopants in GaN). This may lead to a lack of a pn diode in GaN technology based devices. However, in some examples, pn junctions may be used in varactors, e.g., where the capacitance may be modulated by applying a reverse bias to a p-n-depletion region. Accordingly, GaN devices may not be usually used to form varactors.

BRIEF DESCRIPTION OF THE DRAWINGS

[0002] The material described herein is illustrated by way of example and not by way of limitation in the accompanying figures. For simplicity and clarity of illustration, elements illustrated in the figures are not necessarily drawn to scale. For example, the dimensions of some elements may be exaggerated relative to other elements for clarity. Further, where considered appropriate, reference labels have been repeated among the figures to indicate corresponding or analogous elements. In the figures:

[0003] Fig. 1 is a cross-sectional view of a variable capacitance GaN device with multiple stacked two-dimensional electron gas (2DEG) regions, in accordance with some embodiment.

[0004] Fig. 2 is a flow diagram illustrating methods of forming the device structure of Fig. 1, in accordance with some embodiments.

[0005] Figs. 3A-3P are cross-sectional views of the device of Fig. 1 evolving as selected operations in the methods of Fig. 2 are performed, in accordance with some embodiments.

[0006] Fig. 4 illustrates an example operation of the device of Fig. 1, in accordance with some embodiments.

[0007] Fig. 5 illustrates a system in which a mobile computing platform and/or a data server machine employs an IC including at least one GaN device with variable capacitance, in accordance with some embodiments.

[0008] Fig. 6 is a functional block diagram of a computing device, arranged in accordance with at least some implementations of the present disclosure.

DETAILED DESCRIPTION

[0009] One or more embodiments are described with reference to the enclosed figures. While specific configurations and arrangements are depicted and discussed in detail, it should be understood that this is done for illustrative purposes only. Persons skilled in the relevant art will recognize that other configurations and arrangements are possible without departing from the spirit and scope of the description. It will be apparent to those skilled in the relevant art that techniques and/or arrangements described herein may be employed in a variety of other systems and applications other than what is described in detail herein.

[0010] Reference is made in the following detailed description to the accompanying drawings, which form a part hereof and illustrate exemplary embodiments. Further, it is to be understood that other embodiments may be utilized and structural and/or logical changes may be made without departing from the scope of claimed subject matter. It should also be noted that directions and references, for example, up, down, top, bottom, and so on, may be used merely to facilitate the description of features in the drawings. Therefore, the following detailed description is not to be taken in a limiting sense and the scope of claimed subject matter is defined solely by the appended claims and their equivalents.

[0011] In the following description, numerous details are set forth. However, it will be apparent to one skilled in the art, that the present invention may be practiced without these specific details. In some instances, well-known methods and devices are shown in block diagram form, rather than in detail, to avoid obscuring the present invention. Reference throughout this specification to “an embodiment” or “one embodiment” or “some embodiments” means that a particular feature, structure, function, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention. Thus, the appearances of the phrase “in an embodiment” or “in one embodiment” or “some embodiments” in various places throughout this specification are not necessarily referring to the same embodiment of the invention. Furthermore, the particular features, structures, functions, or characteristics may be combined in any suitable manner in one or more embodiments. For example, a first embodiment

may be combined with a second embodiment anywhere the particular features, structures, functions, or characteristics associated with the two embodiments are not mutually exclusive.

[0012] As used in the description and the appended claims, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will also be understood that the term "and/or" as used herein refers to and encompasses any and all possible combinations of one or more of the associated listed items.

[0013] The terms "coupled" and "connected," along with their derivatives, may be used herein to describe functional or structural relationships between components. It should be understood that these terms are not intended as synonyms for each other. Rather, in particular embodiments, "connected" may be used to indicate that two or more elements are in direct physical, optical, or electrical contact with each other. "Coupled" may be used to indicated that two or more elements are in either direct or indirect (with other intervening elements between them) physical or electrical contact with each other, and/or that the two or more elements co-operate or interact with each other (e.g., as in a cause an effect relationship).

[0014] The terms "over," "under," "between," and "on" as used herein refer to a relative position of one component or material with respect to other components or materials where such physical relationships are noteworthy. For example, in the context of materials, one material or materials disposed over or under another may be directly in contact or may have one or more intervening materials. Moreover, one material disposed between two materials may be directly in contact with the two layers or may have one or more intervening layers. In contrast, a first material "on" a second material is in direct contact with that second material/material. Similar distinctions are to be made in the context of component assemblies.

[0015] As used throughout this description, and in the claims, a list of items joined by the term "at least one of" or "one or more of" can mean any combination of the listed terms. For example, the phrase "at least one of A, B or C" can mean A; B; C; A and B; A and C; B and C; or A, B and C.

[0016] A variable capacitance GaN device with multiple stacked two-dimensional electron gas (2DEG) regions are described herein. For example, the device may comprise a first GaN channel layer and an adjacent first polarization layer, resulting in a formation of a first 2DEG region within the first channel layer near the heterojunction. The device may also comprise a second GaN channel layer and an adjacent second polarization layer, resulting in a

formation of a second 2DEG region within the second channel layer near the heterojunction. Each 2DEG region may have corresponding source and drain. A gate stack may be recessed on the second polarization layer. A capacitance between the gate stack and the first 2DEG region, and a capacitance between the gate stack and the second 2DEG region may be fine-tuned, thereby providing a variable capacitance device.

[0017] Fig. 1 is a cross-sectional view of a variable capacitance GaN device 100 (e.g., also referred to as a device 100, or as a varactor 100) with multiple stacked 2DEG regions, in accordance with some embodiments. The device 100 may be formed over a substrate 104. In an example, the substrate 104 may be substantially monocrystalline with a predetermined crystal orientation. Substrate 104 may comprise a variety of materials, including, but not limited to, GaN, SiC, sapphire, and/or silicon. Silicon may be advantageous for monolithic integration of the device 100 with conventional silicon CMOS and for such embodiments, the substrate crystallographic orientation may be any of (100), (111), (110). Other crystallographic orientations may also be possible, and a range of miscut (e.g., 4-11°) may be utilized for better lattice matching between substrate 104 and an overlying semiconductor buffer 108.

[0018] The semiconductor buffer 108 formed on the substrate 104 may have a wide variety of compositions and structures designed to confine lattice defects. In some embodiments, semiconductor buffer 105 may be a III-N layer interfacing with the non-III-N substrate 104. In an example, the semiconductor buffer 108 may comprise one or more GaN material layers, one or more AlN material layers, and/or the like.

[0019] In some embodiments, the device 100 may comprise a channel layer 110, which may be a first channel layer of the device 100. The channel layer 110 may be formed on the semiconductor buffer 108. In some embodiments, the channel layer 110 may comprises GaN. In some embodiments, the channel layer 110 may be binary alloy GaN, and may be substantially undoped to have a carrier mobility of about 1100 cm2/V*s, or more (or less). In some embodiments, the channel layer 110 may have a thickness of at least about 1 micrometer and no more than about 2 micrometers. In some embodiments, the channel layer 110 may have a thickness of at least about 0.5 micrometer and no more than about 2 micrometers.

[0020] A first source 128s1 and a first drain 128d1 may be formed adjacent to, and coupled to, the channel layer 110. The source 128s1 and drain 128d1 may be impurity doped semiconductor regions (e.g., with Si for n-type). The impurity doped semiconductor regions

comprising the source 128s1 and drain 128d1 may be, for example, low bandgap group III-N material, such as $In_xGa_{1-x}N$ and/or InN, for low resistance, or may be simply n-type (e.g., Si-doped) GaN, where *x* may range from 0 to 0.2. In an example, the impurity doping level may be any typically employed for an N+ source/drain of a GaN device. For example, the source 128s1 and the drain 128d1 may have a dopant concentration of at least 1e18 atoms/cm3. For some embodiments, the raised doped N+ material may be substantially monocrystalline. Dislocation density within the source 128s1 and the drain 128d1 may be between 10^9 cm-2 and 10^{12} cm-2, for example. Material having many orders of magnitude higher dislocation density is also possible, and in some embodiments source and drain regions 128s1 and 128d1 may be polycrystalline. Source and drain semiconductor may be of any composition known to be suitable for the device layer material compositions.

[0021] In some embodiments, the source 128s1 may be coupled to source metal contacts 132s1 and 134s1, and the drain 128d1 may be coupled to drain metal contacts 132d1 and 134d1. The metal contacts 132s1, 134s1, 132d1, and 134d1 may be of an ohmic metal, such as, but not limited to, a Ti/Au alloy.

[0022] In some embodiments, a polarization layer 116 may be formed over and adjacent to the channel layer 110. The polarization layer 116 may be coupled between the source 128s1 and the drain 128d1.

[0023] In some embodiments, the polarization layer 116 may include one or more polarization material, e.g., InAlGaN, AlN, AlInN, AlGaN, InGaN. For example, the polarization layer 116 may comprise $In_xAl_yGa_{1-x-y}N$, with *x* between 0% and 20%, and *y* between 10% and 100%. Of particular utility may be $In_xAl_yGa_{1-x-y}N$ with composition, for example, of x being about 17% and y being about 83%, where the polarization layer may be lattice matched to GaN. Such an embodiment may prevent formation of stress (stress that may culminate from lattice mismatch between the polarization layer 116 and the GaN channel layer 110), e.g., as too much stress may induce formation of defects.

[0024] In some embodiments, the polarization layer 116 may create a two-dimensional electron gas (2DEG) region 114 within the channel layer 110, near the heterojunction of the polarization layer 116 and the channel layer 110. In some embodiments, the 2DEG region 114 may exist near the interface of the channel layer 110 and the polarization layer 116, e.g.,

extending about 3-4 nm into the channel layer 110. In an example, the source 128s1 and the drain 128d1 may be electrically coupled through the 2DEG region 114.

[0025] In some embodiments, the device 100 may further comprise a channel layer 112, which may be formed over the polarization layer 116 (e.g., formed on the polarization layer 116). The channel layer 112 may be a second channel layer of the device 100. In some embodiments, another polarization layer 120 may be formed over and adjacent to the channel layer 112.

[0026] In some embodiments, the channel layer 112 may comprises GaN. In some embodiments, the channel layer 112 may be binary alloy GaN, and may be substantially undoped to have a carrier mobility of about 1100 cm2/V*s, or more (or less). In some embodiments, the channel layer 112 may have a thickness of at least about 10 nanometer (nm) and no more than 50 nm. Thus, the channel layer 110 may be substantially thicker than the channel layer 112.

[0027] In some embodiments, the polarization layer 120 may include one or more polarization material, e.g., InAlGaN, AlN, AlInN, AlGaN, InGaN. For example, the polarization layer 120 may comprise $In_xAl_yGa_{1-x-y}N$, with *x* between 0% and 20%, and *y* between 10% and 100%. Of particular utility may be $In_xAl_yGa_{1-x-y}N$ with composition, for example, of x being about 17% and y being about 83%, where the polarization layer may be lattice matched to GaN.

[0028] In some embodiments, the polarization layer 116 may have a thickness of at least about 10 nm and no more than 20 nm, and the polarization layer 120 may have a thickness of at least about 5 nm and no more than about 10 nm. In some embodiments, the polarization layer 116 may be thicker than the polarization layer 120. In some embodiments, the polarization layer 116 may have higher concentration of Al and In, e.g., compared to the respective concentration of Al and In of the polarization layer 120.

[0029] In some embodiments, the polarization layer 120 may create a 2DEG region 118 within the channel layer 112, near the heterojunction of the polarization layer 120 and the channel layer 112.

[0030] The polarization layer 120 may be coupled between a second source 128s2 and a second drain 128d2. The source 128s2 and drain 128d2 may be impurity doped semiconductor regions (e.g., with Si for n-type). The impurity doped semiconductor regions comprising the source 128s2 and drain 128d2 may be, for example, low bandgap group III-N material, such as $In_xGa_{1-x}N$ and/or InN, for low resistance, or may be simply n-type (e.g., Si-doped) GaN. In an

example, the impurity doping level may be any typically employed for an N+ source/drain of a GaN device. For example, the source 128s2 and the drain 128d2 may have a dopant concentration of at least 1e18 atoms/cm3. For some embodiments, the raised doped N+ material may be substantially monocrystalline. Dislocation density within the source 128s2 and the drain 128d2 may be between 109 cm-2 and 1012 cm-2, for example. Material having many orders of magnitude higher dislocation density is also possible, and in some embodiments the source 128s2 and the drain 128d2 may be polycrystalline. Source and drain semiconductor may be of any composition known to be suitable for the device layer material compositions.

[0031] In an example, the source 128s2 and the drain 128d2 may not be connected or attached to the 2DEG region 118, e.g., due to the structure of the source 128s2 and the drain 128d2, as illustrated in Fig. 1. For example, the source 128s2 and the drain 128d2 may be separated from the 2DEG region 118 by sections of the polarization layer 120.

[0032] In some embodiments, the source 128s2 may be coupled to source metal contact 134s2, and the drain 128d2 may be coupled to drain metal contact 134d2. The metal contacts 134s2 and 134d2 may be of an ohmic metal, such as, but not limited to, a Ti/Au alloy.

[0033] Various embodiments discussed herein assume an ohmic source and drain. However, in some other embodiments, the source/drain 128s2, 128d1, 128s2, 128d2 may comprise schottky contacts, as would be readily understood by those skilled in the art, based on the contents of this disclosure.

[0034] In some embodiments, the device 100 may further comprise a gate stack 138g recessed into the polarization layer 120, e.g., to tune a threshold voltage (Vt) of the device 100. The gate stack 138g may include a gate electrode 142g that may be any metal or semiconductor known to have suitable conductivity and work function. In an example, the gate electrode 142g may be a work function metal that may be a mid-gap metal, such as, but not limited to TiN, or slightly p-type, such as, but not limited to a Ni/Au alloy. The gate electrode 142g may electrostatically couple to the channel layer 112 through the field effect. The gate stack 138g may further include a gate dielectric 140 (symbolically illustrated using a thick line), such as any high-k or conventional dielectric material known to be suitable for III-N FETs or III-N devices. For example, the gate dielectric 140 may be a material that has a bulk dielectric constant of 7, or more. In some embodiments, gate dielectric 140 may be Al2O3. Other dielectric materials, such as, but not limited to group III-ON, and other high-k dielectrics such as Gd2O3, HfO2, Ta2O5,

ZrO2, high-K metal silicates such as HfOSiO, TaSiyOx, AlSiO, and other high-K oxynitrides such as HfON, AlON, ZrSiON, HfSiON may also be suitable as gate dielectric 140.

[0035] In some embodiments, the device 100 may also comprise isolation dielectric material 122 and 136, which may comprise low k dielectric material (although only some instances of the isolation dielectric material are labeled in Fig. 1).

[0036] Although two 2DEG regions are illustrated to be formed in the device 100, multiple (e.g., three, four, or even higher) such 2DEG regions may also be formed in the device 100. For example, each such 2DEG region may be associated with a corresponding channel layer and a corresponding polarization layer.

[0037] Although Fig. 1 and various other figures of this disclosure illustrate multiple 2DEG regions (e.g., regions 114 and 118), in some embodiments (and although not shown in the figures), instead of (or in addition to) forming the multiple 2DEG regions, multiple 2-dimensional hole gas (2DHG) regions may also be formed. For example, a first 2DHG region may replace the 2DEG region 114, and a second 2DHG region may replace the 2DEG region 118. For example, in such embodiments, appropriate material for the channel layers 110 and/or 112, and/or appropriate material for the polarization layers 116 and/or 120 may be used for creation of the two 2DHG regions in the channel layers 110 and/or 112. For the case with 2DHG, the crystal orientation of channel layers 110 and 112, and the polarization layers 116 and 120, may be inverted compared to that of the case with 2DEG. The crystal inversion may be accomplished by known epitaxial GaN growth techniques or by flipping the crystal upside down followed by a layer transfer. Thus, for example, one or more 2DEG regions illustrated in one or more figures of this disclosure may be replaced by one or more corresponding 2DHG regions.

[0038] Fig. 2 is a flow diagram illustrating methods 200 of forming the device structure 100 of Fig. 1, in accordance with some embodiments. Figs. 3A-3P are cross-sectional views of the device 100 evolving as selected operations in the methods 200 are performed, in accordance with some embodiments.

[0039] Methods 201 of Fig. 2 begin at operation 204, where an epitaxial growth of multiple 2DEG stack is received. An example of such a stack is illustrated in Fig. 3A, which may comprise the substrate 104, the semiconductor buffer 108 formed on the substrate 104, the channel layer 110 formed on the semiconductor buffer 108, the polarization layer 116 formed on the channel layer 110, the channel layer 112 formed on the polarization layer 116, and the

polarization layer 120 formed on the channel layer 112. Also illustrated in Fig. 3A are the two 2DEG regions 114 and 118, which may be respectively formed on the channel layers 110 and 112.

[0040] Referring again to Fig. 2, the methods 200 may continue at operation 208, where a first isolation etch may be performed, followed by isolation dielectric fill and planarization, as illustrated in Fig. 3B. For example, as illustrated in Fig. 3B, an etch may be performed to selectively remove sections of the channel layer 110, the polarization layer 116, the channel layer 112, and the polarization layer 120. Any appropriate etching techniques may be employed to selectively remove these layers, such as dry etch, wet chemical etch, etc. A top surface of the polarization layer 120, including the etched sections of the various layers, may be filled with isolation dielectric material 122, which may then be planarized, as illustrated in Fig. 3B.

[0041] Referring again to Fig. 2, the methods 200 may continue at operation 212, where a second isolation etch may be performed, as illustrated in Fig. 3C. For example, as illustrated in Fig. 3C, trenches 302 may be formed by selectively etching sections of the channel layer 110, the polarization layer 116, the channel layer 112, the polarization layer 120, and the isolation dielectric material 122. Also, at operation 212, the second isolation etch may be followed by isolation dielectric fill and planarization, as illustrated in Fig. 3D. For example, as illustrated in Fig. 3D, the trenches 302 may be filled with isolation dielectric material 122, which may then be planarized.

[0042] Referring again to Fig. 2, the methods 200 may continue at operation 216, where a third isolation etch may be performed, as illustrated in Fig. 3E. For example, as illustrated in Fig. 3E, trenches 304 may be formed by selectively etching sections of the channel layer 112, the polarization layer 120, and the isolation dielectric material 122. In some embodiments, the third isolation etch may be selectively performed (e.g., using selective etchant), e.g., such that the polarization layer 116 is not etched.

[0043] For example, the etching may be performed in two steps: a time etch to etch the isolation dielectric material 122, the polarization layer 120, and the channel layer 112; and a selective etch that may etch remaining portion of the channel layer 112, without etching the polarization layer 120. Any appropriate etchant for the selective etch may be used.

[0044] Also, at operation 216, the third isolation etch may be followed by isolation dielectric fill and planarization, as illustrated in Fig. 3F. For example, as illustrated in Fig. 3F,

the trenches 304 may be filled with the isolation dielectric material 122, which may then be planarized.

[0045] Referring again to Fig. 2, the methods 200 may continue at operation 220, where regrowth trench formation may be performed, as illustrated in Fig. 3G. For example, trenches 306a, 306b, 306c, and 306d may be formed by selectively etching the isolation dielectric material 122, e.g., for formation of source and drain regions.

[0046] Referring again to Fig. 2, the methods 200 may continue at operation 224, where a first source 128s1, a second source 128s2, a first drain 128d1, and a second drain 128d2 (e.g., see Fig. 1) may be respectively formed on the trenches 306a, 306b, 306c, and 306d, as illustrated in Fig. 3H. Example properties of the source and drain have been discussed with respect to Fig. 1.

[0047] Referring again to Fig. 2, the methods 200 may continue at operation 228, where isolation dielectric fill and planarization may be performed, as illustrated in Fig. 3I. For example, the remaining portions of trenches 306a, ..., 306d (e.g., above the sources 128s1 and 128s2, and drains 128d1 and 128d2) may be overfilled with the isolation dielectric material 122, and the isolation dielectric material 122 may be planarized, as illustrated in Fig. 3I.

[0048] Referring again to Fig. 2, the methods 200 may continue at operation 232, where trenches 308a and 308b may be formed (e.g., above the source 128s1 and drain 128d1), e.g., selectively etching the isolation dielectric material 122, as illustrated in Fig. 3J. Also at 232, contacts for source 128s1 and drain 128d1 may be formed within the tranches 308a and 308b, as illustrated in Fig. 3K. For example, contact 132s1 and contact 132d1 may be respectively formed above the source 128s1 and drain 128d1. For example, the contacts 132s1 and 132d1 may be formed by metal fill in the respectively trenches 308a and 308b, followed by polishing of the metal.

[0049] Referring again to Fig. 2, the methods 200 may continue at operation 236, where interlayer dielectric material 136 may be deposited over the isolation dielectric material 122, and polished, as illustrated in Fig. 3L.

[0050] Referring again to Fig. 2, the methods 200 may continue at operation 240, where trenches 310a, 310b, 310c, and 310d may be formed on the dielectric material 136, e.g., respectively above the source contact 132s1, the source 128s2, the drain contact 132d1, and the drain 128d2, as illustrated in Fig. 3M. Also at 240, metal contacts 134s1, 134s2, 134d1, and

134d2 may be formed within the trenches 310a, 310b, 310c, and 310d, respectively, as illustrated in Fig. 3N. For example, the contacts 134s1, 134s2, 134d1, and 134d2 may be formed by metal fill in the respectively trenches, followed by polishing of the metal.

[0051] Thus, as illustrated in Fig. 3N (and also in Fig. 1), contacts 132s1 and 134s1, in combination, form a source contact for the source 128s1; contacts 132d1 and 134d1, in combination, form a drain contact for the drain 128d1; contact 134s2 forms a source contact for the source 128s2; and contact 134d2 forms a drain contact for the drain 128d2.

[0052] Referring again to Fig. 2, the methods 200 may continue at operation 244, where a gate trench 314 may be formed above the polarization layer 120, as illustrated in Fig. 3O. For example, the gate trench 314 may be recessed into the polarization layer 120, and may be formed by selectively removing the dielectric material 136 and 122, and the polarization layer 120. At 248, the gate stack 138g may be formed in the gate trench 314, as illustrated in Fig. 3P. As discussed with respect to Fig. 1, the gate stack 138g may comprise gate electrode 142g and may optionally comprise gate dielectric 140. The structure of the device 100 in Fig. 3P may be similar to the device 100 in Fig. 1, thereby completing the process of forming the device 100.

[0053] Fig. 4 illustrates an example operation of the device 100 of Fig. 1, in accordance with some embodiments. In Fig. 4, only some of the components of the device 100 is illustrated schematically. For example, Fig. 4 illustrates the source regions 128s1 and 128s2, the drain regions 128d1 and 128d2, the gate electrode 142g, the 2DEG region 114 between the source 128s1 and drain 128d1, and the 2DEG region 118 between the source 128s2 and drain 128d2. In some embodiments, when appropriate voltage is supplied to the gate electrode 142g, a capacitance may be induced between the gate electrode 142g and the 2DEG region 114, represented as C410 (also referred to as bottom capacitance). Similarly, in some embodiments, when appropriate voltage is supplied to the gate electrode 142g, a capacitance may be induced between the gate electrode 142g and the 2DEG region 118, represented as C408 (also referred to as top capacitance). The capacitance of the capacitors 408 and 410 may be fine-tuned, e.g., by tuning the voltage of the gate electrode 142g, and/or the voltages of the source and drain regions 128s1, 128s2, 128d1, 128d2.

[0054] In some embodiments, two of the source and drain regions 128s1, 128s2, 128d1, 128d2 may be electrically coupled to form a first node, and another two of the source and drain regions 128s1, 128s2, 128d1, 128d2 may be electrically coupled to form a second node (although

such couplings are not illustrated in Fig. 4). The voltages to various source and drain regions and the gate electrode 142g may be varied to tune a capacitance between such first and second nodes, thereby forming a variable capacitance device.

[0055] Merely as an example, the source 128s1 and the drain 128d1 may be coupled (e.g., connected by an external connection not illustrated in Fig. 4) to form a first node; and the source 128s2 and the drain 128d2 may be coupled (e.g., connected by another external connection not illustrated in Fig. 4) to form a second node. In such an example, the capacitors 408 and 410 may be coupled in series between the two nodes. In some embodiments, voltages to the first node, the second node, and/or the gate electrode 142g may be controlled to tune a capacitance between the first and second nodes, thereby forming a variable capacitance device.

[0056] Fig. 5 illustrates a system 1500 in which a mobile computing platform 1505 and/or a data server machine 1506 employs an IC including at least one GaN device with variable capacitance, in accordance with some embodiments. The server machine 1506 may be any commercial server, for example including any number of high-performance computing platforms disposed within a rack and networked together for electronic data processing, which in the exemplary embodiment includes a packaged monolithic IC 1550. The mobile computing platform 1505 may be any portable device configured for each of electronic data display, electronic data processing, wireless electronic data transmission, or the like. For example, the mobile computing platform 1505 may be any of a tablet, a smart phone, laptop computer, etc., and may include a display screen (e.g., a capacitive, inductive, resistive, or optical touchscreen), a chip-level or package-level integrated system 1510, and a battery 1515.

[0057] Whether disposed within the integrated system 1510 illustrated in the expanded view 1520, or as a stand-alone packaged chip within the server machine 1506, the IC 1550 includes at least one variable capacitance GaN device, for example as describe elsewhere herein. The IC 1550 may be further coupled to a board, a substrate, or an interposer 1560 along with a power management integrated circuit (PMIC). Functionally, PMIC 1530 may perform battery power regulation, DC-to-DC conversion, etc., and so has an input coupled to battery 1515 and with an output providing a current supply to other functional modules.

[0058] IC 1550, in some embodiments, includes RF (wireless) integrated circuitry (RFIC) further including a wideband RF (wireless) transmitter and/or receiver (TX/RX including a digital baseband and an analog front end module comprising a power amplifier on a transmit

path and a low noise amplifier on a receive path). The RFIC includes at least one III-N HFET adjacent to a substrate tap, for example as describe elsewhere herein. The RFIC has an output coupled to an antenna (not shown) to implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond.

[0059] Fig. 6 is a functional block diagram of a computing device 1600, arranged in accordance with at least some implementations of the present disclosure. Computing device 1600 may be found inside platform 1505 or server machine 1506, for example. Device 1600 further includes a motherboard 1602 hosting a number of components, such as, but not limited to, a processor 1604 (e.g., an applications processor), which may further incorporate at least one variable capacitance GaN device, in accordance with embodiments of the present invention. Processor 1604 may be physically and/or electrically coupled to motherboard 1602. In some examples, processor 1604 includes an integrated circuit die packaged within the processor 1604. In general, the term "processor" or "microprocessor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be further stored in registers and/or memory.

[0060] In various examples, one or more communication chips 1606 may also be physically and/or electrically coupled to the motherboard 1602. In further implementations, communication chips 1606 may be part of processor 1604. Depending on its applications, computing device 1600 may include other components that may or may not be physically and electrically coupled to motherboard 1602. These other components include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), flash memory, a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, touchscreen display, touchscreen controller, battery, audio codec, video codec, power amplifier, global positioning system (GPS) device, compass, accelerometer, gyroscope, speaker, camera, and mass storage device (such as hard disk drive, solid-state drive (SSD), compact disk (CD), digital versatile disk (DVD), and so forth), or the like.

[0061] Communication chips 1606 may enable wireless communications for the transfer of data to and from the computing device 1600. The term "wireless" and its derivatives may be

used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. Communication chips 1606 may implement any of a number of wireless standards or protocols, including but not limited to those described elsewhere herein. As discussed, computing device 1600 may include a plurality of communication chips 1606. For example, a first communication chip may be dedicated to shorter-range wireless communications, such as Wi-Fi and Bluetooth, and a second communication chip may be dedicated to longer-range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

[0062] While certain features set forth herein have been described with reference to various implementations, this description is not intended to be construed in a limiting sense. Hence, various modifications of the implementations described herein, as well as other implementations, which are apparent to persons skilled in the art to which the present disclosure pertains are deemed to lie within the spirit and scope of the present disclosure.

[0063] It will be recognized that the invention is not limited to the embodiments so described, but can be practiced with modification and alteration without departing from the scope of the appended claims. For example the above embodiments may include specific combinations of features as further provided in the following examples.

[0064] Example 1. An apparatus comprising: a first source and a first drain; a first polarization layer adjacent to the first source and the first drain; a first channel layer coupled to the first source and the first drain and adjacent to the first polarization layer, the first channel layer comprising a first two-dimensional electron gas (2DEG) region; a second source and a second drain; a second polarization layer adjacent to the second source and the second drain; and a second channel layer coupled to the second source and the second drain and adjacent to the second polarization layer, the second channel layer comprising a second 2DEG region, wherein the second channel layer is over the first polarization layer.

[0065] Example 2. The apparatus of example 1 or any other example, further comprising: a gate electrode coupled to the second polarization layer.

[0066] Example 3. The apparatus of example 2 or any other example, wherein the first polarization layer or the first channel layer is not attached to the gate electrode.

[0067] Example 4. The apparatus of example 2 or any other example, wherein the gate electrode is coupled to the first polarization layer by a gate dielectric.

[0068] Example 5. The apparatus of any of examples 1-4 or any other example, wherein individual ones of the first polarization layer and the second polarization layer comprises group III-nitride (III-N) polarization material.

[0069] Example 6. The apparatus of any of examples 1-4 or any other example, wherein: the first polarization layer comprises InxAlyGa1-x-yN, and the second polarization layer comprises InaAlbGa1-a-bN, wherein the first polarization layer has higher concentration of Al and In compared to the respective concentration of Al and In of the second polarization layer.

[0070] Example 7. The apparatus of any of examples 1-4 or any other example, wherein: the first polarization layer has a thickness of at least 10 nanometer (nm) and no more than 20 nm; and the second polarization layer has a thickness of at least 5 nm and no more than 10 nm.

[0071] Example 8. The apparatus of any of examples 1-4 or any other example, wherein: the first 2DEG region has higher charge carrier density than the second 2DEG region.

[0072] Example 9. The apparatus of any of examples 1-4 or any other example, wherein: the first channel layer has a thickness of at least 0.5 micrometer and no more than 2 micrometers; and the second channel layer has a thickness of at least 10 nanometer (nm) and no more than 50 nm.

[0073] Example 10. The apparatus of any of examples 1-4 or any other example, wherein: the second 2DEG region does not contact or is not attached to one or both of the second source region or the second drain region.

[0074] Example 11. A variable capacitance device comprising: a first channel layer comprising GaN having a first two-dimensional electron gas (2DEG) region; a second channel layer comprising GaN having a second 2DEG region, wherein a thickness of the first channel layer is greater than a thickness of the second channel layer, and wherein the second channel layer is formed over the first channel layer; and a gate electrode coupled to the first 2DEG region.

[0075] Example 12. The variable capacitance device of example 11 or any other example, wherein the first 2DEG region has higher charge carrier density than the second 2DEG region.

[0076] Example 13. The variable capacitance device of example 11 or any other example, further comprising: a substrate; and a buffer layer formed over the substrate, wherein the second channel layer is formed over the buffer layer.

[0077] Example 14. The variable capacitance device of any of examples 11-13 or any other example, further comprising: a first polarization layer over the first channel layer; and a second polarization layer over the second channel layer.

[0078] Example 15. The variable capacitance device of example 14 or any other example, wherein: the gate electrode is recessed in the first polarization layer, and is not adjacent to the second polarization layer.

[0079] Example 16. The variable capacitance device of example 14 or any other example, wherein: the first polarization layer comprises InxAlyGa1-x-yN, and the second polarization layer comprises InaAlbGa1-a-bN, wherein the first polarization layer has higher concentration of Al and In compared to the respective concentration of Al and In of the second polarization layer.

[0080] Example 17. The variable capacitance device of any of examples 11-13 or any other example, further comprising: a first source and a first drain coupled to the first channel layer; and a second source and a second drain coupled to the second channel layer.

[0081] Example 18. The variable capacitance device of example 17 or any other example, wherein: the first source and the first drain comprises heavily-doped III-N material having a n-type impurity dopant concentration.

[0082] Example 19. A method comprising: epitaxially growing a first channel layer over a substrate, a first polarization layer on the first channel layer, a second channel layer over the first polarization layer, and a second polarization layer over the second channel layer, wherein the first channel layer comprises a first two-dimensional electron gas (2DEG) region and the second channel layer comprises a second 2DEG region; forming a first source and a first drain adjacent to the first polarization layer; and forming a second source and a second drain adjacent to the second polarization layer.

[0083] Example 20. The method of example 19 or any other example, further comprising: forming a gate stack to be recessed in the second polarization layer.

[0084] Example 21. The method of any of examples 19-20 or any other example, further comprising: electrically coupling two of: the first source, the first drain, the second source, and

the second drain; and electrically coupling remaining two of: the first source, the first drain, the second source, and the second drain.

[0085] Example 22. The method of any of examples 19-20 or any other example, further comprising: electrically coupling the first source and the first drain, to form a first node; and electrically coupling the second source and the second drain, to form a second node.

[0086] Example 23. The method of example 22 or any other example, further comprising: controlling a voltage of the gate stack, to tune a capacitance between the first node and the second node.

[0087] Example 24. An apparatus comprising: means for performing the method of any of the examples 19-23 or any other example.

[0088] Example 25. An apparatus comprising: means for epitaxially growing a first channel layer over a substrate, a first polarization layer on the first channel layer, a second channel layer over the first polarization layer, and a second polarization layer over the second channel layer, wherein the first channel layer comprises a first two-dimensional electron gas (2DEG) region and the second channel layer comprises a second 2DEG region; means for forming a first source and a first drain adjacent to the first polarization layer; and means for forming a second source and a second drain adjacent to the second polarization layer.

[0089] Example 26. The apparatus of example 25 or any other example, further comprising: means for forming a gate stack to be recessed in the second polarization layer.

[0090] Example 27. The apparatus of any of examples 25-26 or any other example, further comprising: means for electrically coupling two of: the first source, the first drain, the second source, and the second drain; and means for electrically coupling remaining two of: the first source, the first drain, the second source, and the second drain.

[0091] Example 28. The apparatus of any of examples 25-26 or any other example, further comprising: means for electrically coupling the first source and the first drain, to form a first node; and means for electrically coupling the second source and the second drain, to form a second node.

[0092] Example 29. The apparatus of example 28 or any other example, further comprising: means for controlling a voltage of the gate stack, to tune a capacitance between the first node and the second node.

[0093] However, the above embodiments are not limited in this regard and, in various implementations, the above embodiments may include the undertaking only a subset of such features, undertaking a different order of such features, undertaking a different combination of such features, and/or undertaking additional features than those features explicitly listed. The scope of the invention should, therefore, be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.

CLAIMS

We claim:

1. An apparatus comprising:

a first source and a first drain;

a first polarization layer adjacent to the first source and the first drain;

a first channel layer coupled to the first source and the first drain and adjacent to the first polarization layer, the first channel layer comprising a first two-dimensional electron gas (2DEG) region;

a second source and a second drain;

a second polarization layer adjacent to the second source and the second drain; and

a second channel layer coupled to the second source and the second drain and adjacent to the second polarization layer, the second channel layer comprising a second 2DEG region, wherein the second channel layer is over the first polarization layer.

2. The apparatus of claim 1, further comprising:

a gate electrode coupled to the second polarization layer.

3. The apparatus of claim 2, wherein the first polarization layer or the first channel layer is not attached to the gate electrode.

4. The apparatus of claim 2, wherein the gate electrode is coupled to the first polarization layer by a gate dielectric.

5. The apparatus of any of claims 1-4, wherein individual ones of the first polarization layer and the second polarization layer comprises group III-nitride (III-N) polarization material.

6. The apparatus of any of claims 1-4, wherein:

the first polarization layer comprises $In_xAl_yGa_{1-x-y}N$, and the second polarization layer comprises $In_aAl_bGa_{1-a-b}N$,

wherein the first polarization layer has higher concentration of Al and In compared to the respective concentration of Al and In of the second polarization layer.

7. The apparatus of any of claims 1-4, wherein:

the first polarization layer has a thickness of at least 10 nanometer (nm) and no more than 20 nm; and

the second polarization layer has a thickness of at least 5 nm and no more than 10 nm.

8. The apparatus of any of claims 1-4, wherein:

the first 2DEG region has higher charge carrier density than the second 2DEG region.

9. The apparatus of any of claims 1-4, wherein:

the first channel layer has a thickness of at least 0.5 micrometer and no more than 2 micrometers; and

the second channel layer has a thickness of at least 10 nanometer (nm) and no more than 50 nm.

10. The apparatus of any of claims 1-4, wherein:

the second 2DEG region does not contact or is not attached to one or both of the second source region or the second drain region.

11. A variable capacitance device comprising:

a first channel layer comprising GaN having a first two-dimensional electron gas (2DEG) region;

a second channel layer comprising GaN having a second 2DEG region, wherein a thickness of the first channel layer is greater than a thickness of the second channel layer, and wherein the second channel layer is formed over the first channel layer; and

a gate electrode coupled to the first 2DEG region.

12. The variable capacitance device of claim 11, wherein the first 2DEG region has higher charge carrier density than the second 2DEG region.

13. The variable capacitance device of claim 11, further comprising:

a substrate; and

a buffer layer formed over the substrate,

wherein the second channel layer is formed over the buffer layer.

14. The variable capacitance device of any of claims 11-13, further comprising:

a first polarization layer over the first channel layer; and

a second polarization layer over the second channel layer.

15. The variable capacitance device of claim 14, wherein:

the gate electrode is recessed in the first polarization layer, and is not adjacent to the second polarization layer.

16. The variable capacitance device of claim 14, wherein:

the first polarization layer comprises $In_xAl_yGa_{1-x-y}N$, and the second polarization layer comprises $In_aAl_bGa_{1-a-b}N$, wherein the first polarization layer has higher concentration of Al and In compared to the respective concentration of Al and In of the second polarization layer.

17. The variable capacitance device of any of claims 11-13, further comprising:

a first source and a first drain coupled to the first channel layer; and

a second source and a second drain coupled to the second channel layer.

18. The variable capacitance device of claim 17, wherein:

the first source and the first drain comprises heavily-doped III-N material having a n-type impurity dopant concentration.

19. A method comprising:

epitaxially growing a first channel layer over a substrate, a first polarization layer on the first channel layer, a second channel layer over the first polarization layer, and a second polarization layer over the second channel layer, wherein the first channel layer comprises a first two-dimensional electron gas (2DEG) region and the second channel layer comprises a second 2DEG region;

forming a first source and a first drain adjacent to the first polarization layer; and

forming a second source and a second drain adjacent to the second polarization layer.

20. The method of claim 19, further comprising:

forming a gate stack to be recessed in the second polarization layer.

21. The method of any of claims 19-20, further comprising:

electrically coupling two of: the first source, the first drain, the second source, and the second drain; and

electrically coupling remaining two of: the first source, the first drain, the second source, and the second drain.

22. The method of any of claims 19-20, further comprising:

electrically coupling the first source and the first drain, to form a first node; and

electrically coupling the second source and the second drain, to form a second node.

23. The method of claim 22, further comprising:

controlling a voltage of the gate stack, to tune a capacitance between the first node and the second node.

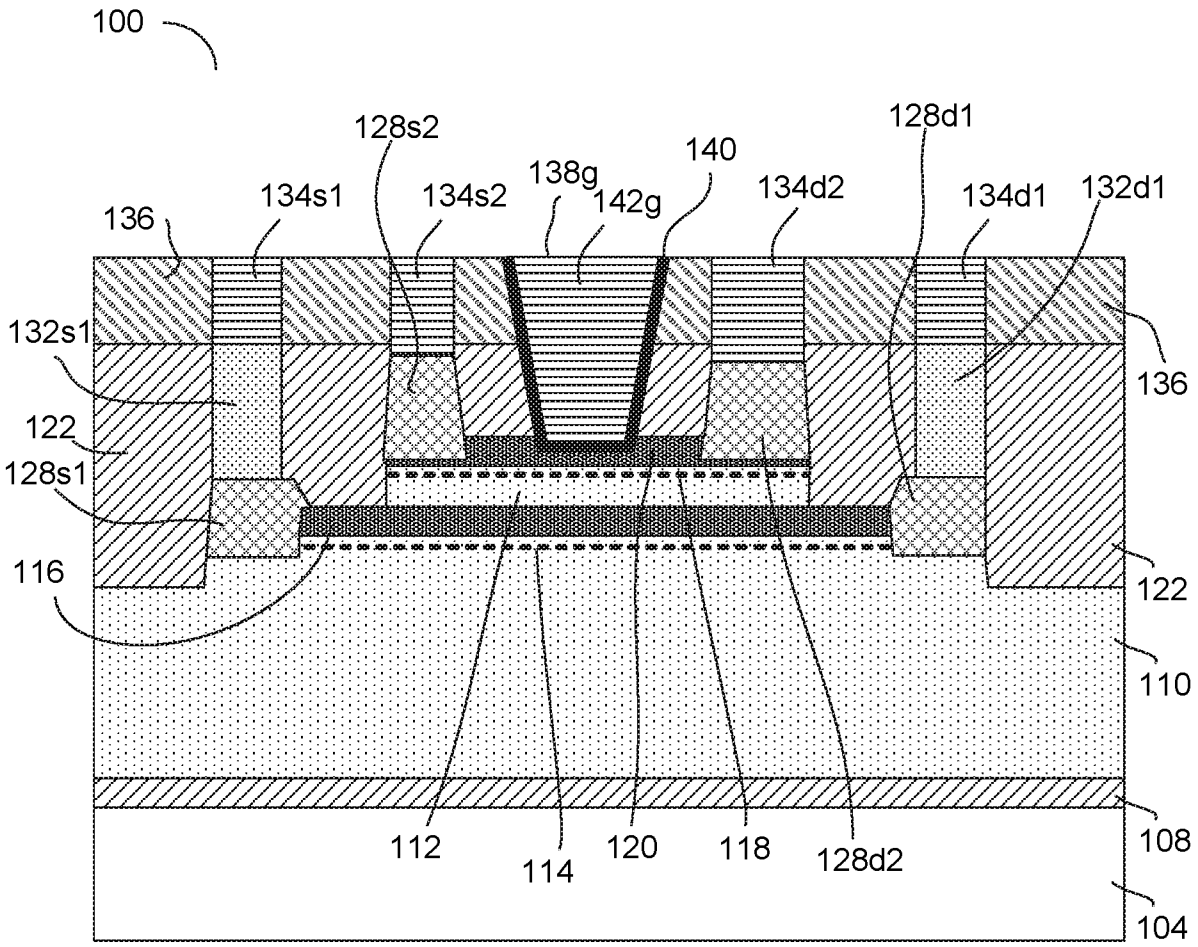
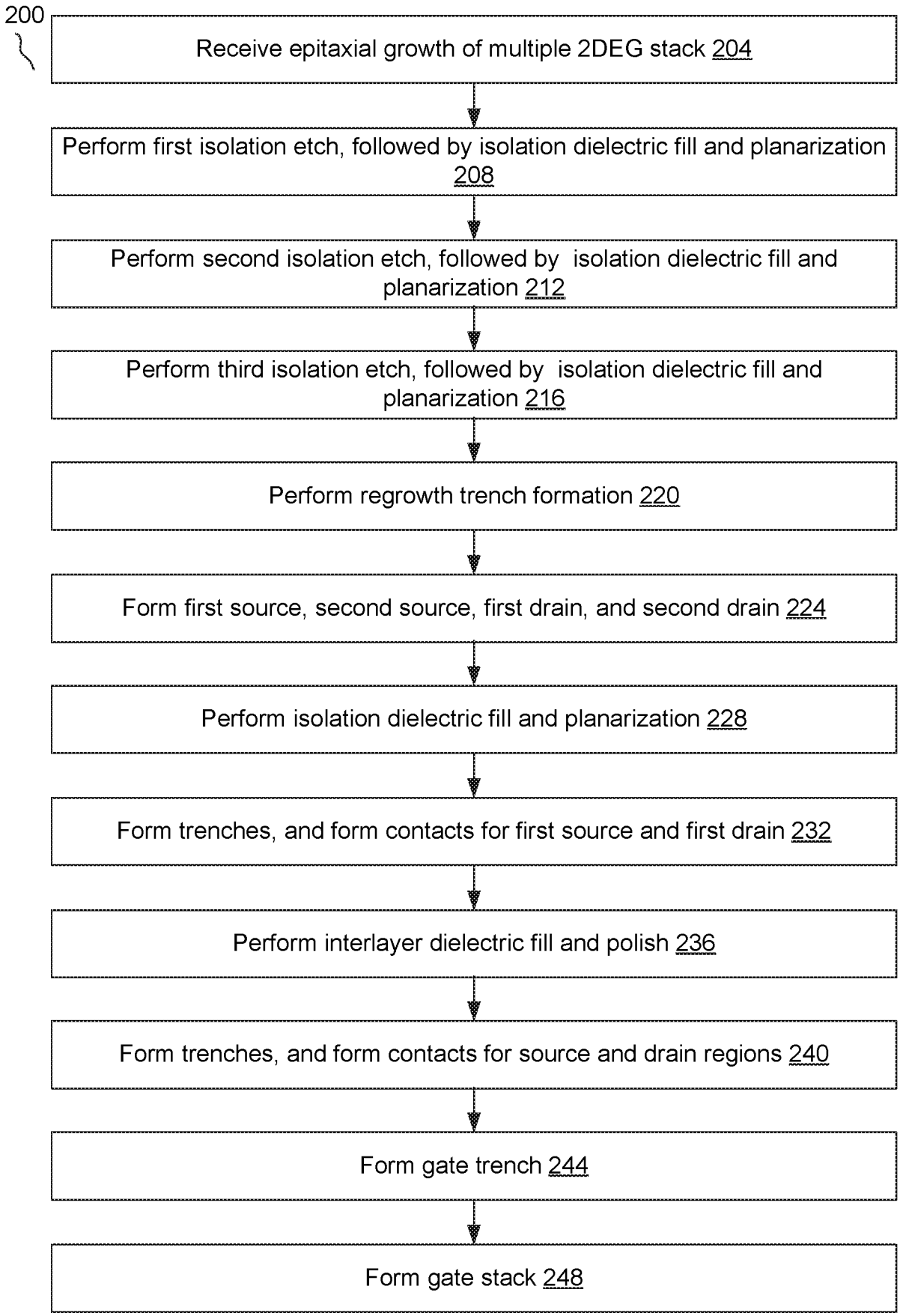

100
128s2
140
128d1
138g
134s1
134s2
142g
134d2
134d1
132d1
136
132s1
136
122
128s1
116
122
110
108
112
114
120
118
128d2
104

Fig. 1


200
Receive epitaxial growth of multiple 2DEG stack 204
Perform first isolation etch, followed by isolation dielectric fill and planarization 208
Perform second isolation etch, followed by isolation dielectric fill and planarization 212
Perform third isolation etch, followed by isolation dielectric fill and planarization 216
Perform regrowth trench formation 220
Form first source, second source, first drain, and second drain 224
Perform isolation dielectric fill and planarization 228
Form trenches, and form contacts for first source and first drain 232
Perform interlayer dielectric fill and polish 236
Form trenches, and form contacts for source and drain regions 240
Form gate trench 244
Form gate stack 248

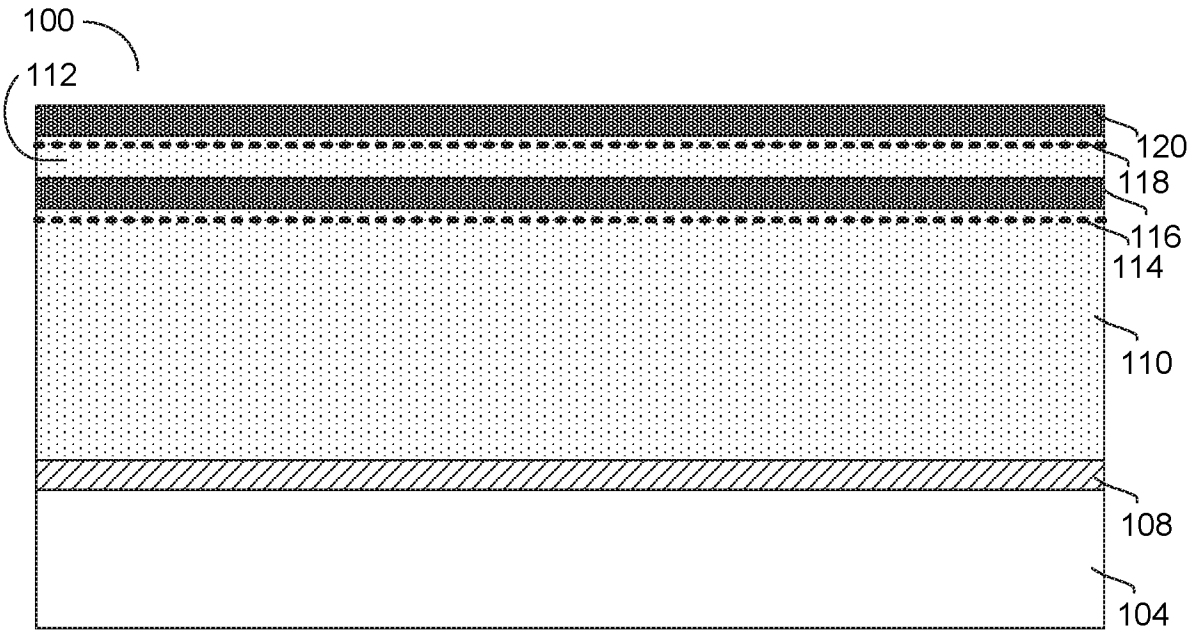

100
112
120
118
116
114
110
108
104

Fig. 3A

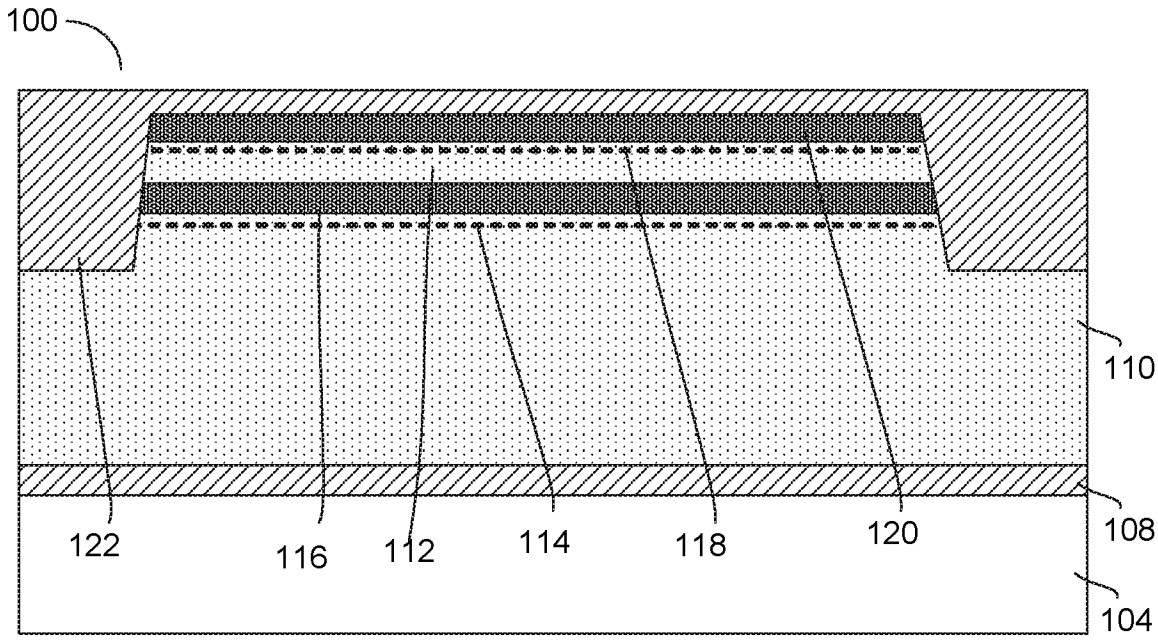

100
110
108
104
122
116
112
114
118
120

Fig. 3B

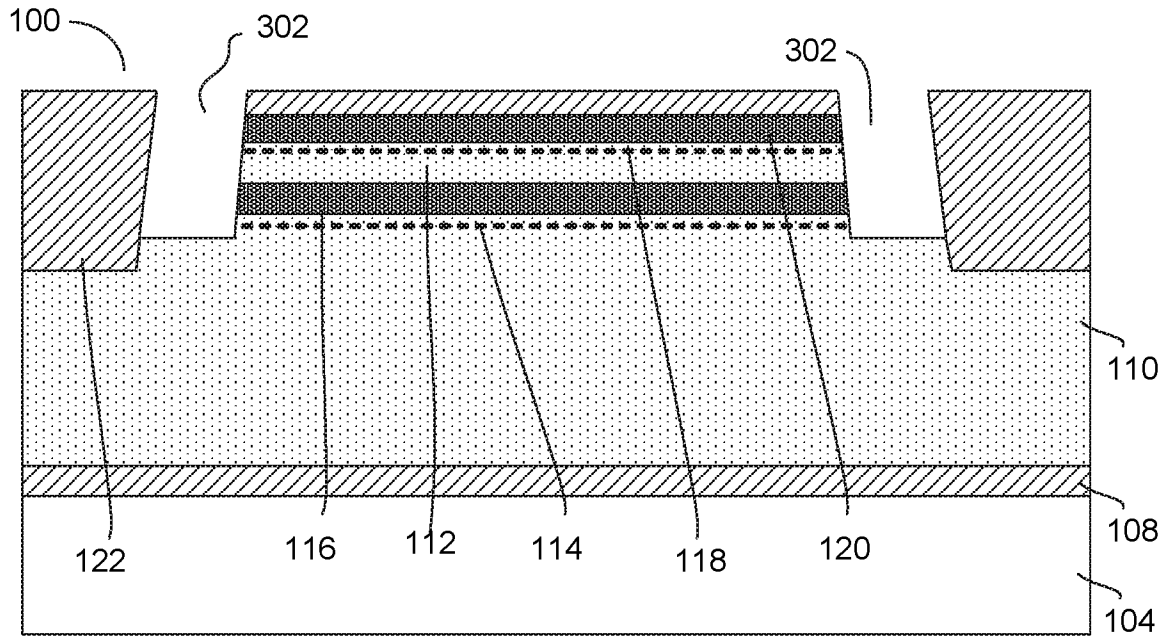

100
302
302
110
108
104
122
116
112
114
118
120

Fig. 3C

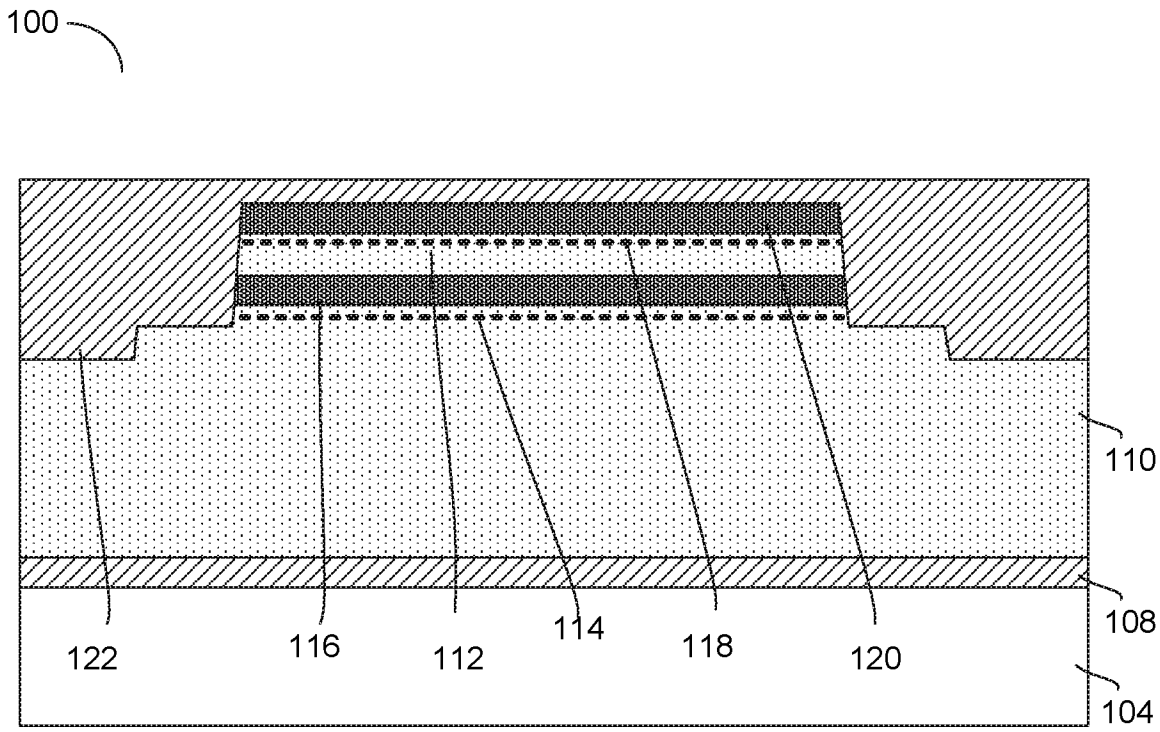

100
110
108
104
122
116
112
114
118
120

Fig. 3D

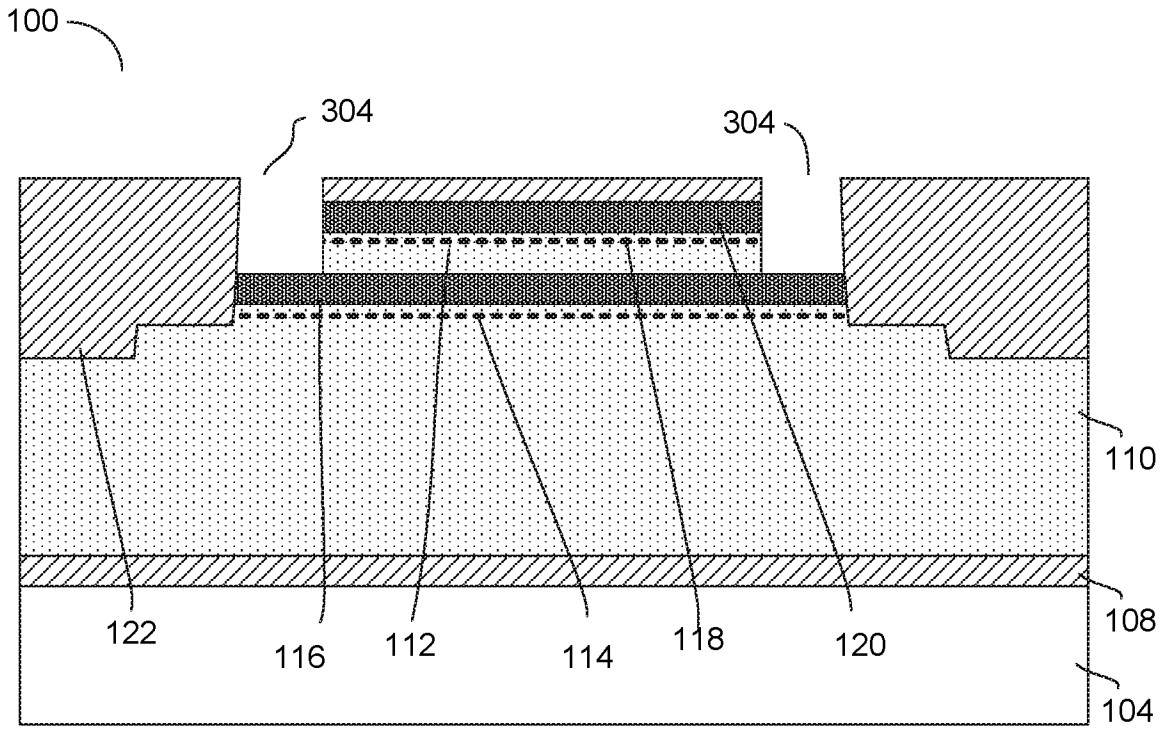

100
304
304
110
108
104
122
116
112
114
118
120

Fig. 3E

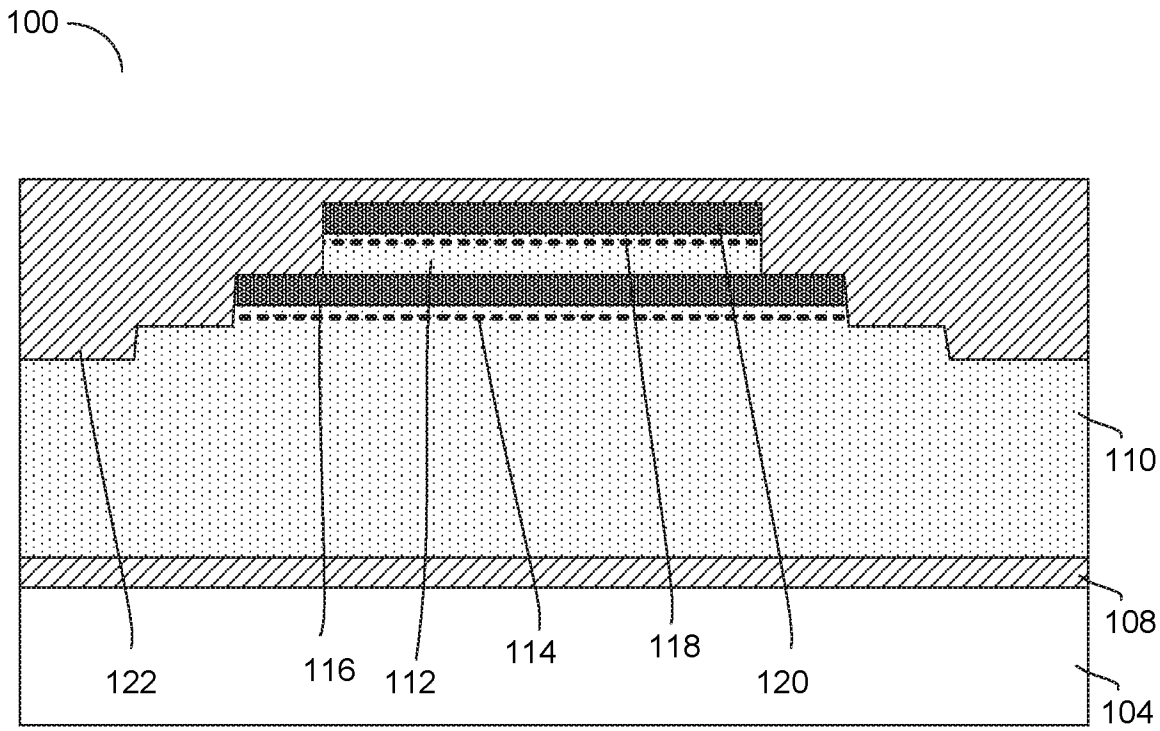

100
110
108
104
122
116
112
114
118
120

Fig. 3F

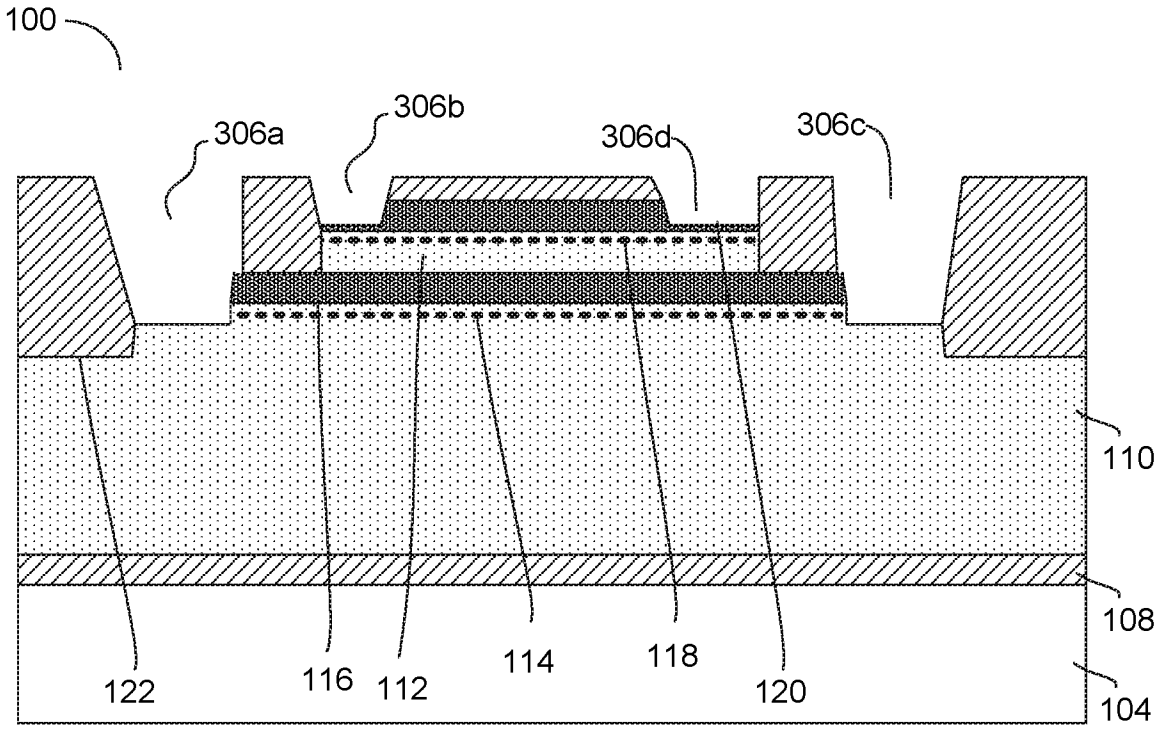

100
306a
306b
306d
306c
110
108
122
116
112
114
118
120
104

Fig. 3G

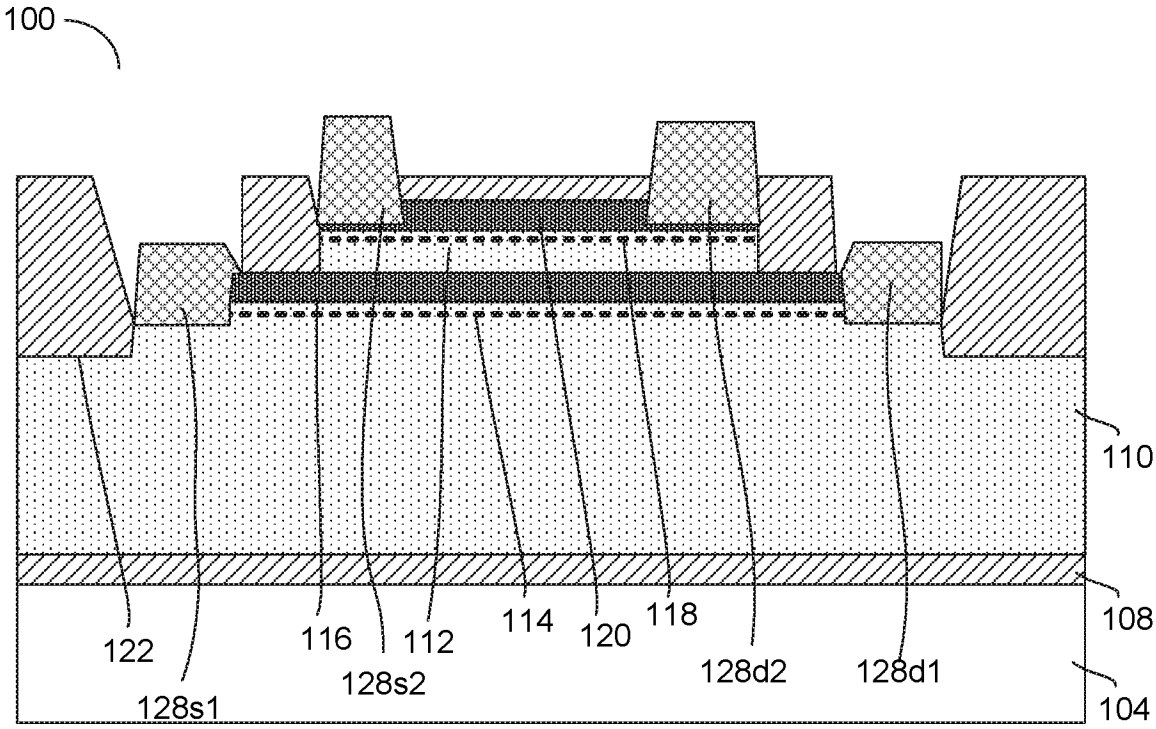

100
110
108
122
128s1
116
128s2
112
114
120
118
128d2
128d1
104

Fig. 3H

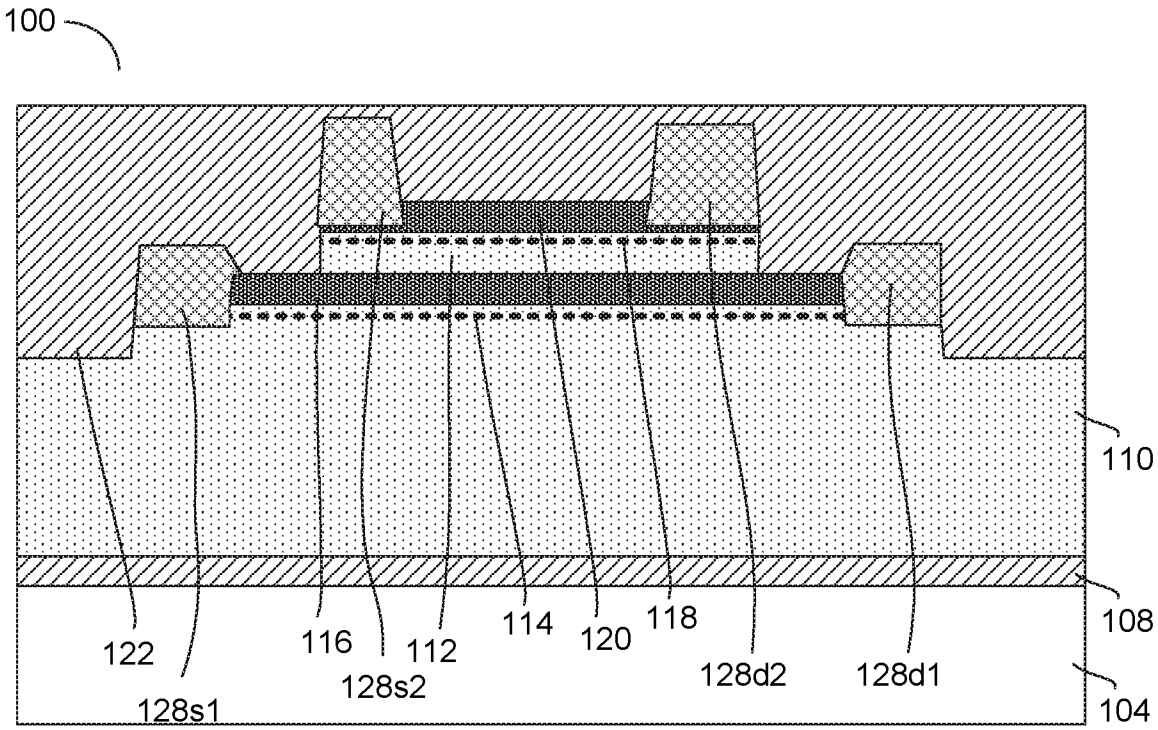

100
110
108
104
122
128s1
116
128s2
112
114
120
118
128d2
128d1

Fig. 3I

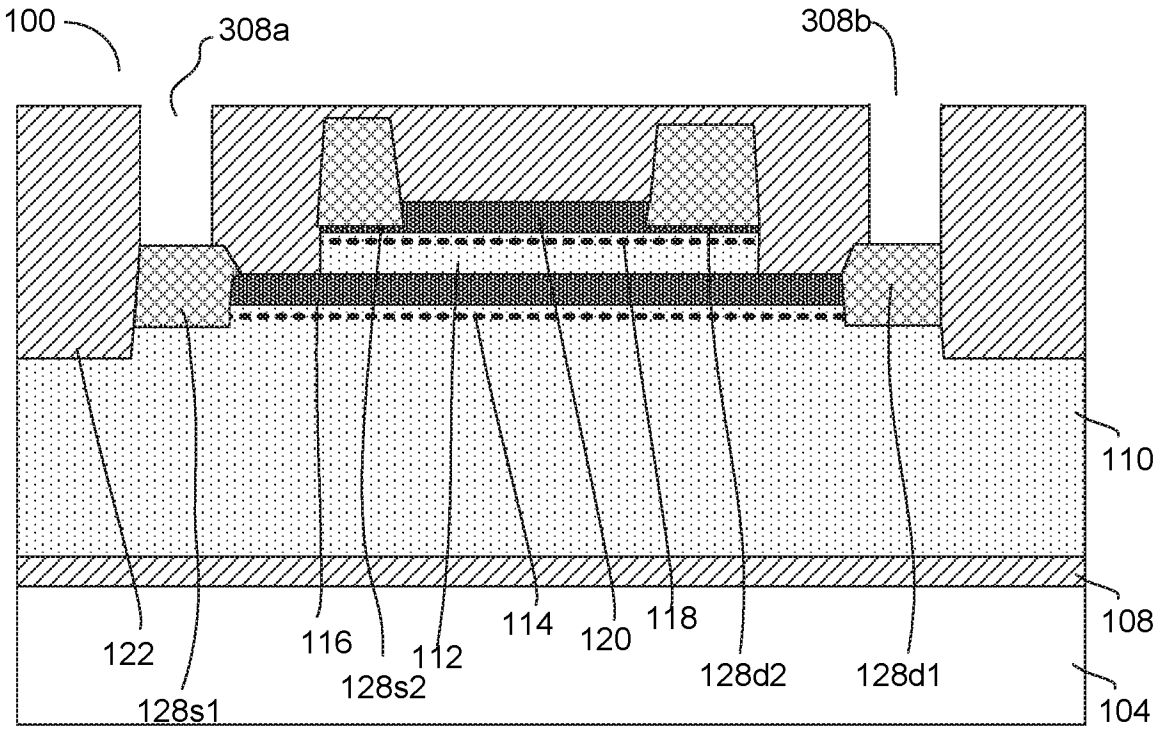

100
308a
308b
110
108
104
122
128s1
116
128s2
112
114
120
118
128d2
128d1

Fig. 3J

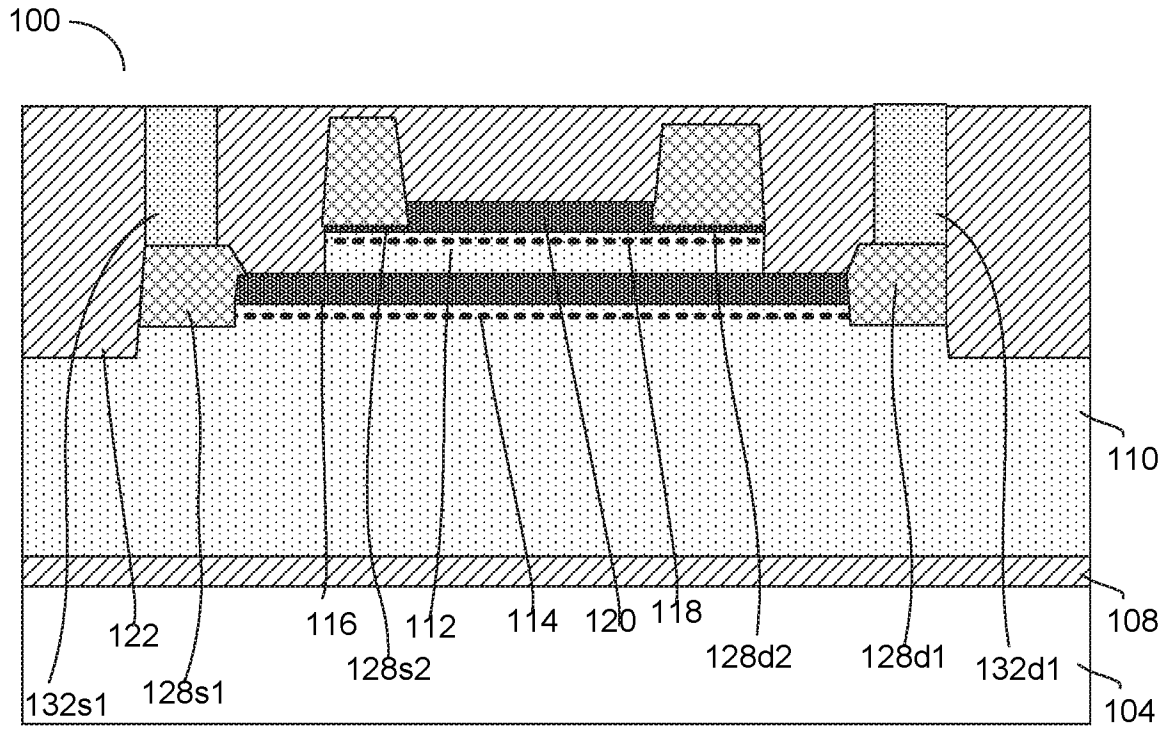

100
110
108
104
122
116
112
114
120
118
128d2
128d1
132d1
132s1
128s1
128s2

Fig. 3K

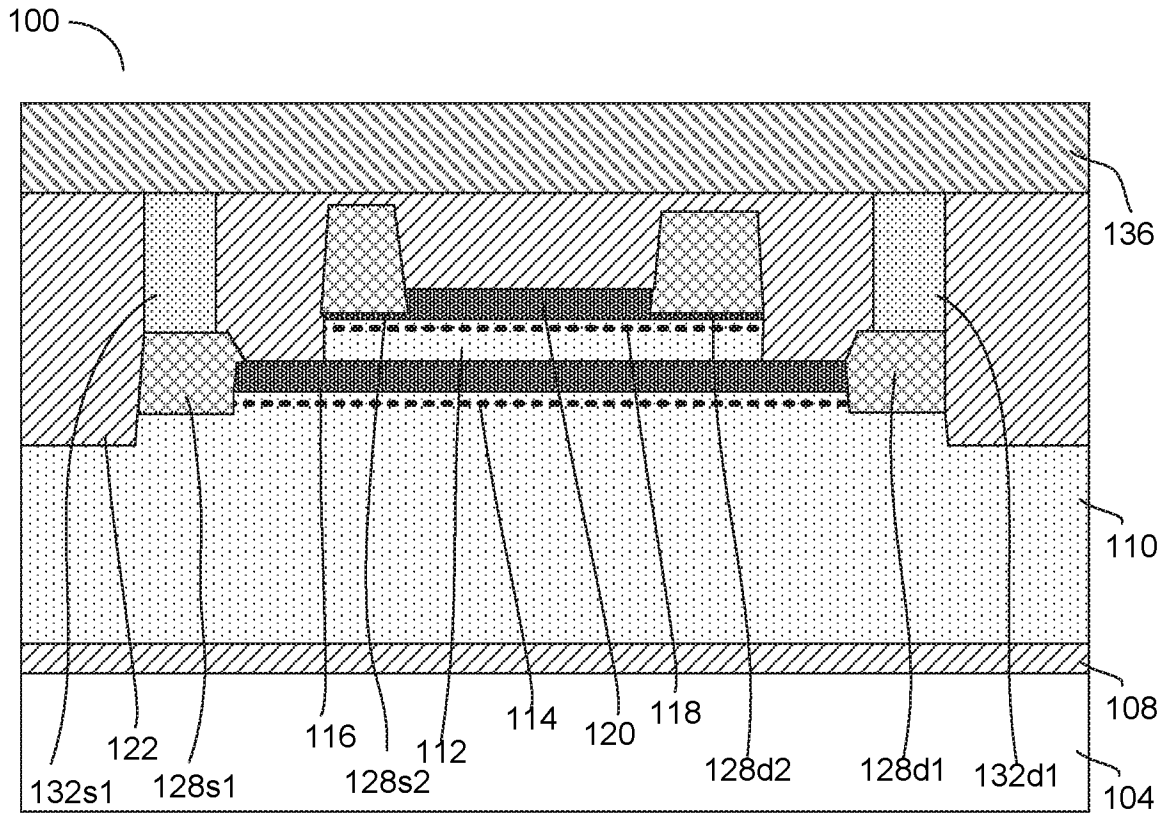

100
136
110
108
104
122
116
112
114
120
118
128d2
128d1
132d1
132s1
128s1
128s2

Fig. 3L

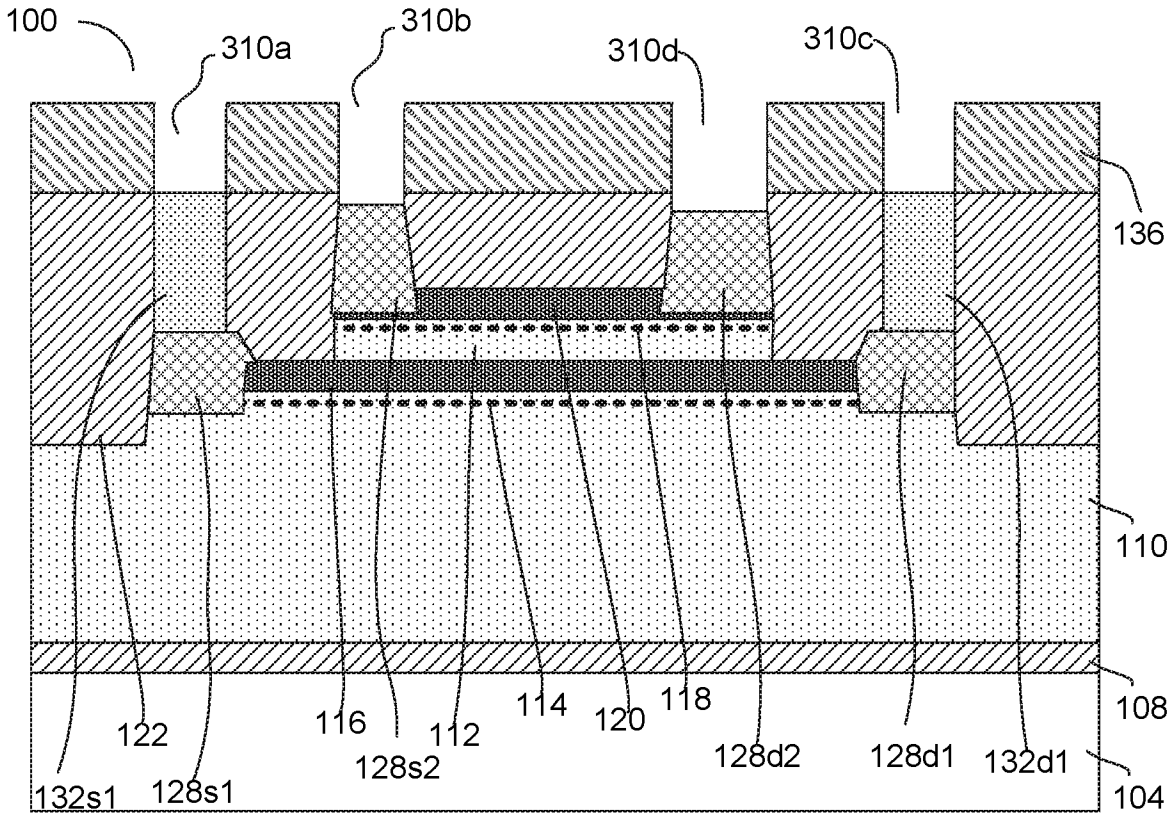

100
310a
310b
310d
310c
136
110
108
104
122
116
112
114
120
118
128d2
128d1
132d1
132s1
128s1
128s2

Fig. 3M

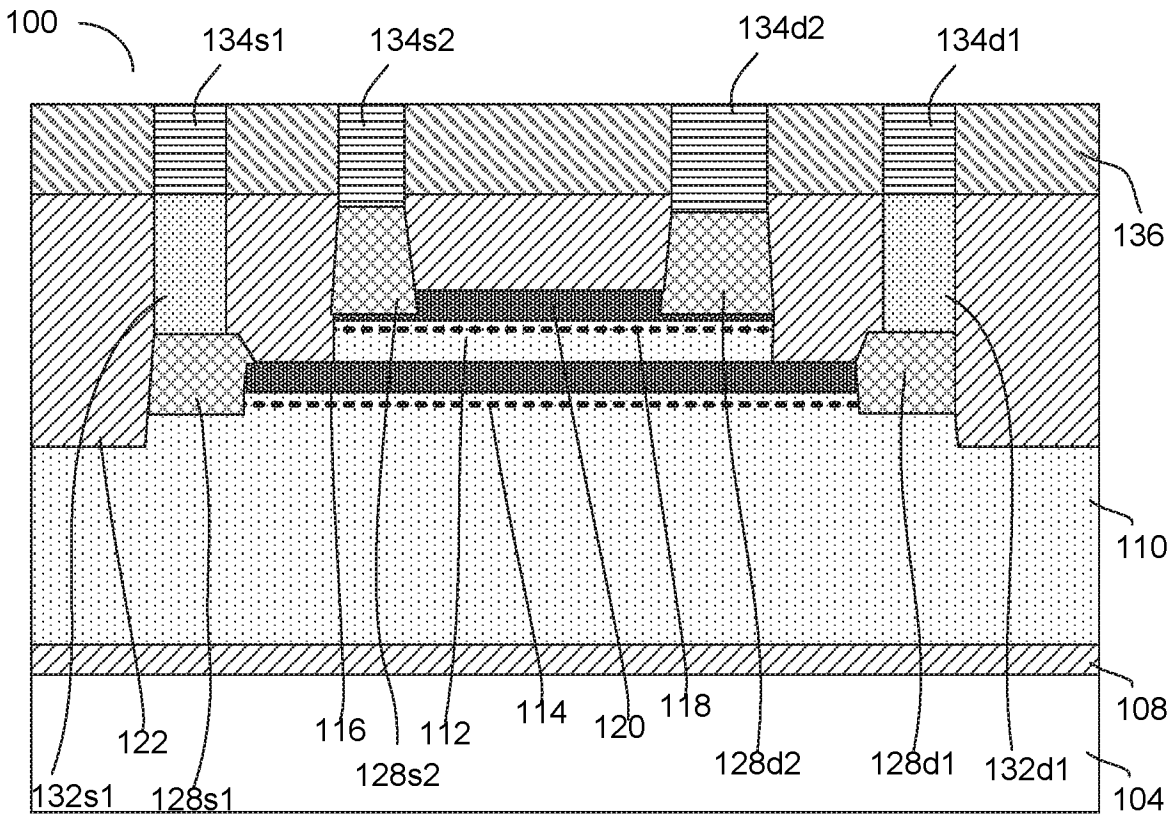

100
134s1
134s2
134d2
134d1
136
110
108
104
122
116
112
114
120
118
128d2
128d1
132d1
132s1
128s1
128s2

Fig. 3N

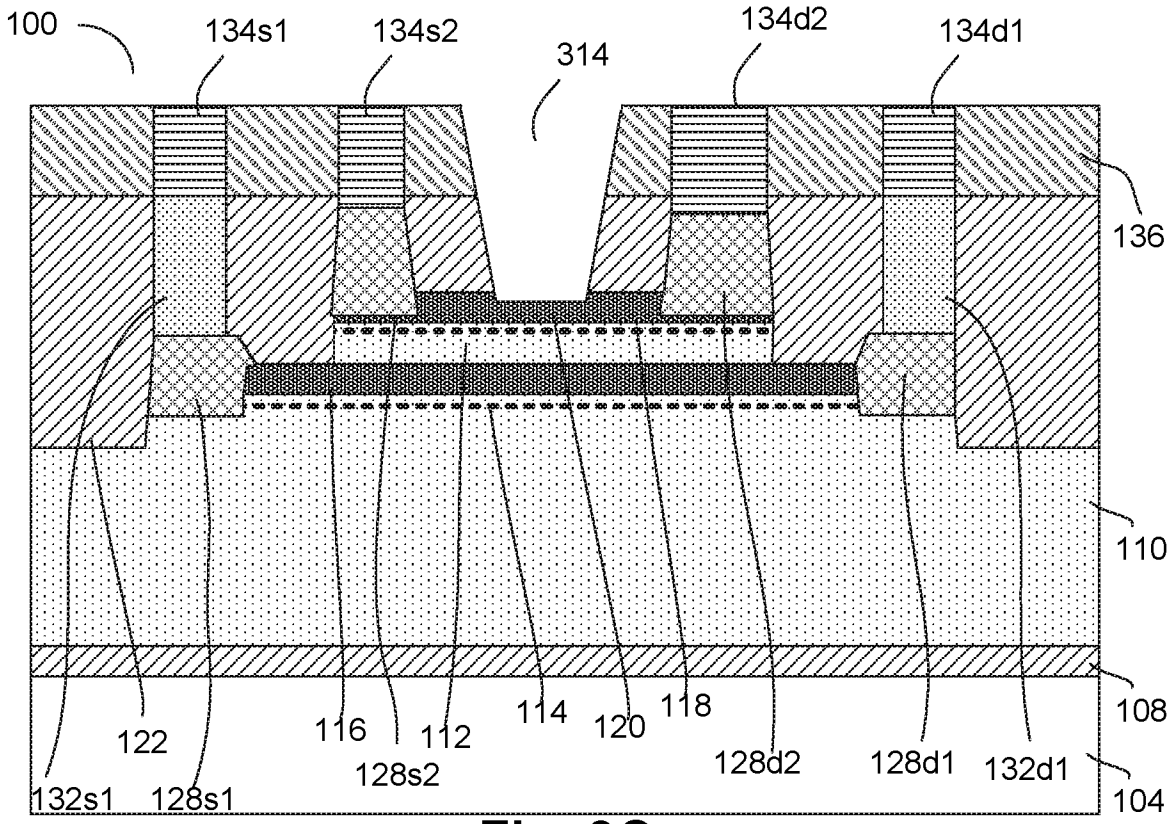

100
134s1
134s2
314
134d2
134d1
136
110
108
104
122
116
112
114
120
118
128d2
128d1
132d1
132s1
128s1
128s2

Fig. 3O

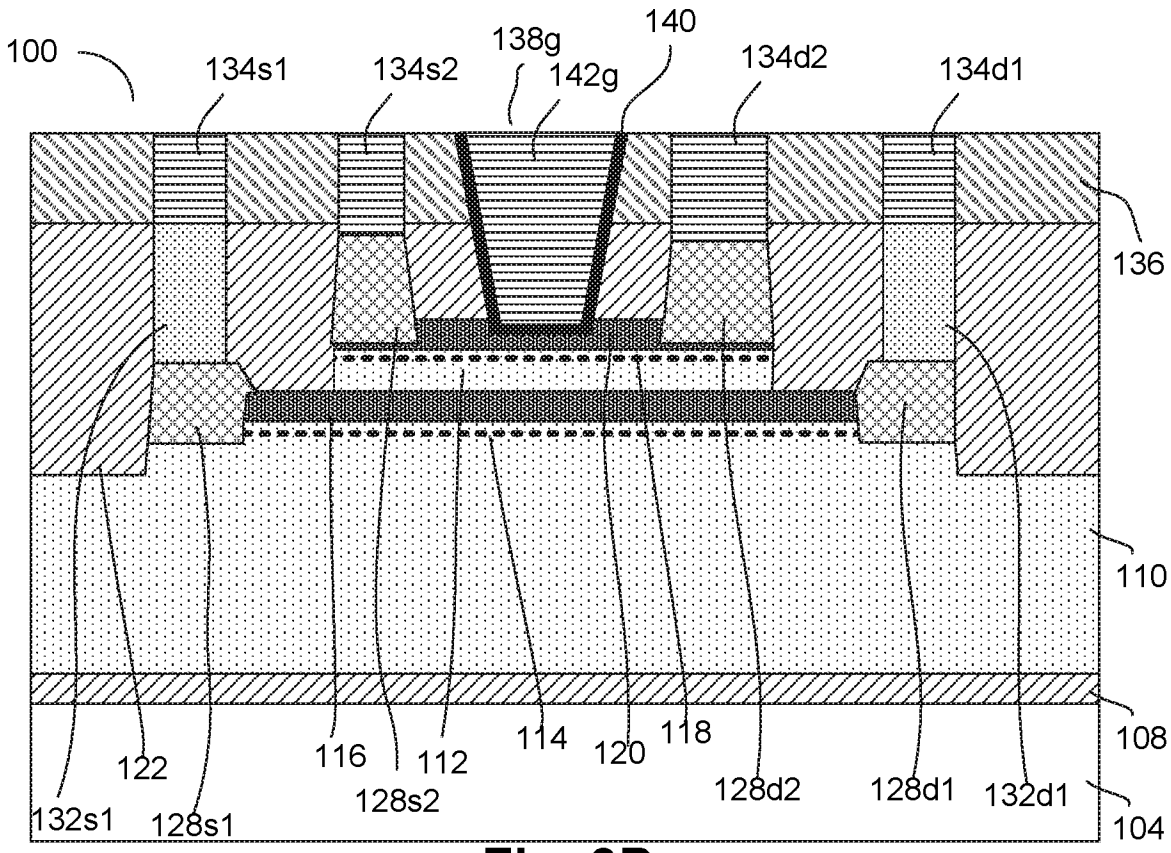

100
134s1
134s2
138g
142g
140
134d2
134d1
136
110
108
104
122
116
112
114
120
118
128d2
128d1
132d1
132s1
128s1
128s2

Fig. 3P

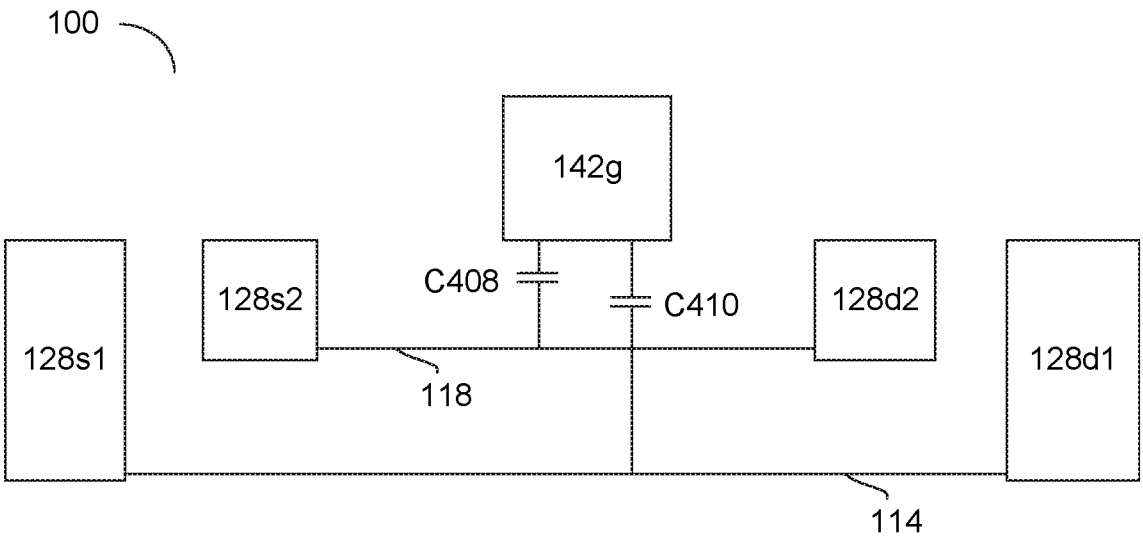


Fig. 4

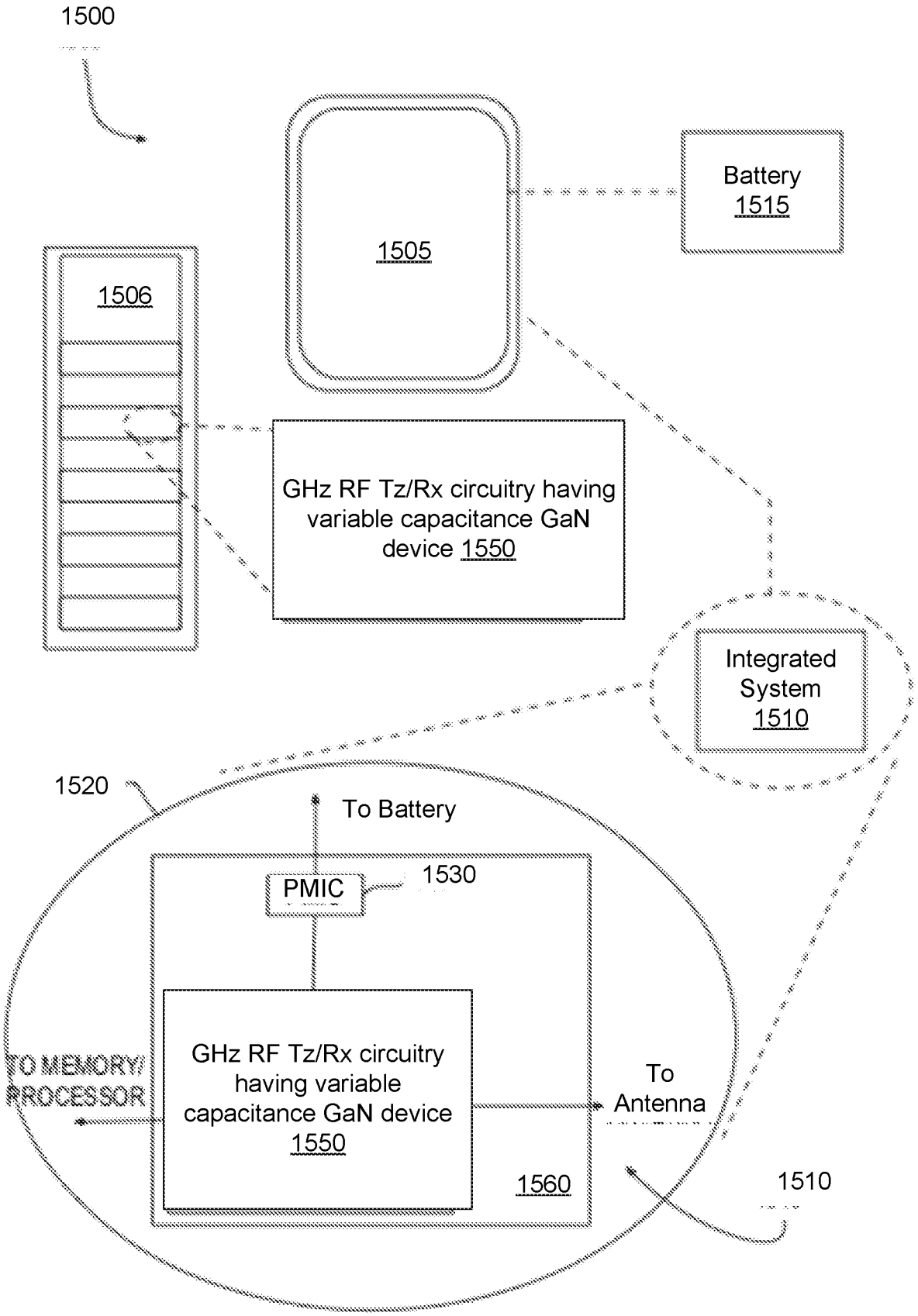

1500
1505
Battery
1515
1506
GHz RF Tz/Rx circuitry having variable capacitance GaN device 1550
Integrated System
1510
1520
To Battery
PMIC
1530
TO MEMORY/ PROCESSOR
GHz RF Tz/Rx circuitry having variable capacitance GaN device 1550
To Antenna
1560
1510

Fig. 5

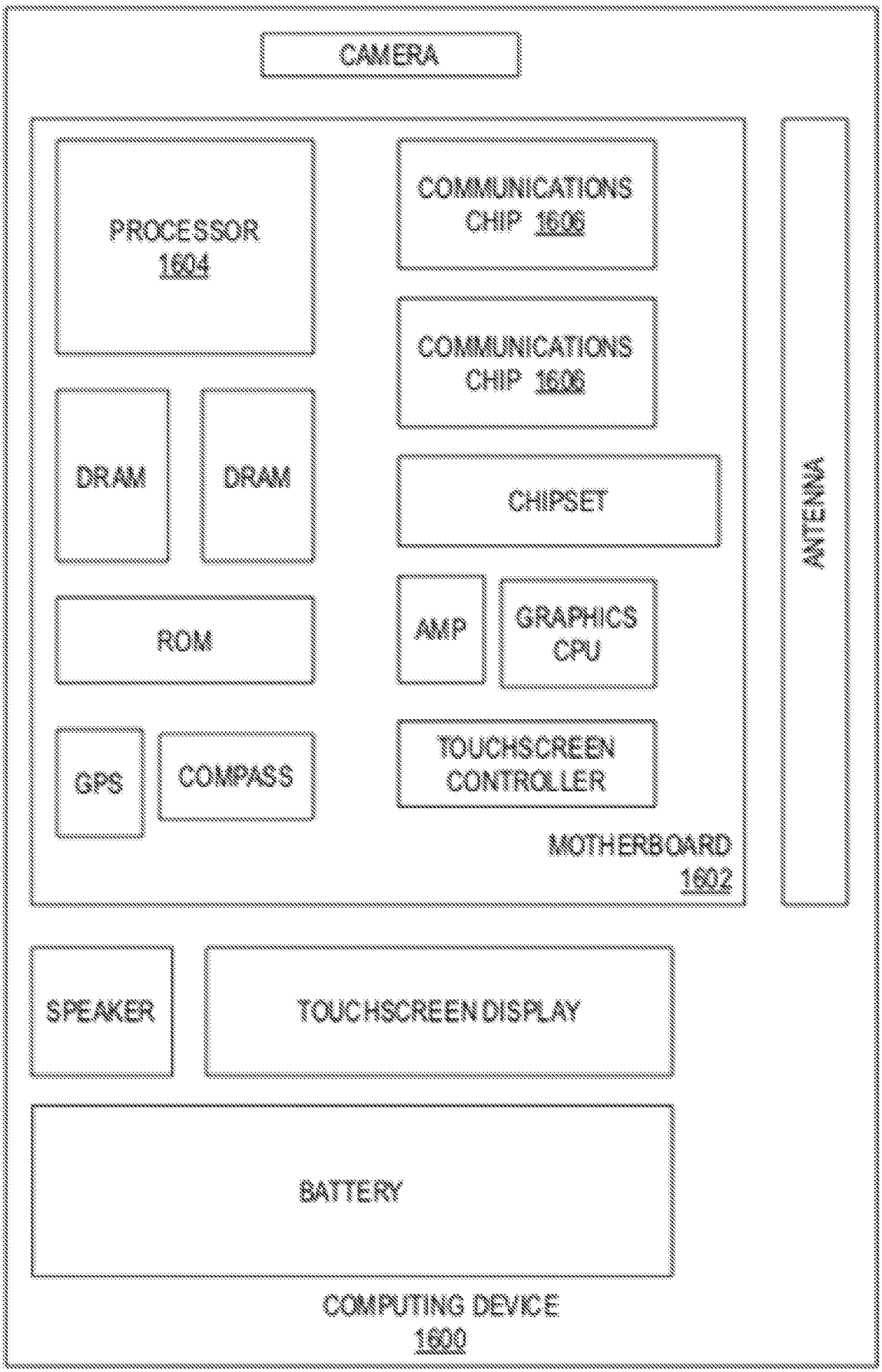

CAMERA
PROCESSOR 1604
COMMUNICATIONS CHIP 1606
COMMUNICATIONS CHIP 1606
DRAM
DRAM
CHIPSET
ROM
AMP
GRAPHICS CPU
GPS
COMPASS
TOUCHSCREEN CONTROLLER
MOTHERBOARD 1602
ANTENNA
SPEAKER
TOUCHSCREEN DISPLAY
BATTERY
COMPUTING DEVICE 1600

Fig. 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2017/054155

A. CLASSIFICATION OF SUBJECT MATTER

H01L 29/778(2006.01)i, H01L 29/66(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 29/778; H01L 21/338; H01L 29/74; H01L 29/66; H01L 29/20

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: source, drain, gate, polarization layer, channel layer, 2DEG, capacitance

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2013-0221409 A1 (NAKAJIMA et al.) 29 August 2013 See paragraphs [0060]-[0136] and figure 7b.	1-10,19-23
Y		11-18
Y	US 2004-0135169 A1 (YOSHII et al.) 15 July 2004 See paragraph [0022], claim 1 and figure 3.	11-18
A	US 2014-0266324 A1 (MITSUBISHI ELECTRIC RESEARCH LABORATORIES, INC.) 18 September 2014 See claims 1-11 and figures 1-5.	1-23
A	JP 2013-041986 A (ADVANCED POWER DEVICE RESEARCH ASSOCIATION) 28 February 2013 See paragraphs [0042]-[0051] and figure 6.	1-23
A	KR 10-2016-0083256 A (KOREA ADVANCED NANO FAB CENTER) 12 July 2016 See paragraphs [0107]-[0126] and figure 15.	1-23

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 June 2018 (28.06.2018)	**28 June 2018 (28.06.2018)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2017/054155

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