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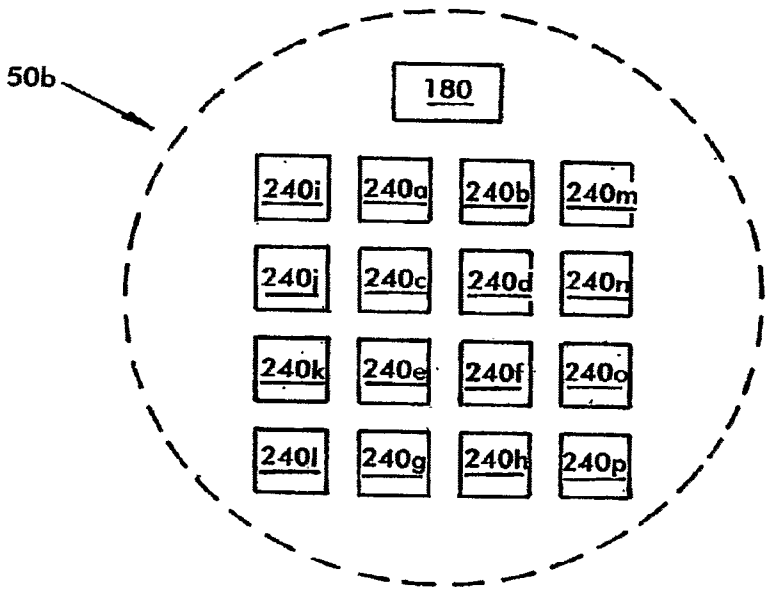
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(54) **Title:** UNIVERSAL PAD ARRANGEMENT FOR SURFACE MOUNTED SEMICONDUCTOR DEVICES



(57) **Abstract:** An apparatus for coupling a plurality of surface mounted semiconductor device packages to a circuit board is provided. Each package including a semiconductor device die and a metal clip including a flat web portion having a bottom surface and at least one peripheral rim portion extending from an edge of said flat web portion, said bottom surface having solderable planar metal electrodes or pads on its bottom surface, the contact pads being formed in plurality of layouts having one or more columns and one or more rows. The apparatus including a circuit board contact pattern including one or more columns and one or more rows of contacts, a number of rows being equal to a largest number of contact pad rows in the plurality of contact pad layouts, a number of columns being equal to a largest number of contact pad columns in the plurality of contact pad layouts. The circuit board contact pattern is usable by all of the plurality of the contact pad layouts of the plurality of semiconductor device packages.

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UNIVERSAL PAD ARRANGEMENT FOR SURFACE MOUNTED SEMICONDUCTOR DEVICES

CROSS-REFERENCE TO RELATED APPLICATION

[0001] The present application is based on and claims priority to U.S. Provisional Patent Application Serial No. 60/729,985, filed on October 25, 2005 and U.S. Patent Application Serial No. 11/551,767, filed October 23, 2006, both entitled UNIVERSAL PAD ARRANGEMENT FOR SURFACE MOUNTED SEMICONDUCTOR DEVICES. The entire contents of these applications are hereby incorporated by reference.

BACKGROUND OF THE INVENTION

[0002] This invention relates to a semiconductor device mounting and more specifically to a universally usable contact pattern for surface mounted semiconductor device die.

[0003] Semiconductor device die, such as flip chip surface mounted die and International Rectifier's DirectFET® packages described, for example in U.S. Patent 6,624,522, carry die which have a particular planar contact pattern. Thus for MOSFET die, planar source, gate and drain contacts are presented, which must align to the respective contacts of an end user's or customer's circuit board. Other die will include diodes, IGBTs, and the like. The contact pattern on the die will differ in shape and number, depending on die size and current and voltage ratings.

[0004] The DirectFET package is a surface-mount package that improves MOSFET performance by lowering both the package's electrical and thermal resistance. The DirectFET package does so with a design that permits direct attachment of the die to a

circuit board via solderable pads on the chip or die and through attachment to the interior of a copper or other conductive material drain clip that allows double-sided cooling. The die in the DirectFET package is a passivated die attached to a copper clip. Solderable metal contacts on the bottom of the die provide contacts such as gate and source contacts for a MOSFET to be mounted on and connected to a circuit board, while the copper clip provides an electrical connection to the MOSFET drain and permits topside cooling.

[0005] The circuit board pattern of contact locations is designed by each end user/customer to meet the contact pattern of the particular package. Thus, the circuit board will be designed with 2, 3, 4, 5, or any other number of spaced contacts of selected areas in some particular rectangular-like or mesh-like pattern.

[0006] The end user must then produce support board with surface contact patterns which match the number and pattern of the device to be mounted. Differences in the patterns and contact numbers increase the end-user's manufacturing process.

SUMMARY OF THE INVENTION

[0007] It is an object of the present invention to provide a universally usable contact pattern for surface mounted semiconductor device die.

[0008] In accordance with the invention, the contact pattern or mesh pattern of a circuit board is designed to match two or more possible patterns of solderable contact pads on a die that may be selected for use with the circuit board by the end user. The die solderable contact pads which are in unselected positions and will not be used by the end user can be insulated by a solder mask during a fabrication process of the die. Alternatively, unused contacts of the circuit board's contact pattern can be insulated.

[0009] An apparatus for coupling a plurality of surface mounted semiconductor device packages to a circuit board is provided. Each package including a semiconductor device die and a metal clip including a flat web portion having a bottom surface and at least one peripheral rim portion extending from an edge of said flat web portion, said

bottom surface being electrically connected to a solderable planar metal electrode on a bottom surface of said die via contact pads, the contact pads being formed in plurality of layouts having one or more columns and one or more rows. The apparatus including a circuit board contact pattern including one or more columns and one or more rows of contacts, a number of rows being equal to a largest number of contact pad rows in the plurality of contact pad layouts, a number of columns being equal to a largest number of contact pad columns in the plurality of contact pad layouts. The circuit board contact pattern is usable by all of the plurality of the contact pad layouts of the plurality of semiconductor device packages.

[0010] Other features and advantages of the present invention will become apparent from the following description of the invention that refers to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] Figure 1 is a side view of a DirectFET® package;

[0012] Figures 2a – 2b are bottom views of surface mounted packages with a first layout, using one column and one or more rows, of contact pads;

[0013] Figures 3a – 3b are bottom views of surface mounted packages with a second layout, using two column and one or more rows, of contact pads;

[0014] Figures 4a – 4d are bottom views of surface mounted packages with a third contact layout, using two or more columns and two or more rows, of contact pads; and

[0015] Figures 5a – 5b are a partial diagram of a circuit board contact pattern of the present invention for coupling surface mounted packages having contact layouts that include one or more columns and one or more rows of contact pads.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

[0016] The present invention provides a novel universally usable contact pattern for use with surface mounted semiconductor device die of a kind having power or other electrodes available for surface mounting on a common support surface, i.e., the moralized pattern on a printed circuit board.

[0017] Figure 1 illustrates a side view of a surface mounted semiconductor DirectFET package 10 that is coupled to a surface of a circuit board (not shown). Solderable contact pads of a semiconductor die are disposed on the bottom surface of the package 10. Some of the various layout types of the solderable contact pads will be illustrated below with reference to Figures 2-4. Prior to the present invention, each package within the layout type required a unique circuit board contact pattern to accommodate unique contact pad layouts of the packages. A circuit board universal contact pattern, explained with reference to Figures 5a and 5b eliminates this requirement.

[0018] Figures 2a and 2b illustrate a bottom view of the surface mounted package having a first layout type of the solderable contact pads. The first layout type uses one column and one or more rows of contact pads. Figure 2a shows a package 10a comprising a die 12 and a metal clip. The metal clip including a flat web portion 14 having a bottom surface and at least one peripheral rim portion 16 extending from an edge of said flat web portion and being electrically connected to a solderable planar metal electrode on a top surface of the die 12. The peripheral rim portion 16 forming one of the contacts, e.g., a MOSFET drain contact with the circuit board. The bottom surface of die 12 has a solderable planar metal electrodes or pads including source contact pads 18 and a gate contact 20a. Figure 2b shows a package 10b that is similar to the package 10a of Figure 2a. In addition to the contact pad 20a the package 10b further includes a second source contact 20b in the second row of contact pads.

[0019] Figures 3a and 3b illustrate a bottom view of the surface mounted package 30 including a second layout type of the solderable contact pads. The second layout type uses two columns and one or two rows of contact pads. Figure 3a shows a package 30a comprising the die 12 and the metal clip. The metal clip includes the flat web portion 14 having a bottom surface and at least one peripheral rim portion 16 extending from an edge of said flat web portion 14 and being electrically connected to a solderable planar metal electrode on a top surface of the die 12. The peripheral rim portion 16 forming one of the contacts, e.g., a MOSFET drain contact, with the circuit board. The bottom surface carries a solderable planar metal electrode consisting of gate contact pad 18 and source electrodes or pads 22a-22b. Figure 3b shows a package 30b that is similar to the package 30a of Figure 3a. In addition to the contact pads 22a and 22b the package 30b further includes source contact pads 22c-22d in the second row of contact pads.

[0020] Figures 4a-4b illustrate a bottom view of the surface mounted package 40 including a third layout type of the solderable contact pads. The third layout type uses two to four columns and two to four rows of electrodes or contact pads. Figure 4a shows a package 40a comprising the die 12 and the metal clip. The metal clip including the flat web portion 14 having a bottom surface has at least one peripheral rim portion 16 extending from an edge of said flat web portion 14 which is electrically connected to a solderable planar drain metal electrode on a top surface of the die 12. The peripheral rim portion 16 forms one of the contacts, e.g., a MOSFET drain contact with the circuit board. The bottom surface contains solderable planar metal electrodes on the bottom surface of the die 12 via gate contact pad 18, and source electrodes 24a-24d. The layout type of the package 40a is different from that of the package 30b of Figure 3b in that it provides additional space 15 for inclusion of additional contact pads as will be shown with reference to Figures 4b and 4d.

[0021] Figure 4b shows the package 40b that is similar to the package 40a of Figure 4a. In addition to the contact pads 24a and 24b the package 40b further includes contact pads 24e-24e in the third row of source contact pads. The package 40c of Figure 4c

includes two more rows of contact pads 24e-24h. Additionally, the package 40d of Figure 4d includes two rows and two columns of additional contact pads 24e-24p over the package 40a of Figure 4a.

[0022] It should be understood that the above-described and illustrated contact pad layout types as used as an example and are not intended to limit the scope of the present invention. The present invention can easily accommodate any number of additional contact pad layout types.

[0023] As stated above, prior to the present invention each surface mounted semiconductor device package required a unique circuit board contact pattern to accommodate unique contact pad layouts. That required provision of unique circuit boards for each circuit design using different semiconductor device packages. In accordance with the present invention the universal contact pattern will accommodate the contact pad layouts of all packages using the same circuit board contact pattern.

[0024] In accordance with the present invention the many different layouts of the solderable contact pads of the surface mounted semiconductor device packages may be accommodated by a universally usable contact pattern of a circuit board for surface mounted semiconductor device packages. Accordingly, Figure 5a illustrates a contact pattern usable by packages having the layout type of the first type, as illustrated in Figures 2a and 2b. The contact pattern 50a includes a contact 180, e.g., a gate contact, and source contacts 200a and 200b. This contact pattern 50a accommodates both packages 10a and 10b of Figures 2a and 2b respectively.

[0025] Similarly, Figure 5b illustrates a circuit board contact pattern usable for packages having the layout type of the third type, as illustrated in Figures 4a and 4d. The contact pattern 50b includes a contact 180, e.g., a gate contact, and contacts 240a – 240p. This contact pattern 50b accommodates packages 40a – 40d of Figures 4a – 2d respectively.

[0026] The circuit board contact pattern of the present invention enables the end-users to design and modify circuits to use packages having various layouts of surface contacts without having to redesign the circuit board. The contact pattern of the circuit board will accommodate the surface mounted packages without having to match the exact number and pattern of the packages' contact pads.

[0027] Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein.

WHAT IS CLAIMED IS:

1. An apparatus for coupling one of a plurality of surface mounted semiconductor device packages to a circuit board, each package including a semiconductor device die and a metal clip including a flat web portion having a bottom surface and at least one peripheral rim portion extending from an edge of said flat web portion, said bottom surface containing spaced solderable planar metal pads on a bottom surface of said die, the contact pads being formed in a plurality of different layouts having one or more columns and one or more rows, the apparatus comprising:

a circuit board contact pattern including one or more columns and one or more rows of contacts, a number of rows being equal to a largest number of contact pad rows in the plurality of contact pad layouts, a number of columns being equal to a largest number of contact pad columns in the plurality of contact pad layouts,

wherein the circuit board contact pattern is usable by all of the plurality of the contact pad layouts of the plurality of semiconductor device packages.

2. The apparatus of claim 1, wherein each of the plurality of semiconductor device packages further comprises unique width and length parameters of the die.

3. The apparatus of claim 1, wherein each of the plurality of semiconductor device packages further comprises contact pads having a unique shape.

4. The apparatus of claim 1, wherein each of the plurality of semiconductor device packages includes a different layout and number of the contact pads.

5. The apparatus of claim 1, wherein each of the plurality of semiconductor device packages includes a first contact pad and one or more second contact pads, the one or more second contact pads being formed into rows and columns.

6. The apparatus of claim 5, wherein the number of rows is in a range from one to four.

7. The apparatus of claim 5, wherein the number of columns is in a range from one to four.

8. An apparatus for coupling a surface mounted semiconductor device package including a semiconductor device die having contact pads to a circuit board, the contact pads having a plurality of layouts including one or more columns and one or more rows, the apparatus comprising:

a circuit board contact pattern including a number of columns equal to a most extensive number of contact pads column wise in the plurality of layouts and a number of rows equal to a most extensive number of contact pads row wise in the plurality of layouts, wherein the circuit board contact pattern accommodates all of the semiconductor device packages.

9. An apparatus for coupling a surface mounted semiconductor device package including a semiconductor device die having contact pads to a circuit board, the contact pads having one or more layouts, the apparatus comprising a circuit board contact pattern able to accommodate the one or more layouts of the contact pads of the semiconductor device packages.

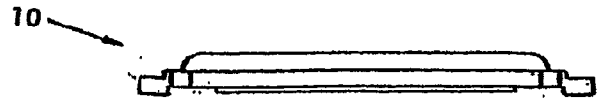


FIG.1

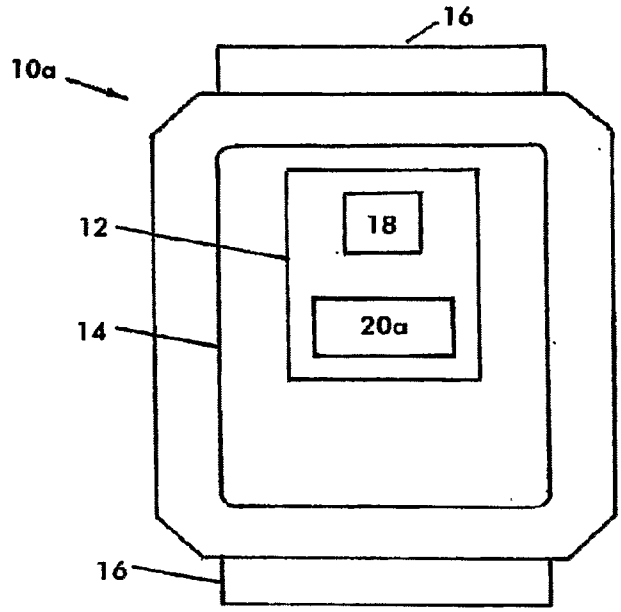


FIG.2a

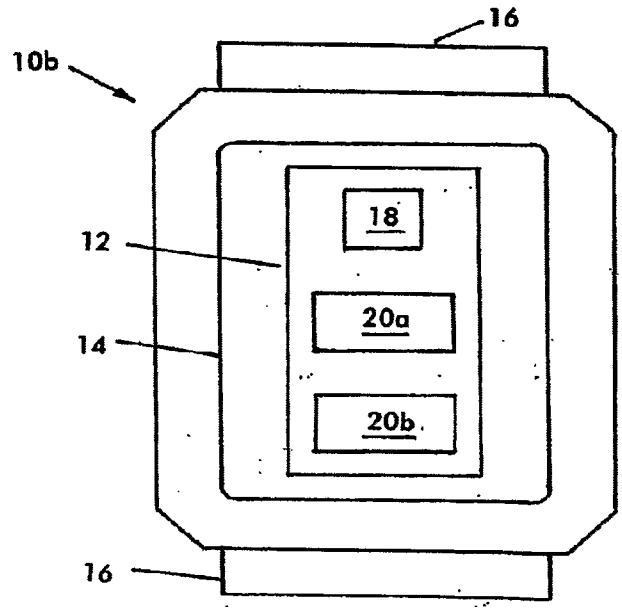


FIG.2b

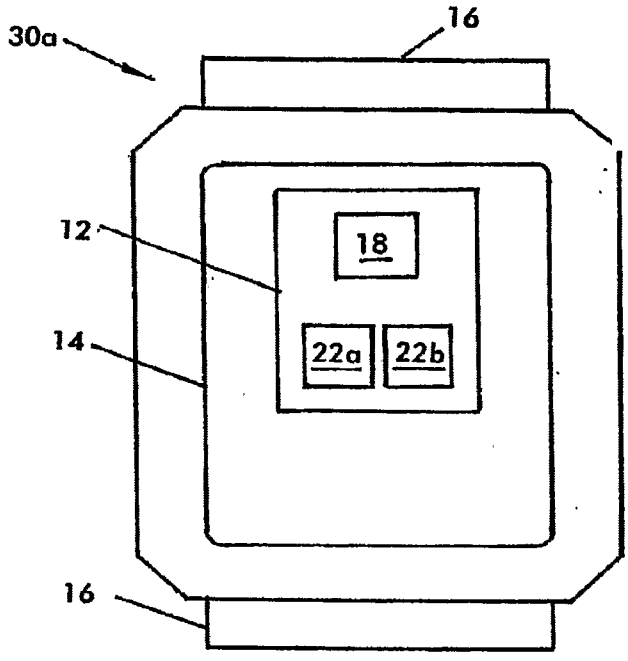


FIG.3a

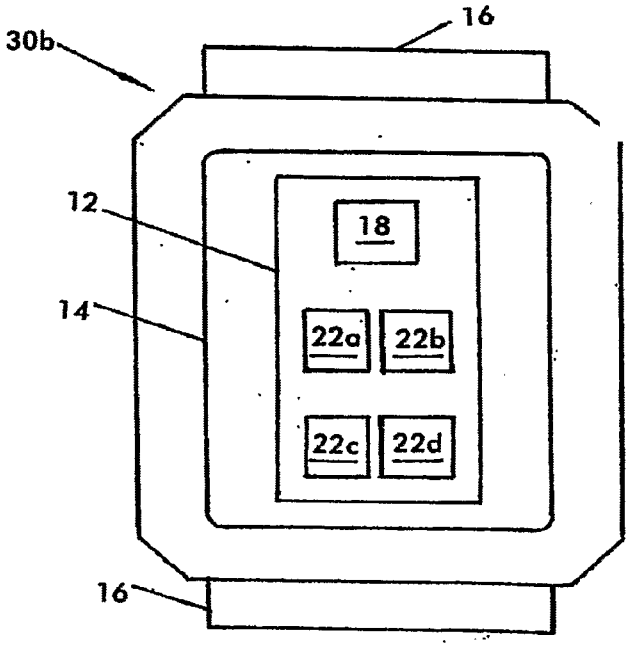


FIG.3b

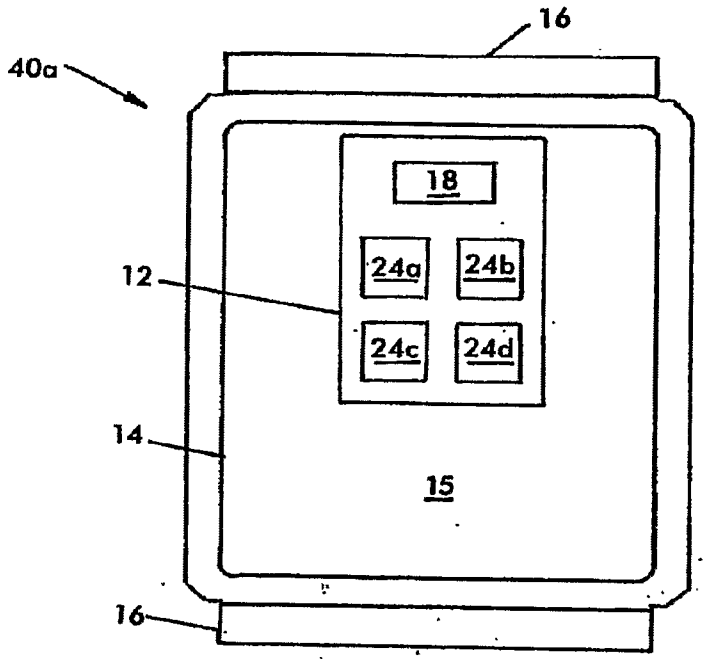

16
40a
18
12
24a
24b
24c
24d
14
15
16

FIG.4a

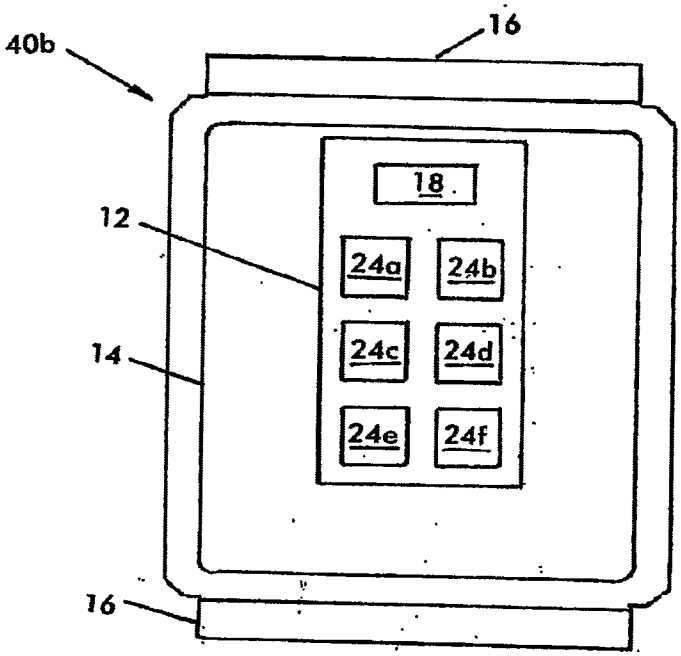

16
40b
18
12
24a
24b
14
24c
24d
24e
24f
16

FIG.4b

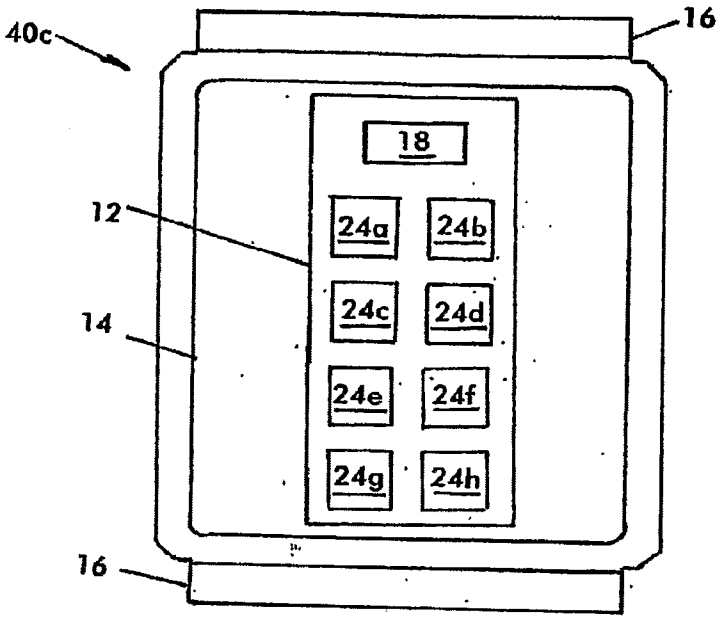

40c
16
18
12
24a
24b
14
24c
24d
24e
24f
24g
24h
16

FIG.4c

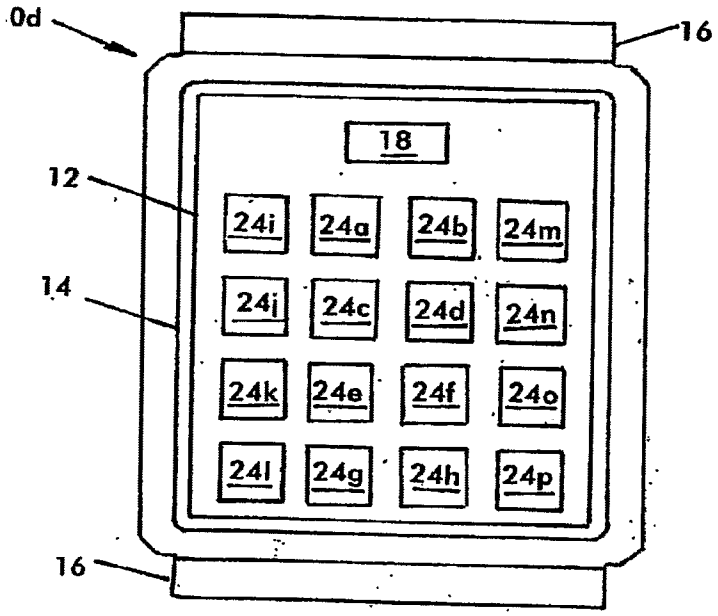

0d
16
18
12
24i
24a
24b
24m
14
24j
24c
24d
24n
24k
24e
24f
24o
24l
24g
24h
24p
16

FIG.4d

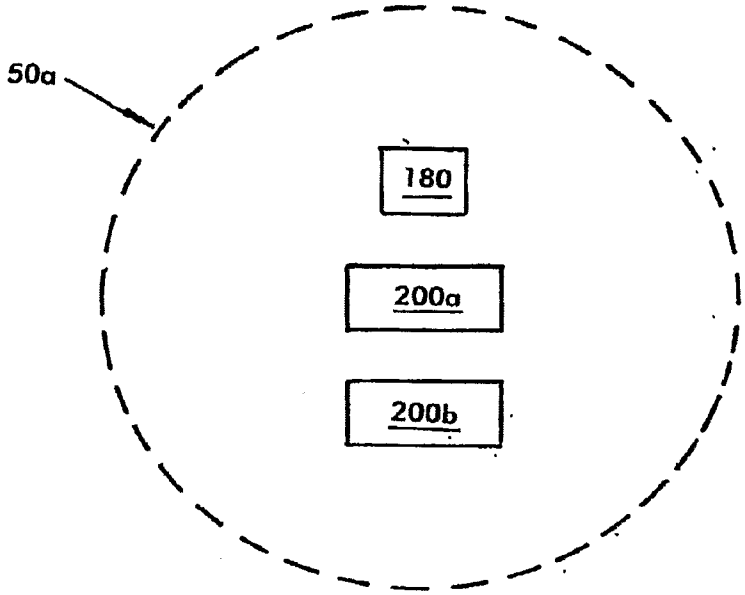

50a
180
200a
200b

FIG.5a

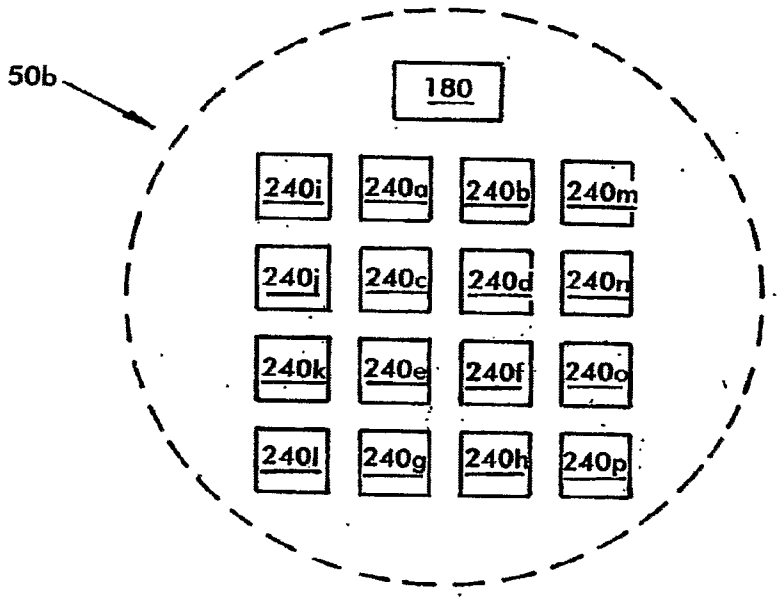

50b
180
240i
240a
240b
240m
240j
240c
240d
240n
240k
240e
240f
240o
240l
240g
240h
240p

FIG.5b