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(54) **METHOD AND APPARATUS FOR ITERATIVE TIMING AND CARRIER RECOVERY**

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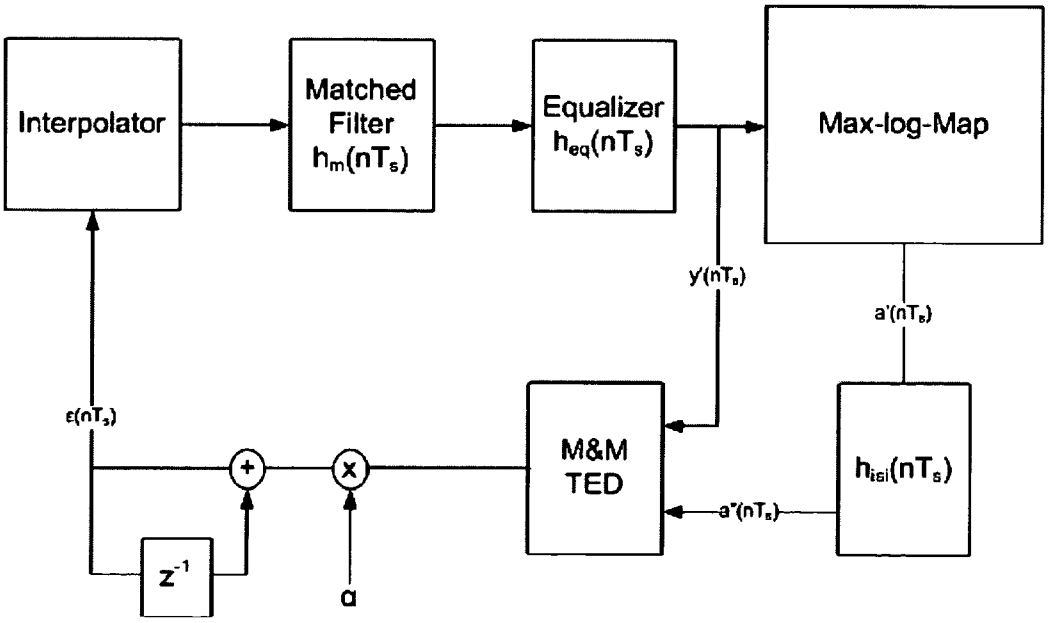
(57) **ABSTRACT**

Method and apparatus for iterative timing recovery for FTN signaling are provided. The iterative timing recovery method and apparatus uses a feedback timing error signal from a forward error correction block with an additional equalizer prior to a maximum a posteriori (MAP) decoder which matches the equalized FTN signal to a truncated inter-symbol interference (ISI) target. A timing error is then generated using a modified M&M timing error detector.



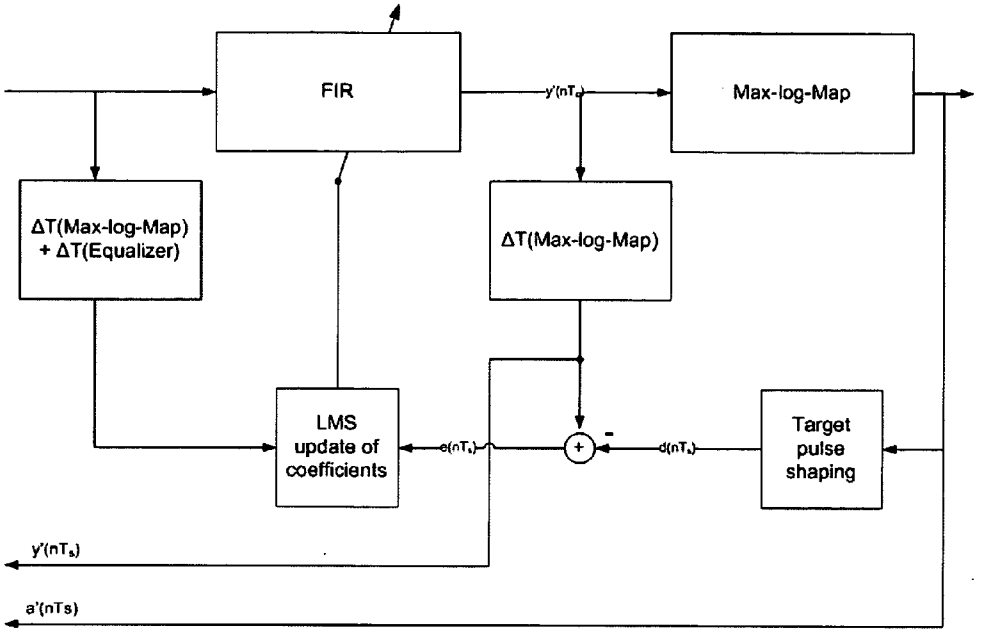


Figure 1

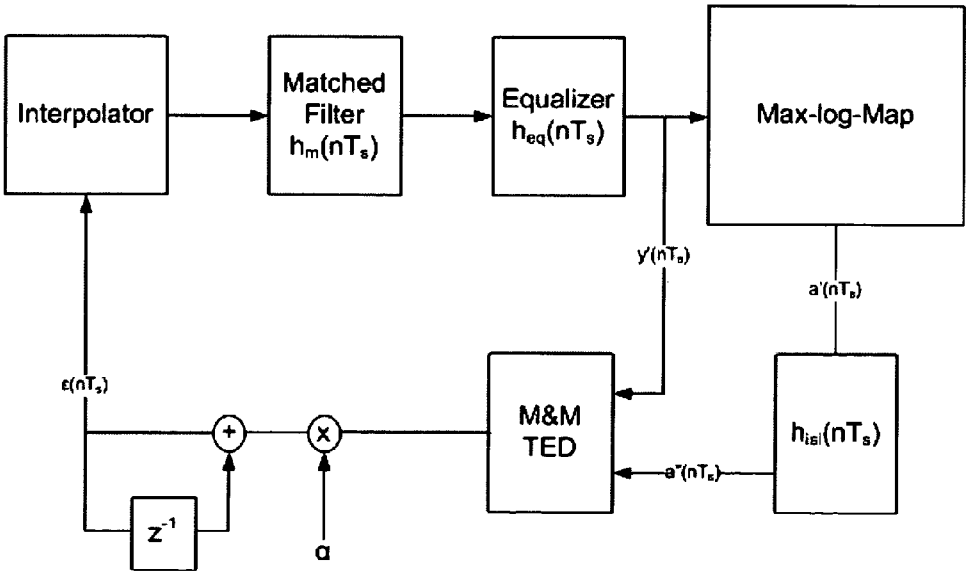


Figure 2

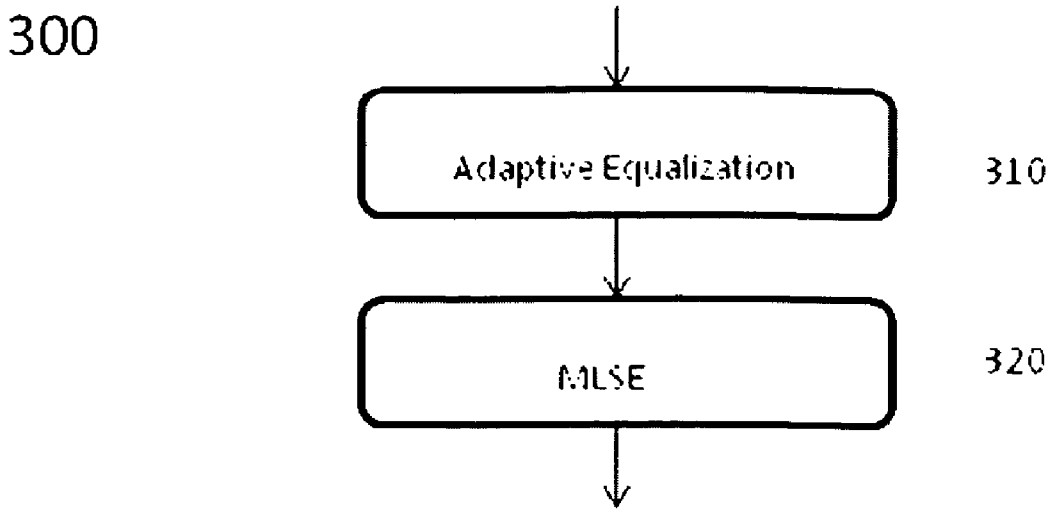


Figure 3

400

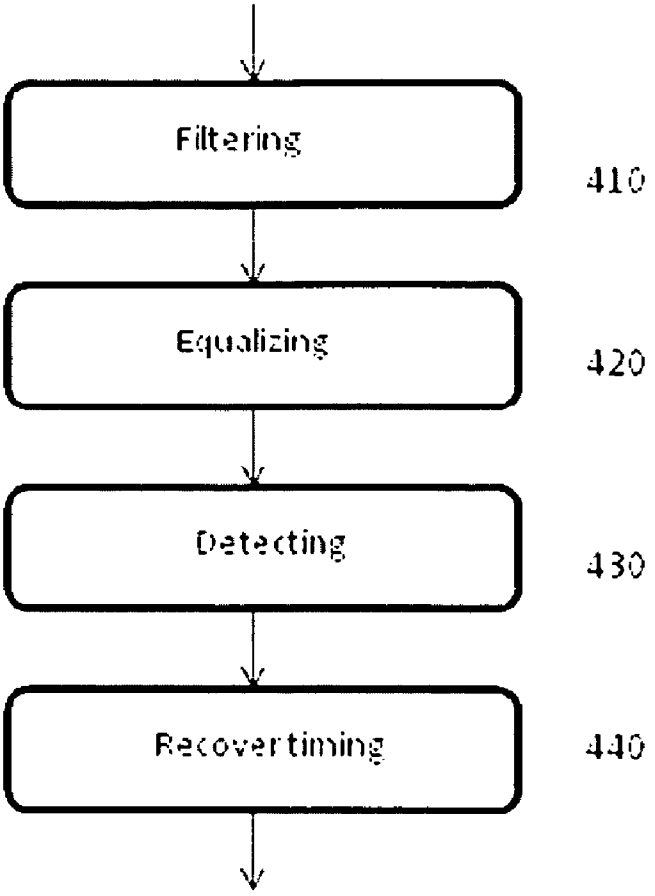

Filtering
410
Equalizing
420
Detecting
430
Recovertiming
440

Figure 4

METHOD AND APPARATUS FOR ITERATIVE TIMING AND CARRIER RECOVERY

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Application Ser. No. 61/217,333, entitled "SYSTEM AND METHODS FOR SATELLITE SYSTEMS," filed May 29, 2009 which is incorporated by reference herein in its entirety.

FIELD OF THE INVENTION

[0002] The present principles relate to iterative timing recovery in receivers systems.

BACKGROUND OF THE INVENTION

[0003] Carrier recovery schemes can be classified into two structures: feed-forward structure and feedback structure.

[0004] The feedback carrier recovery uses a digital Phase Locked Loop (PLL) to track out the carrier phase and frequency offset. However, it relies on a decision directed or non-data-aided approach to estimate the phase error at each time instant. In decision-directed approach, the decision errors will cause additional self noise while the non-data-aided approach can only apply to a limited number of multiple phase shift keying (MPSK) formats. Further, the feedback carrier recovery scheme could be disturbed by cycle slips which may cause a large number of errors due to phase ambiguity. Feed forward carrier recovery is used to reduce the probability of cycle slips.

[0005] The feed forward carrier recovery relies on pre-known data symbols (e.g. pilot or sync symbols) embedded in the data stream. This reduces the bandwidth efficiency since no data is transmitted during a pilot or sync interval. The second disadvantage of the feed-forward carrier recovery is the inability to recover large frequency offsets or phase variations due to phase noise between the measurement blocks.

[0006] Faster-than-Nyquist (FTN) signaling has become important for the next generation of transmission systems since FTN allows an easy trade-off between Signal-to-Noise Ratio (SNR), bandwidth (BW) and bit error rate (BER). Timing recovery in FTN signaling becomes a huge challenge due to strong ISI effects when the symbols period is squeezed to get higher bandwidth efficiency.

[0007] Under the principles of the present invention, an iterative timing recovery is suggested for FTN signaling using a feedback timing error signal from the forward error correction (FEC) block. The FEC block could be realized by a so-called soft decoder like Low Density Parity Check (LDPC), a turbo decoder or a soft output Viterbi algorithm (SOVA). In the current idea a MAP decoder is used to match the intersymbol interference (ISI) response of the FTN signal. An additional equalizer is utilized in front of the maximum a posteriori (MAP) decoder which matches the equalized FTN signal to the truncated ISI target. The timing error is then generated by using a modified Mueller and Muller (M&M) timing error detector (TED).

[0008] The iterative symbol timing recovery is used when ISI becomes a severe problem for FTN signaling.

SUMMARY OF THE INVENTION

[0009] These and other drawbacks and disadvantages of the prior art are addressed by the present principles, which are directed to a method and apparatus for iterative timing and carrier recovery in phase shift keying systems.

[0010] According to an aspect of the present principles, there is provided a method for iterative timing recovery. The method comprises performing adaptive equalization and maximum likelihood sequence estimation in order to recover symbol timing.

[0011] According to another aspect of the present principles, there is also provided an apparatus for iterative timing recovery comprising an comprising adaptive equalizer for performing adaptive equalization and a symbol detector for performing maximum likelihood sequence estimation in order to recover symbol timing.

[0012] According to another aspect of the present principles, there is also provided a method for iterative timing recovery comprising filtering an interpolated first error signal using a matched filter, equalizing the filtered interpolated first error signal, detecting a timing error with an M&M timing error detector to produce a second error signal, and using said second error signal to recover the timing of a signal that uses faster-than-Nyquist signaling.

[0013] According to another aspect of the present principles, there is also provided an apparatus for iterative timing recovery. The apparatus comprises a matched filter for filtering an interpolated first error signal using a matched filter, an equalizer for equalizing the filtered interpolated first error signal, a timing error detector for detecting a timing error with an M&M timing error detector to produce a second error signal, and a recovery circuit for using said second error signal to recover the timing of a signal that uses faster-than-Nyquist signaling.

[0014] These and other aspects, features and advantages of the present principles will become apparent from the following detailed description of exemplary embodiments, which is to be read in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] FIG. **1** shows an apparatus for least-mean-square error (LMSE) estimation with equalization for FTN signaling.

[0016] FIG. **2** shows an apparatus for iterative timing recovery for FTN signaling.

[0017] FIG. **3** shows a method for iterative timing recovery.

[0018] FIG. **4** shows a method for iterative timing recovery for FTN signaling.

DETAILED DESCRIPTION

[0019] An approach for iterative time recovery for transmission systems is described herein.

[0020] FTN signaling can be modeled as a channel response with memory. Furthermore, the optimum signal detector in an Additive White Gaussian noise (AWGN) band limited channel is the maximum likelihood detector or maximum a posteriori detector if a priori information is available. It is also clear that the optimum symbol detector for FTN signaling relies not only on the current symbol but also the neighbor symbols. The interference introduced by the neighbor symbols is called inter-symbol interference (ISI). The ISI distorted signals are modeled with a trellis structure and its memory is often infinite. So infinite states in the trellis have to be considered for symbol detection. One way to solve this problem is to reduce the number of states in the decoding process by using sub-optimum decoding structures. In this

disclosure, the idea of Maximum Likelihood Sequence Estimation (MLSE) is used to achieve the optimum detection performance for channels with memory. Nevertheless modifications have to be done on the MLSE by the reduction of the number of states which is realized by the truncation of the ISI response and leads to a suboptimum but realizable symbol detection. It is clear that the truncation skews the frequency response of the ISI distorted signal and so the MLSE is modified to a combination of MLSE and adaptive equalization detection, which is further described herein.

[0021] The Maximum Likelihood Sequence Estimation (MLSE) was first mentioned by Forney and Viterbi [Fo73] and an optimum detection was given by Viterbi [Vit67] with the Viterbi decoder, which estimates the maximum likelihood path (maximum likelihood sequence) through the trellis. Bahl, Cocke, Raviv and Jelinek further improve the maximum likelihood sequence estimation by the BCJR algorithm [BCJR74] which generates soft output values for each symbol decision. In this thesis a BCJR algorithm is described for FTN signal detection whereas the complexity is further reduced by a Max-log-MAP decoder [Ko90] [Er94]. The Max-log-MAP decoder relies on a backward and forward recursion through the trellis. The most important step on the design of a Maximum Likelihood Sequence Estimation (MLSE) decoder is the definition of the state transition probabilities or so-called branch metrics. Therefore the Euclidian distance between the received symbol y and the ISI response targets t(s,s') is evaluated as it is shown in equation

$$X(s,s')=\|y[nT_s]-t(s,s')\|^2 \tag{1}$$

Where s denotes the successor states and s' denotes the current state in the trellis. The targets t(s,s') for each state transition are generated by folding the possible candidates in the channel memory with the truncated ISI response waveform hm with the truncated ISI length L. For a BPSK modulation we get

$$t(s,s')=\sum_{k=0}^{L} a_m h_{m-k} \tag{2}$$

The Max-log-MAP decoding process is then further divided into the forward, backward recursions and the a posteriori log likelihood ratios LLR computation [WH00]. An example for BSPK modulation is provided as following:

$$\text{(1) Forward recursion} \tag{3}$$
$$A_k(s)=\max_{s'}(A_{k-1}(s')+x_k(s',s))$$

$$\text{(2) Backward recursion} \tag{4}$$
$$B_k(s')=\max_{s}(B_{k-1}(s)+x_k(s',s))$$

$$\text{(3) } A \text{ posteriori } LLR \text{ computation} \tag{5}$$
$$L(u_k \mid y_k)=\max_{u_k=1}(A_{k-1}(s')+B_k(s)+x_k(s',s))-\max_{u_k=0}(A_{k-1}(s')+B_k(s)+x_k(s',s))$$

Note that the subscript k denotes the time index of the trellis.

[0022] We mention that the truncated ISI response has to be used to implement a realizable MLSE detector. Note that there is still an amplitude difference between the truncated ISI response $H_{ISI}(j)$ and the true ISI response $H_{post}(j)$. Therefore an adaptive equalizer should be used before the MLSE detector. To adapt the equalizer the least-mean-square error (LMSE) adaptation [Hay01] is used. The LMSE adaptation minimizes the least mean square error between the equalized symbol $y'(nT_s)$ and the desired symbol $d(nT_s)$ given in following equation.

$$e(nT_s)=y(nT_s)-d(nT_s) \tag{6}$$

The LMSE with equalization is shown in FIG. **1**. The filter coefficient vector $w(nT_s)$ can be expressed as following:

$$w(nT_s)=w((n-1)T_s)+\mu[e(nT_s)\times(nT_s)], \tag{7}$$

where $x(nT_s)=[y(nT_s), y((n-1)T_s), \ldots, y((n-L+1)T_s)]^T$, L the length of the FIR filter and $(\square)^T$ represent the transpose operation and μ is the step size.

[0023] The performance of the classical timing error detection degrades when FTN signaling is used. A modified symbol detector based on MLSE equalization is mentioned above. To improve the timing error detector performance of the fine step in the two-step approach proposed in another disclosure by the applicant, an MLSE equalization iterative timing error detector is proposed in this disclosure. To implement the iterative timing recovery the equation for the iterative search processing for the timing error $\epsilon'(nT_s)$ based on steepest descent given in [MMF98] is adapted to our system.

$$\varepsilon'((n+1)T)_s=\varepsilon'(nT_s)+\alpha\frac{\partial}{\partial\varepsilon'}L(y(nT_s)\mid a,\varepsilon') \tag{8}$$

[0024] To maximize the objective function $L(y(nT_s)|a, \epsilon')$ regarding the timing error ϵ' we use a modified M&M timing error detector to consider the ISI distortion in the timing error estimation. The modified M&M timing error detector is then given as

$$\epsilon'(nT_s)=Re[(a''(nT_s))^*y'(nT_s-T_s+\epsilon)-(a''(nT_s-T_s))^*y'(nT_s+\epsilon)], \tag{9}$$

where $y'(nT_s)$ is the equalizer output, $a'(nT_s)$ denotes the current decision from the MAX-LOG-MAP decoder and $a'(nT_s)$ is convolved with truncated impulse response to produce $a''(nT_s)$ using Equation (2). The proposed iterative timing recovery for FTN signaling is shown in FIG. **2**.

[0025] One embodiment of the present principles is illustrated in FIG. **1**, which shows an apparatus for iterative timing recovery. An FIR filter is used to filter an input signal. The input signal is also in signal communication with a first Max-log-Map and Equalizer block. The FIR filter has coefficients under control by a Least Mean Squared (LMS) block. The LMS block takes as input the output of the first Max-log-Map and Equalizer block, and the output of a summing circuit. The summing circuit has a non-inverting input that is in signal communication with a second Max-log-Map circuit, and a second inverting input coming from a target pulse shaping circuit. The FIR filter output is in signal communication with the second Max-log-Map circuit and a third Max-log-Map circuit. The output of the third Max-log-Map circuit is in signal communication with the input of the target pulse shaping block and is used as an output of the apparatus. The output of the second Max-log-Map circuit is also an output of the apparatus that is representative of the equalized symbol.

[0026] Another embodiment of the present principles is illustrated in FIG. **2**, which shows an apparatus for iterative timing recovery for faster-than-Nyquist (FTN) signaling. An

interpolator output is in signal communication with the input of a matched filter, whose output is in signal communication with an equalizer. The equalizer output is in signal communication with a Max-log-Map block, and in signal communication with a first input of an Mueller & Muller (M&M) timing error detector (TED) block. The Max-log-Map block's output is in signal communication with the input of an inter-symbol interference (ISI) filter, whose output is in signal communication with a second input of the M&M TED. The M&M TED's output is in signal communication with a first input of a multiplier circuit, whose second input is a variable. The output of the multiplier circuit is in signal communication with a first non-inverting input of a summing circuit, whose second input is a delayed version of the summing circuit output, which is also in signal communication with the interpolator input.

[0027] Another embodiment of the present principles is illustrated by FIG. **3**, which shows a method for interative timing recovery. The method is comprised of an adaptive equalization step **310** and a Mean Least Squared estimation step **320**.

[0028] Another embodiment of the present principles is illustrated by FIG. **4**, which shows a method for itnerative timing recovery for FTN signaling, comprising the steps of filtering **410**, equalizing **420**, detecting **430** and recovering timing **440**.

[0029] The functions of the various elements shown in the figures may be provided through the use of dedicated hardware as well as hardware capable of executing software in association with appropriate software. When provided by a processor, the functions may be provided by a single dedicated processor, by a single shared processor, or by a plurality of individual processors, some of which may be shared. Moreover, explicit use of the term "processor" or "controller" should not be construed to refer exclusively to hardware capable of executing software, and may implicitly include, without limitation, digital signal processor ("DSP") hardware, read-only memory ("ROM") for storing software, random access memory ("RAM"), and non-volatile storage.

[0030] Other hardware, conventional and/or custom, may also be included. Similarly, any switches shown in the figures are conceptual only. Their function may be carried out through the operation of program logic, through dedicated logic, through the interaction of program control and dedicated logic, or even manually, the particular technique being selectable by the implementer as more specifically understood from the context.

A description will now be given of the many attendant advantages and features of the present principles, some of which have been mentioned above. For example, one advantage is a method for iterative timing recovery comprising performing adaptive equalization and maximum likelihood sequence estimation in order to recover symbol timing. Another advantage is an apparatus for iterative timing recovery comprising an comprising adaptive equalizer for performing adaptive equalization and a symbol detector for performing maximum likelihood sequence estimation in order to recover symbol timing. Another advantage is a method for iterative timing recovery comprising filtering an interpolated first error signal using a matched filter, equalizing the filtered interpolated first error signal, detecting a timing error with an M&M timing error detector to produce a second error signal, and using said second error signal to recover the timing of a signal that uses faster-than-Nyquist signaling. Yet another advantage is an apparatus for iterative timing recovery comprising a matched filter for filtering an interpolated first error signal using a matched filter, an equalizer for equalizing the filtered interpolated first error signal, a timing error detector for detecting a timing error with an M&M timing error detector to produce a second error signal, and a recovery circuit for using said second error signal to recover the timing of a signal that uses faster-than-Nyquist signaling.

[0031] The present description illustrates the present principles. It will thus be appreciated that those skilled in the art will be able to devise various arrangements that, although not explicitly described or shown herein, embody the present principles and are included within its spirit and scope.

[0032] All examples and conditional language recited herein are intended for pedagogical purposes to aid the reader in understanding the present principles and the concepts contributed by the inventor(s) to furthering the art, and are to be construed as being without limitation to such specifically recited examples and conditions.

[0033] Moreover, all statements herein reciting principles, aspects, and embodiments of the present principles, as well as specific examples thereof, are intended to encompass both structural and functional equivalents thereof. Additionally, it is intended that such equivalents include both currently known equivalents as well as equivalents developed in the future, i.e., any elements developed that perform the same function, regardless of structure.

[0034] Thus, for example, it will be appreciated by those skilled in the art that the block diagrams presented herein represent conceptual views of illustrative circuitry embodying the present principles. Similarly, it will be appreciated that any flow charts, flow diagrams, state transition diagrams, pseudocode, and the like represent various processes which may be substantially represented in computer readable media and so executed by a computer or processor, whether or not such computer or processor is explicitly shown.

[0035] In the claims hereof, any element expressed as a means for performing a specified function is intended to encompass any way of performing that function including, for example, a) a combination of circuit elements that performs that function or b) software in any form, including, therefore, firmware, microcode or the like, combined with appropriate circuitry for executing that software to perform the function. The present principles as defined by such claims reside in the fact that the functionalities provided by the various recited means are combined and brought together in the manner which the claims call for. It is thus regarded that any means that can provide those functionalities are equivalent to those shown herein.

[0036] Reference in the specification to "one embodiment" or "an embodiment" of the present principles, as well as other variations thereof, means that a particular feature, structure, characteristic, and so forth described in connection with the embodiment is included in at least one embodiment of the present principles. Thus, the appearances of the phrase "in one embodiment" or "in an embodiment", as well any other variations, appearing in various places throughout the specification are not necessarily all referring to the same embodiment.

1. A method for iterative timing recovery, comprising:
performing adaptive equalization on an input signal;
performing maximum likelihood sequence estimation on the adaptively equalized input signal to detect symbol timing.

2. An apparatus for symbol timing recovery, comprising:
an adaptive equalizer for performing adaptive equalization on an input signal;
a symbol detector for performing maximum likelihood sequence estimation on the adaptively equalized input signal to detect symbol timing.

3. A method for iterative timing recovery, comprising:
filtering an interpolated first error signal using a matched filter;
equalizing the filtered interpolated first error signal;
detecting a timing error with an M&M timing error detector to produce a second error signal.
using said second error signal to recover the timing of a signal that uses faster-than-Nyquist signaling.

4. An apparatus for iterative timing recovery, comprising:
a matched filter for filtering an interpolated first error signal using;
an equalizer for equalizing the filtered interpolated first error signal;
a timing error detector for detecting a timing error with an M&M timing error detector to produce a second error signal.
a recovery circuit for recovering the timing of a signal that uses faster-than-Nyquist signaling using said second error signal.

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