(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
25 April 2013 (25.04.2013)

(10) International Publication Number
WO 2013/059181 A1

(51) International Patent Classification:
H01L 25/10 (2006.01) *H01L 23/498* (2006.01) *H01L 23/31* (2006.01) *H01L 21/48* (2006.01) *H01L 23/495* (2006.01)

(21) International Application Number: PCT/US2012/060402

(22) International Filing Date: 16 October 2012 (16.10.2012)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
61/547,930 17 October 2011 (17.10.2011) US
13/405,108 24 February 2012 (24.02.2012) US
13/404,458 24 February 2012 (24.02.2012) US
13/404,408 24 February 2012 (24.02.2012) US

(71) Applicant: **INVENSAS CORPORATION** [US/US]; 2702 Orchard Parkway, San Jose, CA 95134 (US).

(72) Inventors: **CHAU, Ellis**; c/o Invensas Corporation, 2702 Orchard Parkway, San Jose, CA 95134 (US). **CO, Reynaldo**; c/o Invensas Corporation, 2702 Orchard Parkway, San Jose, CA 95134 (US). **ALATORRE, Roseann**; c/o Invensas Corporation, 2702 Orchard Parkway, San Jose, CA 95134 (US). **DAMBERG, Philip**; 22117 Clearcreek Court, Cupertino, CA 95014 (US). **WANG, Wei-shun**; c/o Invensas Corporation, 2702 Orchard Parkway, San Jose, CA 95134 (US). **YANG, Se, Young**; c/o Invensas Corporation, 2702 Orchard Parkway, San Jose, CA 95134 (US). **ZHAO, Zhijun**; c/o Invensas Corporation, 2702 Orchard Parkway, San Jose, CA 95134 (US).

(74) Agents: **HAGES, Michael, T.** et al.; Lerner, David, Littenberg, Krumholz, & Mentlik, LLP, 600 South Avenue West, Westfield, NJ 07090 (US).

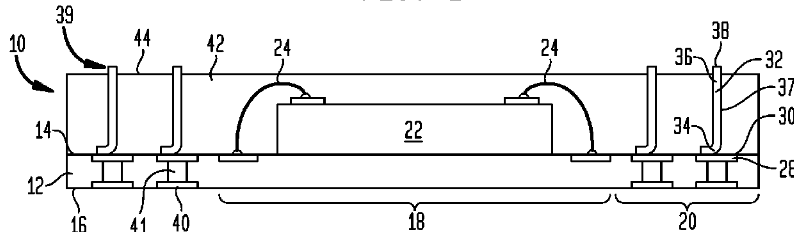
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:
— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:
— *with international search report (Art. 21(3))*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

(54) **Title**: PACKAGE-ON-PACKAGE ASSEMBLY WITH WIRE BOND VIAS



(57) **Abstract**: A microelectronic package (10) can include wire bonds (32) having bases (34) bonded to respective conductive elements (28) on a substrate (12) and ends (36) opposite the bases (34). A dielectric encapsulation layer (42) extends from the substrate (12) and covers portions of the wire bonds (32) such that covered portions of the wire bonds (32) are separated from one another by the encapsulation layer (42), wherein unencapsulated portions (39) of the wire bonds (32) are defined by portions of the wire bonds (32) which are uncovered by the encapsulation layer (42). Unencapsulated portions (39) can be disposed at positions in a pattern having a minimum pitch which is greater than a first minimum pitch between bases (34) of adjacent wire bonds (32).

WO 2013/059181 A1

PACKAGE-ON-PACKAGE ASSEMBLY WITH WIRE BOND VIAS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application is a continuation of U.S. Patent Application Nos. 13/404,408; 13/404,458; and 13/405,108, all of which were filed on February 24, 2012, are entitled Package-On-Package Assembly with Wire Bond Vias, and claim the benefit of the filing date of U.S. Provisional Patent Application No. 61/547,930 filed October 17, 2011, the disclosures of which is incorporated by reference herein.

BACKGROUND OF THE INVENTION

[0002] Microelectronic devices such as semiconductor chips typically require many input and output connections to other electronic components. The input and output contacts of a semiconductor chip or other comparable device are generally disposed in grid-like patterns that substantially cover a surface of the device (commonly referred to as an "area array") or in elongated rows which may extend parallel to and adjacent each edge of the device's front surface, or in the center of the front surface. Typically, devices such as chips must be physically mounted on a substrate such as a printed circuit board, and the contacts of the device must be electrically connected to electrically conductive features of the circuit board.

[0003] Semiconductor chips are commonly provided in packages that facilitate handling of the chip during manufacture and during mounting of the chip on an external substrate such as a circuit board or other circuit panel. For example, many semiconductor chips are provided in packages suitable for surface mounting. Numerous packages of this general type have been proposed for various applications. Most commonly, such packages include a dielectric element, commonly referred to as a "chip carrier" with terminals formed

as plated or etched metallic structures on the dielectric. These terminals typically are connected to the contacts of the chip itself by features such as thin traces extending along the chip carrier itself and by fine leads or wires extending between the contacts of the chip and the terminals or traces. In a surface mounting operation, the package is placed onto a circuit board so that each terminal on the package is aligned with a corresponding contact pad on the circuit board. Solder or other bonding material is provided between the terminals and the contact pads. The package can be permanently bonded in place by heating the assembly so as to melt or "reflow" the solder or otherwise activate the bonding material.

[0004] Many packages include solder masses in the form of solder balls, typically about 0.1 mm and about 0.8 mm (5 and 30 mils) in diameter, attached to the terminals of the package. A package having an array of solder balls projecting from its bottom surface is commonly referred to as a ball grid array or "BGA" package. Other packages, referred to as land grid array or "LGA" packages are secured to the substrate by thin layers or lands formed from solder. Packages of this type can be quite compact. Certain packages, commonly referred to as "chip scale packages," occupy an area of the circuit board equal to, or only slightly larger than, the area of the device incorporated in the package. This is advantageous in that it reduces the overall size of the assembly and permits the use of short interconnections between various devices on the substrate, which in turn limits signal propagation time between devices and thus facilitates operation of the assembly at high speeds.

[0005] Packaged semiconductor chips are often provided in "stacked" arrangements, wherein one package is provided, for example, on a circuit board, and another package is mounted on top of the first package. These arrangements can allow a

number of different chips to be mounted within a single footprint on a circuit board and can further facilitate high-speed operation by providing a short interconnection between packages. Often, this interconnect distance is only slightly larger than the thickness of the chip itself. For interconnection to be achieved within a stack of chip packages, it is necessary to provide structures for mechanical and electrical connection on both sides of each package (except for the topmost package). This has been done, for example, by providing contact pads or lands on both sides of the substrate to which the chip is mounted, the pads being connected through the substrate by conductive vias or the like. Solder balls or the like have been used to bridge the gap between the contacts on the top of a lower substrate to the contacts on the bottom of the next higher substrate. The solder balls must be higher than the height of the chip in order to connect the contacts. Examples of stacked chip arrangements and interconnect structures are provided in U.S. Patent App. Pub. No. 2010/0232129 ("the '129 Publication"), the disclosure of which is incorporated by reference herein in its entirety.

[0006] Microcontact elements in the form of elongated posts or pins may be used to connect microelectronic packages to circuit boards and for other connections in microelectronic packaging. In some instances, microcontacts have been formed by etching a metallic structure including one or more metallic layers to form the microcontacts. The etching process limits the size of the microcontacts. Conventional etching processes typically cannot form microcontacts with a large ratio of height to maximum width, referred to herein as "aspect ratio". It has been difficult or impossible to form arrays of microcontacts with appreciable height and very small pitch or spacing between adjacent microcontacts. Moreover, the

configurations of the microcontacts formed by conventional etching processes are limited.

[0007] Despite all of the above-described advances in the art, still further improvements in making and testing microelectronic packages would be desirable.

SUMMARY OF THE INVENTION

[0008] A microelectronic package can include wire bonds having bases bonded to respective conductive elements on a substrate and ends opposite the bases. A dielectric encapsulation layer extending from the substrate covers portions of the wire bonds such that covered portions of the wire bonds are separated from one another by the encapsulation layer, wherein unencapsulated portions of the wire bonds are defined by portions of the wire bonds which are uncovered by the encapsulation layer. Unencapsulated portions can be disposed at positions in a pattern having a minimum pitch which is greater than a first minimum pitch between bases of adjacent wire bonds.

[0009] Various package structures are disclosed herein which incorporate wire bonds functioning as vertical connections extending upwardly from conductive elements, e.g., conductive pads on a substrate. Such wire bonds can be used in making package on package electrical connections with a microelectronic package overlying a surface of a dielectric encapsulation. In addition, various embodiments of methods are disclosed herein for making a microelectronic package or a microelectronic assembly.

[0010] A microelectronic package according to an aspect of the invention can include a substrate having a first region and a second region, the substrate having a first surface and a second surface remote from the first surface. One or more microelectronic elements may overlie the first surface within the first region. Electrically conductive elements can be

exposed at at least one of the first surface and the second surface of the substrate, and the conductive elements can be exposed within the second region. Some or all of the conductive elements can be electrically connected with the at least one microelectronic element.

[0011] Wire bonds can define edge surfaces and have bases bonded to respective ones of the conductive elements. The bases of the wire bonds can include first portions of the edge surfaces that extend along the conductive elements, and have respective second portions of the edge surfaces disposed at an angle between 25° and 90° relative to the first portions. The wire bonds can have ends remote from the substrate and remote from the bases, e.g., at locations opposite from the bases.

[0012] A dielectric encapsulation layer can extend from at least one of the first or second surfaces. The encapsulation layer may cover portions of the wire bonds such that covered portions of the wire bonds are separated from one another by the encapsulation layer. The encapsulation layer may overlie the second region of the substrate and may overlie another portion such as the first region. Unencapsulated portions of the wire bonds can be defined by portions of the wire bonds that are uncovered by the encapsulation layer. The unencapsulated portions can include the ends. The conductive elements can be disposed at positions in a pattern having a first minimum pitch between respective adjacent conductive elements of the plurality of conductive elements. The unencapsulated portions can be disposed in positions in a pattern having a second minimum pitch between respective ends of adjacent wire bonds of the plurality of wire bonds. In one example, the second pitch can be greater than the first pitch.

[0013] In one example, the angle at which respective portions of the edge surfaces can be disposed can measure between 80° and 90°.

[0014] In one example, each of at least some of the unencapsulated portions of the wire bonds includes a ball-shaped portion. The ball-shaped portion can be integral with a cylindrical portion of such wire bond. In one example, each ball-shaped portion and each cylindrical portion can have at least a core consisting essentially of copper, copper alloy or gold. In one example, the cylindrical portions integral with the ball-shaped portions project beyond a surface of the encapsulation layer.

[0015] In one example, at least some of the wire bonds have a core of a primary metal and a metallic finish including a second metal different from the primary metal overlying the primary metal. In one example, the primary metal can be copper and the metallic finish may include a layer of silver.

[0016] In one example, the conductive elements can be first conductive elements. The microelectronic package can further include a plurality of second conductive elements electrically connected to the unencapsulated portions of the wire bonds, and the second conductive elements may not contact the first conductive elements. In one example, the second conductive elements can be formed by plating in contact with the unencapsulated portions of the wire bonds after forming the encapsulation layer.

[0017] In one example, an end of at least one of the wire bonds can be displaced in a direction parallel to the first surface of the substrate from its base by at least a distance equal to one of: a minimum pitch between the conductive elements, and 100 microns. One or more of the wire bonds can include at least one bend between the base thereof and the unencapsulated portion thereof. The bend of the at least one wire bond can be at a location remote from the base thereof and the unencapsulated portion thereof. In one example, a radius of the bend can be greater than twelve times a diameter

of a cylindrical portion of the at least one wire bond. In one example, the radius of the bend can be less than ten times a diameter of a cylindrical portion of the at least one wire bond. In one example, the unencapsulated portion of the at least one wire bond may project above the encapsulation layer in a direction within 25 degrees of perpendicular relative to the first surface of the substrate.

[0018] In one example, some or all of the conductive elements can be non-solder mask defined.

[0019] In one example, ball bonds can be joined to and overlying portions of the bases of the wire bonds.

[0020] In one example, the at least one microelectronic element can include first and second microelectronic elements overlying the first surface within the first region. Some or all of the conductive elements can be connected with the first microelectronic element, and some or all of the conductive elements can be connected with the second microelectronic element. The first microelectronic element and the second microelectronic element can be electrically connected with one another within the microelectronic package.

[0021] In accordance with an aspect of the invention, the encapsulation layer may have a major surface and an alignment surface sloped with respect to the major surface. At least one unencapsulated portion of a wire bond can be positioned on the major surface with the alignment surface proximate to the major surface at a location adjacent to the unencapsulated portion. In such way, the alignment surface can be configured to guide an electrically conductive protrusion disposed above the alignment surface towards the unencapsulated portion of the wire bond. In one example, the protrusion can include a bond metal, such as a solder ball attached to a circuit element, among other possible configurations.

[0022] In one example, the encapsulation layer can define a corner region thereof, the encapsulation layer further including at least one minor surface positioned within the corner region and being positioned farther from the substrate than the major surface. The alignment surface may extend between the minor surface and the major surface. In one example, the major surface can be a first major surface that overlies the first region of the substrate. The encapsulation layer can further define a second major surface overlying the second region and being positioned closer to the substrate than the major surface. The alignment surface can extend between the first and second major surfaces.

[0023] A microelectronic assembly according to an aspect of the invention can include a first microelectronic package having an alignment surface as described in the foregoing, and a second microelectronic package having a front surface and terminals on the front surface. A plurality of conductive protrusions connects at least some of the unencapsulated portions of the wire bonds with respective ones of the terminals. In such assembly, at least one of the conductive protrusions can be positioned in contact with a portion of the alignment surface. In one example, the conductive protrusions can include solder balls.

[0024] In a variation of a microelectronic package as set forth above, ball bonds can be provided atop at least some of the conductive elements, and edge surfaces of the wire bonds which define the bases of the wire bonds can be formed on and joined to such ball bonds atop the conductive elements.

[0025] In accordance with an aspect of the invention, a microelectronic assembly can be provided which includes a first microelectronic package as set forth in the foregoing, the first microelectronic package having a plurality of terminals exposed at a second surface of the substrate

opposite from the first surface, and the first microelectronic package having peripheral edges extending in a direction between the first and second surfaces of the substrate. A second microelectronic package can have a substrate having contacts thereon, and a second microelectronic element electrically connected with the contacts. The second microelectronic package can have terminals exposed at a surface of such substrate which are electrically connected with the second microelectronic element through the contacts. The terminals of the second microelectronic element can face and be electrically connected with respective unencapsulated portions of the wire bonds.

[0026] A circuit panel can have a first surface and panel contacts exposed at the surface thereof. The first microelectronic package can overlie the circuit panel and have terminals joined to the panel contacts of the circuit panel. A monolithic underfill can overlie at least one of the peripheral edges of the first microelectronic package and be disposed within spaces surrounding the joints between the terminals of the first microelectronic package and the panel contacts of the circuit panel. The underfill can be disposed within spaces surrounding the joints between the terminals of the second microelectronic package and the first microelectronic package.

[0027] In a microelectronic package according to a particular example, the encapsulation layer can define a first surface portion at a first height above the first surface in an area overlying the first region of the substrate, and a second surface portion at a second height above the first surface in an area overlying the second region of the substrate. The second height can be less than the first height. In one example, the microelectronic element can have

a front face spaced above the first surface at a third height. The second height may be less than the third height.

[0028] In a microelectronic package according to a particular example, instead of having edge surfaces bonded, e.g., joined to conductive elements of the substrate, the wire bonds may have ball-bond bases joined to respective ones of the first conductive elements. End surfaces of the wire bonds can be remote from the substrate and remote from the bases at a distance of less than three times a diameter of the base. Each wire bond can define an edge surface extending between the base and the end surface thereof. In one example, the ball bond bases can include a first ball bond joined to the respective conductive elements and second ball bonds joined to the first ball bonds at positions extending from top surfaces of the first ball bonds. The wire bonds can extend between the extending between the end surfaces and the second ball bonds.

[0029] In a microelectronic package according to a particular example, two or more wire bonds can be joined, e.g., bonded to an individual conductive element of the plurality of conductive elements of the substrate. In examples thereof, such wire bonds can be formed with ball bonds bonded to the individual conductive element, or with their edge surfaces bonded to the individual conductive element, or can be formed with a combination of such methods, using techniques such as described herein.

[0030] In a microelectronic package according to an example, the encapsulation layer can be formed to include a major surface and an alignment surface angled with respect to the major surface. The at least one unencapsulated portion of the wire bond can be exposed at the major surface and the alignment surface can extend from the major surface, e.g., intersect with the major surface, at a location in proximity

to the unencapsulated portion such that the alignment surface is configured to guide an electrically conductive protrusion disposed above the alignment surface towards the unencapsulated portion of the wire bond. In one example, the encapsulation layer can be formed to define a corner region thereof and to further include at least one minor surface positioned within the corner region. The minor surface can be positioned farther from the substrate than the major surface. The alignment surface can extend between the minor surface and the major surface.

[0031] In one example, the major surface of the encapsulation layer can be a first major surface that overlies the first region of the substrate. The encapsulation layer can be formed so as to define a second major surface overlying the second region and being positioned closer to the substrate than the major surface. The alignment surface can extend between the minor surface and the major surface.

[0032] A method for making a microelectronic assembly according to an aspect of the invention can include aligning a second microelectronic package with a first microelectronic package as described herein. The second microelectronic package can include a substrate defining a first surface with contacts, e.g., contact pads exposed thereon. In some cases, the contacts can include conductive masses joined thereto. The second microelectronic package can be aligned with the first microelectronic package by moving at least one of the conductive masses into contact with both the alignment surface and at least the end surface of at least one wire bond. Heating or otherwise curing of the conductive masses can be performed to make the electrical connections, e.g., joints between the contacts of the second microelectronic package and the unencapsulated portions of the wire bonds.

[0033] According to an aspect of the invention, a method for making a microelectronic assembly can include aligning a second microelectronic package with a first microelectronic package having a structure such as described herein, wherein a surface of the encapsulation layer extends in a lateral direction beyond an edge of confronting surface of the second microelectronic package. Such method can include depositing an underfill material onto the dispensing area, e.g., either after or possibly before the second microelectronic package is positioned atop the encapsulation layer of the first microelectronic package. The underfill material can then flow into a space defined between the encapsulation layer and the first surface of the substrate of the second microelectronic package. A quantity of the underfill deposited on the dispensing area can flow into the space between confronting surfaces of the first and second microelectronic packages.

[0034] In one example, the second microelectronic package may include four edge surfaces, and the dispensing area can be defined by a portion of the encapsulation layer extending laterally beyond all four edge surfaces to surround the second microelectronic package.

[0035] In one example, the second microelectronic package may include four edge surfaces, and the dispensing area can be defined by a portion of the encapsulation layer extending laterally beyond two adjacent ones of the edge surfaces.

[0036] In one example, the second microelectronic package may include four edge surfaces, and the dispensing area can be defined by a portion of the encapsulation layer extending laterally beyond a single edge surface.

[0037] A method for making a microelectronic assembly according to an aspect of the invention can include positioning first and second microelectronic packages with a plurality of conductive masses between terminals of the

respective packages, e.g., such as to terminals of the first microelectronic package which are defined by the unencapsulated portions of the wire bonds, or which have second conductive elements contacting the unencapsulated portions. A compliant bezel can be assembled around edge surfaces of the first and second microelectronic packages. A joining step can be performed, e.g., by heating, reflowing or otherwise curing the conductive masses to join the respective first contact pads and second contact pads.

[0038] In a method of making a microelectronic package according to one example, a metal wire having a predetermined length can be fed out of a capillary of a bonding tool. A face of the capillary can be moved over first and second surfaces of a forming unit to shape the metal wire segment to have a first portion projecting upwardly in a direction along an exterior wall of the capillary. The bonding tool can be used to bond a second portion of the metal wire to a ball bond joined to a conductive element exposed at a first surface of a substrate. The second portion of the metal wire can be positioned to extend along the conductive element. In one example, the first portion can be positioned at an angle between 25° and 90° to the second portion.

[0039] In a method of making a microelectronic assembly according to one example, a monolithic underfill can be formed surrounding exposed portions of a first microelectronic package such as described above. The monolithic underfill can be formed so as to fill spaces surrounding the joints between the terminals of the first microelectronic package and a circuit panel underlying such package. The step of forming the monolithic underfill can also fill spaces surrounding joints between the terminals of a second microelectronic package disposed above the first microelectronic package, such terminals facing and joined to respective unencapsulated

portions of the wire bonds of the first microelectronic package.

[0040] A method of making a microelectronic package can include forming a sacrificial material layer over a surface of a dielectric encapsulation layer on an in-process unit. The in-process unit may include wire bonds having end surfaces and bases remote from the ends and positioned within the encapsulation layer, each wire bond defining an edge surface extending away between the base and the end surface. The encapsulation can cover portions of the wire bonds, such that unencapsulated portions of the wire bonds are defined by the end surface and a portion of the edge surface thereof that is uncovered by the encapsulation layer. The sacrificial material layer can cover portions of the wire bonds that are uncovered by the encapsulation layer. A portion of the sacrificial material layer and portions of the wire bonds can be planarized such that the portions of the wire bonds uncovered by the encapsulation layer reach a predetermined, substantially uniform height. The method can include removing a remaining portion of the sacrificial material layer from the encapsulation layer.

[0041] A method of making a microelectronic package according to an example can be performed using an in-process unit having wire bonds joined to conductive elements of a substrate thereof and conductive elements at locations on a face of a microelectronic element connected to the substrate. For example, the wire bonds can be connected to a rear face of the microelectronic element. After forming an encapsulation layer covering at least portions of the wire bonds, the method can include simultaneously removing a portion of the encapsulation layer and portions of the wire bonds such the wire bonds are segmented into connection vias which are joined to the conductive elements of the substrate; and into thermal

vias which are joined to the face of the microelectronic element. Both the connection vias and the thermal vias can have end surfaces remote from the bases, e.g., which are exposed at the surface of the encapsulation layer after the removing step. The removing step can be further such that unencapsulated portions of the wire bonds are defined by at least a portion of the end surfaces thereof that are uncovered by the encapsulation layer.

[0042] A method of making a microelectronic package according to an aspect of the invention can include: forming a plurality of wire bonds on an in-process unit including a substrate having a first surface and a second surface remote therefrom. A microelectronic element can be mounted to the first surface of the substrate, a plurality of conductive elements exposed at the first surface, at least some of the conductive elements being electrically connected to the microelectronic element. The wire bonds can have bases joined to the conductive elements and end surfaces remote from the bases. Each wire bond can define an edge surface extending between the base and the end surface. In one example, at least two wire bonds may be formed on an individual conductive element of the conductive elements. A dielectric encapsulation layer can be formed on the in-process unit, wherein the encapsulation layer is formed so as to at least partially cover the first surface and portions of the wire bonds. Unencapsulated portions of the wire bonds are defined by a portion of at least one of the end surface or of the edge surface thereof that is uncovered by the encapsulation layer.

[0043] A method of making a microelectronic package according to an aspect of the invention can include forming a sacrificial structure over an in-process unit including a substrate having a first surface and a second surface remote therefrom. A microelectronic element can be mounted to the

first surface of the substrate. A plurality of conductive elements can be exposed at the first surface, and at least some of the conductive elements can be electrically connected to the microelectronic element. The sacrificial structure can have an opening therein that exposes at least one of the conductive elements. The sacrificial structure may define a surface adjacent the opening and remote from the first surface of the substrate. The method can include forming a plurality of wire bonds having bases joined to the conductive elements and end surfaces remote therefrom, each wire bond defining an edge surface extending between the base and the end surface, and severing the wire bonds at locations outside the openings and adjacent the surface of the sacrificial structure. Thereafter, the sacrificial structure can be removed, and the method can further include forming a dielectric encapsulation layer on the in-process unit. The encapsulation layer can be formed so as to at least partially cover the first surface and portions of the wire bonds. An unencapsulated portion of a wire bond can be defined by a portion of at least one of the end surface or of the edge surface thereof that is uncovered by the encapsulation layer.

[0044] A method of making a microelectronic package according to an aspect of the invention can include feeding a metal wire segment having a predetermined length out of a capillary of a bonding tool. The face of the capillary can be moved over first and second surfaces of a forming unit to shape the metal wire segment to have a first portion projecting upwardly in a direction along an exterior wall of the capillary. The bonding tool can be used to bond a second portion of the metal wire to a conductive element exposed at a first surface of a substrate. The second portion of the metal wire can be positioned to extend along the conductive element, with the first portion positioned at an angle between 25° and

90° to the second portion, for example. Steps (a) through (c) can be repeated to bond a plurality of the metal wires to a plurality of the conductive elements of the substrate. A dielectric encapsulation layer can be formed to overlie the surface of the substrate. The encapsulation layer can be formed so as to at least partially cover the surface of the substrate and portions of the wire bonds. An unencapsulated portion of a wire bond can be defined by a portion of at least one of an end surface of a wire bond or of an edge surface thereof that is uncovered by the encapsulation layer.

[0045] In one example, a first one of the wire bonds can be adapted for carrying a first signal electric potential and a second one of the wire bonds is adapted for simultaneously carrying a second signal electric potential different form the first signal electric potential.

[0046] In one example, the method can include mounting and electrically interconnecting a microelectronic element with the substrate, the method electrically interconnecting the microelectronic element with at least some of the wire bonds.

[0047] In one example, the substrate can be a circuit panel. In one example, the substrate can be a lead frame and the method may include mounting and electrically interconnecting a microelectronic element with the lead frame, the microelectronic element can be electrically interconnected therewith with at least some of the wire bonds.

[0048] In one example, the substrate can be a first microelectronic element. The method can include mounting and electrically interconnecting a second microelectronic element with the first microelectronic element. The method may include electrically interconnecting the second microelectronic element with at least some of the wire bonds through the first microelectronic element.

[0049] In one example, the metal wire segment can be a first metal wire segment. The method may include, after forming the upwardly projecting portion, (i) feeding out a second metal wire segment integral with the first metal wire segment, and (ii) moving the face of the capillary over a third surface of the forming unit to shape the second metal wire segment to have a second portion projecting upwardly along the exterior wall of the capillary. In one example, the second portion may be connected to the first upwardly projecting portion by a third portion of the metal wire.

[0050] In such example, an initial encapsulation layer can be formed, and then at least a portion of the initial encapsulation layer can be recessed to form the encapsulation layer and to define the unencapsulated portions of the wire bonds. In one example, the step of recessing includes laser ablating the initial encapsulation layer. In one example, the step of recessing includes wet blasting the initial encapsulation layer.

[0051] In one example, the method may include molding the encapsulation layer with a temporary film between the encapsulant and a plate of the mold. The wire bonds may extend into the temporary film. The temporary film can be removed to expose the unencapsulated portions of the wire bonds.

[0052] In one example, the method may include applying a portion of a continuous sheet of the temporary film to the mold plate. The method may then form the encapsulation layer in a cavity at least partially defined by the mold plate. The current portion of the temporary film may then be replaced with another portion of the continuous sheet of the temporary film.

[0053] In one example, after forming the encapsulation layer, the method may include forming second conductive

elements contacting the unencapsulated portions of the wire bonds.

[0054] In one example, the step of forming the second conductive elements may include depositing an electrically conductive material onto the unencapsulated portions of the wire bonds.

[0055] In one example, the step of forming the second conductive elements may include plating a metal layer onto the unencapsulated portions of the wire bonds.

[0056] In one example, the step of forming the second conductive elements may include depositing electrically conductive paste onto the unencapsulated portions of the wire bonds.

[0057] In one example, the step of depositing the electrically conductive material may include at least one of dispensing, stenciling, screen printing, or spraying the conductive material onto the unencapsulated portions of the wire bonds.

[0058] In one example, an exterior wall of the capillary may be substantially vertical. The step of moving the face of the capillary over the second surface of the forming unit can be performed such that the first portion of the metal wire segment is between about 80° and 90° with respect to the second portion.

[0059] In one example, two or more wire bonds can be formed on at least one of the conductive elements.

[0060] In one example, the capillary may define an opening through which the metal wire segment is fed and a front wall extending from around the opening to an edge defined with the exterior wall. The front face can define a raised portion adjacent the edge. During the step (b) the raised portion can be pressed into the metal wire at a location proximate to the first portion.

[0061] In one example, the encapsulation layer can be formed to include a major surface and an alignment surface angled with respect to the major surface. The at least one unencapsulated portion of the wire bond can be positioned on the major surface and the alignment surface intersecting the major surface at a location in proximity to the unencapsulated portion. In such case, the alignment surface can be configured to guide an electrically conductive protrusion disposed above the alignment surface towards the unencapsulated portion of the wire bond.

[0062] In one example, the encapsulation layer can be formed to define a corner region thereof and to further include at least one minor surface positioned within the corner region and being positioned farther from the substrate than the major surface, the alignment surface extending between the minor surface and the major surface.

[0063] In one example, the major surface of the encapsulation layer can be a first major surface that overlies the first region of the substrate, the encapsulation layer being further formed to define a second major surface overlying the second region and being positioned closer to the substrate than the major surface. The alignment surface can extend between the minor surface and the major surface.

[0064] In one example, a ball bond can be formed to extend over the second portion of the metal wire after bonding the second portion to the conductive element.

[0065] A method according to an aspect of the invention can include aligning a second microelectronic package with a first microelectronic package made in accordance with the an aspect of the invention herein. The second microelectronic package may include a substrate defining a first surface with contact pads exposed thereon and conductive masses joined with the contact pads. The second microelectronic package can be

aligned with the first microelectronic package by moving at least one of the solder balls into contact with both the alignment surface and at least the end surface of at least one wire bond. The conductive masses can be heated. reflowed or otherwise cured to join the conductive masses with respective ones of the unencapsulated portions of the wire bonds.

[0066] A method according to an aspect of the invention can includepositioning a first microelectronic package over a second microelectronic package, the first microelectronic package including a substrate having a first surface having terminals exposed thereon, the terminals including joining elements projecting away from the first surface.

[0067] The second microelectronic package may include a substrate having a first region and a second region, the substrate having a first surface and a second surface remote from the first surface. At least one microelectronic element may overlie the first surface within the first region. Electrically conductive elements can be exposed at at least one of the first surface and the second surface of the substrate within the second region, at least some of the conductive elements being electrically connected to the at least one microelectronic element. Wire bonds defining edge surfaces can have bases bonded to respective ones of the conductive elements. The bases can include first portions of the edge surfaces that extend along the conductive elements with respective second portions of the edge surfaces being at an angle between 25° and 90° relative to the first portions. The wire bonds can further have ends remote from the substrate and remote from the bases. A dielectric encapsulation layer can extend from at least one of the first or second surfaces and cover portions of the wire bonds such that covered portions of the wire bonds are separated from one another by the encapsulation layer, the encapsulation layer overlying at

least the second region of the substrate. The unencapsulated portions of the wire bonds can be defined by portions of the wire bonds that are uncovered by the encapsulation layer. The unencapsulated portions can include the ends. The joining elements can be heated, cured or reflowed, for example, to join with the unencapsulated wire bond portions of the second microelectronic package.

[0068] In one example, the method can further include a step of forming an underfill filling a space defined between confronting surfaces of the first microelectronic package and the second microelectronic package and surrounding the conductive projections between the terminals of the first microelectronic package and the unencapsulated wire bond portions of the second microelectronic package.

[0069] A microelectronic package according to an aspect of the invention can include a substrate having a first region and a second region, the substrate having a first surface and a second surface remote from the first surface. A microelectronic element can overlie the first surface, such as within the first region. Electrically conductive elements can be exposed at at least one of the first surface and the second surface of the substrate within the second region. At least some of the conductive elements can be electrically connected to the at least one microelectronic element. Wire bonds defining edge surfaces and having bases bonded to respective ones of the conductive elements. The bases may include first portions of the edge surfaces that extend along the conductive elements with respective second portions of the edge surfaces being at an angle, e.g., between 25° and 90° relative to the first portions. The wire bonds can further have ends remote from the substrate and remote from the bases. A dielectric encapsulation layer may extend from at least one of the first or second surfaces and cover portions of the wire bonds. The

covered portions of the wire bonds can be separated from one another by the encapsulation layer. The encapsulation layer may overlie the second region of the substrate and may overlie the first region or another region thereof as well. Unencapsulated portions of the wire bonds can be defined by portions of the wire bonds that are uncovered by the encapsulation layer. The unencapsulated portions may include the ends of the wire bonds, e.g., the ends of the wire bonds which are remote from the conductive elements.

[0070] In one example, the angle between a first portion and a second portion of an edge surface thereof and can be between 45° and 90°. In one example, a first one of the wire bonds is adapted, e.g., configured for carrying a first signal electric potential and a second one of the wire bonds is adapted, e.g., configured for simultaneously carrying a second signal electric potential different from the first signal electric potential.

[0071] Each wire bond may have an edge surface extending between the base and the end thereof. The unencapsulated portions of the wire bonds can be defined by the ends of the wire bonds and portions of edge surfaces adjacent the ends that are uncovered by the encapsulation layer.

[0072] The ends of at least some of the wire bonds may include tapered tips. In an example, the tapered tips may have centroids which are offset in a radial direction from axes of cylindrical portions of the wire bonds.

[0073] In one example, the unencapsulated portions may have bonding tool marks thereon.

[0074] In one example, each of at least some of the unencapsulated portions of the wire bonds includes a ball-shaped portion. Each ball-shaped portion may be integral with a cylindrical portion of such wire bond. Each ball-shaped portion and each cylindrical portion having at

least a core consisting essentially of copper, copper alloy or gold.

[0075] In one example, the ball-shaped portions may have diameters greater than the diameters of the cylindrical portions integral therewith. In such example or other example, the cylindrical portions integral with the ball-shaped portions can be fully covered by the encapsulation layer. In an example, the ball-shaped portions can be partly covered by the encapsulation layer.

[0076] In one example, an oxidation protection layer may contact at least some of the unencapsulated portions of the wire bonds.

[0077] In one example, at least some of the wire bonds have a core of a primary metal and a metallic finish including a second metal different from the primary metal overlying the primary metal. In one example, the metallic finish can include palladium.

[0078] In one example, at least some of the wire bonds can be formed of a primary metal, with a layer of nickel overlying the primary metal and a layer of gold or silver overlying the layer of nickel. In one example, the primary metal can be one of gold or copper.

[0079] In one example, the conductive elements can be first conductive elements, and the microelectronic package further comprising a plurality of second conductive elements electrically connected to the unencapsulated portions of the wire bonds. The second conductive elements can be disposed such that they do not contact the first conductive elements.

[0080] In one example, the second conductive elements can include a monolithic metal layer consisting essentially of a single metal. In one example, the single metal can be one of: nickel, gold, copper, palladium or silver.

[0081] In one example, the second conductive elements can include a conductive paste contacting the unencapsulated portions of the wire bonds.

[0082] In one example, an end of at least one of the wire bonds is displaced in a direction parallel to the first surface of the substrate from its base by at least a distance equal to one of: a minimum pitch between adjacent conductive elements of the plurality of conductive elements, and 100 microns.

[0083] In one example, at least one of the wire bonds includes at least one bend between the base thereof and the unencapsulated portion thereof.

[0084] In one example, the bend of the at least one wire bond can be remote from the base thereof and the unencapsulated portion thereof.

[0085] In one example, the unencapsulated portion of the at least one wire bond can overlie a major surface of the microelectronic element.

[0086] In one example, the bases of the wire bonds can be disposed at positions in a first pattern having a first minimum pitch between respective adjacent bases of the plurality of wire bonds, and the unencapsulated portions of the wire bonds can be disposed at positions in a second pattern having a second minimum pitch between respective adjacent unencapsulated portions of wire bonds of the plurality of wire bonds, the second minimum pitch being greater than the first pitch.

[0087] In one example, the at least one microelectronic element can include first and second microelectronic elements overlying the first surface within the first region, and wherein at least some of the conductive elements are connected with the first microelectronic element, In one example, at least some conductive elements can be connected with the

second microelectronic element. In a particular example, the first microelectronic element and the second microelectronic elements are electrically connected with one another within the microelectronic package

[0088] In one example, at least one of the first conductive elements may have at least two wire bonds joined thereto.

[0089] A microelectronic assembly according to an aspect of the invention can include a first microelectronic package. The first microelectronic package may include a substrate having a first region and a second region, the substrate having a first surface and a second surface remote from the first surface. At least one microelectronic element may overlie the first surface within the first region. Electrically conductive elements may be exposed at at least one of the first surface and the second surface of the substrate within the second region. At least some of the conductive elements may be electrically connected to the at least one microelectronic element. Wire bonds which define edge surfaces can have bases bonded to respective ones of the conductive elements. The bases can include first portions of the edge surfaces that extend along the conductive elements, and respective second portions of the edge surfaces extending at an angle relative to the first portions, for example, between 25° and 90°. The wire bonds can have ends remote from the substrate and remote from the bases. A dielectric encapsulation layer can extend from at least one of the first or second surfaces and cover portions of the wire bonds such that covered portions of the wire bonds are separated from one another by the encapsulation layer. The encapsulation layer can overlie at least the second region of the substrate. Unencapsulated portions of the wire bonds are defined by portions of the wire bonds that are uncovered by the

encapsulation layer. The unencapsulated portions can include the ends.

[0090] Such aspect of the invention can include a second microelectronic package which includes a second microelectronic element and terminals electrically connected to the second microelectronic element and exposed at a surface of the second microelectronic package. A plurality of conductive protrusions can electrically connect at least some of the unencapsulated portions of the wire bonds with respective ones of the terminals of the second microelectronic package.

[0091] In one example, the encapsulation layer of the first microelectronic package can have a major surface and an alignment surface which slopes upwardly away from the major surface. At least one unencapsulated portion of the wire bond can be positioned on the major surface and the alignment surface may extend to a location proximate the major surface and proximate the at least one unencapsulated portion of the wire bond. In such case, a conductive protrusion which connects to the at least one unencapsulated portion of the wire bond can contact the alignment surface.

[0092] In one example, an underfill can be disposed within a space defined between confronting surfaces of the first microelectronic package and the second microelectronic package and between respective adjacent conductive protrusions of the plurality of conductive protrusions.

BRIEF DESCRIPTION OF THE DRAWINGS

[0093] Fig. 1 is sectional view depicting a microelectronic package according to an embodiment of the invention.

[0094] Fig. 2 shows a top plan view of the microelectronic package of Fig. 1.

[0095] Fig. 3 is a sectional view depicting a microelectronic package according to a variation of the embodiment shown in Fig. 1.

[0096] Fig. 4 is a sectional view depicting a microelectronic package according to a variation of the embodiment shown in Fig. 1.

[0097] Fig. 5A is a sectional view depicting a microelectronic package according to a variation of the embodiment shown in Fig. 1.

[0098] Fig. 5B is a fragmentary sectional view depicting a conductive element formed on an unencapsulated portion of a wire bond according to an embodiment of the invention.

[0099] Fig. 5C is a fragmentary sectional view depicting a conductive element formed on an unencapsulated portion of a wire bond according to a variation of that shown in Fig. 5B.

[0100] Fig. 5D is a fragmentary sectional view depicting a conductive element formed on an unencapsulated portion of a wire bond according to a variation of that shown in Fig. 5B.

[0101] Fig. 6 is a sectional view illustrating a microelectronic assembly including a microelectronic package according to one or more of the foregoing embodiments and an additional microelectronic package and a circuit panel electrically connected thereto.

[0102] Fig. 7 is a top elevation view illustrating a microelectronic package according to an embodiment of the invention.

[0103] Fig. 8 is a fragmentary top elevation view further illustrating a microelectronic package according to an embodiment of the invention.

[0104] Fig. 9 is a top elevation view illustrating a microelectronic package including a lead frame type substrate according to an embodiment of the invention.

[0105] Fig. 10 is a corresponding sectional view of the microelectronic package shown in Fig. 9.

[0106] Fig. 11 is a sectional view of a microelectronic assembly including a plurality of microelectronic packages electrically connected together and reinforced with an underfill according to a variation of the embodiment shown in Fig. 6.

[0107] Fig. 12 is a photographic image representing an assembly having bonds between wire bonds of a first component and solder masses of a second component attached thereto.

[0108] Fig. 13A is a fragmentary sectional view illustrating a wire bond via in a microelectronic package according to an embodiment of the invention.

[0109] Fig. 13B is a fragmentary sectional view illustrating a wire bond via in a microelectronic package according to an embodiment of the invention.

[0110] Fig. 13C is an enlarged fragmentary sectional view illustrating a wire bond via in a microelectronic package according to the embodiment shown in Fig. 13B.

[0111] Fig. 13D is a fragmentary sectional view illustrating a wire bond via in a microelectronic package according to an embodiment of the invention.

[0112] Fig. 13E is an enlarged fragmentary sectional view illustrating a wire bond via in a microelectronic package according to the embodiment shown in Fig. 13D.

[0113] Fig. 13F is a fragmentary sectional view illustrating a wire bond via in a microelectronic package according to an embodiment of the invention.

[0114] Fig. 14 illustrates stages in a method of forming a metal wire segment prior to bonding the wire segment to a conductive element according to an embodiment of the invention.

[0115] Fig. 15 further illustrates a method as depicted in Fig. 14 and a forming unit suitable for use in such method.

[0116] Fig. 16 is a top elevation view illustrating wire bonds formed according to an embodiment of the invention.

[0117] Fig. 17 illustrates stages in a method of forming a metal wire segment prior to bonding the wire segment to a conductive element according to an embodiment of the invention.

[0118] Figs. 18 and 19 are sectional views illustrating one stage and another stage subsequent thereto in a method of forming an encapsulation layer of a microelectronic package according to an embodiment of the invention.

[0119] Fig. 20 is an enlarged sectional view further illustrating the stage corresponding to Fig. 19.

[0120] Fig. 21 is a sectional view illustrating a stage of fabricating an encapsulation layer of a microelectronic package according to an embodiment of the invention.

[0121] Fig. 22 is a sectional view illustrating a stage of fabricating an encapsulation layer of a microelectronic package subsequent to the stage shown in Fig. 21.

[0122] Figs. 23A and 23B are fragmentary sectional views illustrating wire bonds according to another embodiment.

[0123] Figs. 24A and 24B are sectional views of a microelectronic package according to a further embodiment.

[0124] Figs. 25A and 25B are sectional views of a microelectronic package according to a further embodiment.

[0125] Fig. 26 shows a sectional view of a microelectronic package according to another embodiment.

[0126] Figs. 27A-C are sectional views showing examples of embodiments of microelectronic packages according to further embodiments.

[0127] Figs. 28A-D show various embodiments of microelectronic packages during steps of forming a

microelectronic assembly according to an embodiment of the disclosure.

[0128] Fig. 29 shows another embodiment of microelectronic packages during steps of forming a microelectronic assembly according to an embodiment of the disclosure.

[0129] Figs. 30 A-C show embodiments of microelectronic packages during steps of forming a microelectronic assembly according to another embodiment of the disclosure.

[0130] Figs. 31 A-C show embodiments of microelectronic packages during steps of forming a microelectronic assembly according to another embodiment of the disclosure.

[0131] Figs. 32A and 32B show a portion of a machine that can be used in forming various wire bond vias in various stages of a method according to another embodiment of the present disclosure.

[0132] Fis. 33 shows a portion of a machine that can be used in forming various wire bond vias according in a method according to another embodiment of the present disclosure.

[0133] Figs 34A-C show various forms of an instrument that can be used in a method for making wire bonds according to an embodiment of the present disclosure.

[0134] Fig. 35 shows a portion of a machine that can be used in forming various wire bond vias according in a method according to another embodiment of the present disclosure.

[0135] Fig. 36 shows a portion of a machine that can be used in forming various wire bond vias according in a method according to another embodiment of the present disclosure.

[0136] Figs. 37 A-D show sectional views illustrating stages of fabricating a microelectronic package according to an embodiment of the present disclosure.

[0137] Figs. 38A and 38B show sectional views illustrating stages of fabricating a microelectronic package according to another embodiment of the present disclosure.

[0138] Figs. 39A-C show sectional views illustrating stages of fabricating a microelectronic package according to another embodiment of the present disclosure.

[0139] Fig. 40 shows a microelectronic package according to an embodiment of the present disclosure.

[0140] Figs. 41-44 show a microelectronic package during various steps of fabrication thereof according to an embodiment of the present disclosure.

DETAILED DESCRIPTION

[0141] Turning now to the figures, where similar numeric references are used to indicate similar features, there is shown in Fig. 1 a microelectronic assembly 10 according to an embodiment of the present invention. The embodiment of Fig. 1 is a microelectronic assembly in the form of a packaged microelectronic element such as a semiconductor chip assembly that is used in computer or other electronic applications.

[0142] The microelectronic assembly 10 of Fig. 1 includes a substrate 12 having a first surface 14 and a second surface 16. The substrate 12 typically is in the form of a dielectric element, which is substantially flat. The dielectric element may be sheet-like and may be thin. In particular embodiments, the dielectric element can include one or more layers of organic dielectric material or composite dielectric materials, such as, without limitation: polyimide, polytetrafluoroethylene ("PTFE"), epoxy, epoxy-glass, FR-4, BT resin, thermoplastic, or thermoset plastic materials. The substrate may be a substrate of a package having terminals for further electrical interconnection with a circuit panel, e.g., a circuit board. Alternatively, the substrate can be a circuit panel or circuit board. In one example thereof, the substrate can be a module board of a dual-inline memory module ("DIMM"). In yet another variation, the substrate can be a microelectronic element such as may be or include a

semiconductor chip embodying a plurality of active devices, e.g., in form of an integrated circuit or otherwise.

[0143] The first surface 14 and second surface 16 are preferably substantially parallel to each other and are spaced apart at a distance perpendicular to the surfaces 14,16 defining the thickness of the substrate 12. The thickness of substrate 12 is preferably within a range of generally acceptable thicknesses for the present application. In an embodiment, the distance between the first surface 14 and the second surface 16 is between about 25 and 500 μm. For purposes of this discussion, the first surface 14 may be described as being positioned opposite or remote from second surface 16. Such a description, as well as any other description of the relative position of elements used herein that refers to a vertical or horizontal position of such elements is made for illustrative purposes only to correspond with the position of the elements within the Figures, and is not limiting.

[0144] In a preferred embodiment, substrate 12 is considered as divided into a first region 18 and a second region 20. The first region 18 lies within the second region 20 and includes a central portion of the substrate 12 and extends outwardly therefrom. The second region 20 substantially surrounds the first region 18 and extends outwardly therefrom to the outer edges of the substrate 12. In this embodiment, no specific characteristic of the substrate itself physically divides the two regions; however, the regions are demarked for purposes of discussion herein with respect to treatments or features applied thereto or contained therein.

[0145] A microelectronic element 22 can be mounted to first surface 14 of substrate 12 within first region 18. Microelectronic element 22 can be a semiconductor chip or

another comparable device. In the embodiment of Fig. 1, microelectronic element 22 is mounted to first surface 14 in what is known as a conventional or "face-up" fashion. In such an embodiment, wire leads 24 can be used to electrically connect microelectronic element 22 to some of a plurality of conductive elements 28 exposed at first surface 14. Wire leads 24 can also be joined to traces (not shown) or other conductive features within substrate 12 that are, in turn, connected to conductive elements 28.

[0146] Conductive elements 28 include respective "contacts" or pads 30 that are exposed at the first surface 14 of substrate 12. As used in the present description, when an electrically conductive element is described as being "exposed at" the surface of another element having dielectric structure, it indicates that the electrically conductive structure is available for contact with a theoretical point moving in a direction perpendicular to the surface of the dielectric structure toward the surface of the dielectric structure from outside the dielectric structure. Thus, a terminal or other conductive structure that is exposed at a surface of a dielectric structure may project from such surface; may be flush with such surface; or may be recessed relative to such surface and exposed through a hole or depression in the dielectric. The conductive elements 28 can be flat, thin elements in which pad 30 is exposed at first surface 14 of substrate 12. In one embodiment, conductive elements 28 can be substantially circular and can be interconnected between each other or to microelectronic element 22 by traces (not shown). Conductive elements 28 can be formed at least within second region 20 of substrate 12. Additionally, in certain embodiments, conductive elements 28 can also be formed within first region 18. Such an arrangement is particularly useful when mounting

microelectronic element 122 (Fig. 3) to substrate 112 in what is known as a "flip-chip" configuration, where contacts on the microelectronic element 122 can be connected to conductive elements 128 within first region 118 by solder bumps 126 or the like that are positioned beneath microelectronic element 122. In an embodiment, conductive elements 28 are formed from a solid metal material such as copper, gold, nickel, or other materials that are acceptable for such an application, including various alloys including one or more of copper, gold, nickel or combinations thereof.

[0147] At least some of conductive elements 28 can be interconnected to corresponding second conductive elements 40, such as conductive pads, exposed at second surface 16 of substrate 12. Such an interconnection can be completed using vias 41 formed in substrate 12 that can be lined or filled with conductive metal that can be of the same material as conductive elements 28 and 40. Optionally, conductive elements 40 can be further interconnected by traces on substrate 12.

[0148] Microelectronic assembly 10 further includes a plurality of wire bonds 32 joined to at least some of the conductive elements 28, such as on the pads 30 thereof. Wire bonds 32 are bonded along a portion of the edge surface 37 thereof to the conductive elements 28. Examples of such bonding include stitch bonding, wedge bonding and the like. As will be described in further detail below, a wire bonding tool can be used to stitch-bond a segment of wire extending from a capillary of the wire bonding tool to a conductive element 28 while severing the stitch-bonded end of the wire from a supply of wire in the capillary. The wire bonds are stitch-bonded to the conductive elements 28 at their respective "bases" 34. Hereinafter, the "base" 34 of such stitch-bonded wire bond 32 refers to the portion of the wire

bond which forms a joint with the conductive element 28. Alternatively, wire bonds can be joined to at least some of the conductive elements using ball bonds, examples of which are shown and described in co-pending, commonly assigned U.S. Patent Application, the entire disclosure of which is incorporated by reference herein.

[0149] The incorporation of various forms of edge bonds, as described herein, can allow for conductive elements 28 to be non-solder-mask-defined ("NSMD") type conductive elements. In packages using other types of connections to conductive elements, for example solder balls or the like, the conductive elements are solder-mask defined. That is the conductive elements are exposed in openings formed in a solder mask material layer. In such an arrangement, the solder mask layer can partially overlie the conductive elements or can contact the conductive elements along an edge thereof. By contrast, a NSMD conductive element is one that is not contacted by a solder mask layer. For example, the conductive element can be exposed on a surface of a substrate that does not have a solder mask layer or, if present, a solder mask layer on the surface can have an opening with edges spaced away from the conductive element. Such NSMD conductive elements can also be formed in shapes that are not round. Solder-mask defined pads can often be round when intended to be used to bond to an element via a solder mass, which forms a generally round profile on such a surface. When using, for example, an edge bond to attach to a conductive element, the bond profile itself is not round, which can allow for a non-round conductive element. Such non-round conductive elements can be, for example oval, rectangular, or of a rectangular shape with rounded corners. They can further be configured to be longer in the direction of the edge bond to accommodate the bond, while being shorter in the direction of the wire bond's

32 width. This can allow for a finer pitch at the substrate 12 level. In one example, the conductive elements 28 can be between about 10% and 25% larger than the intended size of base 34 in both directions. This can allow for variations in the precision with which the bases 34 are located and for variations in the bonding process.

[0150] In some embodiments, an edge bonded wire bond, as described above, which can be in the form of a stitch bond, can be combined with a ball bond. As shown in Fig. 23A a ball bond 1333 can be formed on a conductive element 1328 and a wire bond 1332 can be formed with a base 1338 stitch bonded along a portion of the edge surface 1337 to ball bond 1372. In another example, the general size and placement of the ball bond can be as shown at 1372'. In another variation shown in Fig. 23B, a wire bond 1332 can be edge bonded along conductive element 1328, such as by stitch bonding, as described above. A ball bond 1373 can then be formed on top of the base 1338 of wire bond 1334. In one example, the size and placement of the ball bond can be as shown at 1373'. Each of the wire bonds 32 can extend to a free end 36 remote from the base 34 of such wire bond and remote from substrate 12. The ends 36 of wire bonds 32 are characterized as being free in that they are not electrically connected or otherwise joined to microelectronic element 22 or any other conductive features within microelectronic assembly 10 that are, in turn, connected to microelectronic element 22. In other words, free ends 36 are available for electronic connection, either directly or indirectly as through a solder ball or other features discussed herein, to a conductive feature external to assembly 10. The fact that ends 36 are held in a predetermined position by, for example, encapsulation layer 42 or otherwise joined or electrically connected to another conductive feature does not mean that they are not "free" as described herein, so

long as any such feature is not electrically connected to microelectronic element 22. Conversely, base 34 is not free as it is either directly or indirectly electrically connected to microelectronic element 22, as described herein. As shown in Fig. 1, the bases 34 of the wire bonds 32 typically are curved at their stitch-bond (or other edge-bonded) joints with the respective conductive elements 28. Each wire bond has an edge surface 37 extending between the base 34 thereof and the end 36 of such wire bond. The particular size and shape of base 34 can vary according to the type of material used to form wire bond 32, the desired strength of the connection between wire bond 32 and conductive element 28, or the particular process used to form wire bond 32. Alternative embodiments are possible where wire bonds 32 are additionally or alternatively joined to conductive elements 40 exposed on second surface 16 of substrate 12, extending away therefrom.

[0151] In an alternative arrangement shown in Fig. 40, base 2734 can be substantially rounded in shape, extending outward from an edge surface 2737 of wire bond 2732 defined between base 2734 and end 2736. The particular size and shape of base 2734 can vary according to the type of material used to form wire bond 2732, the desired strength of the connection between wire bond 2732 and conductive element 2728, or the particular process used to form wire bond 2732. Exemplary methods for making wire bonds 2728 are and are described in U.S. Pat. No. 7,391,121 to Otremba and in U.S. Pat. App. Pub. No. 2005/0095835 (describing a wedge-bonding procedure that can be considered a form of wire bonding) the disclosures of which are both incorporated herein by reference in their entireties. Alternative embodiments are possible where wire bonds 2732 are additionally or alternatively joined to conductive elements 2740 exposed on second surface 2716 of substrate 2712, extending away therefrom. Examples of ball-bonded wire bonds

are shown and described in commonly owned co-pending United States Application No. 13/405,125 entitled "METHOD FOR PACKAGE-ON-PACKAGE ASSEMBLY WITH WIRE BONDS TO ENCAPSULATION SURFACE", which names as inventors Reynaldo Co and Laura Mirkarimi, the disclosure of which is incorporated by reference herein.

[0152] In a particular example, a first one of the wire bonds 32 may be adapted, i.e., constructed, arranged, or electrically coupled to other circuitry on the substrate for carrying a first signal electric potential, and a second one of the wire bonds 32 may be so adapted for simultaneously carrying a second signal electric potential different from the first signal electric potential. Thus, when a microelectronic package as seen in Figs. 1 and 2 is energized, the first and second wire bonds can simultaneously carry first and second different signal electric potentials.

[0153] Wire bond 32 can be made from a conductive material such as copper, copper alloy or gold. Additionally, wire bonds 32 can be made from combinations of materials, such as from a core of a conductive material, such as copper or aluminum, for example, with a coating applied over the core. The coating can be of a second conductive material, such as aluminum, nickel or the like. Alternatively, the coating can be of an insulating material, such as an insulating jacket.

[0154] In particular embodiments, the wire bonds may have a core of primary metal and a metallic finish including a second metal different from the primary metal overlying the primary metal. For example, the wire bonds may have a primary metal core of copper, copper alloy or gold and the metallic finish can include palladium. Palladium can avoid oxidation of a core metal such as copper, and may serve as a diffusion barrier to avoid diffusion a solder-soluble metal such as gold in solder joints between unencapsulated portions 39 of the wire bonds

and another component as will be described further below. Thus, in one embodiment, the wire bonds can be formed of palladium-coated copper wire or palladium-coated gold wire which can be fed through the capillary of the wire bonding tool.

[0155] In an embodiment, the wire used to form wire bonds 32 can have a thickness, i.e., in a dimension transverse to the wire's length, of between about 15 µm and 150 µm. In general, a wire bond is formed on a conductive element, such as conductive element 28, a pad, trace or the like, using specialized equipment that is known in the art. The free end 36 of wire bond 32 has an end surface 38. End surface 38 can form at least a part of a contact in an array formed by respective end surfaces 38 of a plurality of wire bonds 32. Fig. 2 shows an exemplary pattern for such an array of contacts formed by end surfaces 38. Such an array can be formed in an area array configuration, variations of which could be implemented using the structures described herein. Such an array can be used to electrically and mechanically connect the microelectronic assembly 10 to another microelectronic structure, such as to a printed circuit board ("PCB"), or to other packaged microelectronic elements, an example of which is shown in Fig. 6. In such a stacked arrangement, wire bonds 32 and conductive elements 28 and 40 can carry multiple electronic signals therethrough, each having a different signal potential to allow for different signals to be processed by different microelectronic elements in a single stack. Solder masses 52 can be used to interconnect the microelectronic assemblies in such a stack, such as by electronically and mechanically attaching end surfaces 38 to conductive elements 40.

[0156] Microelectronic assembly 10 further includes an encapsulation layer 42 formed from a dielectric material. In

the embodiment of Fig. 1, encapsulation layer 42 is formed over the portions of first surface 14 of substrate 12 that are not otherwise covered by or occupied by microelectronic element 22, or conductive elements 28. Similarly, encapsulation layer 42 is formed over the portions of conductive elements 28, including pad 30 thereof, that are not otherwise covered by wire bonds 32. Encapsulation layer 42 can also substantially cover microelectronic element 22, wire bonds 32, including the bases 34 and at least a portion of edge surfaces 37 thereof. A portion of wire bonds 32 can remain uncovered by encapsulation layer 42, which can also be referred to as unencapsulated portions 39, thereby making the wire bond available for electrical connection to a feature or element located outside of encapsulation layer 42. In an embodiment, end surfaces 38 of wire bonds 32 remain uncovered by encapsulation layer 42 within major surface 44 of encapsulation layer 42. Other embodiments are possible in which a portion of edge surface 37 is uncovered by encapsulation layer 42 in addition to or as an alternative to having end surface 38 remain uncovered by encapsulation layer 42. In other words, encapsulation layer 42 can cover all of microelectronic assembly 10 from first surface 14 and above, with the exception of a portion of wire bonds 36, such as end surfaces 38, edge surfaces 37 or combinations of the two. In the embodiments shown in the Figures, a surface, such as major surface 44 of encapsulation layer 42 can be spaced apart from first surface 14 of substrate 12 at a distance great enough to cover microelectronic element 22. Accordingly, embodiments of microelectronic assembly 10 in which ends 38 of wire bonds 32 are flush with surface 44, will include wire bonds 32 that are taller than the microelectronic element 22, and any underlying solder bumps for flip chip connection. Other configurations for encapsulation layer 42, however, are possible. For

example, the encapsulation layer can have multiple surfaces with varying heights. In such a configuration, the surface 44 within which ends 38 are positioned can be higher or lower than an upwardly facing surface under which microelectronic element 22 is located.

[0157] Encapsulation layer 42 serves to protect the other elements within microelectronic assembly 10, particularly wire bonds 32. This allows for a more robust structure that is less likely to be damaged by testing thereof or during transportation or assembly to other microelectronic structures. Encapsulation layer 42 can be formed from a dielectric material with insulating properties such as that described in U.S. Patent App. Pub. No. 2010/0232129, which is incorporated by reference herein.

[0158] Fig. 3 shows an embodiment of microelectronic assembly 110 having wire bonds 132 with ends 136 that are not positioned directly above the respective bases 34 thereof. That is, considering first surface 114 of substrate 112 as extending in two lateral directions, so as to substantially define a plane, end 136 or at least one of the wire bonds 132 is displaced in at least one of these lateral directions from a corresponding lateral position of base 134. As shown in Fig. 3, wire bonds 132 can be substantially straight along the longitudinal axis thereof, as in the embodiment of Fig. 1, with the longitudinal axis being angled at an angle 146 with respect to first surface 114 of substrate 112. Although the cross-sectional view of Fig. 3 only shows the angle 146 through a first plane perpendicular to first surface 114, wire bond 132 can also be angled with respect to first surface 114 in another plane perpendicular to both that first plane and to first surface 114. Such an angle can be substantially equal to or different than angle 146. That is the displacement of end 136 relative to base 134 can be in two lateral directions

and can be by the same or a different distance in each of those directions.

[0159] In an embodiment, various ones of wire bonds 132 can be displaced in different directions and by different amounts throughout the assembly 110. Such an arrangement allows for assembly 110 to have an array that is configured differently on the level of surface 144 compared to on the level of substrate 12. For example, an array can cover a smaller overall area or have a smaller pitch on surface 144 compared to that at first surface 114 of substrate 112. Further, some wire bonds 132 can have ends 138 that are positioned above microelectronic element 122 to accommodate a stacked arrangement of packaged microelectronic elements of different sizes. In another example, wire bonds 132 can be configured such that the end of one wire bond is positioned substantially above the base of a second wire bond, wherein the end of that second wire bond being positioned elsewhere. Such an arrangement can be referred to as changing the relative position of a contact end surface 136 within an array of contacts, compared to the position of a corresponding contact array on second surface 116. In another example, shown in Fig. 8, wire bonds 132 can be configured such that the end 136A of one wire bond 132A is positioned substantially above the base 134B of another wire bond 134B, the end 132B of that wire bond 134B being positioned elsewhere. Such an arrangement can be referred to as changing the relative position of a contact end surface 136 within an array of contacts, compared to the position of a corresponding contact array on second surface 116. Within such an array, the relative positions of the contact end surfaces can be changed or varied, as desired, depending on the microelectronic assembly's application or other requirements. Fig. 4 shows a further embodiment of a microelectronic subassembly 210 having

wire bonds 232 with ends 236 in displaced lateral positions with respect to bases 234. In the embodiment of Fig. 4, the wire bonds 132 achieve this lateral displacement by including a curved portion 248 therein. Curved portion 248 can be formed in an additional step during the wire bond formation process and can occur, for example, while the wire portion is being drawn out to the desired length. This step can be carried out using available wire-bonding equipment, which can include the use of a single machine.

[0160] Curved portion 248 can take on a variety of shapes, as needed, to achieve the desired positions of the ends 236 of the wire bonds 232. For example, curved portions 248 can be formed as S-curves of various shapes, such as that which is shown in Fig. 4 or of a smoother form (such as that which is shown in Fig. 5). Additionally, curved portion 248 can be positioned closer to base 234 than to end 236 or vice-versa. Curved portion 248 can also be in the form of a spiral or loop, or can be compound including curves in multiple directions or of different shapes or characters.

[0161] In a further example shown in Fig. 26, the wire bonds 132 can be arranged such that the bases 134 are arranged in a first pattern having a pitch thereof. The wire bonds 132 can be configured such that the unencapsulated portions thereof 139 including end surfaces 138, can be disposed at positions in a pattern having a minimum pitch between adjacent unencapsulated portions 38 of the wire bonds 32 exposed at the surface 44 of the encapsulation layer that is greater than the minimum pitch between adjacent bases of the plurality of bases 134 and, accordingly, the conductive elements 128 to which the bases are joined). To achieve this, the wire bonds can include portions which extend in one or more angles relative to a normal direction to the conductive elements, such as shown in Fig. 26. In another example, the wire bonds can be

curved as shown, for example in Fig. 4, such that the ends 238 are displaced in one or more lateral directions from the bases 134, as discussed above. As further shown in Fig. 26, the conductive elements 128 and the ends 138 can be arranged in respective rows or columns and the lateral displacement of end surfaces 138 at some locations, such as in one row of the ends, from the respective conductive elements on the substrate to which they are joined can be greater than the lateral displacement of the unencapsulated portions at other locations from the respective conductive elements to which they are connected. To achieve this, the wire bonds 132 can, for example be at different angles 146A, 146B with respect to the surface 116 of the substrate 112.

[0162] Fig. 5A shows a further exemplary embodiment of a microelectronic package 310 having a combination of wire bonds 332 having various shapes leading to various relative lateral displacements between bases 334 and ends 336. Some of wire bonds 332A are substantially straight with ends 336A positioned above their respective bases 334A, while other wire bonds 332B include a subtle curved portion 348B leading to a somewhat slight relative lateral displacement between end 336B and base 334B. Further, some wire bonds 332C include curved portions 348C having a sweeping shape that result in ends 336C that are laterally displaced from the relative bases 334C at a greater distance than that of ends 334B. Fig. 5 also shows an exemplary pair of such wire bonds 332Ci and 332Cii that have bases 334Ci and 334Cii positioned in the same row of a substrate-level array and ends 336Ci and 336Cii that are positioned in different rows of a corresponding surface-level array. In some cases, the radius of bends in the wire bonds 332Ci, 332Cii can be large such that the curves in the wire bonds may appear continuous. In other cases, the radius of the bends may be relatively small, and the wire bonds may even

have straight portions or relatively straight portions between bends in the wire bonds. Moreover, in some cases the unencapsulated portions of the wire bonds can be displaced from their bases by at least one minimum pitch between the contacts 328 of the substrate. In other cases, the unencapsulated portions of the wire bonds can be displaced from their bases by at least 200 microns.

[0163] A further variation of a wire bond 332D is shown that is configured to be uncovered by encapsulation layer 342 on a side surface 47 thereof. In the embodiment shown free end 336D is uncovered, however, a portion of edge surface 337D can additionally or alternatively be uncovered by encapsulation layer 342. Such a configuration can be used for grounding of microelectronic assembly 10 by electrical connection to an appropriate feature or for mechanical or electrical connection to other featured disposed laterally to microelectronic assembly 310. Additionally, Fig. 5 shows an area of encapsulation layer 342 that has been etched away, molded, or otherwise formed to define a recessed surface 345 that is positioned closer to substrate 12 than major surface 342. One or more wire bonds, such as wire bond 332A can be uncovered within an area along recessed surface 345. In the exemplary embodiment shown in Fig. 5, end surface 338A and a portion of edge surface 337A are uncovered by encapsulation layer 342. Such a configuration can provide a connection, such as by a solder ball or the like, to another conductive element by allowing the solder to wick along edge surface 337A and join thereto in addition to joining to end surface 338. Other configurations by which a portion of a wire bond can be uncovered by encapsulation layer 342 along recessed surface 345 are possible, including ones in which the end surfaces are substantially flush with recessed surface 345 or other configurations shown herein with respect to any other surfaces

of encapsulation layer 342. Similarly, other configurations by which a portion of wire bond 332D is uncovered by encapsulation layer 342 alongside surface 347 can be similar to those discussed elsewhere herein with respect to the variations of the major surface of the encapsulation layer.

[0164] Fig. 5A further shows a microelectronic assembly 310 having two microelectronic elements 322 and 350 in an exemplary arrangement where microelectronic element 350 is stacked, face-up, on microelectronic element 322. In this arrangement, leads 324 are used to electrically connect microelectronic element 322 to conductive features on substrate 312. Various leads are used to electronically connect microelectronic element 350 to various other features of microelectronic assembly 310. For example, lead 380 electrically connects microelectronic element 350 to conductive features of substrate 312, and lead 382 electrically connects microelectronic element 350 to microelectronic element 322. Further, wire bond 384, which can be similar in structure to various ones of wire bonds 332, is used to form a contact surface 386 on the surface 344 of encapsulation layer 342 that electrically connected to microelectronic element 350. This can be used to directly electrically connect a feature of another microelectronic assembly to microelectronic element 350 from above encapsulation layer 342. Such a lead could also be included that is connected to microelectronic element 322, including when such a microelectronic element is present without a second microelectronic element 350 affixed thereon. An opening (not shown) can be formed in encapsulation layer 342 that extends from surface 344 thereof to a point along, for example, lead 380, thereby providing access to lead 380 for electrical connection thereto by an element located outside surface 344. A similar opening can be formed over any of the

other leads or wire bonds 332, such as over wire bonds 332C at a point away from the ends 336C thereof. In such an embodiment, ends 336C can be positioned beneath surface 344, with the opening providing the only access for electrical connection thereto.

[0165] Additional arrangements for microelectronic packages having multiple microelectronic elements are shown in Figs. 27A-C. These arrangements can be used in connection with the wire bond arrangements shown, for example in Fig. 5A and in the stacked package arrangement of Fig. 6, discussed further below. Specifically, Fig. 27A shows an arrangement in which a lower microelectronic element 1622 is flip-chip bonded to conductive elements 1628 on the surface 1614 of substrate 1612. The second microelectronic element 1650 can overlie the first microelectronic element 1622 and be face-up connected to additional conductive elements 1628 on the substrate, such as through wire bonds 1688. Fig. 27B shows an arrangement where a first microelectronic element 1722 is face-up mounted on surface 1714 and connected through wire bonds 1788 to conductive elements 1728. Second microelectronic element 1750 can have contacts exposed at a face thereof which face and are joined to corresponding contacts at a face of the first microelectronic element 1722 which faces away from the substrate. through a set of contacts 1726 of the second microelectronic element 1750 which face and are joined to corresponding contacts on the front face of the first microelectronic element 1722. These contacts of the first microelectronic element 1722 which are joined to corresponding contacts of the second microelectronic element can in turn be connected through circuit patterns of the first microelectronic element 1722 and be connected by ire bonds 1788 to the conductive elements 1728 on substrate 1712.

[0166] Fig. 27C shows an example in which first and second microelectronic elements 1822, 1850 are spaced apart from one another in a direction along a surface 1814 of substrate 1812. Either one or both of the microelectronic elements (and additional microelectronic elements) can be mounted in face-up or flip-chip configurations described herein. Further, any of the microelectronic elements employed in such an arrangement can be connected to each other through circuit patterns on one or both such microelectronic elements or on the substrate or on both, which electrically connect respective conductive elements 1828 to which the microelectronic elements are electrically connected.

[0167] Fig. 5B further illustrates a structure according to a variation of the above-described embodiments in which a second conductive element 43 can be formed in contact with an unencapsulated portion 39 of a wire bond exposed at or projecting above a surface 44 of the encapsulation layer 42, the second conductive element not contacting the first conductive element 28 (Fig. 1). In one embodiment as seen in Fig. 5B, the second conductive element can include a pad 45 extending onto a surface 44 of the encapsulation layer which can provide a surface for joining with a bonding metal or bonding material of a component thereto.

[0168] Alternatively, as seen in Fig. 5C, the second conductive element 48 can be a metallic finish selectively formed on the unencapsulated portion 39 of a wire bond. In either case, in one example, the second conductive element 43 or 48 can be formed, such as by plating, of a layer of nickel contacting the unencapsulated portion of the wire bond and overlying a core of the wire bond, and a layer of gold or silver overlying the layer of nickel. In another example, the second conductive element may be a monolithic metal layer consisting essentially of a single metal. In one example, the

single metal layer can be nickel, gold, copper, palladium or silver. In another example, the second conductive element 43 or 48 can include or be formed of a conductive paste contacting the unencapsulated portion 39 of the wire bond. For example, stenciling, dispensing, screen printing, controlled spraying, e.g., a process similar to inkjet printing, or transfer molding can be used to form second conductive elements 43 or 48 on the unencapsulated portions 39 of the wire bonds.

[0169] Fig. 5D further illustrates a second conductive element 43D which can be formed of a metal or other electrically conductive material as described for conductive elements 43, 48 above, wherein the second conductive element 43D is formed at least partly within an opening 49 extending into an exterior surface 44 of the encapsulation layer 42. In one example, the opening 49 can be formed by removing a portion of the encapsulation layer after curing or partially curing the encapsulation layer so as to simultaneously expose a portion of the wire bond thereunder which then becomes the unencapsulated portion of the wire bond. For example, the opening 49 can be formed by laser ablation, etching. In another example, a soluble material can be pre-placed at the location of the opening prior to forming the encapsulation layer and the pre-placed material then can be removed after forming the encapsulation layer to form the opening.

[0170] In a further example, as seen in Figs. 24A-24B, multiple wire bonds 1432 can have bases joined with a single conductive element 1428. Such a group of wire bonds 1432 can be used to make additional connection points over the encapsulation layer 1442 for electrical connection with conductive element 1428. The exposed portions 1439 of the commonly-joined wire bonds 1432 can be grouped together on surface 1444 of encapsulation layer 1442 in an area, for

example about the size of conductive element 1428 itself or another area approximating the intended size of a bonding mass for making an external connection with the wire bond 1432 group. As shown, such wire bonds 1432 can be either ball-bonded (Fig. 24A) or edge bonded (Fig. 24B) on conductive element 1428, as described above, or can be bonded to the conductive element as described above with respect to Figs. 23A or 23B or both.

[0171] As shown in Figs. 25A and 25B, ball-bonded wire bonds 1532 can be formed as stud bumps on at least some of the conductive elements 1528. As described herein a stud bump is a ball-bonded wire bond where the segment of wire extending between the base 1534 and the end surface 1538 has a length of at most 300% of the diameter of the ball-bonded base 1534. As in other embodiments, the end surface 1538 and optionally a portion of the edge surface 1537 of the stud bump can be unencapsulated by the encapsulation layer 1542. As shown in Fig. 25B such a stud bump 1532A can be formed on top of another stud bump 1532B to form, essentially, a base 1534 of a wire bond 1532 made up of the two ball bonds with a wire segment extending therefrom up to the surface 1544 of the encapsulation layer 1542. Such wire bonds 1532 can have a height that is less than, for example, the wire bonds described elsewhere in the present disclosure. Accordingly, the encapsulation layer can include a major surface 1544 in an area, for example overlying the microelectronic element 1522 and a minor surface 1545 spaced above the surface 1514 of the substrate 1512 at a height less than that of the major surface 1544. Such arrangements can also be used to form alignment features and to reduce the overall height of a package employing stud bump type wire bonds as well as other types of wire bonds disclosed herein, while accommodating conductive masses 1552 that can connect the unencapsulated portions 1539

of the wire bonds 1532 with contacts 1543 on another microelectronic package 1588.

[0172] Fig. 6 shows a stacked package of microelectronic assemblies 410 and 488. In such an arrangement solder masses 452 electrically and mechanically connect end surfaces 438 of assembly 410 to conductive elements 440 of assembly 488. The stacked package can include additional assemblies and can be ultimately attached to contacts 492 on a PCB 490 or the like for use in an electronic device. In such a stacked arrangement, wire bonds 432 and conductive elements 430 can carry multiple electronic signals therethrough, each having a different signal potential to allow for different signals to be processed by different microelectronic elements, such as microelectronic element 422 or microelectronic element 489, in a single stack.

[0173] In the exemplary configuration in Fig. 6, wire bonds 432 are configured with a curved portion 448 such that at least some of the ends 436 of the wire bonds 432 extend into an area that overlies a major surface 424 of the microelectronic element 422. Such an area can be defined by the outer periphery of microelectronic element 422 and extending upwardly therefrom. An example of such a configuration is shown from a view facing toward first surface 414 of substrate 412 in Fig. 18, where wire bonds 432 overlie a rear major surface of the microelectronic element 422, which is flip-chip bonded at a front face 425 thereof to substrate 412. In another configuration (Fig. 5), the microelectronic element 422 can be mounted face-up to the substrate 312, with the front face 325 facing away from the substrate 312 and at least one wire bond 336 overlying the front face of microelectronic element 322. In one embodiment, such wire bond 336 is not electrically connected with microelectronic element 322. A wire bond 336 bonded to substrate 312 may also

overlie the front or rear face of microelectronic element 350. The embodiment of microelectronic assembly 410 shown in Fig. 7 is such that conductive elements 428 are arranged in a pattern forming a first array in which the conductive elements 428 are arranged in rows and columns surrounding microelectronic element 422 and may have a predetermined pitch between individual conductive elements 428. Wire bonds 432 are joined to the conductive elements 428 such that the respective bases 434 thereof follow the pattern of the first array as set out by the conductive elements 428. Wire bonds 432 are configured, however, such that the respective ends 436 thereof can be arranged in a different pattern according to a second array configuration. In the embodiment shown the pitch of the second array can be different from, and in some cases finer than that of the first array. However, other embodiments are possible in which the pitch of the second array is greater than the first array, or in which the conductive elements 428 are not positioned in a predetermined array but the ends 436 of the wire bonds 432 are. Further still, conductive elements 428 can be configured in sets of arrays positioned throughout substrate 412 and wire bonds 432 can be configured such that ends 436 are in different sets of arrays or in a single array.

[0174] Fig. 6 further shows an insulating layer 421 extending along a surface of microelectronic element 422. Insulating layer 421 can be formed from a dielectric or other electrically insulating material prior to forming the wire bonds. The insulating layer 421 can protect microelectronic element from coming into contact with any of wire bonds 423 that extend thereover. In particular, insulating layer 421 can avoid electrical short-circuiting between wire bonds and short-circuiting between a wire bond and the microelectronic element 422. In this way, the insulating layer 421 can help avoid malfunction or possible damage due to unintended

electrical contact between a wire bond 432 and the microelectronic element 422.

[0175] The wire bond configuration shown in Figs. 6 and 7 can allow for microelectronic assembly 410 to connect to another microelectronic assembly, such as microelectronic assembly 488, in certain instances where the relative sizes of, for example, microelectronic assembly 488 and microelectronic element 422 would not otherwise permit. In the embodiment of Fig. 6 microelectronic assembly 488 is sized such that some of the contact pads 440 are in an array within an area smaller than the area of the front or rear surface 424 or 426 of the microelectronic element 422. In a microelectronic assembly having substantially vertical conductive features, such as pillars, in place of wire bonds 432, direct connection between conductive elements 428 and pads 440 would not be possible. However, as shown in Fig. 6, wire bonds 432 having appropriately-configured curved portions 448 can have ends 436 in the appropriate positions to make the necessary electronic connections between microelectronic assembly 410 and microelectronic assembly 488. Such an arrangement can be used to make a stacked package where microelectronic assembly 418 is, for example, a DRAM chip or the like having a predetermined pad array, and wherein microelectronic element 422 is a logic chip configured to control the DRAM chip. This can allow a single type of DRAM chip to be used with several different logic chips of varying sizes, including those which are larger than the DRAM chip because the wire bonds 432 can have ends 436 positioned wherever necessary to make the desired connections with the DRAM chip. In an alternative embodiment, microelectronic package 410 can be mounted on printed circuit board 490 in another configuration, where the unencapsulated surfaces 436 of wire bonds 432 are electrically connected to pads 492 of

circuit board 490. Further, in such an embodiment, another microelectronic package, such as a modified version of package 488 can be mounted on package 410 by solder balls 452 joined to pads 440.

[0176] Figs. 9 and 10 show a further embodiment of a microelectronic assembly 510 in which wire bonds 532 are formed on a lead-frame structure. Examples of lead frame structures are shown and described in U.S. Patent Nos. 7,176,506 and 6,765,287 the disclosures of which are hereby incorporated by reference herein. In general, a lead frame is a structure formed from a sheet of conductive metal, such as copper, that is patterned into segments including a plurality of leads and can further include a paddle, and a frame. The frame is used to secure the leads and the paddle, if used, during fabrication of the assembly. In an embodiment, a microelectronic element, such as a die or chip, can be joined face-up to the paddle and electrically connected to the leads using wire bonds. Alternatively, the microelectronic element can be mounted directly onto the leads, which can extend under the microelectronic element. In such an embodiment, contacts on the microelectronic element can be electrically connected to respective leads by solder balls or the like. The leads can then be used to form electrical connections to various other conductive structures for carrying an electronic signal potential to and from the microelectronic element. When the assembly of the structure is complete, which can include forming an encapsulation layer thereover, temporary elements of the frame can be removed from the leads and paddle of the lead frame, so as to form individual leads. For purposes of this disclosure, the individual leads 513 and the paddle 515 are considered to be segmented portions of what, collectively, forms a substrate 512 that includes conductive elements 528 in portions that are integrally formed therewith. Further, in

this embodiment, paddle 515 is considered to be within first region 518 of substrate 512, and leads 513 are considered to be within second region 520. Wire bonds 524, which are also shown in the elevation view of Fig. 10, connect microelectronic element 22, which is carried on paddle 515, to conductive elements 528 of leads 515. Wire bonds 532 can be further joined at bases 534 thereof to additional conductive elements 528 on leads 515. Encapsulation layer 542 is formed onto assembly 510 leaving ends 538 of wire bonds 532 uncovered at locations within surface 544. Wire bonds 532 can have additional or alternative portions thereof uncovered by encapsulation layer 542 in structures that correspond to those described with respect to the other embodiments herein.

[0177] Fig. 11 further illustrates use of an underfill 620 for mechanically reinforcing the joints between wire bonds 632 of one package 610A and solder masses 652 of another package 610B mounted thereon. As shown in Fig. 11, although the underfill 620 need only be disposed between confronting surfaces 642, 644 of the packages 610A, 610B, the underfill 620 can contact edge surfaces of package 610A and may contact a first surface 692 of the circuit panel 690 to which the package 610 is mounted. Further, portions of the underfill 620 that extend along the edge surfaces of the packages 610A, 610B, if any, can be disposed at an angle between 0° and 90° relative to a major surface of the circuit panel over which the packages are disposed, and can be tapered from a greater thickness adjacent the circuit panel to a smaller thickness at a height above the circuit panel and adjacent one or more of the packages.

[0178] A package arrangement shown in Figs. 28A-D can be implemented in one technique for making an underfill layer, and in particular a portion thereof that is disposed between confronting faces of packages 1910A and 1910B, such as surface

1942 of package 1910A and surface 1916 of package 1910B. As shown in Fig. 28A, package 1910A can extend beyond an edge surface 1947 of package 1910B such that, for example, the surface 1944 of encapsulation layer 1942 has a portion thereof that is exposed outside of package 1910B. Such an area can be used as a dispensing area 1949 whereby a device can deposit an underfill material in a flowable state on the dispensing area from a vertical position relative thereto. In such an arrangement, the dispensing area 1949 can be sized such that the underfill material can be deposited in a mass on the surface without spilling off of the edge of the surface while reaching a sufficient volume to flow under package 1910B where it can be drawn by capillary into the area between the confronting surfaces of packages 1910A and 1910B, including around any joints therebetween, such as solder masses or the like. As the underfill material is drawn between confronting surfaces, additional material can be deposited on the dispensing area such that a continuous flow is achieved that does not significantly spill over the edge of package 1910A. As shown in Fig. 28B, the dispensing area 1949 can surround package 1910B and have a dimension D in an orthogonal direction away from a peripheral edge of package 1910B of about one millimeter (1 mm) on each side thereof. Such an arrangement can allow for dispensing on one side of package 1910B or more than one side, either sequentially or simultaneously. Alternative arrangements are shown in Fig. 28C, wherein the dispensing area 1949 extends along only two adjacent sides of package 1910B and have a dimension D' of about 1 mm in a direction orthogonally away from a peripheral edge of the second package, and Fig. 28D, wherein the dispensing area 1949 extends along a single side of package 1910B and may have a dimension D" in an orthogonal direction

away from the peripheral edge of the package of, for example 1.5 mm to 2 mm.

[0179] In an arrangement where microelectronic packages 2010A and 2010B are of similar sizes in a horizontal profile, a compliant bezel 2099 can be used to secure the packages 2010A and 2010B together during attachment by, for example, joining of terminals of the second package with the elements comprising the unencapsulated portions 2039 of the wire bonds 2032, e.g., by heating or curing of conductive masses 2052, e.g., reflowing of solder masses, to join the packages 2010A and 2010B together. Such an arrangement is shown in Fig. 29 in which package 2010B is assembled over package 2010A with conductive masses 2052, e.g., solder masses, for example, joined to terminals 2043 on package 2010B. The packages can be aligned so that the solder masses 2052 align with unencapsulated portions 2039 of the wire bonds 2032 of package 2010A or with second conductive elements joined with the end surfaces 2038 of the wire bonds 2032, as described above. The bezel 2099 can then be assembled around packages 2010A and 2010B to maintain such alignment during a heating process in which the terminals of the second package are joined with the wire bonds 2032 or second conductive elements of the first package. For example, a heating process can be used to reflow solder masses 2052 to bond the terminals of the second package with the wire bonds 2032 or second conductive elements. Bezel 2099 can also extend inward along portions of surface 2044 of package 2010B and along surface 2016 of package 2010A to maintain the contact between the packages before and during reflow. The bezel 2099 can be of a resiliently compliant material such as rubber, TPE, PTFE (polytetrafluoroethylene), silicone or the like and can be undersized relative to the size of the assembled packages such that a compressive force is applied by the bezel when in place. The bezel 2099 can

also be left in place during the application of an underfill material and can include an opening to accommodate such application therethrough. The compliant bezel 2099 can be removed after package assembly.

[0180] Additionally or alternatively, the assembly of microelectronic packages 2110A and 2110B, as shown in Figs. 30A-F, a lower package 2110A can include at least one alignment surface 2151. One example of this is shown in Fig. 30A in which alignment surfaces 2151 are included in encapsulation layer 2142 near the corners of the package 2110B. The alignment surfaces are sloped relative to the major surface and define an angle of between about 0° and up to and including 90° relative to major surface 2144 at some location therefrom, the alignment surfaces extending locations proximate the major surface 2144 and respective minor surfaces 2145 that are spaced above substrate 2112 at a greater distance than major surface 2144. The minor surfaces 2145 can be disposed adjacent the corners of package 2110A and can extend partially between intersecting sides thereof. As shown in Fig. 30B, the alignment surfaces can also form inside corners opposite the intersecting sides of the package 2110A and can be included in similar form along all corners, for example four corners, of package 2110A. As illustrated in Fig. 30C, the alignment surfaces 2151 can be positioned at an appropriate distance from unencapsulated portions of corresponding wire bonds 2132 such that when a second package 2110B having protrusions, e.g., electrically conductive protrusions such as conductive masses or solder balls joined thereto is stacked on top of package 2110A, the alignment surfaces 2151 will guide the solder balls into the proper position overlying the unencapsulated portions of the wire bonds 2132 that correspond with the alignment surfaces 2151. The solder balls can then be reflowed to join with the

unencapsulated portions of the wire bonds 2132 of package 2110A.

[0181] A further arrangement employing alignment surfaces 2251 is shown in Figs. 31A-C, wherein the alignment surfaces 2251 extend between a raised inner surface 2244 to a lower outer surface 2245. In such an arrangement, inner surface 2244 can overlie microelectronic element 2222 and can be spaced above substrate 2212 accordingly. Outer surface 2245 can be spaced closer to substrate 2212 in a direction of the thickness of the substrate and can be positioned vertically between surface 2214 of substrate 2212 and surface 2223 of microelectronic element 2222. One or more unencapsulated portions of wire bonds 2232 can be positioned relative to the alignment surfaces 2251 to achieve alignment of solder balls 2252 or other conductive protrusion as described with respect to Figs. 30A-C. As described above, such a stepped arrangement can be used with or without the described alignment functionality to achieve an overall lower assembly height given a certain bond mass size. Further, the incorporation of a raised inner surface 2244 can lead to increased resistance of package 2210A to warping.

[0182] Fig. 12 is a photographic image showing exemplary joints between the wire bonds 632 of a first component 610A and corresponding solder masses 652 of a second component such as a microelectronic package 610B. In Fig. 12, reference 620 indicates where an underfill can be disposed.

[0183] Figs. 13A, 13B, 13C, 13D, 13E and 13F illustrate some possible variations in the structure of the wire bonds 32 as described above relative to Fig. 1. For example, as seen in Fig. 13A, a wire bond 732A may have an upwardly extending portion 736 which terminates in an end 738A having the same radius as the radius of portion 736.

[0184] Fig. 13B illustrates a variation in which the ends 738B are tips which are tapered relative to portion 736. In addition, as seen in Fig. 13C, a tapered tip 738B of a wire bond 732A may have a centroid 740 which is offset in a radial direction 741 from an axis of a cylindrical portion of the wire bond integral therewith. Such shape may be a bonding tool mark resulting from a process of forming the wire bond as will be described further below. Alternatively, a bonding tool mark other than as shown at 738B may be present on the unencapsulated portion of the wire bond. As further seen in Fig. 13A, the unencapsulated portion 739 of a wire bond may project away from the substrate 712 at an angle 750 within 25 degrees of perpendicular to the surface 730 of the substrate on which the conductive elements 728 are disposed.

[0185] Fig. 13D illustrates that an unencapsulated portion of a wire bond 732D can include a ball-shaped portion 738D. Some of all of the wire bonds on the package can have such structure. As seen in Fig. 13D, the ball-shaped portion 738D can be integral with a cylindrical portion 736 of the wire bond 732D, wherein the ball-shaped portion and at least a core of the cylindrical portion of the wire bond consist essentially of copper, copper alloy or gold. As will be described further below, the ball-shaped portion can be formed by melting a portion of the wire exposed at an opening of the capillary of the bonding tool during a pre-shaping process before stitch-bonding the wire bond to a conductive element 728 of the substrate. As seen in Fig. 13D, the diameter 744 of the ball-shaped portion 738D may be greater than the diameter 746 of the cylindrical wire bond portion 736 that is integral therewith. In a particular embodiment such as shown in Fig. 13D, the cylindrical portion of a wire bond 732D that is integral with the ball-shaped portion 738D can project beyond a surface 752 of the encapsulant layer 751 of the

package. Alternatively, as seen in Fig. 13E, the cylindrical portion of a wire bond 732D may be fully covered by the encapsulant layer. In such case, as seen in Fig. 13E, the ball-shaped portion 738D of the wire bond 732D may in some cases be partly covered by the encapsulation layer 751.

[0186] Fig. 13F further illustrates a wire bond 732F having a core 731 of a primary metal and a metallic finish 733 thereon which includes a second metal overlying the primary metal, such as the palladium-clad copper wire or palladium-clad gold wire as described above. In another example, an oxidation protection layer of a non-metallic material such as a commercially available "organic solderability preservative" (OSP) can be formed on the unencapsulated portion of a wire bond to avoid oxidation thereof until the unencapsulated portion of the wire bond is joined to a corresponding contact of another component.

[0187] Fig. 14 illustrates a method by which wire bonds 32 (Fig. 1) as described herein can be shaped and then stitch-bonded to the conductive elements 28 on a substrate. As seen therein at stage A, a segment 800, i.e., an integral portion having a predetermined length 802, of a metal wire such as a gold or copper wire or composite wire as described above described above relative to Fig. 1 is fed out of a capillary 804 of a bonding tool. In order to ensure that a predetermined length of the metal wire is fed out from the capillary, the initial wire length can be zeroed or otherwise set to a known length by the bonding tool stitch-bonding the wire then extending from the capillary before beginning to feed the wire out for processing. At that time, the segment may extend in a straight direction 801 perpendicular to a face 806 of the capillary. As seen at stage B, the face 806 of the capillary 804 then is moved in at least a first direction 814 along, e.g., parallel to a first surface 812 of a forming unit

810 to bend the metal wire segment 800 away from the perpendicular direction. The forming unit 810 may be a specially designed tool having surfaces suitable to assist in the forming, i.e., shaping, of the metal wire segment prior to the metal wire segment being bonded to the conductive element of the substrate.

[0188] As seen at stage B during the pre-forming process, a portion of the segment 800 may then extend in a direction parallel to the surface 812. Thereafter, as seen at stage C, the capillary is moved over a second surface 816 which then causes at least a portion of the segment 800 to project upwardly in a direction 818 along an exterior wall 820 of the capillary. After pre-forming the metal wire segment 800 in this manner, the capillary of the bonding tool is now moved away from the forming unit 810 and moved towards the conductive element 28 (Fig. 1) of the substrate where it then stitch bonds a portion 822 of the metal wire segment adjacent to the capillary opening 808 and the capillary face 806 to the conductive element. As a result, an end 838 of the metal wire segment 800 remote from the capillary opening 808 becomes an end 38 (Fig. 1) of the wire bond remote from the conductive element 28.

[0189] Fig. 15 further illustrates an example of movement of the capillary over surfaces of a forming unit 810 in a method according to an embodiment of the invention. As seen therein, the forming unit 810 may have a first depression 830 in which the capillary 804 is disposed when the segment 800 is fed out of the opening 808 of the capillary at stage A of the forming process. The depression may include a channel or groove 832 which can help guide the segment 800 onto a surface 812 at stage B. The forming unit may further include a channel 834 or groove for guiding the segment 800 in stage B of the process. As further shown in Fig. 15, the forming unit

may include a further depression 840 having an interior surface 816 against which the capillary moves in stage C of the process to cause the metal wire segment to be bent in direction 818 against the exterior wall 820 of the capillary. The depression 840 in one example may have a triangular shape as seen in Fig. 15.

[0190] In an embodiment, a variation of the capillary shown in Fig. 14 can be used that incorporates a vertical or near-vertical side wall 2820. As shown in Fig. 35, the side wall 2820 of capillary 2804 can be substantially vertical or, in other words, parallel to the wire segment 2800 or perpendicular to the face 2806 of the capillary 2804. This can allow for formation of a wire bond (32 in Fig. 1) that is closer to vertical, i.e., closer to an angle of 90° away from the surface of the first surface of the substrate, than achieved by a side wall at an exterior of the capillary that defines an angle having a measure substantially less than 90°, such as the capillary shown in Fig. 14. For example, using a forming tool 2810, a wire bond can be achieved that is disposed at an angle from the first portion which extends between 25° and 90°, or between about 45° and 90° or between about 80° and 90° with respect to the first wire portion 2822.

[0191] In another variation, a capillary 3804 can include a surface 3808 that projects beyond the face 3806 thereof. This surface 3808 can be included, for example over the edge of the side wall 3820. In the method for forming a wire bond (32 in Fig. 1, for example), the capillary 3804 can be pressed against the first portion 3822 of the wire segment 3800 during forming of wire segment, e.g., when the capillary moves in a direction along a forming surface 3816 which extends in a direction away from surface 3812. In this example, surface 3808 presses into the first portion 3822 at a location near the bend from which the remaining wire segment 3800 extends.

This can cause deformation of the wire segment 3800 such that it may press against the wall 3820 of the capillary 3804 and move to a somewhat more vertical position once the capillary 3804 is removed. In other instances, the deformation from the surface 3808 can be such that a position of the wire segment 3800 can be substantially retained when the capillary 3804 is removed.

[0192] Fig. 16 is a photographic image showing that wire bonds 932 formed according to one or more of the methods described herein can have ends 938 which are offset from their respective bases 934. In one example, an end 938 of a wire bond can be displaced from its respective base such that the end 938 is displaced in a direction parallel to the surface of the substrate beyond a periphery of the conductive element to which it is connected. In another example, an end 938 of a wire bond can be displaced from its respective base 934 such that the end 938 is displaced in a direction parallel to the surface of the substrate beyond a periphery 933 of the conductive element to which it is connected.

[0193] Fig. 17 illustrates a variation of the above-described pre—forming process which can be used to form wire bonds 332Cii (Fig. 5) having a bend and which have ends 1038 displaced in a lateral direction 1014A from the portions 1022 which will be stitch-bonded to the conductive elements as bases 1034 of the wire bonds.

[0194] As seen in Fig. 17, the first three stages A, B, and C of the process can be the same as described above with reference to Fig. 14. Then, referring to stages C and D therein, a portion 1022A of the wire bond adjacent the face 806 of the capillary 804 is clamped by a tool which can be integrated with the forming unit. The clamping may be performed actively or passively as a result of the motion of the capillary over the forming unit. In one example, the

clamping can be performed by pressing a plate having a non-slip surface thereon onto the metal wire segment 800 to preclude movement of the metal wire segment.

[0195] While the metal wire segment 800 is clamped in this manner, at stage D shown in Fig. 17, the capillary tool moves in a direction 1016 along a third surface 1018 of the forming unit 1010 and feeds out a length of wire equivalent to the distance moved along surface 1018. Thereafter, at stage E, the capillary is moved downwardly along a third surface 1024 of the forming unit to cause a portion of the wire to be bent upwardly along an exterior surface 1020 of the capillary 804. In such way, an upwardly projecting portion 1026 of the wire can be connected to another upwardly projecting portion 1036 by a third portion 1048 of the metal wire.

[0196] A method for forming a microelectronic package 2710, having ball bonded wire bonds 2732, as shown in Fig. 40, includes various steps as illustrated in Figs. 41-44. Fig. 41 shows microelectronic assembly 2710' at a step where microelectronic element 2722 has been electrically and mechanically connected to substrate 2712 on first surface 2714 and within first region 2718, thereof. Microelectronic element 2722 is shown in Fig. 14 as being mounted on substrate 2712 in a flip-chip arrangement by solder masses 2726. Alternatively face-up bonding, could be used instead, as seen above in Fig. 40. In the embodiment of the method step shown in Fig. 11, a dielectric underfill layer 2766 may be provided between microelectronic element 2722 and substrate 2712.

[0197] Fig. 42 shows microelectronic assembly 10'' having wire bonds 2732 applied on pads 2730 of conductive elements 2728 exposed on first surface 2714 of substrate 2712. As discussed, wire bonds 2732 can be applied by heating an end of a wire segment to soften the end such that it forms a deposition bond to conductive element 2728 when pressed

thereto, forming base 2734. The wire is then drawn out away from conductive element 2728 and manipulated, if desired, in a specified shape before being cut or otherwise severed to form end 36 and end surface 2738 of wire bond 2732. Alternatively, wire bonds 2732 can be formed from, for example, an aluminum wire by wedge bonding. Wedge bonding is formed by heating a portion of the wire adjacent the end thereof and dragging it along the conductive element 2728 with pressure applied thereto. Such a process is described further in U.S. Pat. No. 7,391,121, the disclosure of which is incorporated by reference herein.

[0198] In Fig. 43 encapsulation layer 2742 has been added to microelectronic assembly 2710''' by being applied over first surface 2714 of substrate, extending upwardly therefrom and along edge surfaces 2737 of wire bonds 2732. Encapsulation layer 2742 also covers underfill layer 2766. Encapsulation layer 2742 can be formed by depositing a resin over microelectronic assembly 2710' shown in Fig. 42. This can be done by placing assembly 2710' in an appropriately configured mold having a cavity in the desired shape of the encapsulation layer 2742 that can receive assembly 2710'. Such a mold and the method of forming a encapsulation layer therewith can be as shown and described in U.S. Pat. App. Pub. No 2010/0232129, the disclosure of which is incorporated by reference herein it its entirety. Alternatively, encapsulation layer 2742 can be prefabricated to the desired shape from an at least partially compliant material. In this configuration, compliant properties of the dielectric material allow encapsulation layer 2742 to be pressed into position over wire bonds 2732 and microelectronic element 2722. In such a step, wire bonds 2732 penetrate into the compliant material forming respective holes therein, along which encapsulation layer 2742 contacts edge surfaces 2737.

Further, microelectronic element 2722 may deform the compliant material so that it can be received therein. The compliant dielectric material can be compressed to expose end surfaces 2738 on outer surface 2744. Alternatively, any excess compliant dielectric material can be removed from encapsulation layer to form a surface 2744 on which ends surfaces 2738 of wire bonds 2732 are uncovered or cavities 2764 can be formed that uncover end surfaces 38 at a location within surface 2763.

[0199] In the embodiment shown in Fig. 43, encapsulation layer is formed such that, initially, surface 2744 thereof is spaced above end surfaces 2738 of wire bonds 2732. To expose the end surfaces 2738, the portion of encapsulation layer 2742 that is above end surfaces 2738 can be removed, exposing a new surface 2744' that is substantially flush with end surfaces 2742, as shown in Fig. 44. Alternatively, cavities (not shown) can be formed in which end surfaces 2738 are uncovered by encapsulation layer 2742. In a further alternative, encapsulation layer 2742 can be formed such that surface 2744 is already substantially flush with end surfaces 2738 or such that surface 2744 is positioned below end surfaces 2738. Removal, if necessary, of a portion of encapsulation layer 2742 can be achieved by grinding, dry etching, laser etching, wet etching, lapping, or the like. If desired, a portion of the ends 2738 of wire bonds 2732 can also be removed in the same, or an additional, step to achieve substantially planar end surface 2738 that are substantially flush with surface 2744. If desired, cavities can also be formed after such a step, or stud bumps can also be applied. The resulting microelectronic assembly 2710 can then be affixed on a PCB or otherwise incorporated in a further assembly, for example a stacked package, as shown in Fig. 6.

[0200] After formation of the wire segment and bonding thereof to a conductive element to form a wire bond, particularly of the ball bond type discussed above, the wire bond (32 in Fig. 1, for example) is then separated from a remaining portion of the wire within the capillary (such as 804 in fig. 32A). This can be done at any location remote from the base 34 of the wire bond 32 and is preferably done at a location remote from the base 34 by a distance at least sufficient to define the desired height of the wire bond 32. Such separation can be carried out by a mechanism disposed within the capillary 804 or disposed outside of the capillary 804, between the face 806 and the base 34 of the wire bond 32. In one method, the wire segment 800 can be separated by effectively burning through the wire 800 at the desired separation point, which can be done by application of a spark or flame thereto. To achieve greater accuracy in wire bond height, different forms of cutting the wire segment 800 can be implemented. As described herein, cutting can be used to describe a partial cut that can weaken the wire at a desired location or cutting completely through the wire for total separation of the wire bond 32 from the remaining wire segment 800.

[0201] In one example shown in Fig. 32 a cutting blade 805 can be integrated into the bond head assembly, such as within capillary 804. As shown, an opening 807 can be included in the side wall 820 of the capillary 804 through which cutting blade 805 can extend. The cutting blade 805 can be moveable in and out of the interior of the capillary 804 so that it can alternately allow the wire 800 to freely pass therethrough or engage the wire 800. Accordingly, the wire 800 can be drawn out and the wire bond 32 formed and bonded to a conductive element 28 with the cutting blade 805 in a position outside of the capillary interior. After bond formation, the wire

segment 800 can be clamped using a clamp 803 integrated in the bond head assembly to secure the position of the wire. The cutting blade 803 can then be moved into the wire segment to either fully cut the wire or to partially cut or weaken the wire. A full cut can form end surface 38 of the wire bond 32 at which point the capillary 804 can be moved away from the wire bond 32 to, for example, form another wire bond. Similarly, if the wire segment 800 is weakened by the cutting blade 805, movement of the bond head unit with the wire still held by the wire clamp 803 can cause separation by breaking the wire 800 at the area weakened by the partial cut.

[0202] The movement of the cutting blade 805 can be actuated by pneumatics or by a servo motor using an offset cam. In other examples the cutting blade 805 movement can be actuated by a spring or a diaphragm. The triggering signal for the cutting blade 805 actuation can be based on a time delay that counts down from formation of the ball bond or can be actuated by movement of the capillary 804 to a predetermined height above the wire bond base 34. Such a signal can be linked to other software that operates the bonding machine so that the cutting blade 805 position can be reset prior to any subsequent bond formation. The cutting mechanism can also include a second blade (not shown) at a location juxtaposed with blade 805 with the wire therebetween, so as to cut the wire by movement of one or more of the first and second blades relative to the other of the first and second blades, such as in one example, from opposite sides of the wire.

[0203] In another example, a laser 809 can be assembled with the bond head unit and positioned to cut the wire. As shown in Fig. 33, a laser head 809 can be positioned outside of capillary 804 such as by mounting thereto or to another point on the bond head unit that includes capillary 804. The

laser can be actuated at a desired time, such as those discussed above with respect to the cutting blade 805 in Fig. 32, to cut the wire 800, forming end surface 38 of the wire bond 32 at a desired height above the base 34. In other implementations, the laser 809 can be positioned to direct the cutting beam through or into the capillary 804 itself and can be internal to the bond head unit. In an example, a carbon dioxide laser can be used or, as an alternative, a Nd:YAG or a Cu vapor laser could be used.

[0204] In another embodiment a stencil unit 824 as shown in Figs. 34A-C can be used to separate the wire bonds 32 from the remaining wire segment 800. As shown in Fig. 34A, the stencil 824 can be a structure having a body that defines an upper surface 826 at or near the desired height of the wire bonds 32. The stencil 824 can be configured to contact the conductive elements 28 or any portions of the substrate 12 or package structure connected thereto between the conductive elements 28. The stencil includes a plurality of holes 828 that can correspond to the desired locations for the wire bonds 32, such as over conductive elements 28. The holes 828 can be sized to accept the capillary 804 of the bond head unit therein so that the capillary can extend into the hole to a position relative to the conductive element 28 to bond the wire 800 to the conductive element, 28 to form the base 34, such as by ball bonding or the like. In one example, the stencil can have holes through which individual ones of the conductive elements are exposed. In another example, a plurality of the conductive elements can be exposed by a single hole of the stencil. For example, a hole can be a channel-shaped opening or recess in the stencil through which a row or column of the conductive elements are exposed at a top surface 826 of the stencil.

[0205] The capillary 804 can then be moved vertically out of the hole 828 while drawing out the wire segment to a desired length. Once cleared from the hole 828, the wire segment can be clamped within the bond head unit, such as by clamp 803, and the capillary 804 can be moved in a lateral direction (such as parallel to the surface 826 of stencil 824) to move the wire segment 800 into contact with an edge 829 of the stencil 824 defined by the intersection of the surface of the hole 828 and the outside surface 826 of the stencil 824. Such movement can cause separation of the wire bond 32 from a remaining portion of the wire segment 800 that is still held within the capillary 804. This process can be repeated to form the desired number of wire bonds 32 in the desired locations. In an implementation, the capillary can be moved vertically prior to wire separation such that the remaining wire segment projects beyond the face 806 of the capillary 804 by a distance 802 sufficient to form a subsequent ball bond. Fig. 34B shows a variation of stencil 824 in which the holes 828 can be tapered such that they have a diameter that increases from a first diameter at surface 826 to a greater diameter away from surface 826. In another variation, as shown in Fig. 34C, the stencil can be formed having an outer frame 821 having a thickness sufficient to space apart surface 826 at the desired distance from substrate 12. Frame 821 can at least partially surround a cavity 823 configured to be positioned adjacent substrate 12 with a thickness of the stencil 824 extending between the surface 826 and the open area 823 such that the portion of stencil 824 that includes the holes 828 is spaced apart from the substrate 12 when positioned thereon.

[0206] Figs. 18, 19 and 20 illustrate one technique that can be used when forming the encapsulation layer by molding in order that unencapsulated portions 39 (Fig. 1) of the wire

bonds project beyond a surface 44 of the encapsulation layer 42. Thus, as seen in Fig. 18, a film-assisted molding technique can be used by which a temporary film 1102 is placed between a plate 1110 of a mold and a cavity 1112 in which a subassembly including the substrate, wire bonds 1132 joined thereto, and a component such as a microelectronic element may be joined. Fig. 18 further shows a second plate 1111 of the mold which can be disposed opposite the first plate 1110.

[0207] Then, as seen in Figs. 19-20, when the mold plates 1110, 1111 are brought together, the ends 1138 of wire bonds 1132 can project into the temporary film 1102. When a mold compound is flowed in the cavity 1112 to form encapsulation layer 1142, the mold compound does not contact the ends 1138 of the wire bonds because they are covered by the temporary film 1102. After this step, the mold plates 1110, 1111 are removed from the encapsulation layer 1142, the temporary film 1102 can now be removed from the mold surface 1144, which then leaves the ends 1138 of the wire bonds 1132 projecting beyond the surface 1144 of the encapsulation layer.

[0208] The film-assisted molding technique may be well adapted for mass production. For example, in one example of the process, a portion of a continuous sheet of the temporary film can be applied to the mold plate. Then the encapsulation layer can be formed in a cavity 1112 that is at least partially defined by the mold plate. Then, a current portion of the temporary film 1102 on the mold plate 1110 can be replaced by automated means with another portion of the continuous sheet of the temporary film.

[0209] In a variation of the film-assisted molding technique, instead of using a removable film as described above, a water-soluble film can be placed on an inner surface of the mold plate 1110 prior to forming the encapsulation layer. When the mold plates are removed, the water soluble

film can be removed by washing it away so as to leave the ends of the wire bonds projecting beyond the surface 1144 of the encapsulation layer as described above.

[0210] In an example of the method of Figs. 18 and 19, the heights of the wire bonds 1132 above the surface 1144 of encapsulation layer 1142 can vary among the wire bonds 1132, as shown in Fig. 37A. A method for further processing the package 1110 such that the wire bonds 1132 project above surface 1142 by substantially uniform heights is shown in Figs. 37B-D and utilizes a sacrificial material layer 1178 that can be formed to cover the unencapsulated portions of the wire bonds 1132 by application thereof over surface 1144. The sacrificial layer 1178 can then be planarized to reduce the height thereof to the desired height for wire bonds 1132, which can be done by lapping, grinding, or polishing or the like. As also illustrated in the Figures, the planarization of the sacrificial layer 1178 can begin by reducing the height thereof to a point where the wire bonds 1132 become exposed at the surface of the sacrificial layer 1178. The planarization process can then also planarize the wire bonds 1132 simultaneously with the sacrificial layer 1178 such that, as the height of the sacrificial layer 1178 is continued to be reduced, the heights of the wire bonds 1132 are also reduced. The planarization can be stopped once the desired height for the wire bonds 1132 is reached. It is noted that in such a process the wire bonds 1132 can be initially formed such that their heights, while being non-uniform, are all greater than the targeted uniform height. After planarization reduces the wire bonds 1132 to the desired height, the sacrificial layer 1178 can be removed such as by etching or the like. The sacrificial layer 1178 can be formed from a material that can allow for removal by etching using an etchant that will not significantly affect the encapsulant material. In one

example, the sacrificial layer 1178 can be made from a water soluble plastic material.

[0211] Figs. 21 and 22 illustrate another method by which unencapsulated portions of the wire bonds can be formed which project beyond a surface of the encapsulation layer. Thus, in the example seen in Fig. 21, initially wire bonds 1232 may be flush with or may not even be exposed at a surface 1244 of the encapsulation layer 1242. Then, as shown in Fig. 22, a portion of the encapsulation layer, e.g., a molded encapsulation layer, can be removed to cause the ends 1238 to project beyond the modified encapsulation layer surface 1246. Thus, in one example, laser ablation can be used to recess the encapsulation layer uniformly to form a planar recessed surface 1246. Alternatively, laser ablation can be performed selectively in areas of the encapsulation layer adjoining individual wire bonds.

[0212] Among other techniques that can be used to remove at least portions of the encapsulation layer selectively to the wire bonds include "wet blasting" techniques. In wet blasting, a stream of abrasive particles carried by a liquid medium is directed towards a target to remove material from the surface of the target. The stream of particles may sometimes be combined with a chemical etchant which may facilitate or accelerate the removal of material selectively to other structure such as the wire bonds which are to remain after wet blasting.

[0213] In the example shown in Figs. 38A and 38B, in a variation of the method shown in Figs. 21 and 22, wire bond loops 1232' can be formed that have bases 1234a on conductive elements 1228 at one end and are attached to a surface of the microelectronic element 1222 at the other end 1234b. For attachment of the wire bond loops 1232' to the microelectronic element 1222, the surface of the microelectronic element 1223

can be metalized such as by sputtering, chemical vapor deposition, plating or the like. The bases 1234a can be ball bonded, as shown, or edge bonded, as can the ends 1232b joined to the microelectronic element 1222. As further shown in Fig. 38A, the dielectric encapsulation layer 1242 can be formed over substrate 1212 to cover the wire bond loops 1232'. The encapsulation layer 1242 can then be planarized, such as by grinding, lapping, polishing, or the like, to reduce the height thereof and to separate the wire bond loops 1232' into connection wire bonds 1232A that are available for joining to at least the end surfaces 1238 thereof for electrical connection to the conductive elements 1228 and thermal dissipation bonds 1232B that are joined to the microelectronic element 1222. The thermal dissipation bonds can be such that they are not electrically connected to any of the circuitry of the microelectronic element 1222 but are positioned to thermally conduct heat away from the microelectronic element 1222 to the surface 1244 of the encapsulation layer 1242. Additional processing methods can be applied to the resulting package 1210', as described elsewhere herein.

[0214] Another method for forming wire bonds 2632 to a predetermined height is shown in Figs. 39A-C. In such a method a sacrificial encapsulation layer 2678 can be formed over the surface 2614 of substrate 2612, at least in the second 2620 region thereof. The sacrificial layer 2678 can also be formed over the first region 2618 of the substrate 2612 to cover the microelectronic element 2622 in a similar manner to the encapsulation layers described with respect to Fig. 1, above. The sacrificial layer 2678 includes at least one opening 2679 and in some embodiments a plurality of openings 2679 to expose the conductive elements 2628. The openings 2679 can be formed during molding of the sacrificial layer 2678 or after molding by etching, drilling, or the like.

In one embodiment, a large opening 2679 can be formed to expose all of the conductive elements 2628, while in other embodiments a plurality of large openings 2679 can be formed to expose respective groups of conductive elements 2628. In further embodiments, openings 2629 can be formed that correspond to individual conductive elements 2628. The sacrificial layer 2678 is formed having a surface 2677 at a desired height for the wire bonds 2632 such that the wire bonds 2632 can be formed by bonding bases 2634 thereof to the conductive elements 2628 and then drawing out the wire to reach the surface 2677 of the sacrificial layer 2678. Then, the wire bonds can be drawn laterally of the opening to overlie portions of the surface 2677 of the sacrificial layer 2678. The capillary of the bond forming instrument (such as capillary 804 as shown in Fig. 14) can be moved to press the wire segment into contact with the surface 2677 such that the pressure on the wire between the surface 2677 and the capillary causes the wire to sever on surface 2677, as shown in Fig. 39A.

[0215] The sacrificial layer 2678 can then be removed by etching or another similar process. In an example, the sacrificial layer 2678 can be formed from a water soluble plastic material such that it can be removed by exposure to water without affecting the other components of the in-process unit 2610''. In another embodiment, sacrificial layer 2678 can be made from a photoimageable material such as a photoresist such that it can be removed by exposure to a light source. A portion of sacrificial layer 2678' can remain between microelectronic element 2622 and surface 2614 of substrate 2612 that can act as an underfill surrounding solder balls 2652. After removal of the sacrificial layer 2678 an encapsulation layer 2642 is formed over the in-process unit to form package 2610. The encapsulation layer 2642 can be

similar to those described above and can substantially cover surface 2614 of substrate 2612 and microelectronic element 2622. Encapsulation layer 2642 can further support and separate the wire bonds 2632. In the package 2610 shown in Fig. 29C, the wire bonds include portions of the edge surfaces 2637 thereof that are exposed at surface 2644 of the encapsulant 2642 and extend substantially parallel thereto. In other embodiments, the wire bonds 2632 and the encapsulation layer 2642 can be planarized to form a surface 2644 with wire bonds that have end surfaces exposed thereon and substantially flush therewith.

[0216] The above-described embodiments and variations of the invention can be combined in ways other than as specifically described above. It is intended to cover all such variations which lie within the scope and spirit of the invention.

CLAIMS

1. A microelectronic package comprising:

a substrate having a first region and a second region, the substrate having a first surface and a second surface remote from the first surface;

at least one microelectronic element overlying the first surface within the first region;

electrically conductive elements exposed at at least one of the first surface and the second surface of the substrate within the second region, at least some of the conductive elements being electrically connected to the at least one microelectronic element;

wire bonds defining edge surfaces and having bases bonded to respective ones of the conductive elements, the bases including first portions of the edge surfaces that extend along the conductive elements with respective second portions of the edge surfaces being at an angle between 25° and 90° relative to the first portions, the wire bonds further having ends remote from the substrate and remote from the bases; and

a dielectric encapsulation layer extending from at least one of the first or second surfaces and covering portions of the wire bonds such that covered portions of the wire bonds are separated from one another by the encapsulation layer, the encapsulation layer overlying at least the second region of the substrate, wherein unencapsulated portions of the wire bonds are defined by portions of the wire bonds that are uncovered by the encapsulation layer, the unencapsulated portions including the ends wherein the conductive elements are disposed at positions in a pattern having a first minimum pitch between respective adjacent conductive elements of the plurality of conductive elements, and wherein the unencapsulated portions are disposed in positions in a pattern

having a second minimum pitch between respective ends of adjacent wire bonds of the plurality of wire bonds, the second pitch being greater than the first pitch.

2. The microelectronic package as set forth in claim 1, wherein the angle is between 80° and 90°.

3. The microelectronic package as set forth in claim 1, wherein each of at least some of the unencapsulated portions of the wire bonds includes a ball-shaped portion, each ball-shaped portion being integral with a cylindrical portion of such wire bond, each ball-shaped portion and each cylindrical portion having at least a core consisting essentially of copper, copper alloy or gold.

4. The microelectronic package as set forth in claim 3, wherein the cylindrical portions integral with the ball-shaped portions project beyond a surface of the encapsulation layer.

5. The microelectronic package as set forth in claim 1, wherein at least some of the wire bonds have a core of a primary metal and a metallic finish including a second metal different from the primary metal overlying the primary metal.

6. The microelectronic package as set forth in claim 5, wherein the primary metal is copper and the metallic finish includes a layer of silver.

7. The microelectronic package as set forth in claim 1, wherein the conductive elements are first conductive elements, the microelectronic package further comprising a plurality of second conductive elements electrically connected to the unencapsulated portions of the wire bonds, wherein the second

conductive elements do not contact the first conductive elements.

8. The microelectronic package as set forth in claim 7, wherein the second conductive elements are formed by plating in contact with the unencapsulated portions of the wire bonds after forming the encapsulation layer.

9. The microelectronic package as set forth in claim 1, wherein an end of at least one of the wire bonds is displaced in a direction parallel to the first surface of the substrate from its base by at least a distance equal to one of: a minimum pitch between the conductive elements, and 100 microns, wherein at least one of the wire bonds includes at least one bend between the base thereof and the unencapsulated portion thereof and, wherein the bend of the at least one wire bond is remote from the base thereof and the unencapsulated portion thereof.

10. The microelectronic package as set forth in claim 9, wherein a radius of the bend is greater than twelve times a diameter of a cylindrical portion of the at least one wire bond.

11. The microelectronic package as set forth in claim 9, wherein the radius of the bend is less than ten times a diameter of a cylindrical portion of the at least one wire bond.

12. The microelectronic package as set forth in claim 9, wherein the unencapsulated portion of the at least one wire bond projects above the encapsulation layer in a direction

within 25 degrees of perpendicular relative to the first surface of the substrate.

13. The microelectronic package as set forth in claim 1, wherein the conductive elements are non-solder mask defined.

14. The microelectronic package as set forth in claim 1, further comprising ball bonds joined to and overlying portions of the bases of the wire bonds.

15. The microelectronic package as set forth in claim 1, wherein the at least one microelectronic element includes first and second microelectronic elements overlying the first surface within the first region, wherein at least some of the conductive elements are connected with the first microelectronic element, and wherein at least some conductive elements are connected with the second microelectronic element, and wherein the first microelectronic element and the second microelectronic elements are electrically connected with one another within the microelectronic package

16. A microelectronic package comprising:

a substrate having a first region and a second region, the substrate having a first surface and a second surface remote from the first surface;

at least one microelectronic element overlying the first surface within the first region;

first electrically conductive elements exposed at at least one of the first surface and the second surface of the substrate within the second region, at least some of the first conductive elements being electrically connected to the at least one microelectronic element;

wire bonds having bases joined to respective ones of the first conductive elements, and end surfaces remote from the substrate and remote from the bases, each wire bond defining an edge surface extending between the base and the end surface thereof;

a dielectric encapsulation layer extending from at least one of the first or second surfaces and filling spaces between the wire bonds such that the wire bonds are separated from one another by the encapsulation layer, the encapsulation layer overlying at least the second region of the substrate, wherein unencapsulated portions of the wire bonds are defined by at least portions of the end surfaces of the wire bonds that are uncovered by the encapsulation layer,

the encapsulation layer including a major surface and an alignment surface sloped with respect to the major surface, at least one unencapsulated portion of the wire bond being positioned on the major surface and the alignment surface being proximate to the major surface at a location adjacent to the unencapsulated portion such that the alignment surface is configured to guide an electrically conductive protrusion disposed above the alignment surface towards the unencapsulated portion of the wire bond.

17. The microelectronic package as set forth in claim 16, wherein the protrusion includes a bond metal.

18. The microelectronic package as set forth in claim 17, wherein the bond metal includes a solder ball attached to a circuit element.

19. The microelectronic package as set forth in claim 16, wherein the encapsulation layer defines a corner region thereof, the encapsulation layer further including at least

one minor surface positioned within the corner region and being positioned farther from the substrate than the major surface, the alignment surface extending between the minor surface and the major surface.

20. The microelectronic package as set forth in claim 16, wherein the major surface is a first major surface that overlies the first region of the substrate, the encapsulation layer further defining a second major surface overlying the second region and being positioned closer to the substrate than the major surface, the alignment surface extending between the first and second major surfaces.

21. A microelectronic assembly, comprising:

a first microelectronic package as set forth in claim 16;

a second microelectronic package defining a front surface having terminals thereon; and

a plurality of conductive protrusions connecting at least some of the unencapsulated portions of the wire bonds with respective ones of the terminals;

wherein at least one of the conductive protrusions is positioned in contact with a portion of the alignment surface.

22. The microelectronic assembly as set forth in claim 21, wherein the conductive protrusions include solder balls.

23. A microelectronic package comprising:

a substrate having a first region and a second region, the substrate having a first surface and a second surface remote from the first surface;

at least one microelectronic element overlying the first surface within the first region;

electrically conductive elements exposed at at least one of the first surface and the second surface of the substrate within the second region, at least some of the conductive elements being electrically connected to the at least one microelectronic element;

ball bonds joined to at least some of the conductive elements;

wire bonds defining edge surfaces and having bases bonded to the ball bonds atop the at least some conductive elements, the bases including first portions of the edge surfaces that extend over the conductive elements with respective second portions of the edge surfaces being at an angle between 25° and 90° relative to the first portions, the wire bonds further having ends remote from the substrate and remote from the bases; and

a dielectric encapsulation layer extending from at least one of the first or second surfaces and covering portions of the wire bonds such that covered portions of the wire bonds are separated from one another by the encapsulation layer, the encapsulation layer overlying at least the second region of the substrate, wherein unencapsulated portions of the wire bonds are defined by portions of the wire bonds that are uncovered by the encapsulation layer, the unencapsulated portions including the ends.

24. A microelectronic assembly comprising:

a first microelectronic package as set forth in claim 1 and further including a plurality of terminals exposed at the second surface of the substrate, and peripheral edges extending in a direction between the first and second surfaces of the substrate;

a second microelectronic package including a substrate having contacts thereon, a second microelectronic element

electrically connected with the contacts, and terminals exposed at a surface of the substrate and electrically connected with the second microelectronic element through the contacts, the terminals of the second microelectronic element facing and being electrically connected with respective unencapsulated portions of the wire bonds;

a circuit panel including a first surface and panel contacts exposed at the surface thereof, the first microelectronic package overlying the circuit panel and having the terminals of the first microelectronic package joined to the panel contacts of the circuit panel; and

a monolithic underfill overlying at least one of the peripheral edges of the first microelectronic package and disposed within spaces surrounding the joints between the terminals of the first microelectronic package and the panel contacts of the circuit panel, and disposed within spaces surrounding the joints between the terminals of the second microelectronic package and the first microelectronic package.

25. A microelectronic package comprising:

a substrate having a first region and a second region, the substrate having a first surface and a second surface remote from the first surface;

at least one microelectronic element overlying the first surface within the first region;

first electrically conductive elements exposed at at least one of the first surface and the second surface of the substrate within the second region, at least some of the first conductive elements being electrically connected to the at least one microelectronic element;

wire bonds having bases joined to respective ones of the first conductive elements, and end surfaces remote from the substrate and remote from the bases, each wire bond defining

an edge surface extending between the base and the end surface thereof;

a dielectric encapsulation layer extending from the first surface and filling spaces between the wire bonds such that the wire bonds are separated from one another by the encapsulation layer, the encapsulation layer defining a first surface portion at a first height above the first surface in an area overlying the first region of the substrate and a second surface portion at a second height above the first surface in an area overlying the second region of the substrate, wherein the second height is less than the first height, and wherein unencapsulated portions of the wire bonds are defined by at least portions of the end surfaces of the wire bonds that are uncovered by the encapsulation layer.

26. The microelectronic package as set forth in claim 25, wherein the microelectronic element defines a front face spaced above the first surface at a third height, and wherein the second height is further less than the third height.

27. A microelectronic package comprising:

a substrate having a first region and a second region, the substrate having a first surface and a second surface remote from the first surface;

at least one microelectronic element overlying the first surface within the first region;

first electrically conductive elements exposed at at least one of the first surface and the second surface of the substrate within the second region, at least some of the first conductive elements being electrically connected to the at least one microelectronic element;

wire bonds having ball-bond bases joined to respective ones of the first conductive elements, and end surfaces remote

from the substrate and remote from the bases by a distance of less than three times a diameter of the base, each wire bond defining an edge surface extending between the base and the end surface thereof;

a dielectric encapsulation layer extending from the first surface and filling spaces between the wire bonds such that the wire bonds are separated from one another by the encapsulation layer, wherein unencapsulated portions of the wire bonds are defined by at least portions of the end surfaces of the wire bonds that are uncovered by the encapsulation layer.

28. The microelectronic package as set forth in claim 27, wherein the ball bond bases include a first ball bond joined to the respective conductive elements and second ball bonds joined to the first ball bonds, the end surfaces extending between the end surfaces and the second ball bonds.

29. A microelectronic package comprising:

a substrate having a first region and a second region, the substrate having a first surface and a second surface remote from the first surface;

at least one microelectronic element overlying the first surface within the first region;

first electrically conductive elements exposed at at least one of the first surface and the second surface of the substrate within the second region, at least some of the first conductive elements being electrically connected to the at least one microelectronic element;

wire bonds having bases joined to at least some of the first conductive elements, and end surfaces remote from the substrate and remote from the bases, each wire bond defining an edge surface extending between the base and the end surface

thereof, wherein at least two of the wire bonds are joined to an individual first conductive element of the plurality of first conductive elements;

a dielectric encapsulation layer extending from at least one of the first or second surfaces and filling spaces between the wire bonds such that the wire bonds are separated from one another by the encapsulation layer, the encapsulation layer overlying at least the second region of the substrate, wherein unencapsulated portions of the wire bonds are defined by at least portions of the end surfaces of the wire bonds that are uncovered by the encapsulation layer.

30. A method of making a microelectronic package comprising:

forming a dielectric encapsulation layer on an in-process unit including a substrate having a first surface and a second surface remote therefrom, a microelectronic element mounted to the first surface of the substrate, a plurality of conductive elements exposed at the first surface, at least some of the conductive elements being electrically connected to the microelectronic element, and wire bonds having bases joined to the conductive elements and end surfaces remote from the bases, each wire bond defining an edge surface extending away between the base and the end surface;

wherein the encapsulation layer is formed so as to at least partially cover the first surface and portions of the wire bonds such that unencapsulated portions of the wire bonds are defined by a portion of at least one of the end surface or of the edge surface thereof that is uncovered by the encapsulation layer, the encapsulation layer further being formed to include a major surface and an alignment surface angled with respect to the major surface, at least one unencapsulated portion of the wire bond being positioned on

the major surface and the alignment surface intersecting the major surface at a location in proximity to the unencapsulated portion such that the alignment surface is configured to guide an electrically conductive protrusion disposed above the alignment surface towards the unencapsulated portion of the wire bond.

31. The method as set forth in claim 30, wherein encapsulation layer is further formed to define a corner region thereof and to further include at least one minor surface positioned within the corner region and being positioned farther from the substrate than the major surface, the alignment surface extending between the minor surface and the major surface.

32. The method as set forth in claim 30, wherein the major surface of the encapsulation layer is a first major surface that overlies the first region of the substrate, the encapsulation layer being further formed to define a second major surface overlying the second region and being positioned closer to the substrate than the major surface, the alignment surface extending between the minor surface and the major surface.

33. A method for making a microelectronic assembly, comprising:

aligning a second microelectronic package with a first microelectronic package made according to the method of claim 30, the second microelectronic package including a substrate defining a first surface with contact pads exposed thereon and conductive masses joined with the contact pads, wherein the second microelectronic package is aligned with the first microelectronic package by moving at least one of the solder

balls into contact with both the alignment surface and at least the end surface of at least one wire bond; and

reflowing the conductive masses to join the conductive masses with respective ones of the unencapsulated portions of the wire bonds.

34. A method for making a microelectronic assembly, comprising:

aligning a second microelectronic package with a first microelectronic package made according to a method including:

forming a dielectric encapsulation layer on an in-process unit including a substrate having a first surface and a second surface remote therefrom, a microelectronic element mounted to the first surface of the substrate, a plurality of conductive elements exposed at the first surface, at least some of the conductive elements being electrically connected to the microelectronic element, and wire bonds having bases joined to the conductive elements and end surfaces remote from the bases, each wire bond defining an edge surface extending away between the base and the end surface, wherein the encapsulation layer is formed so as to at least partially cover the first surface and portions of the wire bonds, such that unencapsulated portions of the wire bonds are defined by a portion of at least one of the end surface or of the edge surface thereof that is uncovered by the encapsulation layer;

the second microelectronic package including a substrate defining a first surface with contact pads exposed thereon and being sized relative to the first microelectronic package such that it can be aligned such that dispensing area defined by a portion of the encapsulation layer extending laterally beyond an edge surface of the second microelectronic package; and

depositing an underfill material onto the dispensing area such that the underfill material flows into a space defined between the encapsulation layer and the first surface of the substrate of the second microelectronic package and a quantity of the underfill on the dispensing area can flow into the space between confronting surfaces of the first and second microelectronic packages.

35. The method as set forth in claim 34, wherein the second microelectronic package includes four edge surfaces, and wherein the dispensing area is defined by a portion of the encapsulation layer extending laterally beyond all four edge surfaces to surround the second microelectronic package.

36. The method as set forth in claim 34, wherein the second microelectronic package includes four edge surfaces, and wherein the dispensing area is defined by a portion of the encapsulation layer extending laterally beyond two adjacent ones of the edge surfaces.

37. The method as set forth in claim 34, wherein the second microelectronic package includes four edge surfaces, and wherein the dispensing area is defined by a portion of the encapsulation layer extending laterally beyond a single edge surface.

38. A method for making a microelectronic assembly, comprising:

positioning a plurality of conductive masses between a first microelectronic package and a second microelectronic package, the second microelectronic package including a substrate defining a first surface with second contact pads exposed thereon, wherein the conductive masses are further

positioned between respective first contact pads and second contact pads, and the first microelectronic package being made by a method including:

forming a dielectric encapsulation layer on an in-process unit including a substrate having a first surface and a second surface remote therefrom, a microelectronic element mounted to the first surface of the substrate, a plurality of conductive elements exposed at the first surface and a plurality of terminals exposed at the second surface, at least some of the conductive elements being electrically connected to the microelectronic element, and wire bonds having bases joined to the conductive elements and end surfaces remote from the bases, each wire bond defining an edge surface extending away between the base and the end surface, wherein the encapsulation layer is formed so as to at least partially cover the first surface and portions of the wire bonds, such that unencapsulated portions of the wire bonds are defined by a portion of at least one of the end surface or of the edge surface thereof that is uncovered by the encapsulation layer;

assembling a compliant bezel around edge surfaces of the first and second microelectronic packages; and

reflowing the conductive masses to join the respective first contact pads and second contact pads.

39. A method of making a microelectronic package comprising:

a) feeding a metal wire segment having a predetermined length out of a capillary of a bonding tool;

b) moving the face of the capillary over first and second surfaces of a forming unit to shape the metal wire segment to have a first portion projecting upwardly in a direction along an exterior wall of the capillary; and

c) using the bonding tool to bond a second portion of the metal wire to a ball bond joined on a conductive element exposed at a first surface of a substrate, the second portion of the metal wire being positioned to extend along the conductive element with the first portion positioned at an angle between 25° and 90° to the second portion;

d) repeating steps (a) through (c) to bond a plurality of the metal wires to a plurality of the conductive elements of the substrate; and

e) then forming a dielectric encapsulation layer overlying the surface of the substrate, wherein the encapsulation layer is formed so as to at least partially cover the surface of the substrate and portions of the wire bonds, such that unencapsulated portions of the wire bonds are defined by a portion of at least one of an end surface or of an edge surface thereof that is uncovered by the encapsulation layer.

40. A method of making a microelectronic assembly, comprising:

joining a first microelectronic package with a second microelectronic package, the second microelectronic package including a substrate having a first surface spaced apart from and facing the encapsulation layer, and the first microelectronic package being made by a method including:

forming a dielectric encapsulation layer on an in-process unit including a substrate having a first surface and a second surface remote therefrom, a microelectronic element mounted to the first surface of the substrate, a plurality of conductive elements exposed at the first surface and a plurality of terminals exposed at the second surface, at least some of the conductive elements being electrically connected to the microelectronic element, and wire bonds

having bases joined to the conductive elements and end surfaces remote from the bases, each wire bond defining an edge surface extending away between the base and the end surface, wherein the encapsulation layer is formed so as to at least partially cover the first surface and portions of the wire bonds, such that unencapsulated portions of the wire bonds are defined by a portion of at least one of the end surface or of the edge surface thereof that is uncovered by the encapsulation layer;

joining the first microelectronic package with a circuit panel having a surface spaced apart from and facing the second surface of the substrate, the first microelectronic package and circuit panel being joined between the terminals of the first microelectronic package and contact pads exposed on the surface of the circuit panel; and

forming a monolithic underfill surrounding exposed portions of the first microelectronic package and filling the spaces surrounding the joints between the terminals of the first microelectronic package and the circuit panel and the joints between the terminals of the second microelectronic package and the first package.

41. A method of making a microelectronic package comprising:

forming a sacrificial material layer over a surface of a dielectric encapsulation layer on an in-process unit, the in-process unit further including wire bonds having end surfaces and bases remote from the ends and positioned within the encapsulation layer, each wire bond defining an edge surface extending away between the base and the end surface, wherein the encapsulation covers portions of the wire bonds, such that unencapsulated portions of the wire bonds are defined by the end surface and a portion of the edge surface

thereof that is uncovered by the encapsulation layer, and wherein the sacrificial material layer covers the portions of the wire bonds that are uncovered by the encapsulation layer;

planarizing a portion of the sacrificial material layer and portions of the wire bonds such that the portions of the wire bonds uncovered by the encapsulation layer reach a predetermined, substantially uniform height; and

removing any remaining portion of the sacrificial material layer.

42. A method of making a microelectronic package comprising:

forming a plurality of wire bonds on an in-process unit including a substrate having a first surface and a second surface remote therefrom, a microelectronic element mounted to the first surface of the substrate, a plurality of conductive elements exposed at the first surface, at least some of the conductive elements being electrically connected to the microelectronic element, the wire bonds having first bases joined to the conductive elements and second bases joined to a back surface of the microelectronic element, each wire bond defining an edge surface extending between the first base and the second base;

forming a dielectric encapsulation layer on the in-process unit, wherein the encapsulation layer is formed so as to at cover the first surface and the wire bonds;

simultaneously removing a portion of the encapsulation layer and portions of the wire bonds such the wire bonds are segmented into connection vias including the first bases and thermal vias including the second bases, both the connection vias and the thermal vias having end surfaces remote from the bases, the removing step being further such that unencapsulated portions of the wire bonds are defined by at

least a portion of the end surfaces thereof that are uncovered by the encapsulation layer.

43. A method of making a microelectronic package comprising:

forming a plurality of wire bonds on an in-process unit including a substrate having a first surface and a second surface remote therefrom, a microelectronic element mounted to the first surface of the substrate, a plurality of conductive elements exposed at the first surface, at least some of the conductive elements being electrically connected to the microelectronic element, the wire bonds having bases joined to the conductive elements and end surfaces remote from the bases, each wire bond defining an edge surface extending between the base and the end surface, wherein at least two wire bonds are formed on at least one of the conductive elements; and

forming a dielectric encapsulation layer on the in-process unit, wherein the encapsulation layer is formed so as to at least partially cover the first surface and portions of the wire bonds, such that unencapsulated portions of the wire bonds are defined by a portion of at least one of the end surface or of the edge surface thereof that is uncovered by the encapsulation layer.

44. A method of making a microelectronic package comprising:

forming a sacrificial structure over an in-process unit including a substrate having a first surface and a second surface remote therefrom, a microelectronic element mounted to the first surface of the substrate, a plurality of conductive elements exposed at the first surface, at least some of the conductive elements being electrically connected to the

microelectronic element, the sacrificial structure having an opening therein that exposes at least one of the conductive elements, the sacrificial structure defining a surface adjacent the opening and remote from the first surface of the substrate;

forming a plurality of wire bonds including feeding a metal wire segment having a predetermined length out of a capillary of a bonding tool, the wire bonds having bases joined to the conductive elements and end surfaces remote therefrom, each wire bond defining an edge surface extending between the base and the end surface, and severing the wire bonds at locations outside the openings and adjacent the surface of the sacrificial structure;

removing the sacrificial structure; and

forming a dielectric encapsulation layer on the in-process unit, wherein the encapsulation layer is formed so as to at least partially cover the first surface and portions of the wire bonds, such that unencapsulated portions of the wire bonds are defined by a portion of at least one of the end surface or of the edge surface thereof that is uncovered by the encapsulation layer.

FIG. 1

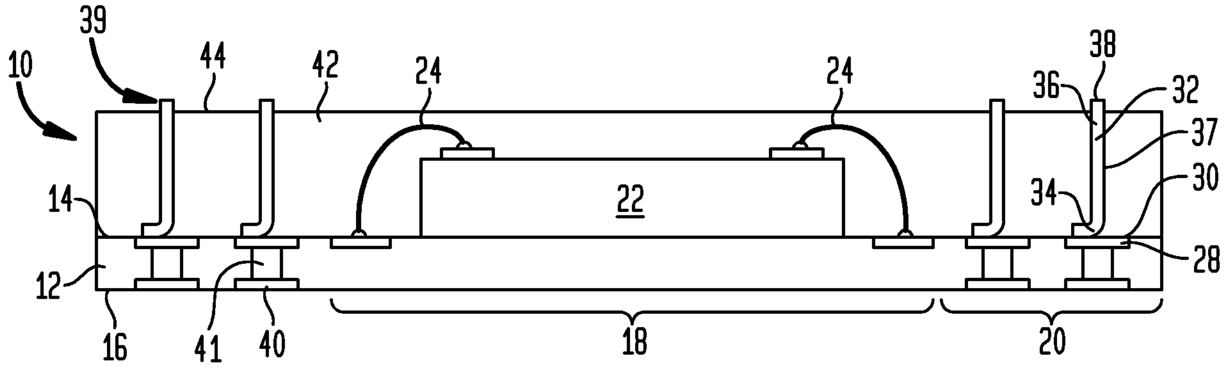


FIG. 2

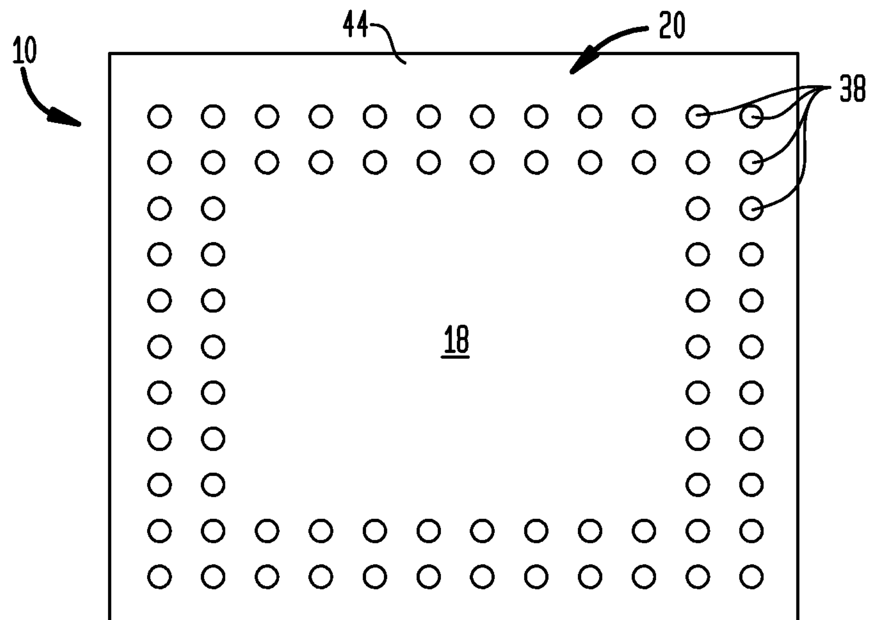


FIG. 3

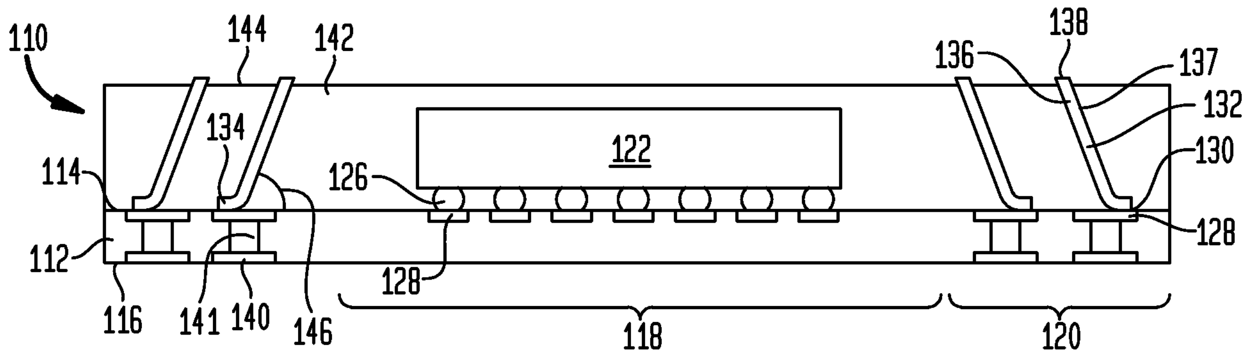


FIG. 4

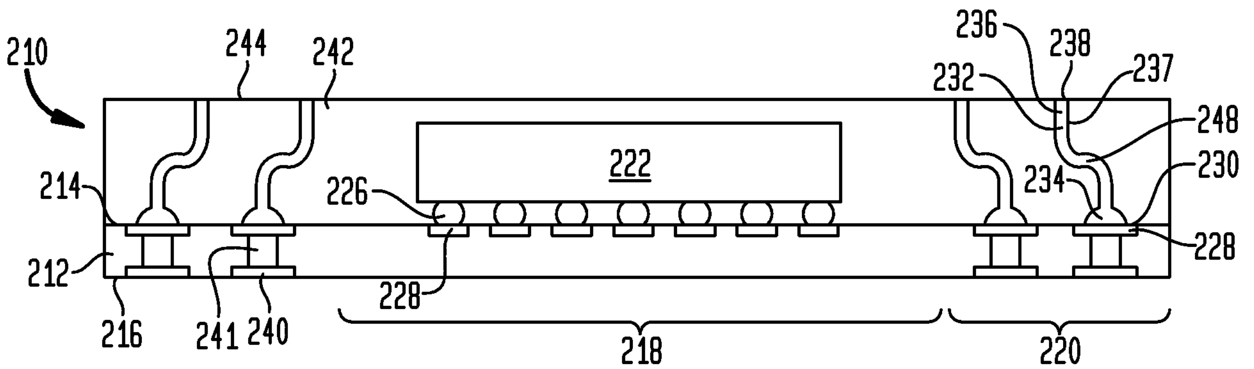


FIG. 5A

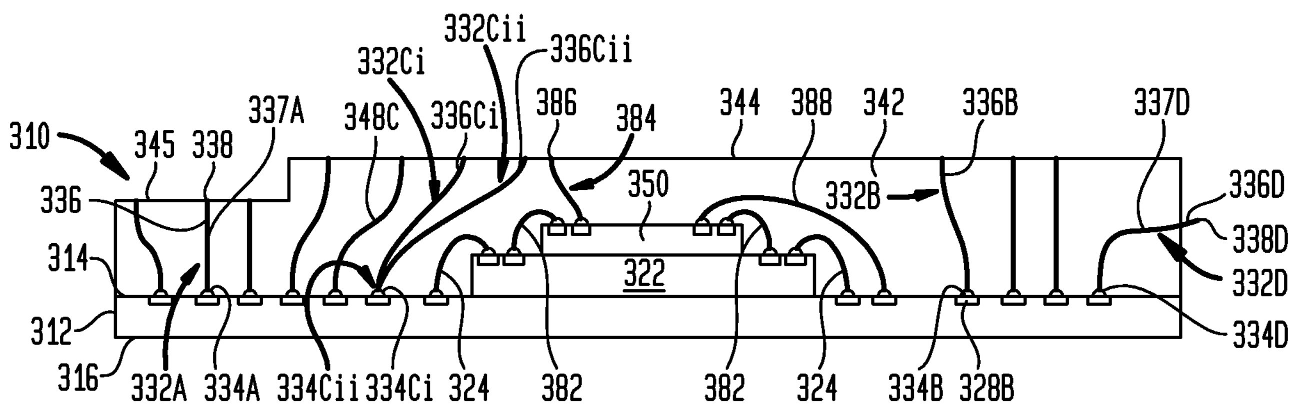


FIG. 5B

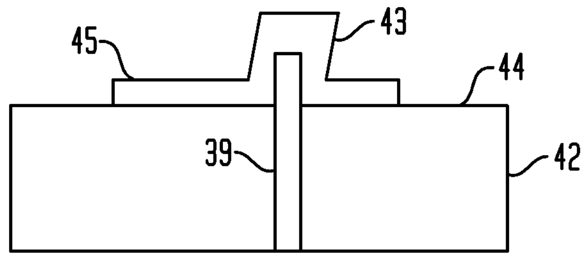


FIG. 5C

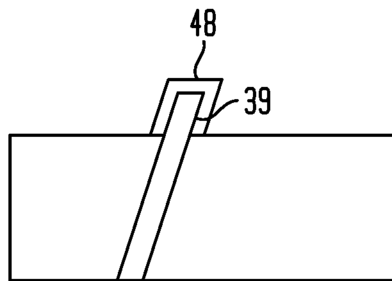


FIG. 5D

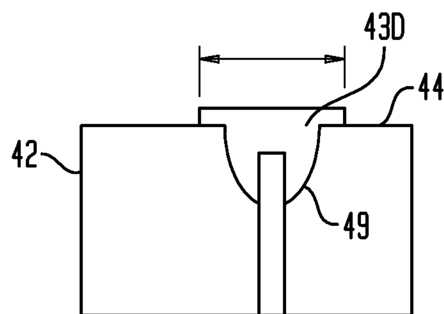


FIG. 6

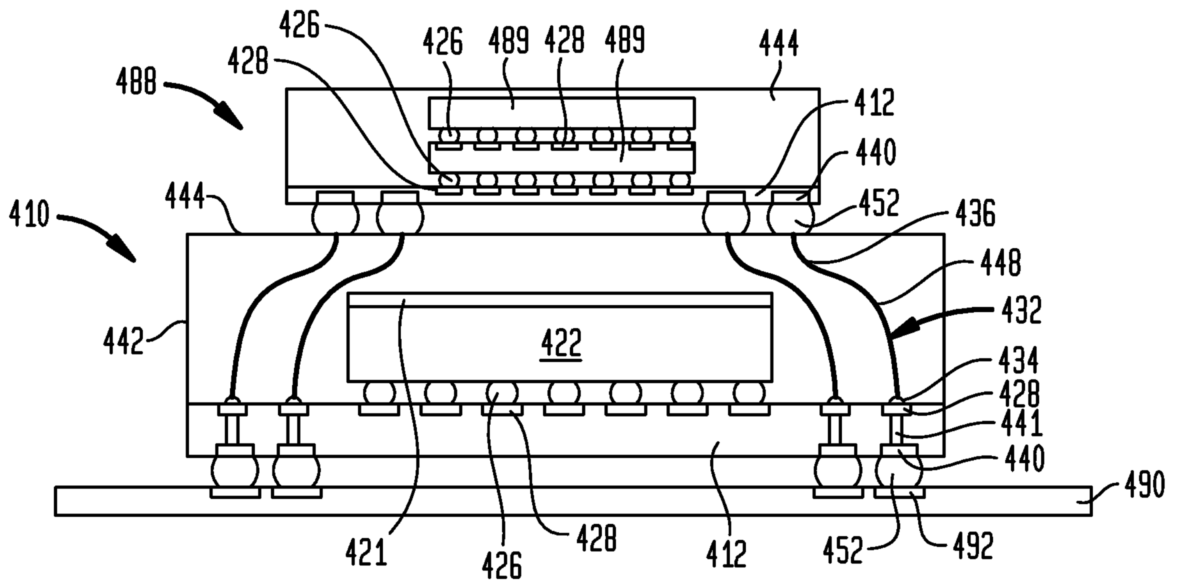


FIG. 7

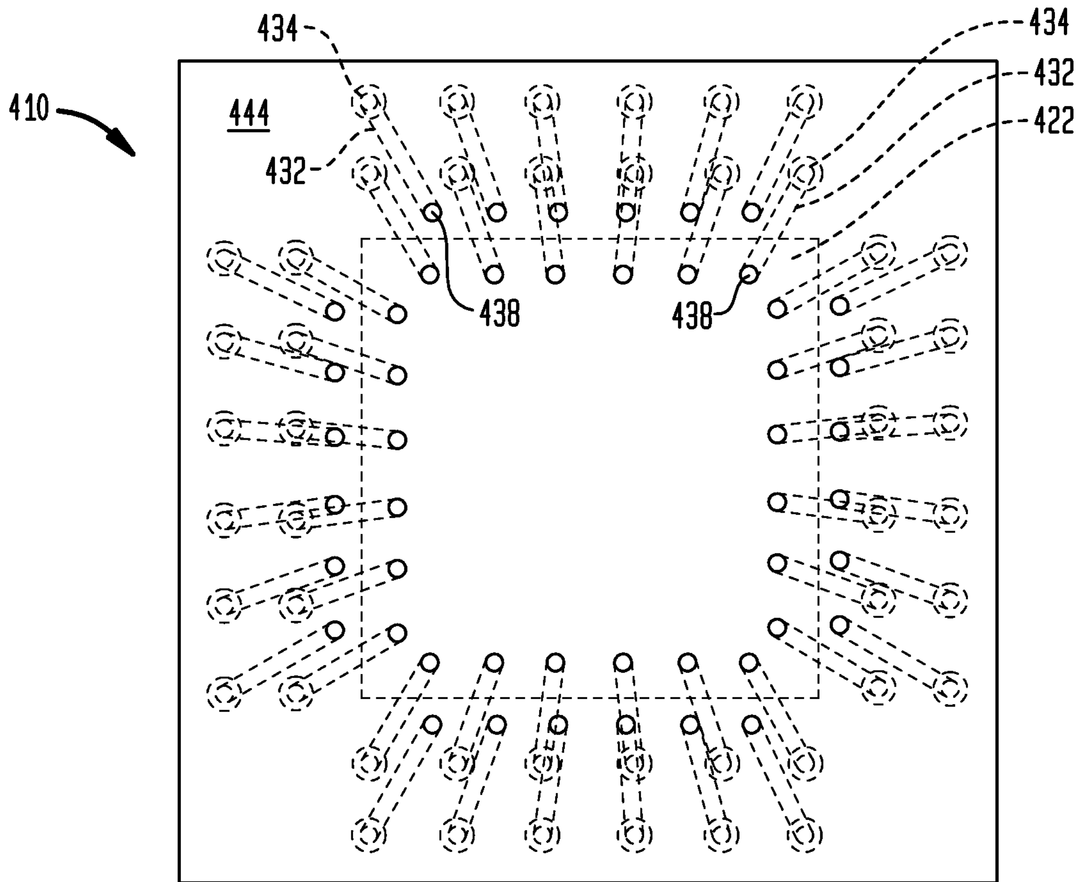


FIG. 8

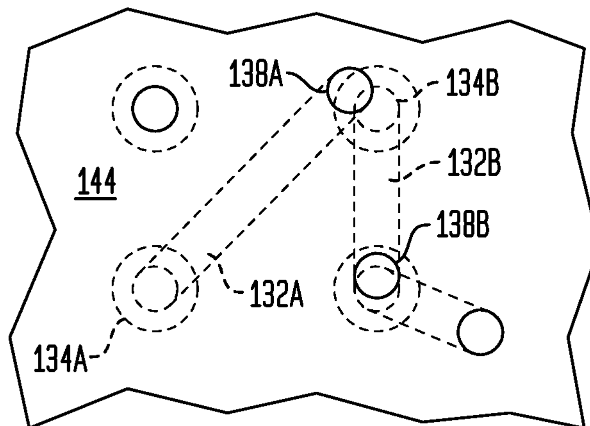


FIG. 9

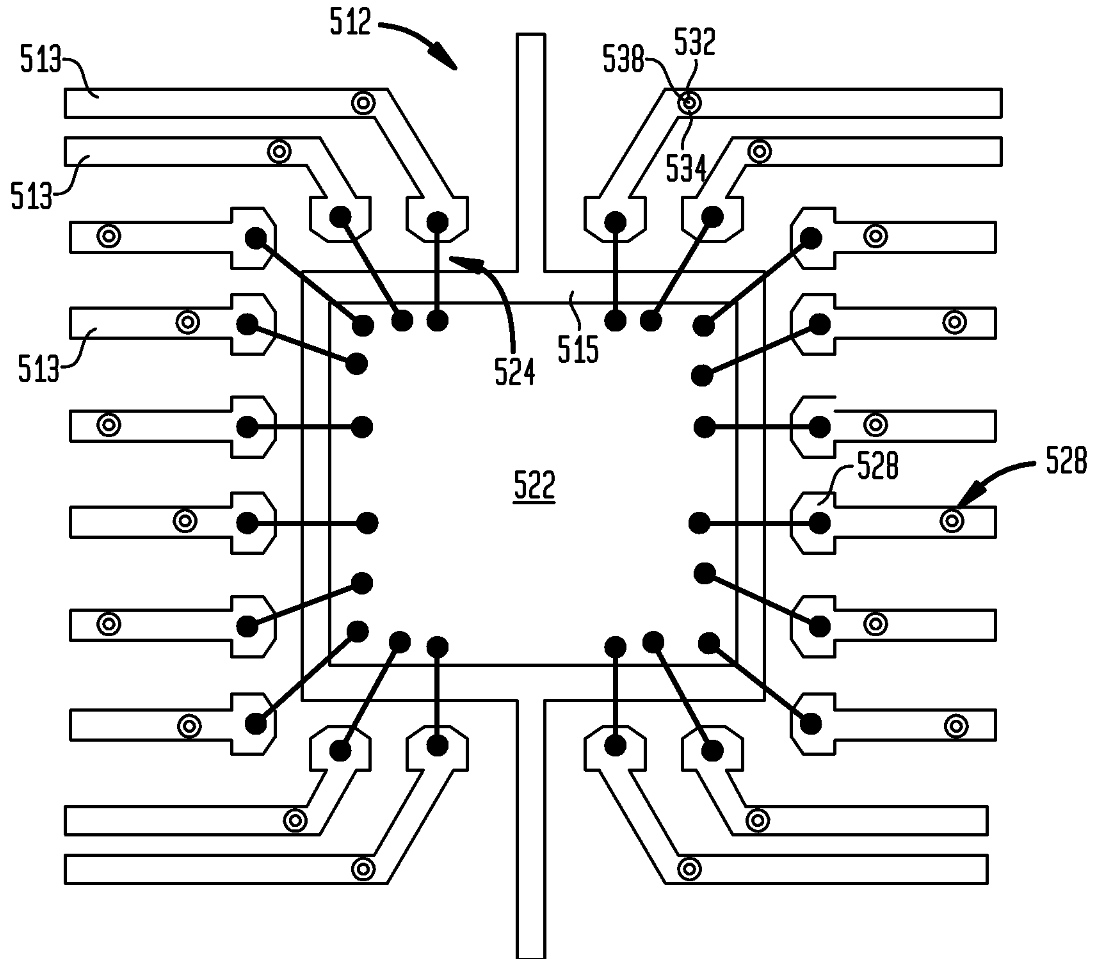


FIG. 10

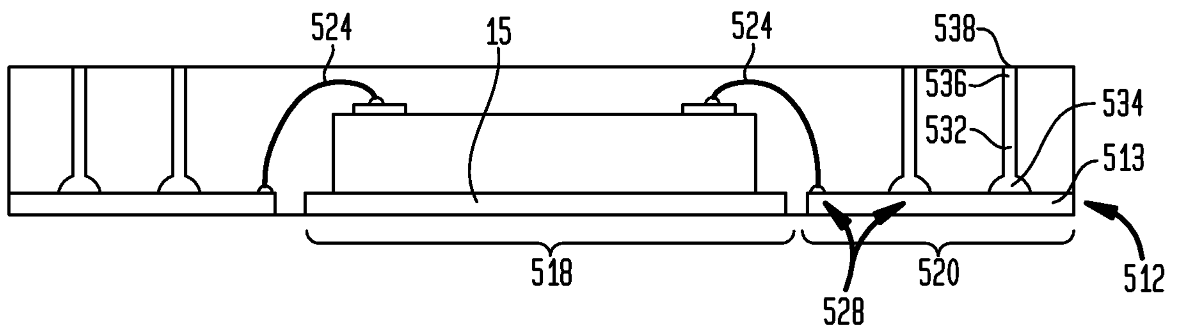
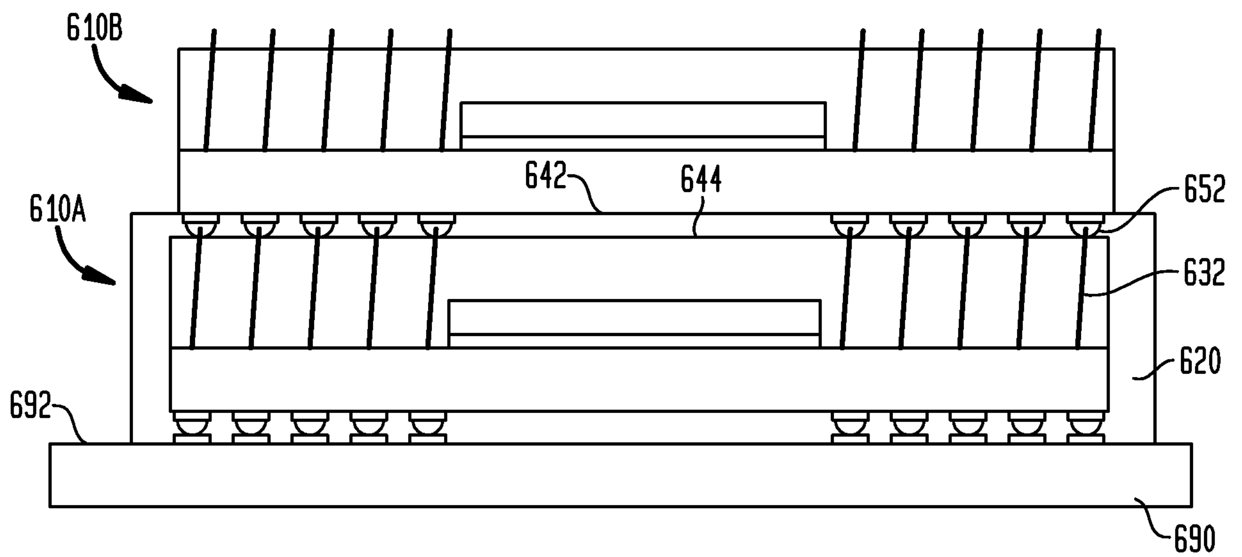


FIG. 11



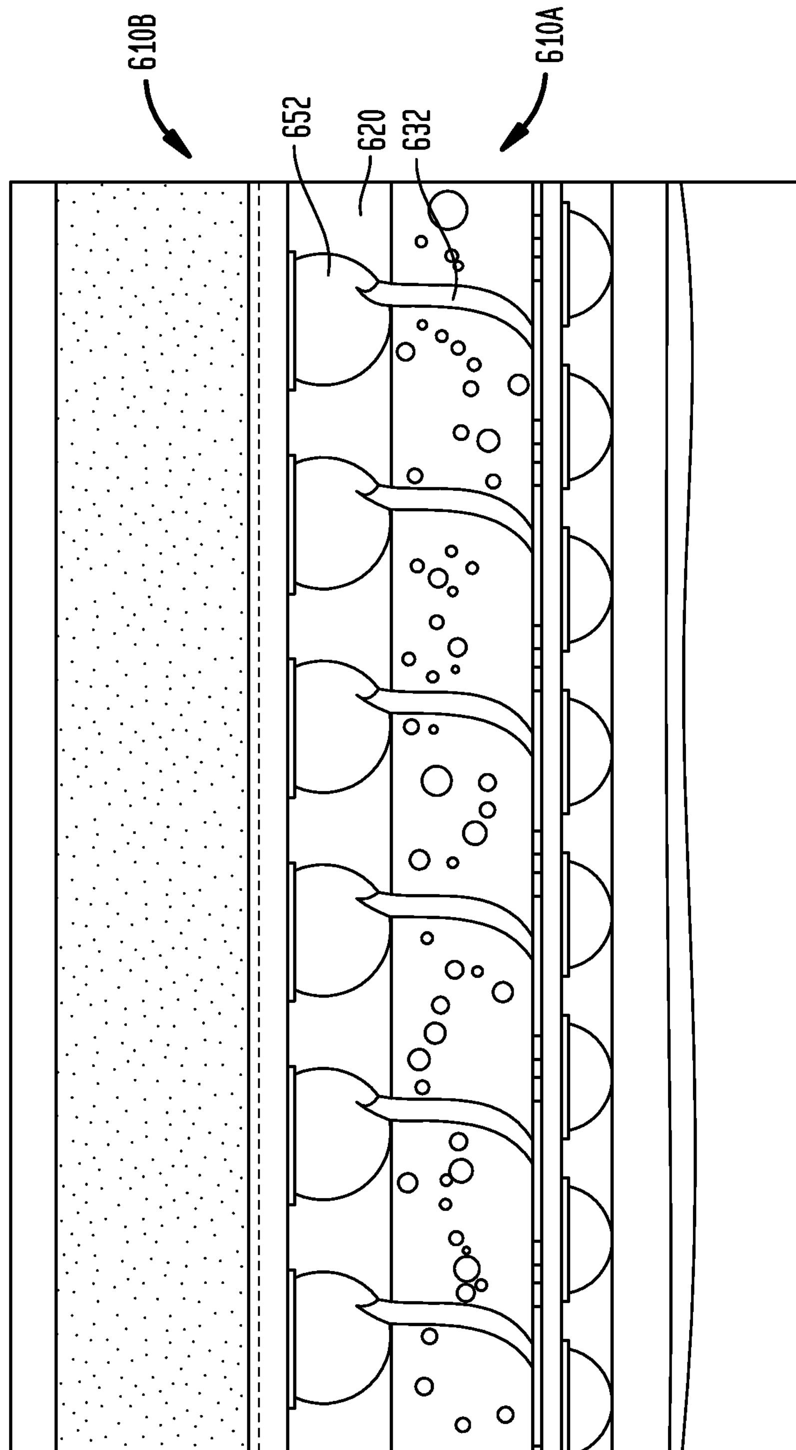


FIG. 12

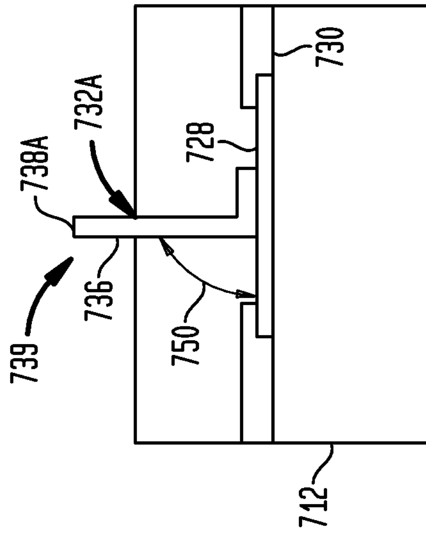


FIG. 13A

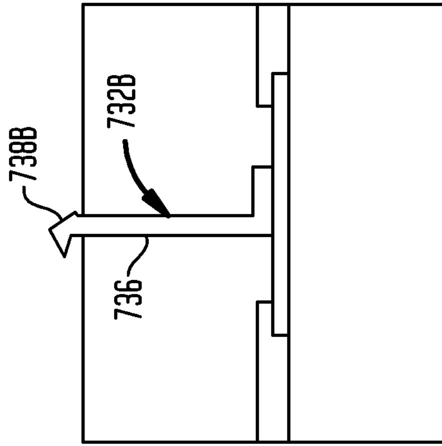


FIG. 13B

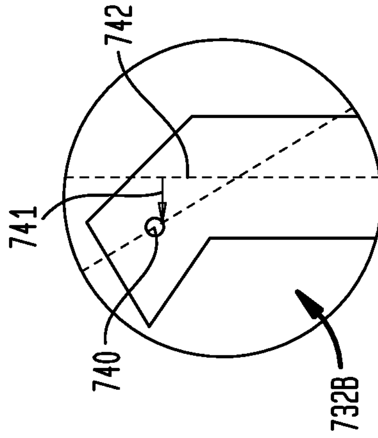


FIG. 13C

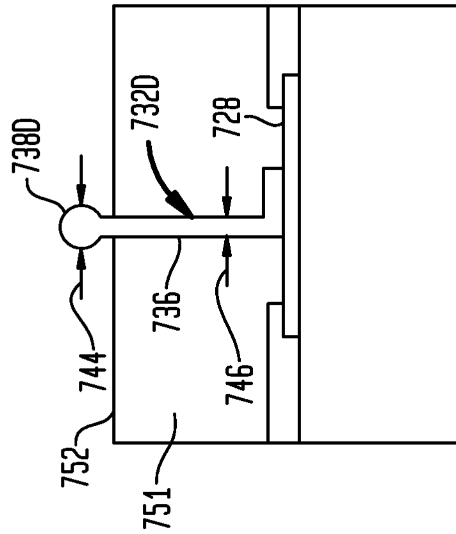


FIG. 13D

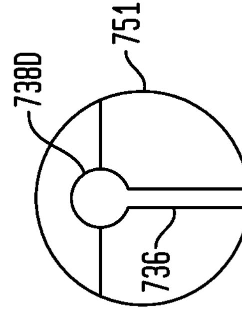


FIG. 13E

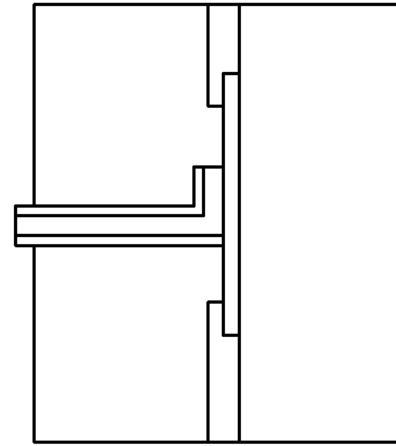


FIG. 13F

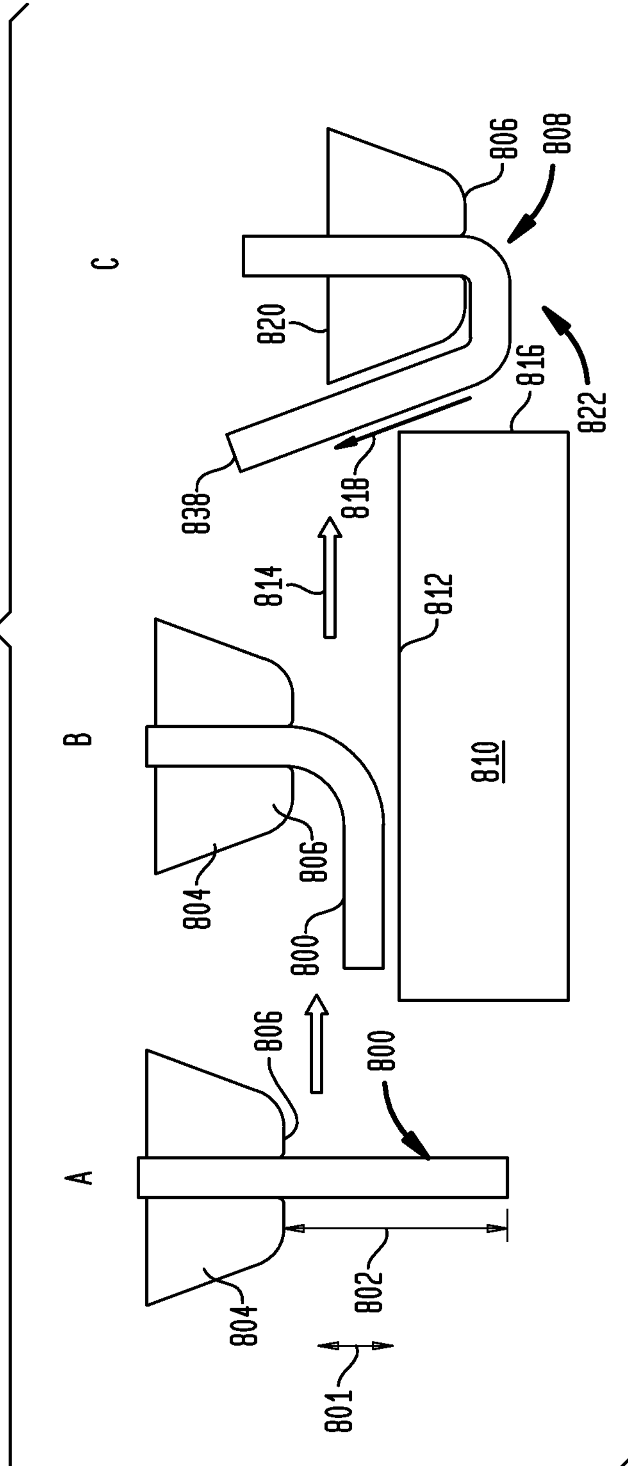


FIG. 14
A
B
C
800
801
802
804
806
808
810
812
814
816
818
820
822
838

FIG. 15

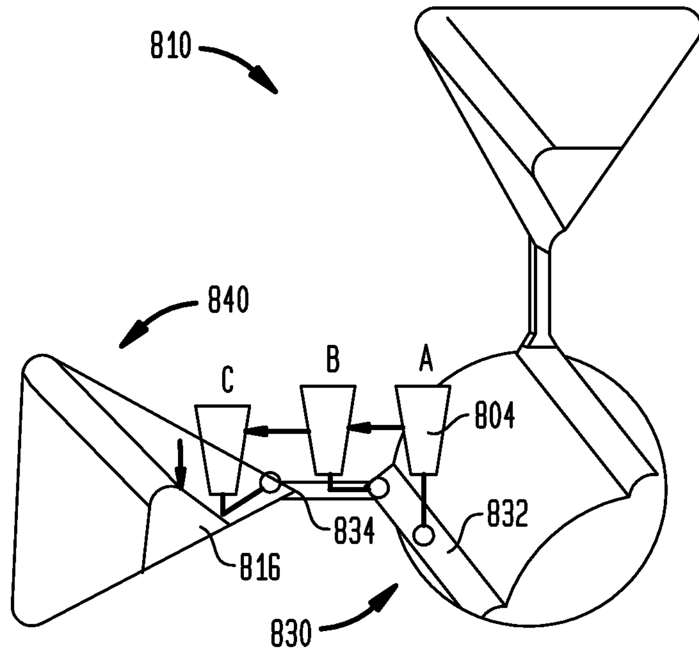
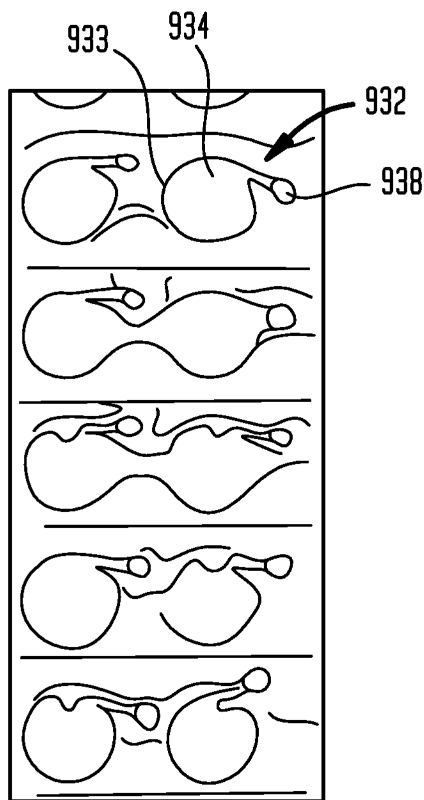


FIG. 16



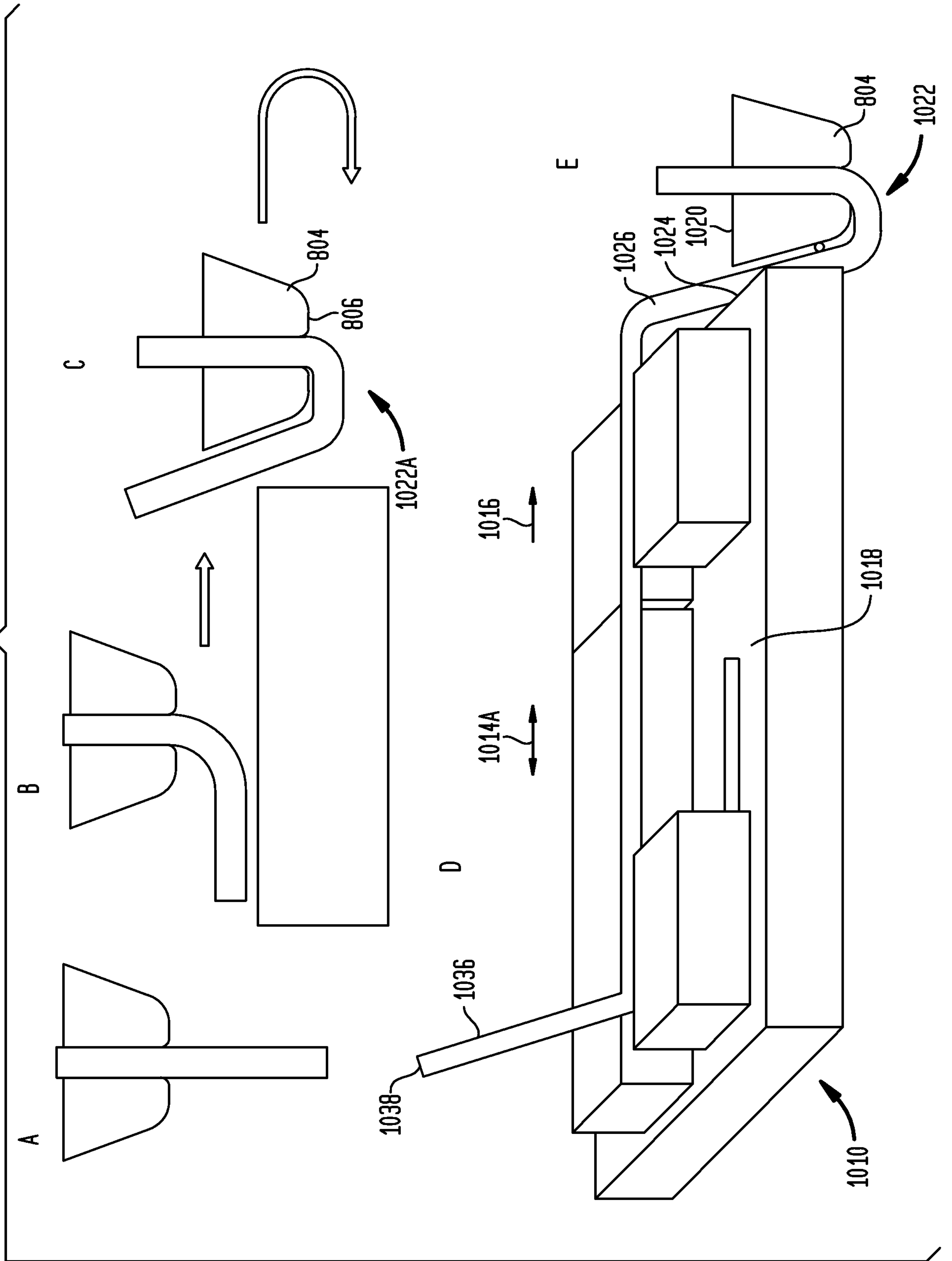


FIG. 17
A
B
C
D
E
804
806
1022A
1016
1014A
1036
1038
1010
1018
1020
1024
1026
1022

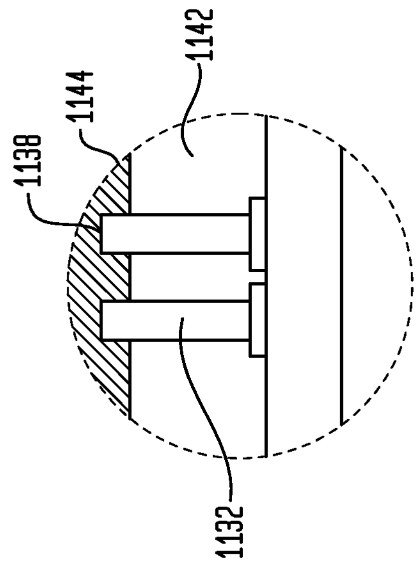


FIG. 20

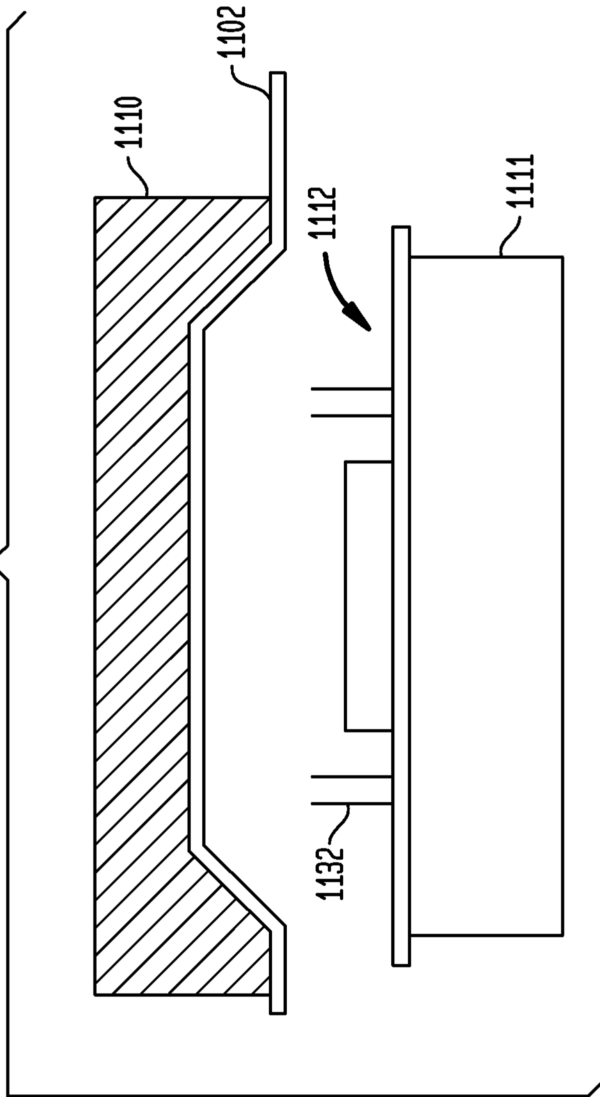


FIG. 18

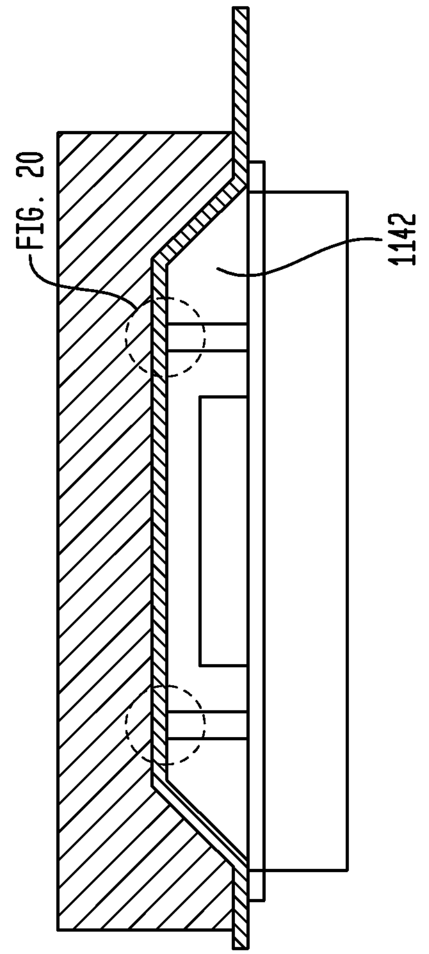


FIG. 19

FIG. 21

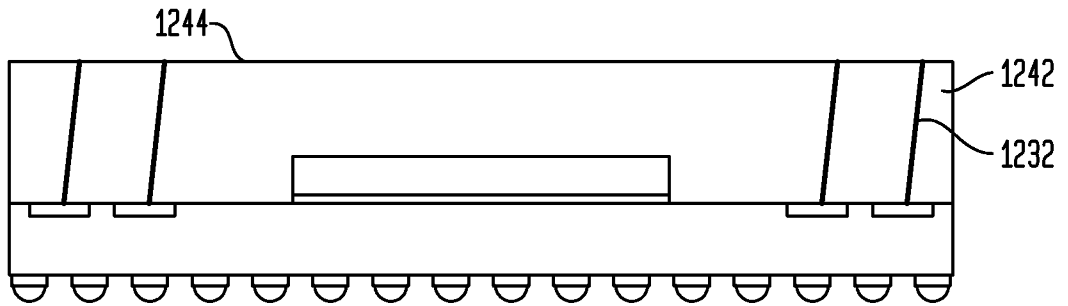


FIG. 22

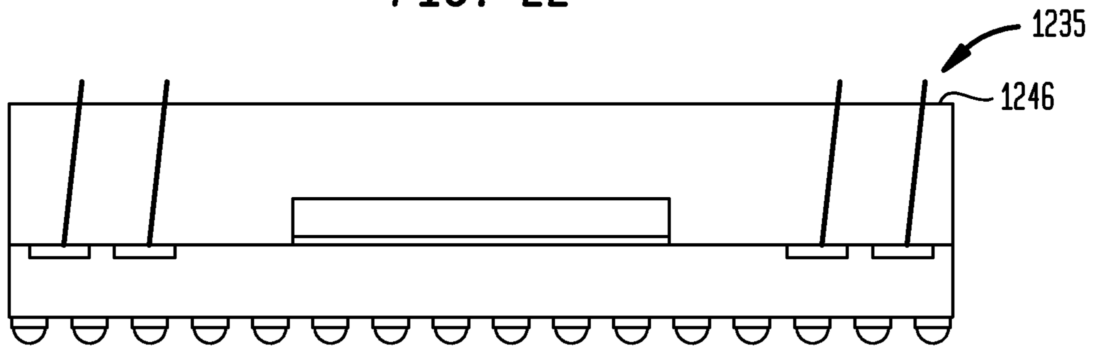


FIG. 23A

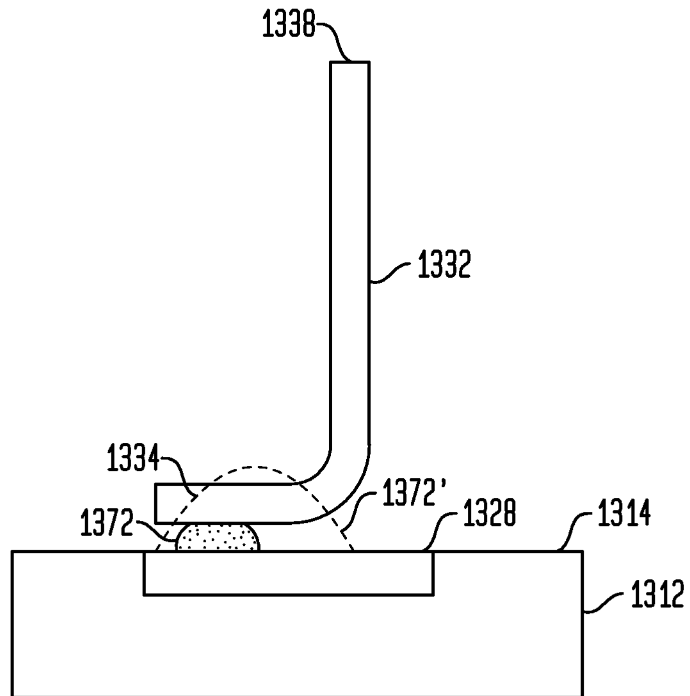


FIG. 23B

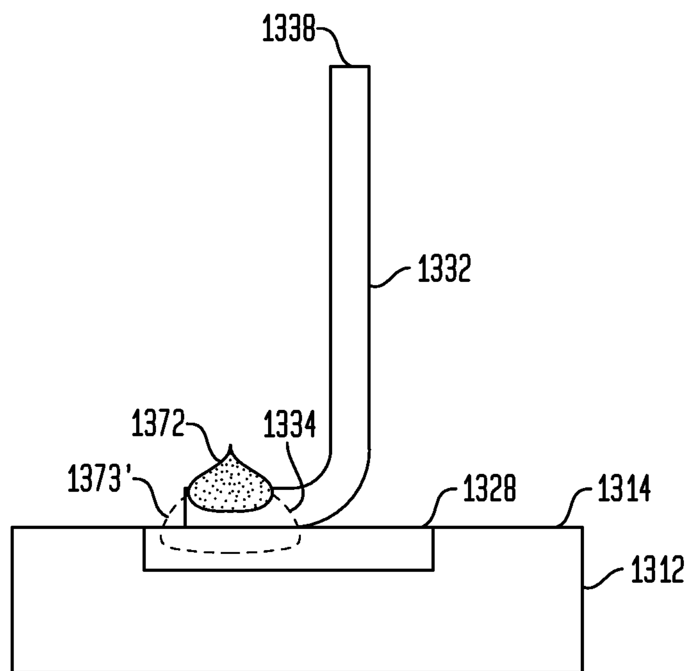


FIG. 24A

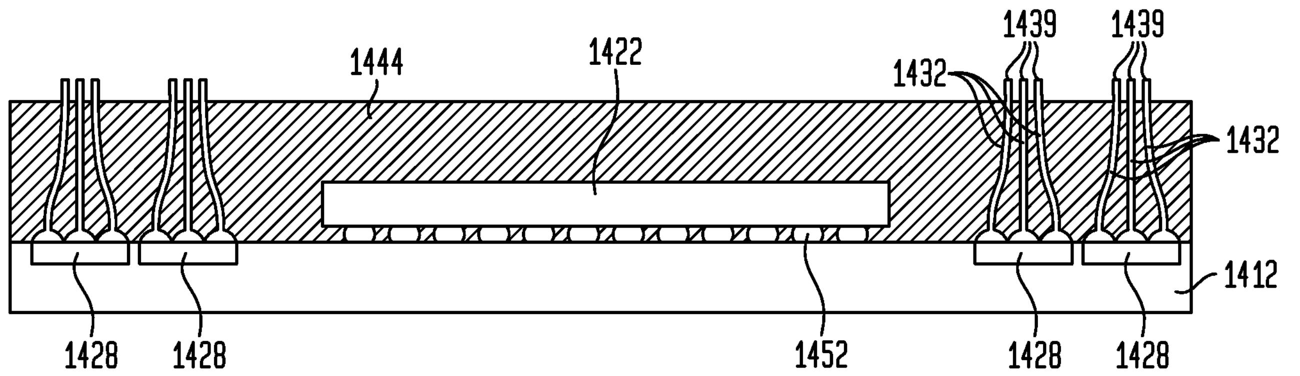


FIG. 24B

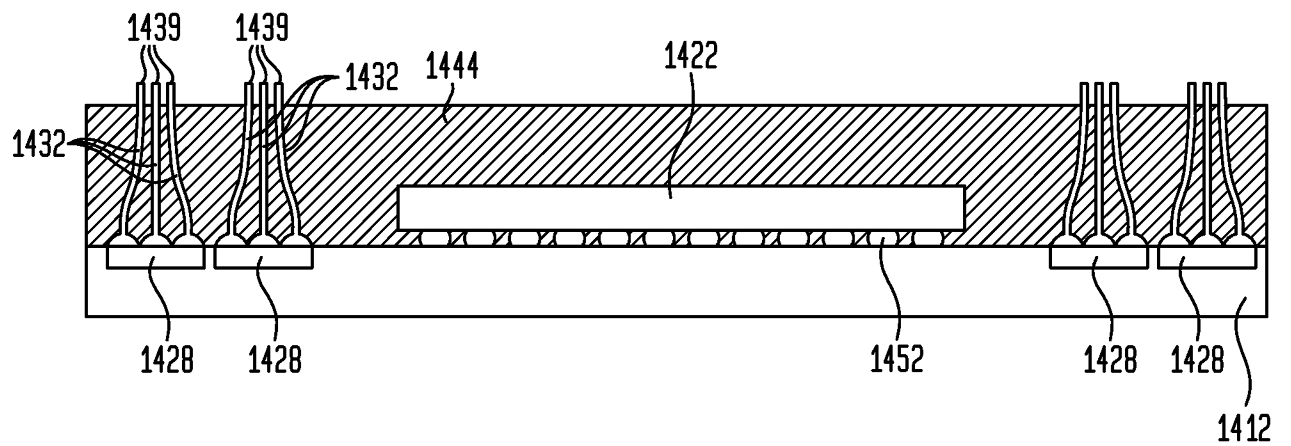


FIG. 25A

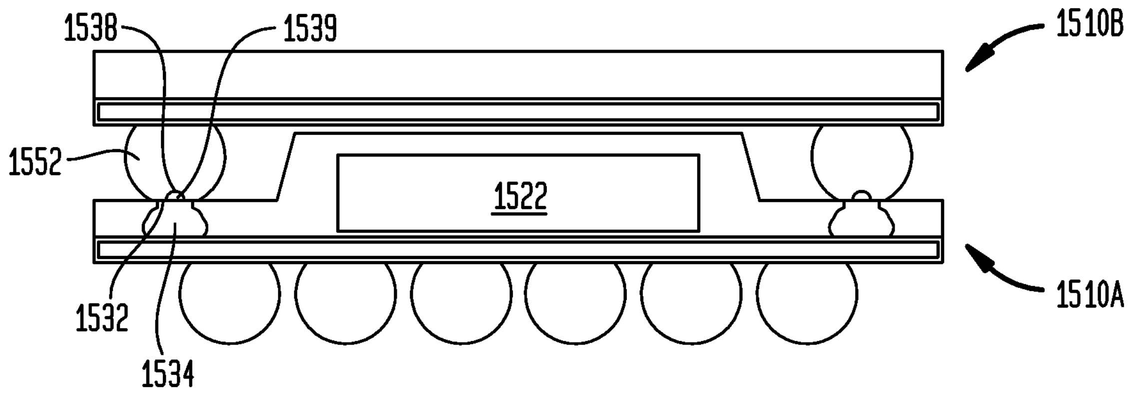


FIG. 25B

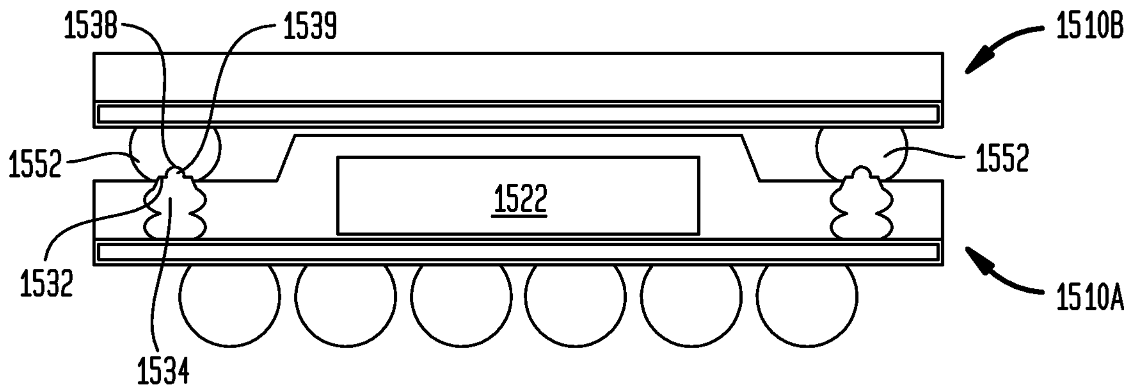


FIG. 26

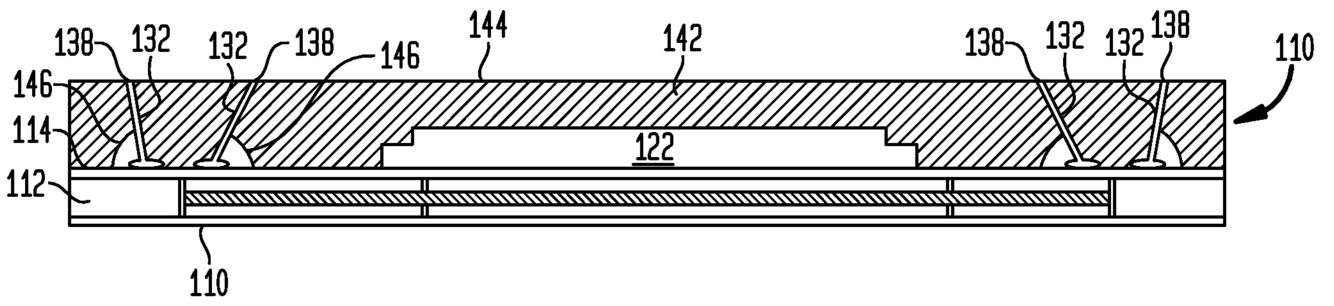


FIG. 27A

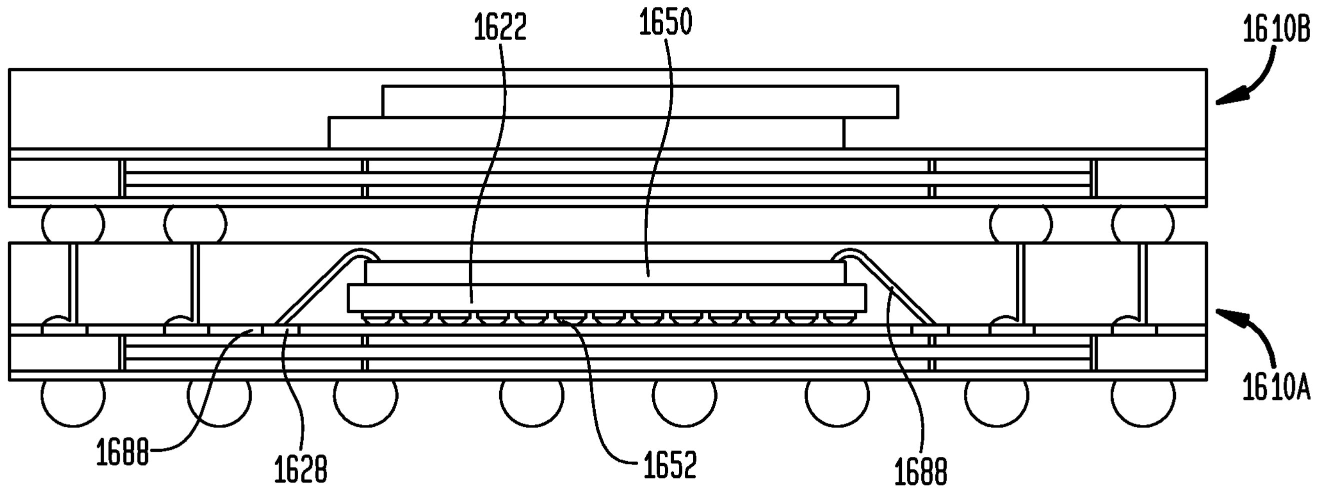


FIG. 27B

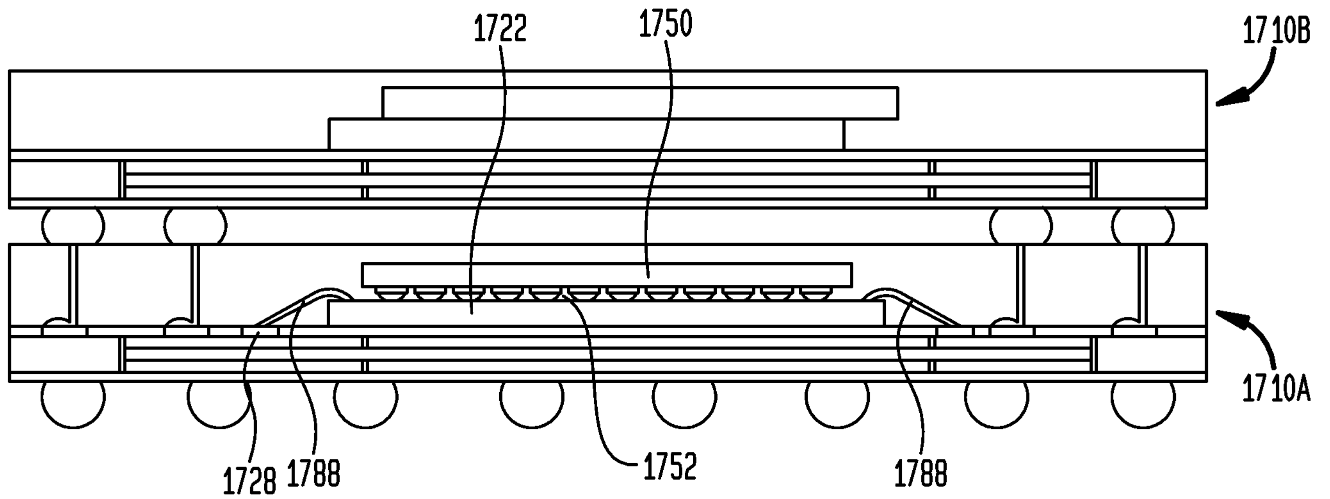


FIG. 27C

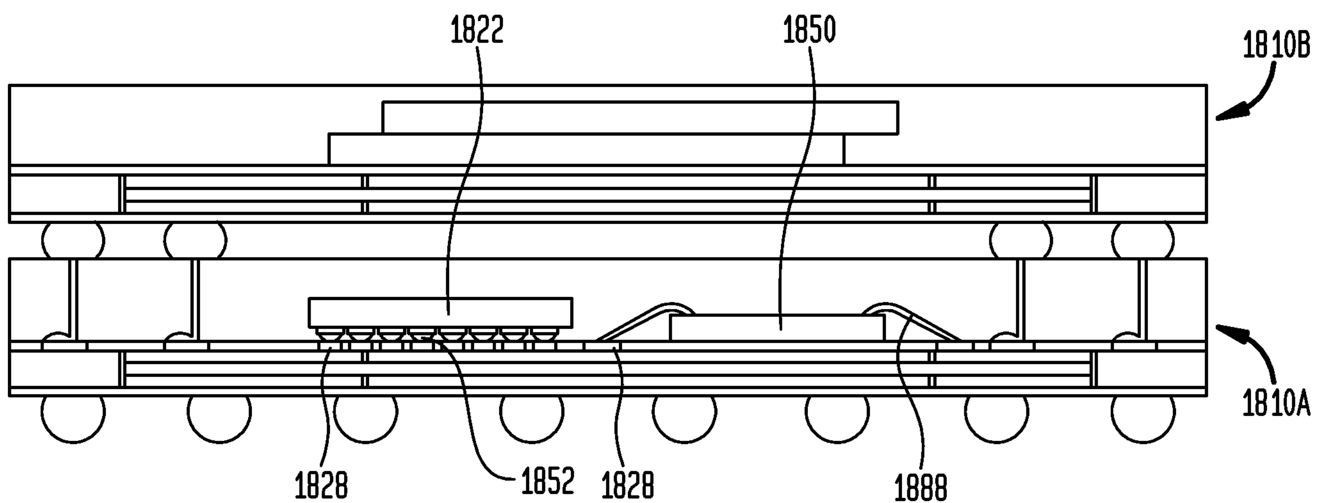


FIG. 28A

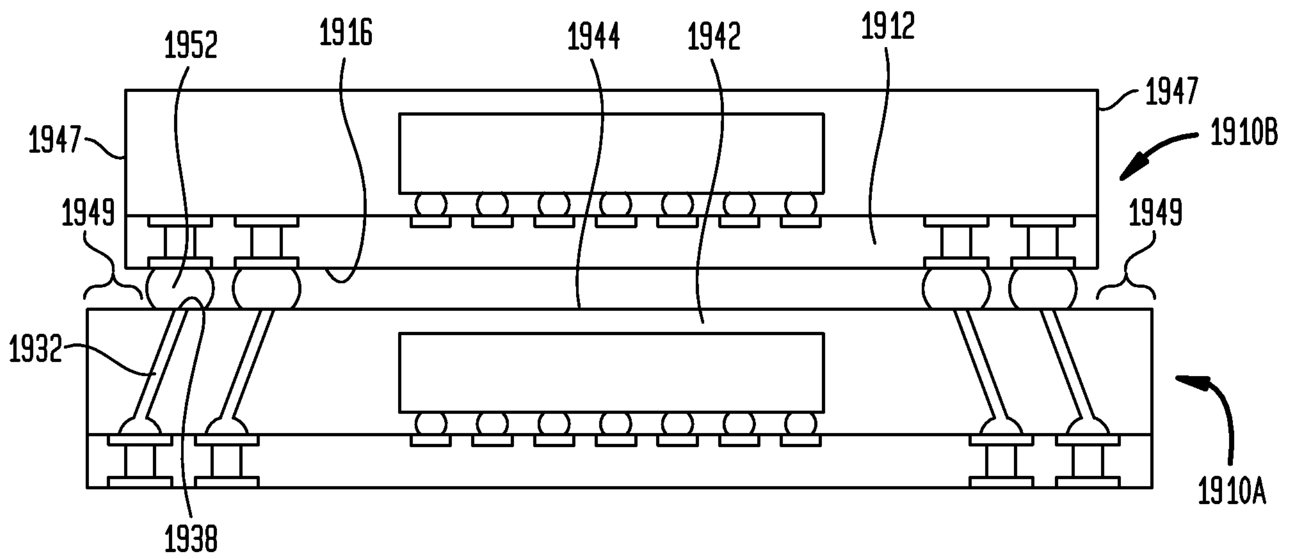


FIG. 28B

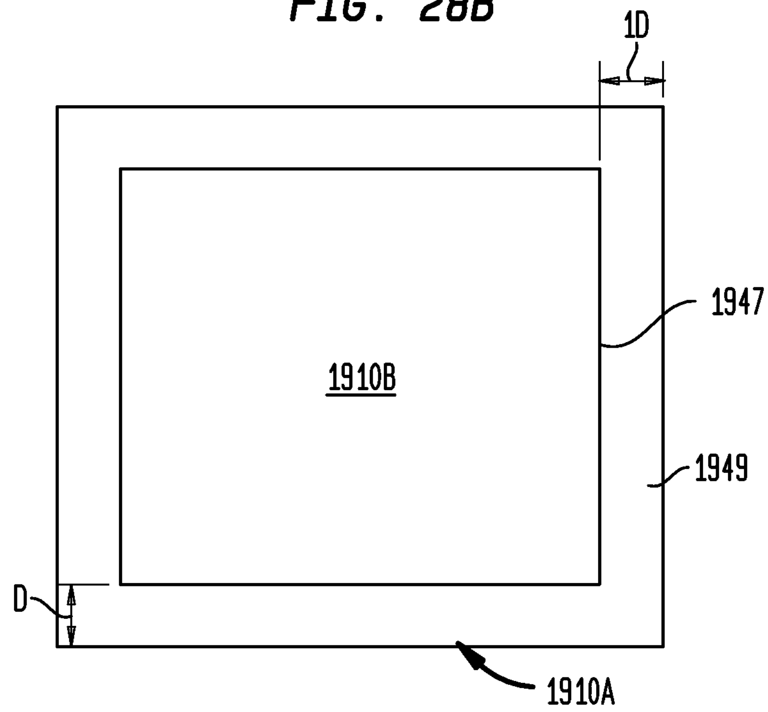


FIG. 28C

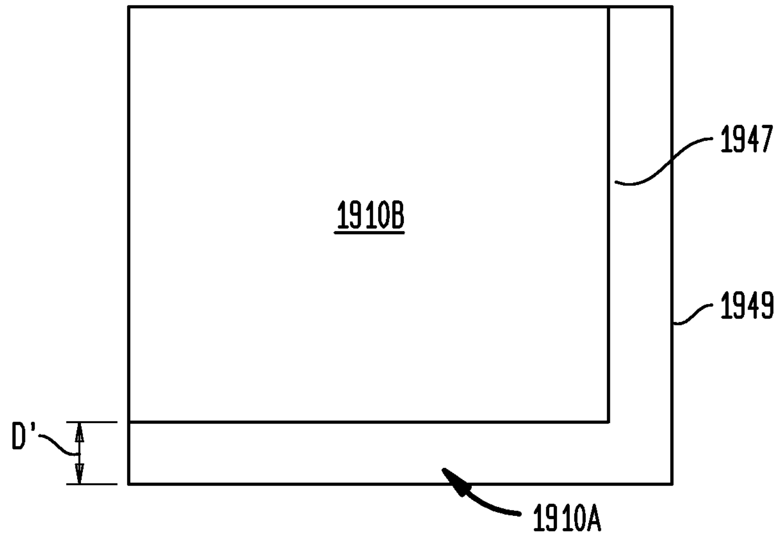
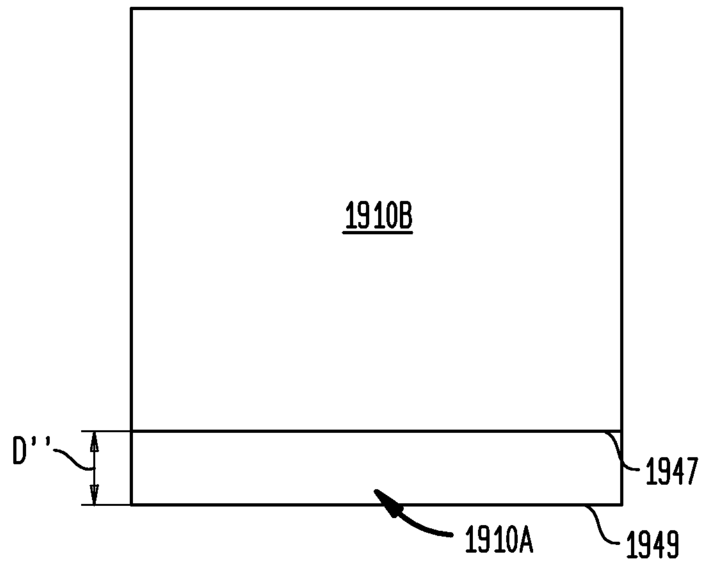


FIG. 28D



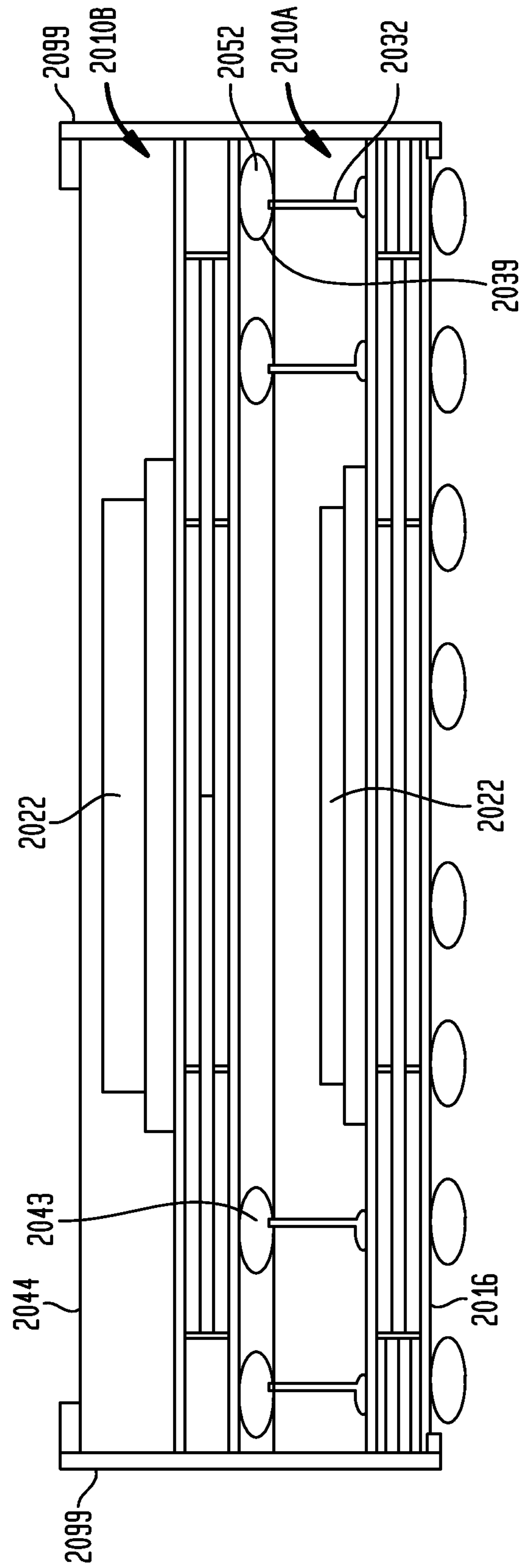


FIG. 29

FIG. 30A

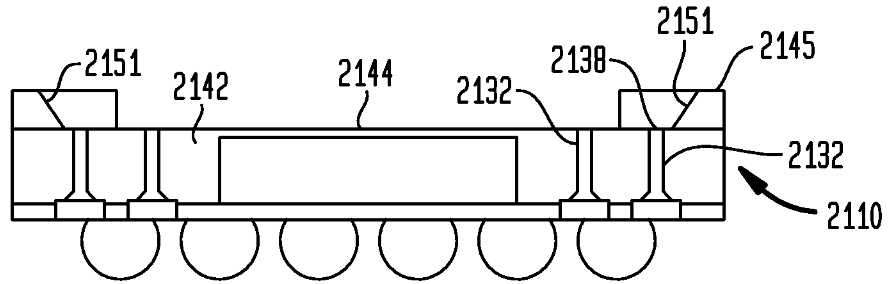


FIG. 30B

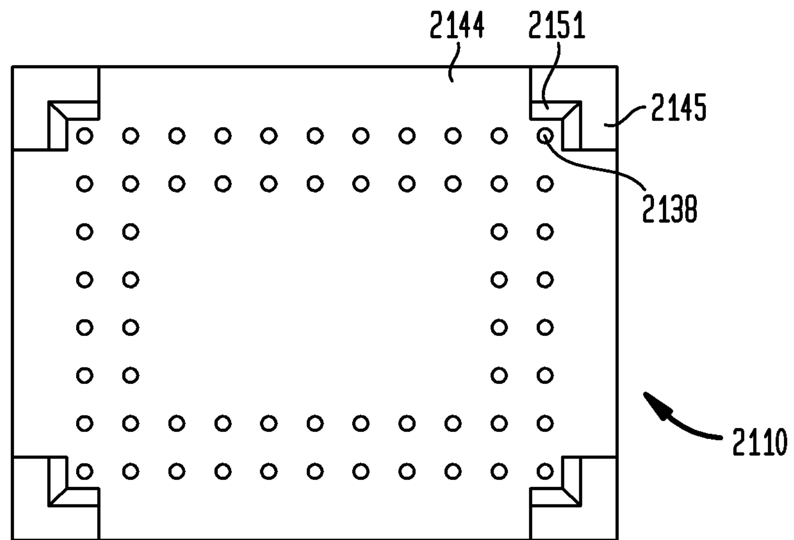


FIG. 30C

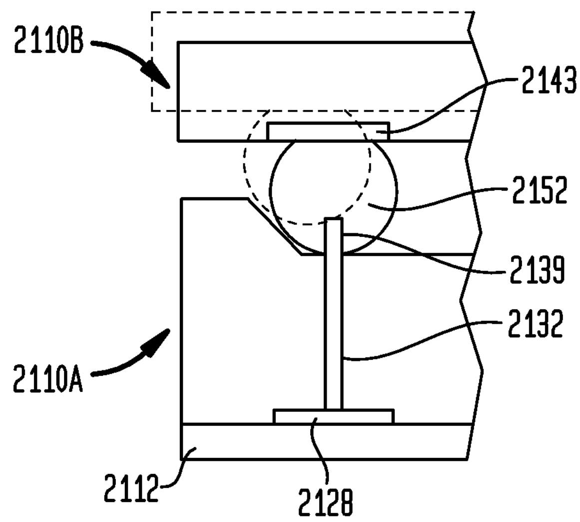


FIG. 31A

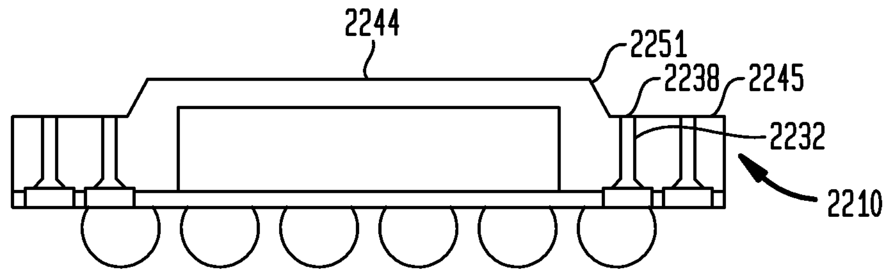


FIG. 31B

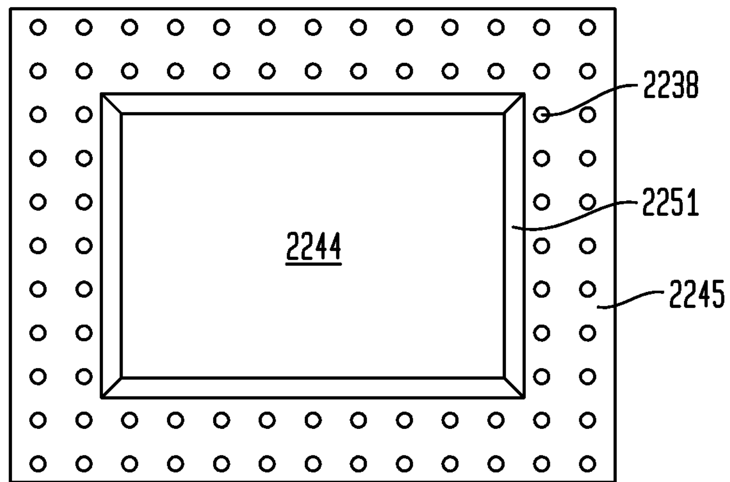


FIG. 31C

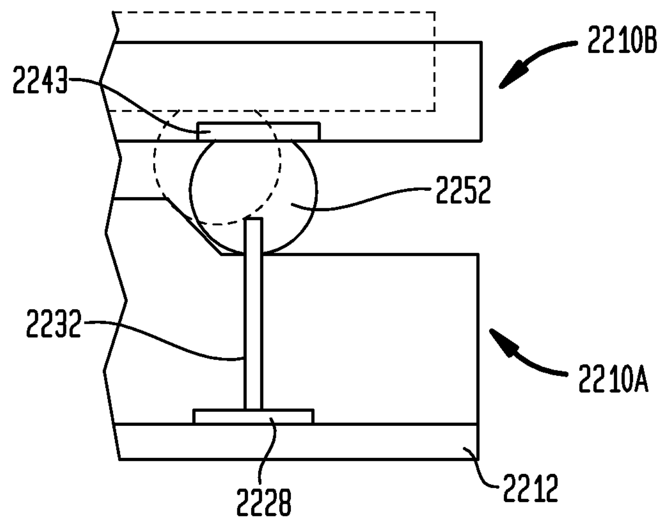


FIG. 32A

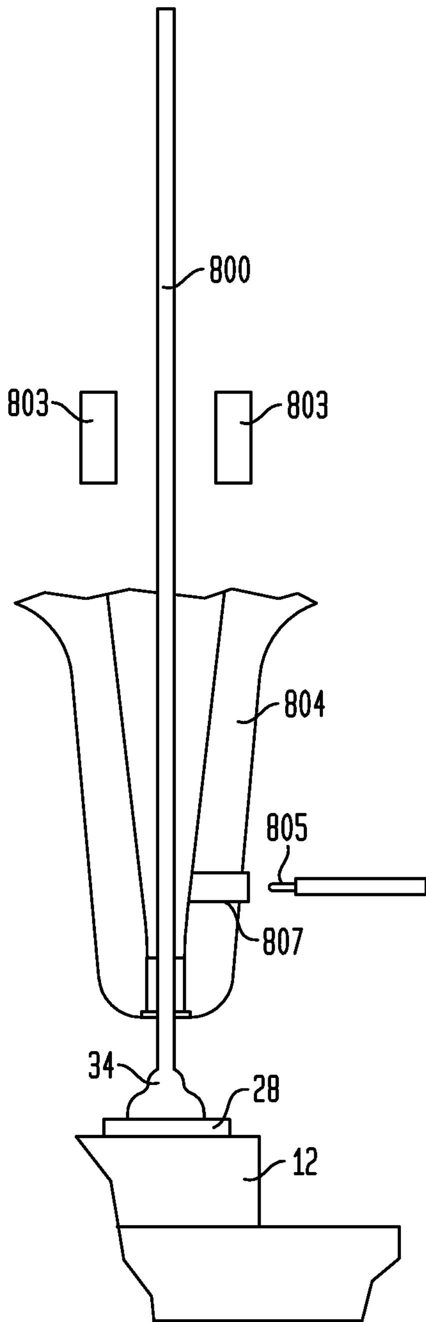


FIG. 32B

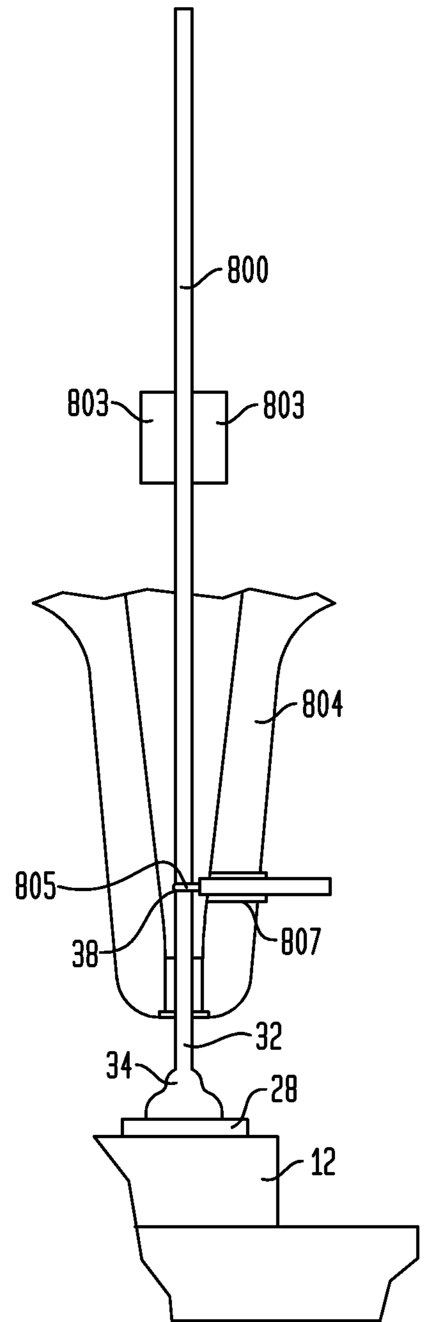


FIG. 33

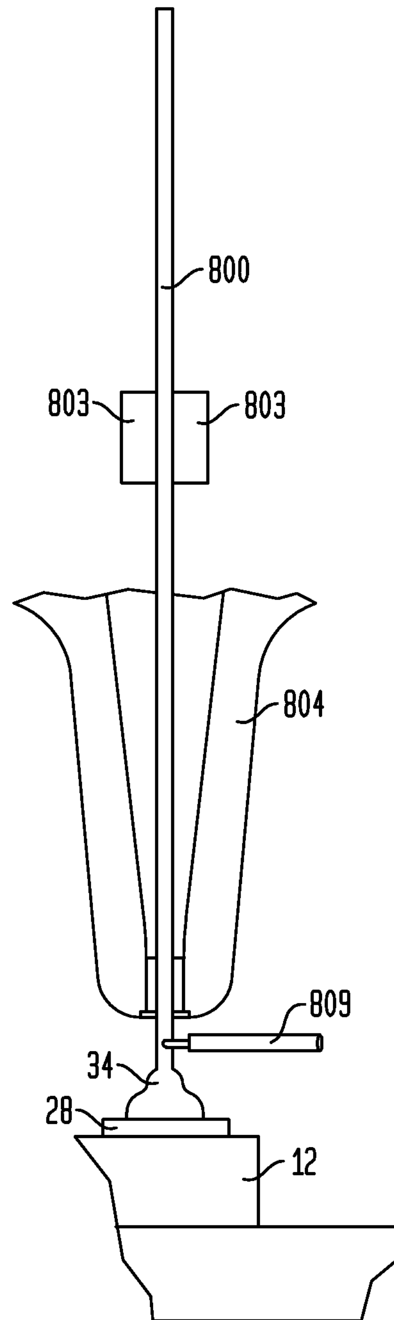


FIG. 34A

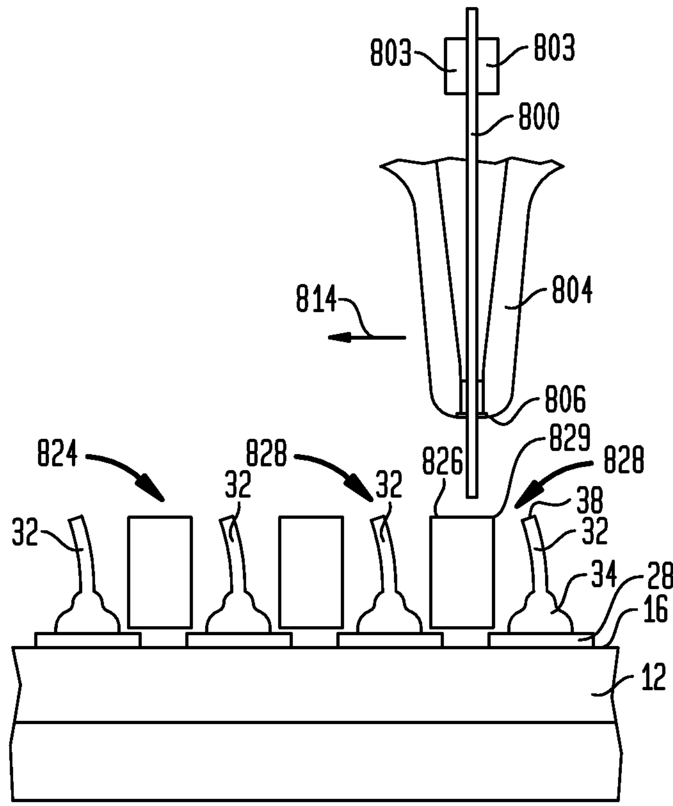


FIG. 34B

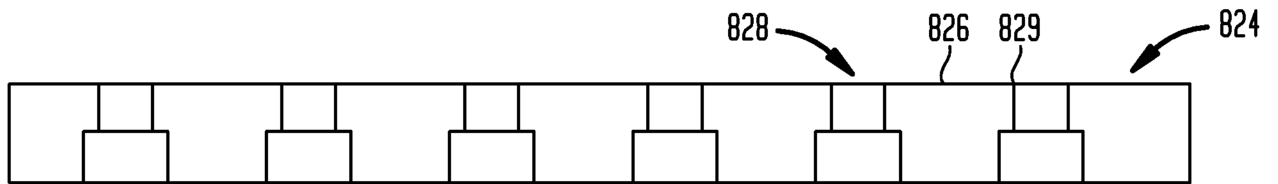


FIG. 34C

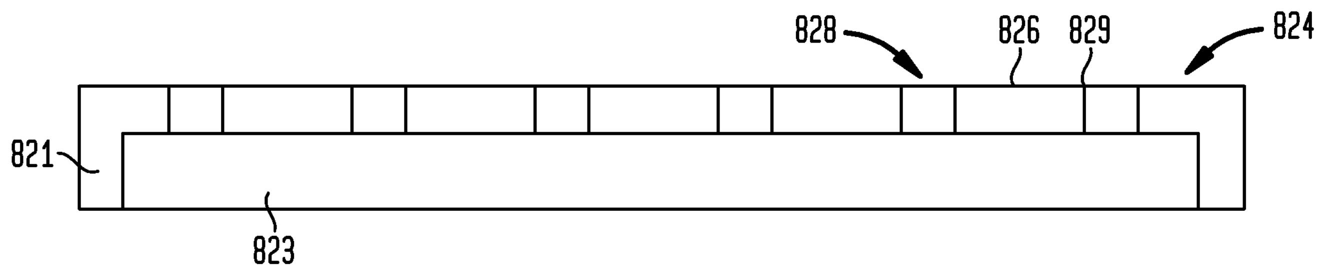
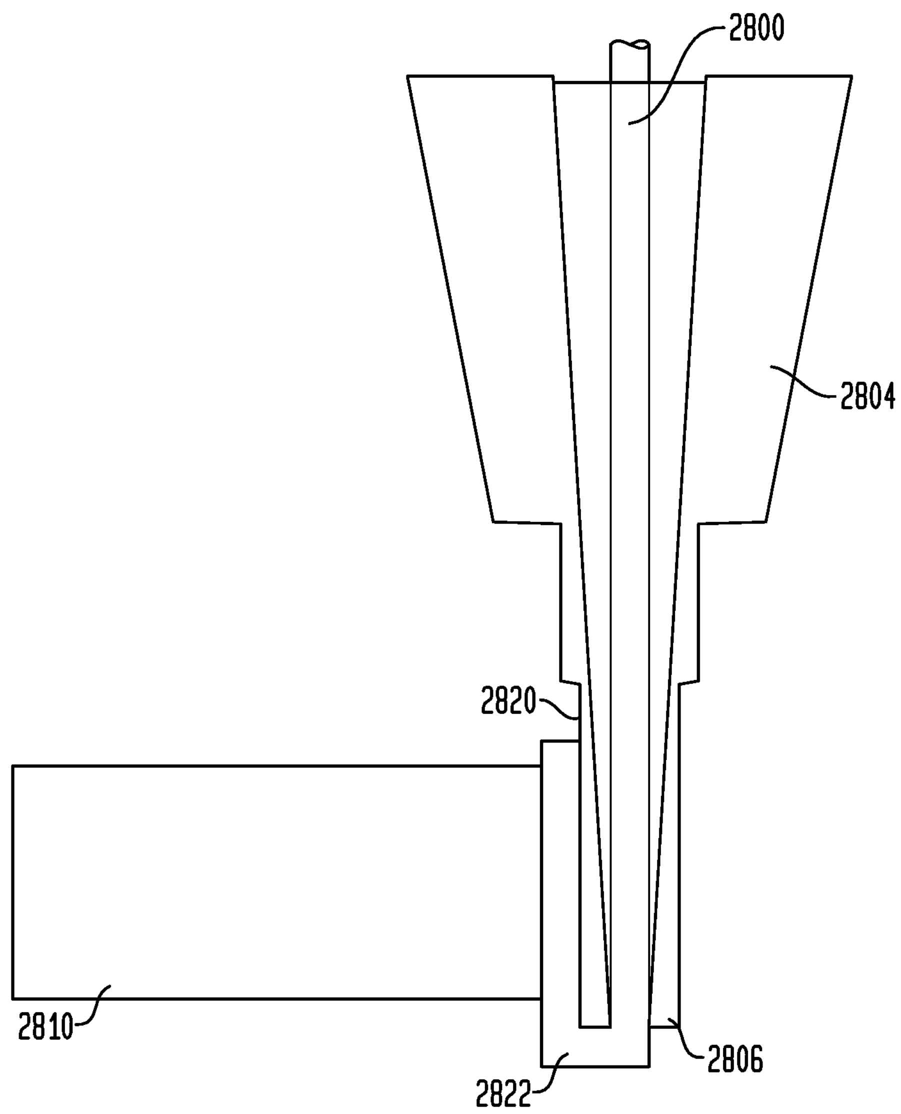


FIG. 35



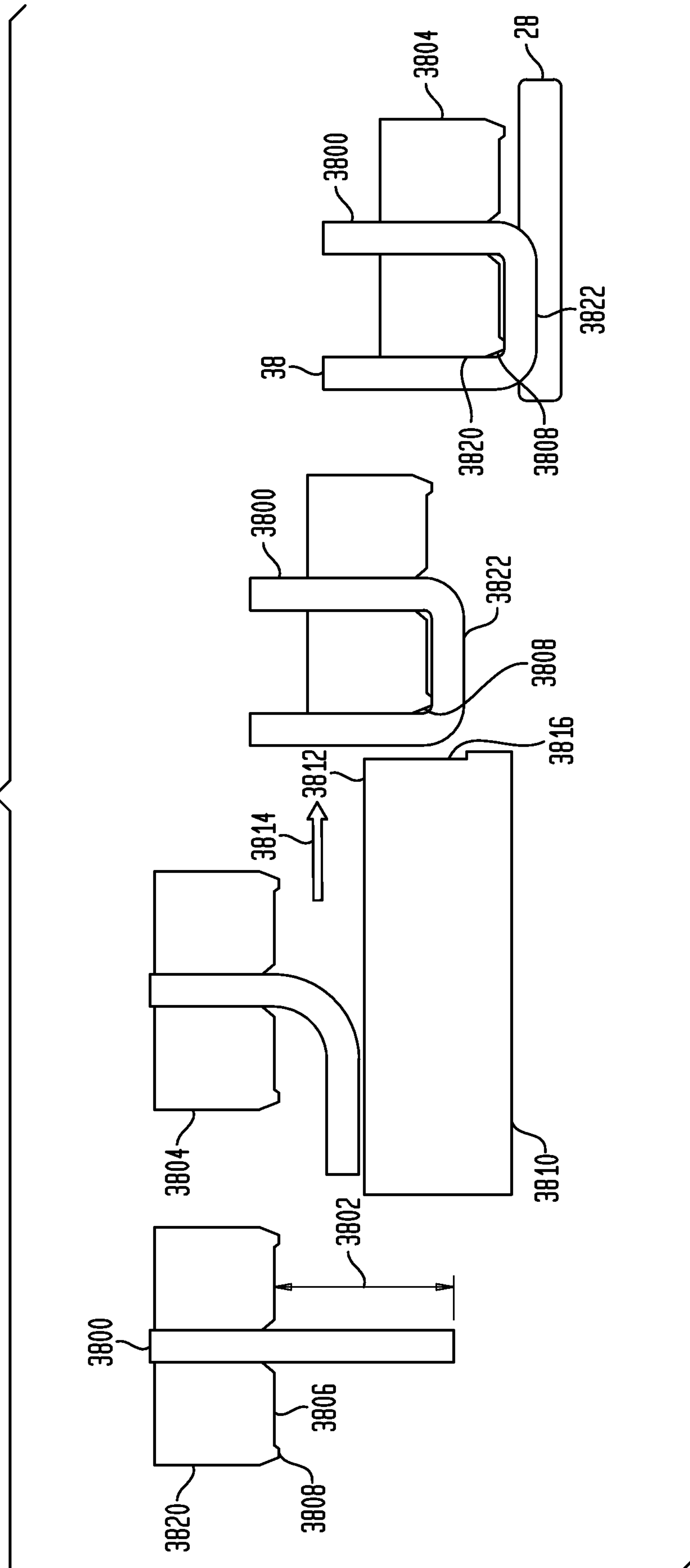


FIG. 36

FIG. 37A

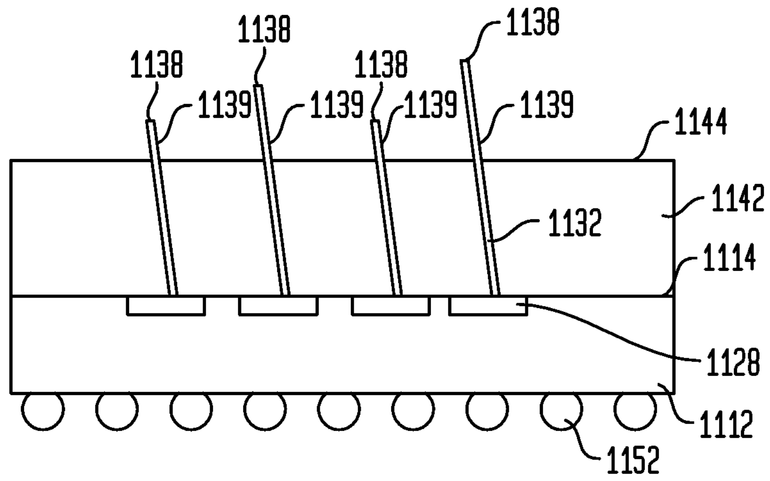


FIG. 37B

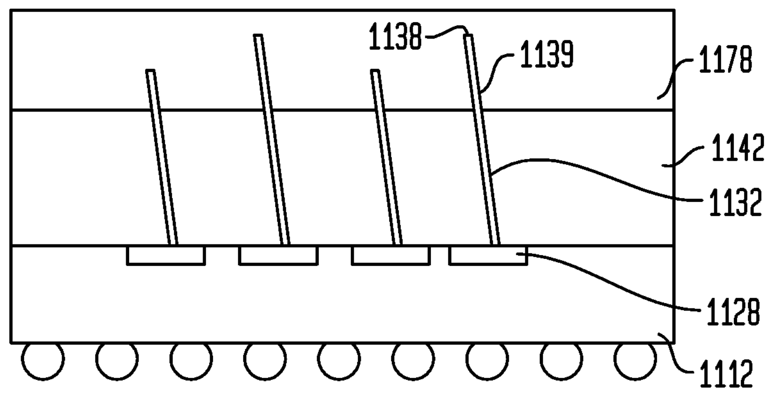


FIG. 37C

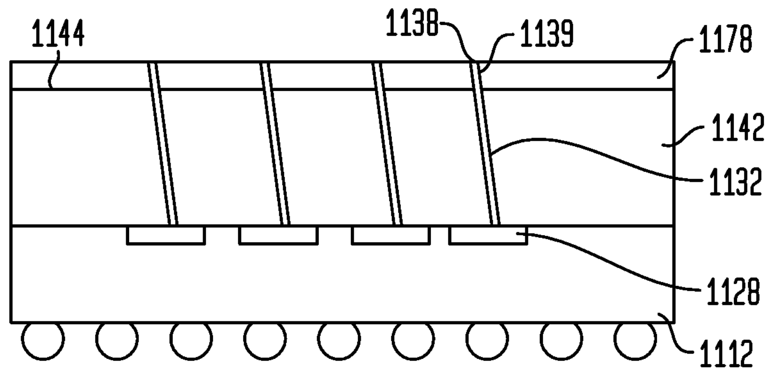


FIG. 37D

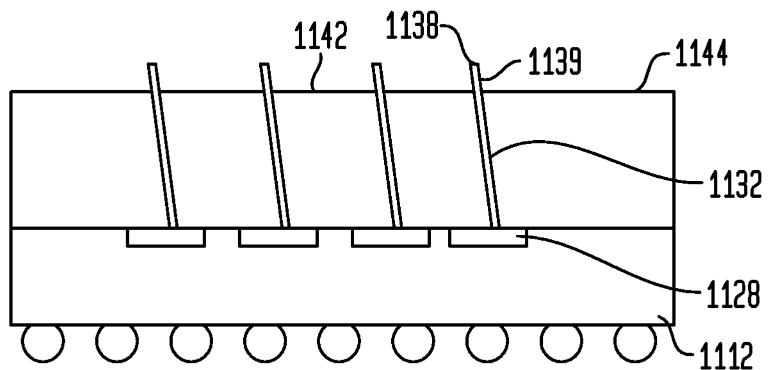


FIG. 38A

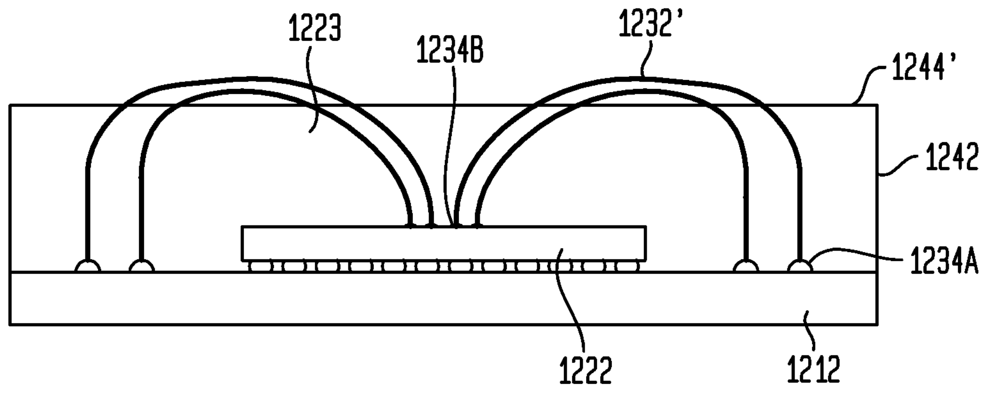


FIG. 38B

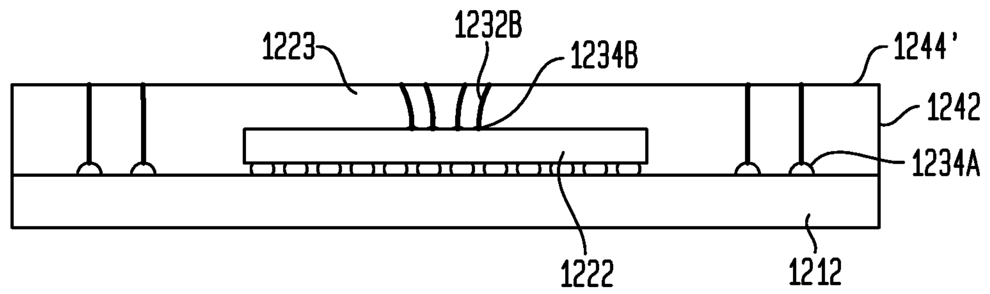


FIG. 39A

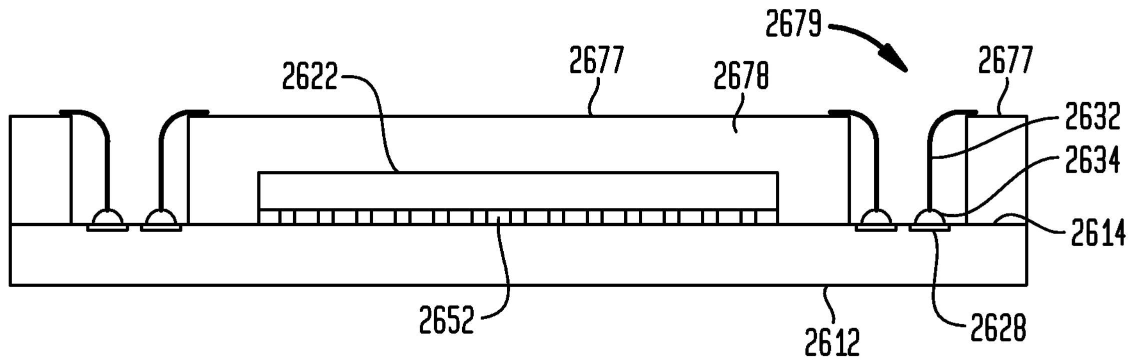


FIG. 39B

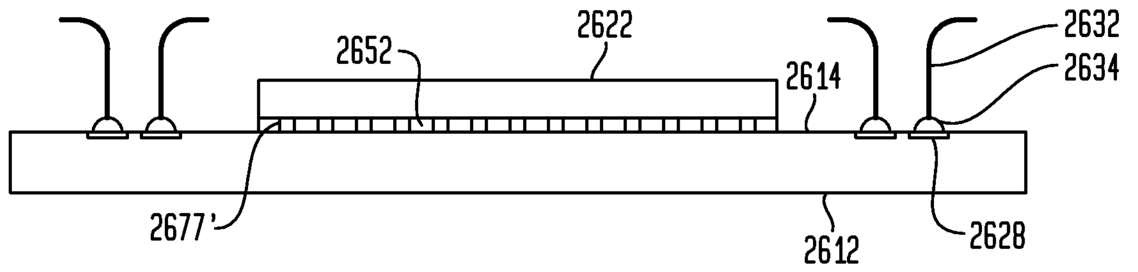


FIG. 39C

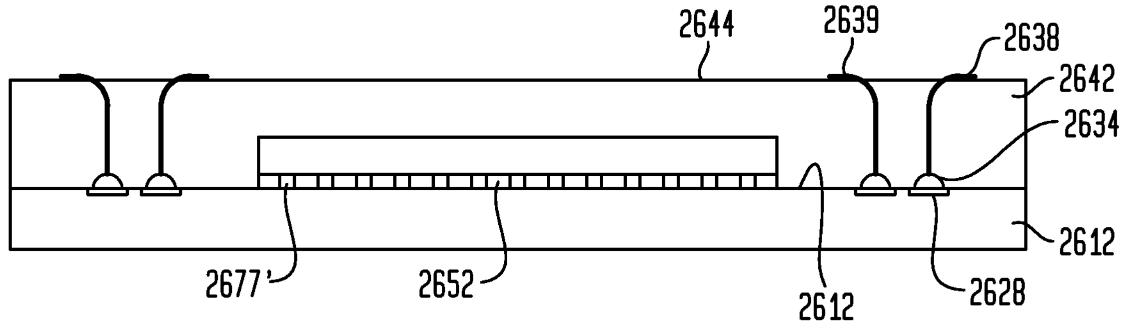


FIG. 40

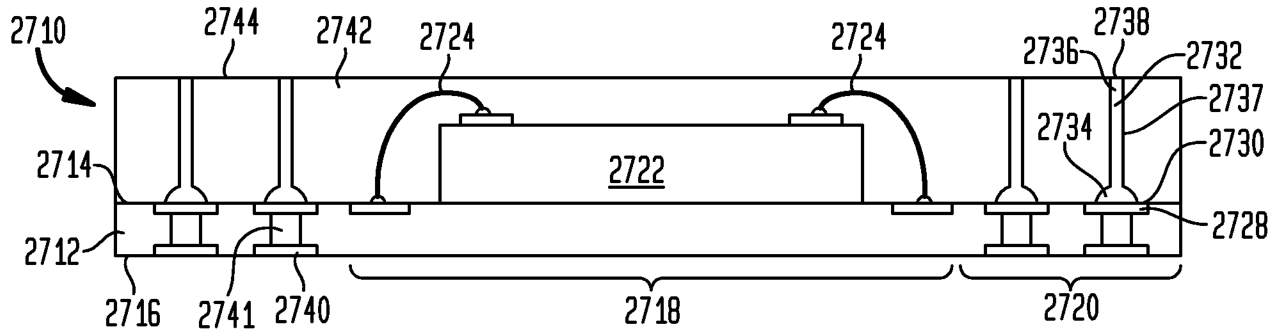


FIG. 41

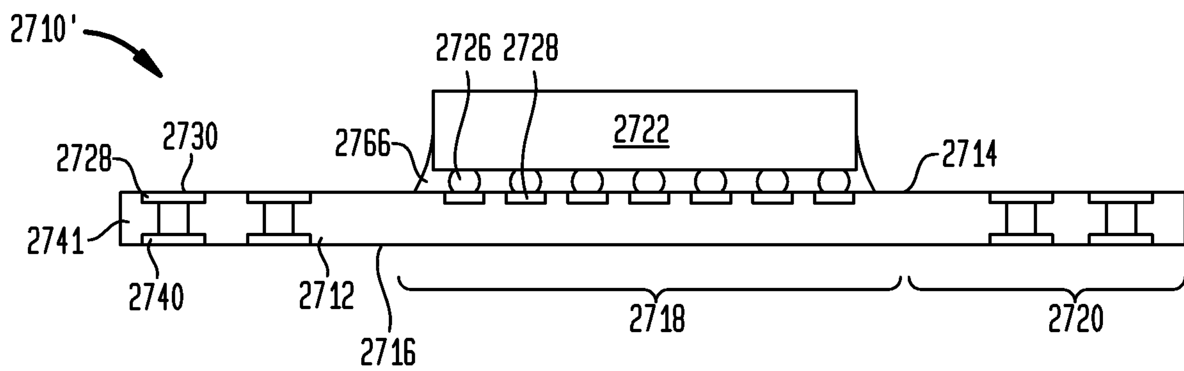


FIG. 42

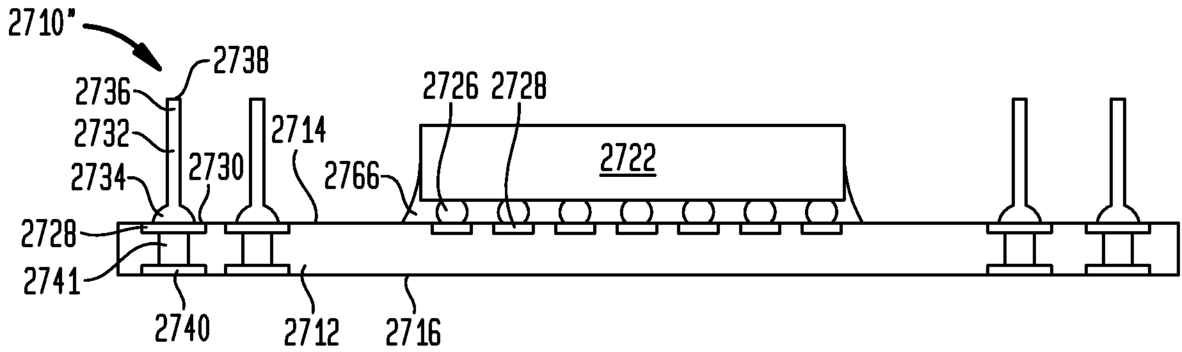


FIG. 43

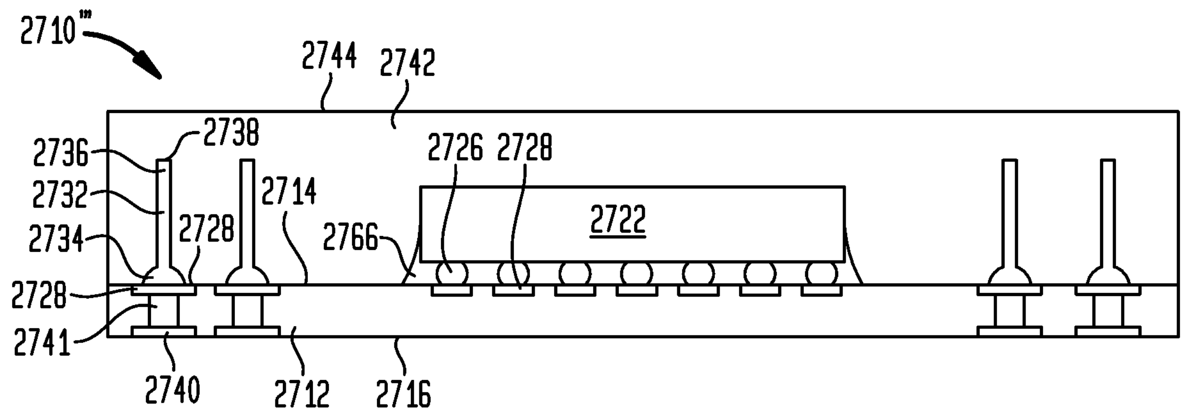
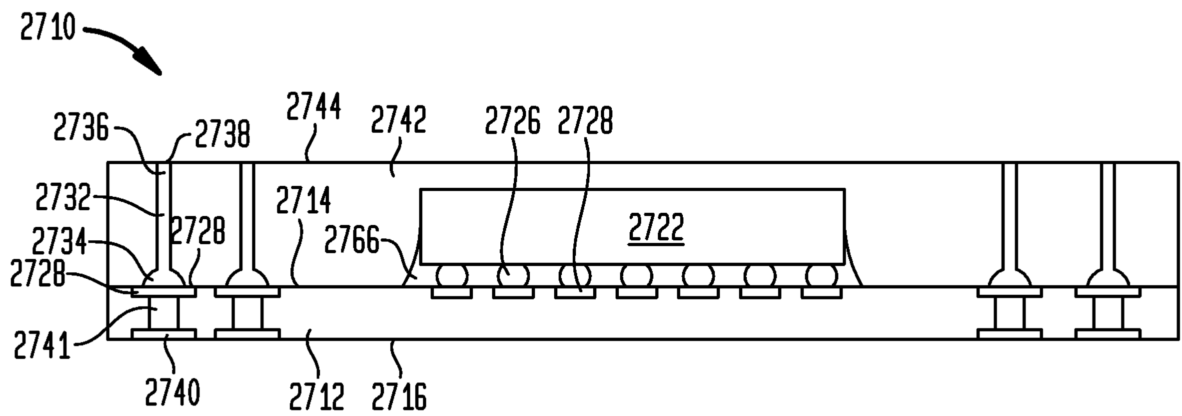


FIG. 44



INTERNATIONAL SEARCH REPORT

International application No
PCT/US2012/060402

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L25/10 H01L23/31 H01L23/495 H01L23/498 H01L21/48
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 7 242 081 B1 (LEE YONGGILL [TW]) 10 July 2007 (2007-07-10) column 4, line 57; figures 7a,7b column 5, line 27 - line 28; figures 5-9b column 5, line 65 - column 6, line 2 column 6, line 8 - line 10 -----	1,2,7,8, 15
A	MEISER S: "KLEIN UND KOMPLEX", ELEKTRONIK, IRL PRESS LIMITED, DE, vol. 41, no. 1, 7 January 1992 (1992-01-07), pages 72-77, XP000277326, ISSN: 0013-5658 figure 2 -----	1

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
7 February 2013	02/04/2013

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Manook, Rhoda

1

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2012/060402

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☒ Claims Nos.: 16-23, 25-44
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
see FURTHER INFORMATION sheet PCT/ISA/210

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
1, 2, 7, 8, 15

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1, 2

The subject-matter (S-M) of independent product claim 1 is not inventive in view of document US7242081 (document D1) and in the light of document MEISER S: "KLEIN UND KOMPLEX",ELEKTRONIK, IRL PRESS LIMITED, DE, vol. 41, no. 1, 7 January 1992, pages 72-77, ISSN: 0013-5658 (document D2) & cannot therefore serve as a common concept (Rule 13(1) PCT) for claims 2,3,5,7,9,13,14,15 & 24 being directly dependent upon this common concept.
The S-M of claim 1 lacks an inventive step according to the argumentation detailed in the non unity reasoning section 1.1.
(re. claim 2)
With regards to claim 2, the special technical feature with respect to the known claim 1 is that the angle is between 80° and 90°.

1.1. claims: 7, 8, 15

Although the special technical features of the dependent claims 7-8,15 are not the same, they could be searched without any effort and are thus included in the first searched group of claims.

---

2. claims: 3, 4

(re. claim 3)
With regards to claim 3, the special technical feature with respect to the known claim 1 is that each of at least some of the unencapsulated portions of the wire bonds includes a ball-shaped portion, each ball-shaped portion being integral with a cylindrical portion of such wire bond, each ball-shaped portion and each cylindrical portion having at least a core consisting essentially of copper, copper alloy or gold.
The problem to be solved by claim 3 is anchoring of the wire bond end, ensuring the wire is exposed on the encapsulation even after thermal processing.

---

3. claims: 5, 6

(re. claim 5)
With regards to claim 5, the special technical feature with respect to the known claim 1 is that at least some of the wire bonds have a core of a primary metal and a metallic finish including a second metal different from the primary metal overlying the primary metal.
The problem to be solved by claim 5 is preventing oxidation of the wirebond.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

---

4. claims: 9-12

   (re. claim 9)
   With regards to claim 9, the special technical feature with respect to the known claim 1 is that an end of at least one of the wire bonds is displaced in a direction parallel to the first surface of the substrate from its base by at least a distance equal to one of: a minimum pitch between the conductive elements, and 100 microns, wherein at least one of the wire bonds includes at least one bend between the base thereof and the unencapsulated portion thereof and, wherein the bend of the at least one wire bond is remote from the base thereof and the unencapsulated portion thereof.
   The problem to be solved by claim 9 is buffering for thermal expansion.

---

5. claim: 13

   (re. claim 13)
   With regards to claim 13, the special technical feature with respect to the known claim 1 is that the conductive elements are non-solder mask defined.
   The problem to be solved by claim 13 is configured to accommodate the edge bond of the first portion, while allowing for variations in the precision with which the edge bond are located and for variations in the bonding process. (see application par. 149)

---

6. claim: 14

   (re. claim 14)
   With regards to claim 14, the special technical feature with respect to the known claim 1 is that ball bonds are joined to and overlying portions of the bases of the wire bonds.
   The problem to be solved by claim 14 is ensuring that the bond-wires are mechanically stable (see application fig. 23b) i.e. reinforcing of the wedge-bond.

---

7. claim: 24

   (re. claim 24)
   With regards to claim 24, the special technical feature with respect to the known claim 1 is that further including a plurality of terminals exposed at the second surface of the substrate, and peripheral edges extending in a direction between the first and second surfaces of the substrate;
   a second microelectronic package including a substrate having contacts thereon, a second microelectronic element electrically connected with the contacts, and terminals

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

exposed at a surface of the substrate and electrically connected with the second microelectronic element through the contacts, the terminals of the second microelectronic element facing and being electrically connected with respective unencapsulated portions of the wire bonds;
a circuit panel including a first surface and panel contacts exposed at the surface thereof, the first microelectronic package overlying the circuit panel and having the terminals of the first microelectronic package joined to the panel contacts of the circuit panel; and
a monolithic underfill overlying at least one of the peripheral edges of the first microelectronic package and disposed within spaces surrounding the joints between the terminals of the first microelectronic package and the panel contacts of the circuit panel, and disposed within spaces surrounding the joints between the terminals of the second microelectronic package and the first microelectronic package.
The problem to be solved by claim 24 is assembling multiple packages for high density whilst maintaining the same package footprint.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

Continuation of Box II.2

Claims Nos.: 16-23, 25-44

The present application contains 44 claims, of which six are independent product claims and nine are independent method claims. In the set of claims there is no clear distinction between the independent claims because of overlapping scope. Furthermore there are so many claims, and they are drafted in such a way that the claims as a whole are not in compliance with the provisions of clarity and conciseness of Art. 6 PCT (see also Rule 6.1(a) PCT), as it is particularly burdensome for a skilled person to establish the subject-matter for which protection is actually sought. Hence, the non-compliance with the substantive provisions is to such an extent, that the search was performed taking into consideration this non-compliance in determining the extent of the search (PCT Guidelines 9.19 and 9.25). Consequently this search has been carried out for those parts of the claimed subject-matter that appeared to be clear enough and concise per se, namely the group of claims formed by claim 1 and the dependent claims thereon, that is to say claims 1-15 and 24, apparently covering the embodiments shown in figures 1, 3, 13a,13b,13d,13f,23a,23b,27a,27b and 27c, comprising a reasonable definition of what is understood to be the invention for which protection is sought, and constituting subject matter that could reasonably be expected to be claimed later in the procedure, namely that of a wedge-bonded (also known as a stitch bond, see application par. 148) wirebond connection and not a ball-bonded bond wire connection to the substrate.

The applicant's attention is drawn to the fact that claims relating to inventions in respect of which no international search report has been established need not be the subject of an international preliminary examination (Rule 66.1(e) PCT). The applicant is advised that the EPO policy when acting as an International Preliminary Examining Authority is normally not to carry out a preliminary examination on matter which has not been searched. This is the case irrespective of whether or not the claims are amended following receipt of the search report or during any Chapter II procedure. If the application proceeds into the regional phase before the EPO, the applicant is reminded that a search may be carried out during examination before the EPO (see EPO Guideline C-VI, 8.2), should the problems which led to the Article 17(2) declaration be overcome.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2012/060402

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 7242081 B1	10-07-2007	TW I331382 B	01-10-2010
		US 7242081 B1	10-07-2007
		US 2007254406 A1	01-11-2007