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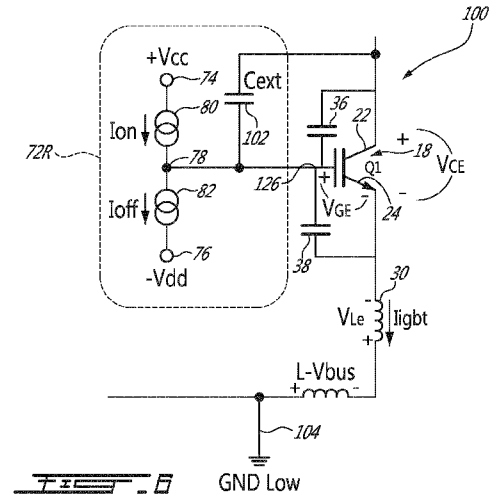
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(54) **Title:** GATE DRIVER CONTROLLING A COLLECTOR TO EMITTER VOLTAGE VARIATION OF AN ELECTRONIC SWITCH AND CIRCUITS INCLUDING THE GATE DRIVER



(57) **Abstract:** The present disclosure introduces a gate driver used to drive a power electronic switch of a commutation cell. The gate driver comprises a turn-off current source connected to a gate of the power electronic switch and an additional current source. The additional current source is in parallel to the turn-off current source of the gate driver and is configured to control a collector to emitter voltage variation at turn off of the power electronic switch. A circuit combining the gate driver with a commutation cell having a power electronic switch, a circuit combining a pair of gate drivers with a leg having two commutation cells including two power electronic switches and a converter including such circuits are also disclosed.

## GATE DRIVER CONTROLLING A COLLECTOR TO EMITTER VOLTAGE VARIATION OF AN ELECTRONIC SWITCH AND CIRCUITS INCLUDING THE GATE DRIVER

### TECHNICAL FIELD

**[0001]** The present disclosure relates to the field of power electronics. More specifically, the present disclosure relates to a gate driver for controlling a collector to emitter voltage variation of an electronic switch and to circuits including the gate driver.

### BACKGROUND

**[0002]** Commutation cells are commonly used in electronic systems that require conversion of a voltage source, including both DC-DC and DC-AC converters. Figure 1 is an idealized circuit diagram of a conventional commutation cell having a single power electronic switch and a single freewheel diode with a voltage source and a current load. A commutation cell 10 converts a DC voltage  $V_{bus}$  from a voltage source 12 (or from a capacitor 20) into a current source  $I_{out}$  11 (or into an inductance) that usually generates a voltage  $V_{out}$  appropriate for a load 14, which may be a resistive load, an electric motor, and the like. The commutation cell 10 comprises a freewheel diode 16, a controlled power electronic switch 18, for example an isolated gate bipolar transistor (IGBT) as shown on Figure 1. Another commutation cell may replace the IGBT with a metal-oxide-semiconductor field-effect transistor (MOSFET), with a bipolar transistor, and the like. The communication cell 10 also comprises the capacitor 20 and an inductance 28. The capacitor 20 limits variations of the voltage  $V_{bus}$  of the voltage source 12 while the inductance 28 limits the variations of the output current  $I_{out}$  11. A gate driver (not shown in Figure 1 but shown on later Figures) controls turning on and off of the power electronic switch 18. Figure 1 illustrates a configuration of the commutation cell 10, of the load 14, and of the voltage source 12, in which energy flows from the

voltage source 12 to the load 14, i.e. from left to right on the drawing. The commutation cell 10 can also be used in a reverse configuration in which energy flows in the opposite direction.

**[0003]** When turned on, the power electronic switch 18 allows current to pass therethrough, from its collector 22 to its emitter 24. The power electronic switch 18 can be approximated as a closed circuit. When the power electronic switch 18 turns off, it becomes an open circuit and a collector to emitter voltage  $V_{ce}$  is built thereacross.

**[0004]** The gate driver applies a variable control voltage between the gate 26 and the emitter 24 of the power electronic switch 18. For some types of power electronic switches such as bipolar transistors, the gate driver may act as a current source instead of as a voltage source. Generally, when the voltage applied between the gate 26 and the emitter 24 is "high", the power electronic switch 18 allows passing of current from the collector 22 to the emitter 24. When the voltage applied between the gate 26 and the emitter 24 is "low", the power electronic switch 18 limits passage of current therethrough while the voltage  $V_{ce}$  increases. In more details, a voltage difference between the gate 26 and the emitter 24, denoted  $V_{ge}$ , is controlled by the gate driver. When  $V_{ge}$  is greater than a threshold  $V_{ge(th)}$  for the power electronic switch 18, the switch 18 is turned on and the voltage  $V_{ce}$  between the collector 22 and the emitter 24 becomes near zero. When  $V_{ge}$  is lower than  $V_{ge(th)}$ , the power electronic switch 18 is turned off and a current from the collector 22 to the emitter 24 becomes near zero while, at the same time,  $V_{ce}$  tends to reach  $V_{bus}$ .

**[0005]** When the power electronic switch 18 is turned on, the current  $I_{out}$  11 flows from the voltage source 12 (and transiently from the capacitor 20) through the load 14 and through the collector 22 and the emitter 24. When the power electronic switch 18 is turned off, the current  $I_{out}$  11 circulates from the load 14 and passes in the freewheel diode 16. Turning on and off of the power electronic switch 18 at a high frequency allows the current  $I_{out}$  11, in the output

inductance 28, to remain fairly constant.

**[0006]** It should be observed that, in the case of other power electronic switch types, for example bipolar transistors, the term "gate" may be replaced with "base", the base being controlled by a current as opposed to the gate that is controlled by a voltage. These distinctions do not change the overall operation principles of the commutation cell 10.

**[0007]** Figure 2 is another circuit diagram of the conventional commutation cell of Figure 1, showing parasitic inductances and capacitances. In contrast with the idealized model of Figure 1, connections between components of an actual commutation cell define parasitic (stray) inductances while isolation between components defines parasitic capacitances. Though the parasitic inductances are distributed at various places within the commutation cell 10, a suitable model presented in Figure 2 shows two (2) distinct inductances representing the overall parasitic inductance, including an emitter inductance 30 of the power electronic switch 18 and an inductance 32 representative of all other parasitic inductances (other than the emitter inductance 30) around a high frequency loop 34 formed by the freewheel diode 16, the power electronic switch 18 and the capacitor 20. The high frequency loop 34 is a path where current changes significantly upon switching of the power electronic switch 34. It should be noted that an output inductance  $L_{out}$  28 is not part of the high frequency loop because its current remains fairly constant through the commutation period. Significant parasitic capacitances include a collector to gate capacitance 36 and a gate to emitter capacitance 38.

**[0008]** Figure 3 is an illustration of an equivalent circuit of a typical IGBT. The IGBT 40 combines, in a single device, the simple and low power capacitive gate-source characteristics of metal-oxide-semiconductor field-effect transistors (MOSFET) with high-current and low-saturation-voltage capability of bipolar transistors. An IGBT 40 can be used as the power

electronic switch 18 of Figures 1 and 2 and has the same gate, 26, collector 22 and emitter 24. In more details, the equivalent circuit of the IGBT 40 is made from one MOSFET 42 and two bipolar transistors 44, 46 connected in a thyristor configuration 48, the equivalent circuit of the thyristor being the same as the output stage of the IGBT 40: two bipolar transistors, including one PNP transistor 44 and one NPN transistor 46, that polarize each other. The input of the IGBT 40 is made from an equivalent MOSFET 42 that is voltage-controlled, has low-power gate driver dissipation and provides high speed switching. The output of the IGBT 40 is made with the two bipolar transistors 44, 46 connected in the thyristor configuration 48 to provide a powerful output.

**[0009]** While the bipolar transistors 44, 46 are capable of supporting high power levels, their reaction time does not match that of the MOSFET 42.

**[0010]** When the IGBT 40 is subjected to a sufficient gate to emitter voltage  $V_{ge}$ , the MOSFET 42 turns on first. This causes current to circulate through the base-emitter junction of the PNP transistor 44, turning the PNP transistor 44 on. This, in turn, turns on the NPN transistor 46, following which the IGBT 40 is ready to deliver high-level current through the collector 22 and the emitter 24.

**[0011]** The MOSFET 42 can take the whole current of the IGBT 40 under light loads, via a drift region 50, which implies that the IGBT 40 is capable of turning on quickly with a well-controlled variation ( $di/dt$ ) of the current flowing through the collector 22 and the emitter 24. To carry the current at full rating of the IGBT 40 under heavier loads, the bipolar transistors 44, 46 need to turn on. Speed of the full turn on of the IGBT 40 depends on the temperature and on the amplitude of the current flowing through the collector 22 and the emitter 24.

**[0012]** The MOSFET 42 also switches off first at turn off of the IGBT 40. Even when the MOSFET 42 is completely off, the two bipolar transistors 44, 46 remain conductive for a brief moment, until minority carriers located on

their base-emitter junctions are removed. The body region 52 of the IGBT 40 allows the thyristor 48 to turn off by turning the NPN transistor 46 off first. Once the NPN transistor 48 is off, the minority carriers of the base-emitter junction of the PNP transistor 44 are removed, effectively terminating the turn off process of the IGBT 40.

**[0013]** Because the output stage of the IGBT 40 formed by the bipolar transistors 44, 46 is slower than its input stage formed by the MOSFET 42, there is a limit above which speeding up a control signal applied at the gate 26 will have no significant impact on the switching time of the IGBT 40. For example, during turn on, at a greater current load than can be handled by the MOSFET 42, the full current load can only be supported once the thyristor 48 (i.e. the two bipolar transistors 44, 46) is turned on. In the same way, during turn off, even when accelerating a control signal applied at the gate 26, the thyristor 48 remains conductive until the minority carriers are removed.

**[0014]** The inherent non-linearity of the various components of the IGBT 40 complicates its control and makes it difficult to operate with maximal efficiency. While it is desired to rapidly switch the IGBT 40 on and off in order to reduce as much as possible losses during the commutation process, it is also desired to avoid excessive collector to emitter overvoltage of the IGBT 40 while also avoiding excessive recovery current of the freewheel diode 16.

**[0015]** Figure 4 is a graph showing an example of switching losses of an IGBT as a function of gate resistance values. Energy losses, denoted  $E_{on}$  when related to turn-on of the IGBT 40 and  $E_{off}$  when related to turn-off of the IGBT 40, are expressed in millijoules (mJ) as a function of a value of a gate resistor ( $R_G$ ) that represents an output impedance of the gate driver controlling the IGBT 40. Because the IGBT 40 behaves as a voltage controlled current source while in its linear region, the collector to emitter current flowing through the IGBT 40 increases with a voltage  $V_{ge}$  applied between the gate 26 and the emitter 24. It is well known that bipolar transistors are faster at turn on than at

turn off. For this reason, losses at turn on of the IGBT 40 are mainly dependent on the resistance value  $R_G$  of the gate driver, which defines an equivalent on/off current source and provides the voltage  $V_{ge}$  between the gate 26 and the emitter 24. On the other hand, the MOSFET 42 may be turned off completely while the thyristor 48 is still conducting, until the charges on the base-emitter of the bipolar transistors 44, 46 are completely removed. As a result, a slope of the losses as a function of the gate resistor  $R_G$  is lower for the turn off than the same curve for the turn on. On Figure 4, though losses are somewhat temperature-dependent, losses at turn on (60, 62) are impacted by recovery current in the freewheel diode 16 and therefore tend to be greater than losses at turn off (64, 66)

**[0016]** Figure 5 is a circuit diagram of a conventional IGBT leg having a pair of power electronic switches and further showing a gate driver. Typically, three (3) legs as shown on Figure 5 provide power to a three-phase AC motor. Alternatively, a pair of such legs can provide power to a single-phase AC motor. Some elements of the IGBT leg 70 are not shown on Figure 5, in order to simplify the illustration. Figure 5 includes elements introduced in the foregoing description of Figures 1 and 2. The IGBT leg 70 includes two (2) similar power electronic switches 18 and matching freewheel diodes 16. Pairs formed of the switches 18 and diodes 16 operate in tandem, the switch 18 at the top of the IGBT leg 70 (Q2) operating with the diode 16 at the bottom (D1), and vice-versa. Figure 5 further shows a gate driver 72 connected to one (Q1) of the illustrated power electronic switches 18; another gate driver 72 connected to the other (Q2) power electronic switch 18 is not shown to simplify the illustration. In Figure 5, the interconnection of two (2) switches 18 creates distinct parasitic inductances, including two (2) emitter inductances 30 and two (2) collector inductances 33.

**[0017]** The gate driver 72 has a positive supply voltage 74 and a negative supply voltage 76, an output 78 of the gate driver 72 being connected

to the gate 26 of the power electronic switch 18. The positive supply voltage 74 of the gate driver 72 has a value denoted  $+V_{cc}$ , for example +15 volts above a ground reference (not shown) while the negative supply voltage 76 has value denoted  $-V_{dd}$ , for example -5 volts below the ground reference. An input (not shown) of the gate driver 72 is connected to a controller (also not shown) of the IGBT leg 70, as is well known in the art. A voltage at the output 78 of the gate driver 72 may go up to  $+V_{cc}$  and may go down to  $-V_{dd}$  in order to control and limit the voltage at the gate 26. The gate driver 72 may have an output resistance  $R_G$  (not shown). The input resistance of the power electronic switch 18 at the gate 26 may be very high, especially in the case of an IGBT 40 because its gate 26 actually consists of a MOSFET gate whose input resistance can be considered as infinite. However, presence of the parasitic capacitances 36 and 38 causes currents  $I_{on}$  and  $I_{off}$  to flow therethrough from the output 78 when the gate driver 72 alternates between  $+V_{cc}$  and  $-V_{dd}$ . Values and waveforms of the currents  $I_{on}$  and  $I_{off}$  are determined by the gate driver 72 voltages  $+V_{cc}$  and  $V_{dd}$ , and by the impedance formed by the output resistance  $R_G$ , if any, of the gate driver 72 and by the parasitic capacitances 36 and 38.

**[0018]** On Figure 5, a current  $I_{igbt}$  flowing through the bottom power electronic switch 18 and through the bottom emitter parasitic inductance 30 is essentially equal to  $I_{out}$  11 when the bottom power electronic switch 18 is closed. At that time,  $I_{out}$  11 flows in the direction as shown on Figure 5. The current  $I_{igbt}$  quickly reduces to zero (substantially) when the bottom power electronic switch 18 turns off.

**[0019]** When one of the power electronic switches 18 turns on or off, the current  $I_{igbt}$  flowing therethrough increases or diminishes at a fast rate. These variations of  $I_{igbt}$ , denoted  $di/dt$ , generate voltage across its emitter inductance 30, according to the well-known equation (1):

$$V_L = L \cdot \frac{di}{dt} \quad (1)$$

**[0020]** wherein  $V_L$  is a voltage induced across an inductance and  $L$  is an inductance value.

**[0021]** For each of the power electronic switches 18, a voltage  $V_{Le}$  is generated across the emitter parasitic inductance 30. On Figure 5, the polarities shown across the high frequency loop inductances, including the collector inductances 33 and the emitter inductances 30, reflect voltages obtained upon turn off of the power electronic switches 18, when the  $I_{igbt}$  current diminishes very rapidly,  $di/dt$  thus taking a negative value. Upon turn on of the power electronic switches 18, voltages across the high frequency loop inductances, including the collector inductances 33 and the emitter inductances 30, are in the opposite direction.

**[0022]** It may be observed that a MOSFET leg, having a similar structure as the IGBT leg 70, may be built, in which case the power electronic switches 18 comprise a pair of MOSFETs replacing the IGBTs.

**[0023]** Referring back to Figure 2, these voltages  $V_{Ls}$  and  $V_{Le}$  are in series with  $V_{bus}$  from the voltage source 12. When the power electronic switch 18 turns off, the collector 22 to emitter 24 voltage increases until the freewheel diode 16 turns on. At that time, addition of  $V_{bus}$ ,  $V_{Ls}$  and  $V_{Le}$  result in important overvoltage applied between the collector 22 and the emitter 24 of the power electronic switch 18. The same situation applies to both power electronic switches 18 (Q1 and Q2) of Figure 5. Though power electronic switches are rated for operation at some level of voltage, extreme overvoltage can reduce the lifetime of any power electronic switch to thereby lead to its premature failure or even break the device.

**[0024]** Solutions exist that tend to limit overvoltage across power electronic switches by slowing down the slope of the gate-emitter voltage. However, excessive limitation of the overvoltage can imply longer switching times of the current, reducing commutation cell performance.

**[0025]** Therefore, there is a need for methods and circuits capable of

reducing overvoltage occurring upon switching in commutation cells without causing undue switching delays.

#### SUMMARY

**[0026]** According to the present disclosure, there is provided a gate driver for driving a power electronic switch of a commutation cell. The gate driver comprises a turn-off current source connected to a gate of the power electronic switch and an additional current source in parallel to the turn-off current source and configured to control a variation of a collector to emitter voltage of the power electronic switch at turn off of the power electronic switch.

**[0027]** According to another aspect of the present disclosure, there is also provided a circuit comprising a commutation cell. The commutation cell includes a power electronic switch having a collector, a gate and an emitter. Isolation between the collector and the gate forms a parasitic capacitance. The commutation cell further includes a freewheel diode, a capacitor and an inductance. A gate driver drives the power electronic switch. The gate driver includes a turn-off current source connected to the gate of the power electronic switch, and an additional current source in parallel to the turn-off current source. The additional current source is configured to control a collector to emitter voltage variation at turn off of the power electronic switch.

**[0028]** According to yet another aspect of the present disclosure, there is also provided a circuit comprising a leg having two commutation cells. Each commutation cell has a power electronic switch. Two gate drivers including turn-on and turn-off current sources are configured to turn on and then off one of the two power electronic switches while turning off and then on the other of the two power electronic switches. Two additional current sources are also included, each additional current source being in parallel with a turn-off current source of one of the two gate drivers.

**[0029]** A fourth aspect of the present disclosure relates to a converter

configured to perform a conversion selected from a DC to DC conversion, a DC to AC conversion and an AC to DC conversion. The convertor includes one of the above described circuits, the circuit having at least one commutation cell having a power electronic switch, a gate driver including turn-on and turn-off current sources and an additional current source in parallel with the turn-off current source.

**[0030]** The foregoing and other features will become more apparent upon reading of the following non-restrictive description of illustrative embodiments thereof, given by way of example only with reference to the accompanying drawings.

#### BRIEF DESCRIPTION OF THE DRAWINGS

**[0031]** Embodiments of the disclosure will be described by way of example only with reference to the accompanying drawings, in which:

**[0032]** Figure 1 is an idealized circuit diagram of a conventional commutation cell having a single power electronic switch and a single freewheel diode with a voltage source and a current load;

**[0033]** Figure 2 is another circuit diagram of the conventional commutation cell of Figure 1, showing parasitic inductances and capacitances;

**[0034]** Figure 3 is an illustration of an equivalent circuit of a typical IGBT;

**[0035]** Figure 4 is a graph showing an example of switching losses of an IGBT as a function of gate resistance values;

**[0036]** Figure 5 is a circuit diagram of a conventional IGBT leg having a pair of power electronic switches and further showing a gate driver;

- [0037]** Figure 6 is a circuit diagram of a gate driver having an additional capacitor to control the voltage variation across the IGBT of a commutation cell according to an embodiment;
- [0038]** Figures 7a and 7b show two examples of current sources that may be used as a part of the gate driver of Figure 6;
- [0039]** Figure 8 is a graph illustrating the non-linearity of parasitic capacitances of an IGBT;
- [0040]** Figure 9 is a graph showing a typical waveform of a high voltage IGBT at turn off using a gate driver having a single turn-off current source, without external capacitor; and
- [0041]** Figure 10 is a graph showing a predicted waveform of the high voltage IGBT at turn off using the gate driver of Figure 6, with an external capacitor.
- [0042]** Like numerals represent like features on the various drawings.

#### DETAILED DESCRIPTION

**[0043]** Various aspects of the present disclosure generally address one or more of the problems of overvoltage present in commutation cells at the time of switch off and the problems of excessive recovery current present in commutation cells at the time of switch on. Generally stated, the risk of failure of power electronic switches is expected to be reduced when overvoltage and excessive recovery current are under control. This may be achieved, at least in part, by maintaining the power electronic switches close to their linear region during the commutation process.

**[0044]** In one aspect, the present disclosure introduces a gate driver for driving a commutation cell comprising a power electronic switch. The power electronic switch has a collector, a gate and an emitter. Isolation between the collector and the gate forms a parasitic capacitance. The gate driver is

configured as a pair of current sources connected to the gate of the power electronic switch, the current sources respectively providing a turn-on current and a turn-off current. An additional current source is placed in parallel to the turn-off current source of the gate driver and is configured to limit collector to emitter voltage variation ( $dV/dt$ ) at turn off of the power electronic switch. Presence of the additional current source is instrumental in maintaining the power electronic switch into its linear operating region at turn-off.

**[0045]** In more details, in order to control the voltage variation across the collector and emitter of a power electronic switch such as an IGBT at turn off, the present technology slows down a variation of the gate voltage so that it remains slightly below the maximum rate of variation sustainable by the slowest sub-component of the whole power electronic switch.

**[0046]** Circuits operable to limit overvoltage in commutation cells, especially at turn off of IGBTs, are described in international patent applications PCT/CA2012/001125 and PCT/CA2013/000805, in US provisional applications no 61/808,254 and 61/904,038, and in "Reducing switching losses and increasing IGBT drive efficiency with Reflex™ gate driver technology", available at [http://www.advbe.com/docs/DeciElec2013-Jean\\_Marc\\_Cyr-TM4.pdf](http://www.advbe.com/docs/DeciElec2013-Jean_Marc_Cyr-TM4.pdf), all of which are authored by Jean-Marc Cyr *et al.*, the disclosure of these being incorporated by reference herein. The present technology provides a reduction of overvoltage at turn off of a power electronic switch of a commutation cell. Solutions presented herein are generally compatible with other solutions to limit recovery current of the opposite diode and overvoltage across power electronic switches. As such, the solutions presented herein can be used alone or in combination with those described in international patent applications PCT/CA2012/001125 and PCT/CA2013/000805, in US provisional applications no 61/808,254 and 61/904,038, and in "Reducing switching losses and increasing IGBT drive efficiency with Reflex™ gate driver technology" to Jean-Marc Cyr *et al.*

**[0047]** Figure 6 is a circuit diagram of a gate driver having an additional capacitor to control the voltage variation across the IGBT of a commutation cell according to an embodiment. Presence of the additional capacitor helps maintaining the IGBT in its linear region during the collector to emitter voltage variation ( $dV_{ce}/dt$ ) period of the switching process. A commutation cell 100 comprises a power electronic switch 18. Other components of the communication cell 100, including a freewheel diode, a voltage source (e.g. an input capacitor) and a current load (e.g. an output inductance), are not shown in order to simplify the illustration; these elements have been introduced hereinabove. The power electronic switch 18 has a collector 22, a gate 26 and an emitter 24. Isolation between the collector 22 and the gate 26 forms a parasitic capacitance 36. A gate driver 72R shown on Figure 6 comprises a turn-on current source 80 and a turn-off current source 82 connected to the gate 26 of the power electronic switch 18. The turn-on current source 80 provides a turn-on current  $I_{on}$  at turn on of the power electronic switch 18. The turn-off current source 82 provides a turn-off current  $I_{off}$  at turn off of the power electronic switch 18. An additional current source (described hereinbelow) is placed in parallel to the current sources 80, 82 of the gate driver 72R and is configured to limit collector to emitter voltage variation  $dV_{ce}/dt$  at turn off of the power electronic switch 18. Presence of the additional current source brings no significant effect at turn-on of the power electronic switch 18 because the  $dV_{ce}/dt$  is mainly driven by the recovery current of the freewheel diode and a parasitic capacitor of the freewheel diode (including the collector to emitter capacitor of the opposite power electronic switch in parallel with that freewheel diode) and the collector to emitter capacitor of the power electronic switch (including the freewheel diode capacitor in parallel therewith).

**[0048]** Presence within the gate driver 72R of the additional current source slows down a change of a gate to emitter voltage  $V_{ge}$  and, consequently, of the collector to emitter voltage  $V_{ce}$ , at turn off of the power

electronic switch 18. This helps maintaining the power electronic switch 18 in its linear region when the collector to emitter voltage  $V_{ce}$  increases. Without limitation, the additional current source may be constructed by connecting an external capacitor 102 in parallel with the parasitic capacitance 36, between the collector 22 and the gate 26. A value  $C_{ext}$  of the external capacitor 102 may be determined using equation (2):

$$C_{ext} = \frac{I_{off}}{dV_{cg}/dt} - C_{res} \quad (2)$$

**[0049]** wherein:

**[0050]**  $C_{ext}$  is the value of the external capacitor 102;

**[0051]**  $I_{off}$  is a current provided by the gate driver 72R at turn off;

**[0052]**  $dV_{cg}/dt$  is a desired maximum variation of the collector to gate voltage  $V_{cg}$ ; and

**[0053]**  $C_{res}$  is a value of the parasitic capacitance 36 between the collector 22 and the gate 26.

**[0054]** As expressed hereinbelow, the value of  $C_{res}$  varies as a function of a collector to emitter voltage of the IGBT. The value of the external capacitor  $C_{ext}$  should be calculated, using equation (2), at high collector to emitter voltage, when  $C_{res}$  is at its minimum.

**[0055]** Figure 6 shows a ground reference 104. Voltages  $+V_{cc}$  and  $-V_{dd}$  of the gate driver 72R are defined in relation to the ground reference 104.

**[0056]** Figures 7a and 7b show two examples of current sources that may be used as a part of the gate driver of Figure 6. Gate drivers 72R1 (Figure 7a) and 72R2 (Figure 7b) are variations of the gate driver 72R of Figure 6. Gate drivers 72R1 and 72R2 both include the additional current source formed of the external capacitor 102 placed in parallel with the parasitic capacitance 36 (shown on other Figures) of the power electronic switches 18.

**[0057]** Another example of the current source may comprise a simple gate resistor having a value  $R_G$ . The performance of such a current source is affected by the variation of  $V_{ge(th)}$ , which changes with the current circulating in the power switch. The current source  $I_{off}$  provided by the gate resistor at turn off may be determined using equation (3):

$$I_{off} = \frac{(-V_{dd} - V_{Le}) - V_{ge(th)}}{R_G} \quad (3)$$

**[0058]** wherein:

**[0059]**  $-V_{dd}$  is a voltage applied to the turn-off current source 82 of the gate driver 72R at turn off;

**[0060]**  $V_{Le}$  is a voltage on the emitter inductance 30;

**[0061]**  $V_{ge(th)}$  is a gate emitter threshold voltage of the power electronic switch 18; and

**[0062]**  $R_G$  is an output resistance value of the gate driver 72R, when the gate driver behaves as a current source.

**[0063]** While addition of the additional current source can be beneficial in controlling voltage variation at turn off of any commutation cell, it is particularly efficient in cases where the power electronic switch is a high voltage high power electronic non-linear switch, for example an isolated gate bipolar transistor.

**[0064]** While Figure 6 shows an additional current source 102 added to a gate driver of a commutation cell 100, inclusion of the additional current source is also applicable to the IGBT leg 70 of Figure 5. In this case, one additional current source such as 102 is added in parallel to the existing current sources 80, 82 of each of the gate drivers 72. The additional current sources 102 may be matched or unmatched. Without limitation, the two additional current sources may comprise a pair of external capacitors 102 of substantially equal values, both of which are placed in parallel with collector to

gate capacitances 36 of corresponding power electronic switches 18.

**[0065]** Figure 8 is a graph illustrating the non-linearity of parasitic capacitances of an IGBT. The graph shows how values of the collector to gate parasitic capacitance 36 ( $C_{res}$ ), of the gate to emitter parasitic capacitance 38 ( $C_{ies}$ ) and of a collector to emitter parasitic capacitance ( $C_{oes}$ ) vary as a function of the voltage  $V_{ce}$  between the collector 22 and the emitter 24. The parasitic capacitors of IGBTs are deeply nonlinear, as evidenced by the logarithmic vertical scale of the graph of Figure 8. The capacitance values are fairly high when the voltage  $V_{ce}$  across the isolation barrier formed between the collector 22 and the emitter 24 is low. The capacitance values are much reduced when the voltage  $V_{ce}$  is high. For that reason, because the value  $C_{res}$  of the parasitic capacitance 36 is small when the IGBT is subject to a high collector to emitter voltage  $V_{ce}$ , addition of the external capacitor 102 injecting in the gate 26 a current calculated as taught in the present disclosure allows maintaining the IGBT in its linear region without inducing significant effect at low values of the collector to emitter voltage  $V_{ce}$ .

**[0066]** A variation of the current flowing into the collector and emitter of the IGBT induces the voltage  $V_{Le}$  across the emitter inductance 30. During  $dV_{ce}/dt$ , current circulates in an output capacitor  $C_{oes}$  of the IGBT. Because the added current source limits the  $dV_{ce}/dt$  to a fixed predetermined value, virtually no voltage is induced across the emitter inductance 30 ( $L_e$ ). Though  $V_{Le}$  is added to the power supply voltage source with the polarity indicated on Figure 6, this value is near zero. If a gate resistor is used as a current source, considering equation (3), it can be observed that  $V_{Le}$  limits the voltage of the current  $I_{off}$  provided by the gate driver 72R at turn off. Current circulating in the collector to gate parasitic capacitance 36 (known as a 'Miller Current') and in the external capacitor 102 is maintained to a low value, reducing switching losses caused by the addition of the external capacitor 102. In some practical realizations, it has been found that an optimal value of the external capacitor

102 was in the order of magnitude of the smallest value of the collector to gate parasitic capacitance 36, in which case impact of the addition of the external capacitor 102 to energy dissipation in the gate driver 72R was not significant.

**[0067]** Figure 9 is a graph showing a typical waveform of a high voltage IGBT at turn off using a gate driver having a single turn-off current source, without external capacitor. Figure 10 is a graph showing a predicted waveform of the high voltage IGBT at turn off using the gate driver of Figure 6, with an external capacitor. Both figures use the emitter inductance 30 to limit the overvoltage. The gate driver of Figure 6 includes the additional current source induced by the  $dV_{ce}/dt$  across the external capacitor 102. Figures 9 and 10 use equivalent scales on their vertical (voltage) and horizontal (time) axes. Comparing the graphs of Figures 9 and 10, both graphs show a rapid increase 110 of the collector to emitter voltage  $V_{ce}$  upon turn off of the IGBT. Both graphs show that the  $V_{ce}$  eventually reaches a plateau 114 or 116 and then a steady level 120 equal to the DC voltage  $V_{bus}$  when the switching process is complete. However, without the additional current source of Figure 6, Figure 9 shows a high overvoltage peak 112 of the  $V_{ce}$  occurring at the end of the rapid increase 110, before the plateau 114 that leads to the steady level 120. In the case of Figure 9, it may be observed that the equivalent input MOSFET of the IGBT goes out of its linear region during the collector to emitter voltage rise, at turn off. The high overvoltage peak 112 between the collector and the emitter  $V_{ce}$  is caused by a delay of the gate to emitter voltage  $V_{ge}$  before returning into its linear region. In contrast, as shown on Figure 10, the high overvoltage peak 112 is eliminated and replaced by a lower plateau 116 leading to the steady level 120. The IGBT stays in its linear region during the entire switching process at turn off. The difference is due to the presence of the additional current source of Figure 6 built with the external capacitor 102 generating a current during the  $dV/dt$  that helps eliminating the delay on the gate to emitter voltage  $V_{ge}$ , maintaining the gate to emitter voltage  $V_{ge}$  in its linear region. Without limiting the present disclosure, the examples of Figures 9 and 10 show

a bus voltage  $V_{bus}$  of about 600 volts, the rapid increase 110 of the collector to emitter voltage  $V_{ce}$  having a duration of about 100 to 150  $\mu$ sec.

**[0068]** The foregoing provides a description of a solution applicable to commutation cells that may be used in any configurations, including a full leg of semiconductors in DC-DC converters as well as to DC-AC converters or AC-DC converters, to provide, for example, alternative current to a connected load such as a motor of an electric vehicle.

**[0069]** Those of ordinary skill in the art will realize that the description of the gate driver and circuits are illustrative only and are not intended to be in any way limiting. Other embodiments will readily suggest themselves to such persons with ordinary skill in the art having the benefit of the present disclosure. Furthermore, the disclosed gate driver and circuits may be customized to offer valuable solutions to existing needs and problems of overvoltage occurring upon switching in commutation cells.

**[0070]** In the interest of clarity, not all of the routine features of the implementations of the gate driver and circuits are shown and described. It will, of course, be appreciated that in the development of any such actual implementation of the gate driver and circuits, numerous implementation-specific decisions may need to be made in order to achieve the developer's specific goals, such as compliance with application-, system-, and business-related constraints, and that these specific goals will vary from one implementation to another and from one developer to another. Moreover, it will be appreciated that a development effort might be complex and time-consuming, but would nevertheless be a routine undertaking of engineering for those of ordinary skill in the field of power electronics having the benefit of the present disclosure.

**[0071]** It is to be understood that the gate driver and circuits are not limited in its application to the details of construction and parts illustrated in the accompanying drawings and described hereinabove.

**[0072]** The proposed gate driver and circuits are capable of other embodiments and of being practiced in various ways. It is also to be understood that the phraseology or terminology used herein is for the purpose of description and not limitation. Hence, although the, gate driver and circuits have been described hereinabove by way of illustrative embodiments thereof, the scope of the claims should not be limited by the embodiments set forth in the examples, but should be given the broadest interpretation consistent with the description as a whole.

**WHAT IS CLAIMED IS:**

1. A gate driver for driving a power electronic switch of a commutation cell, comprising:
  - a turn-off current source connected to a gate of the power electronic switch; and
  - an additional current source in parallel to the turn-off current source and configured to control a variation of a collector to emitter voltage of the power electronic switch at turn off of the power electronic switch.
2. The gate driver of claim 1, wherein the additional current source is configured to limit a rate of variation of a voltage at the gate of the power electronic switch.
3. The gate driver of any one of claims 1 or 2, wherein the additional current source is configured to maintain a gate to emitter voltage of the power electronic switch in a linear region at turn off of the power electronic switch.
4. The gate driver of any one of claims 1 to 3, wherein the additional current source comprises an external capacitor connected between the collector and the gate of the power electronic switch.
5. The gate driver of claim 4, wherein the external capacitor is connected in parallel to a parasitic capacitance between the collector and the gate of the power electronic switch.

6. The gate driver of claim 5, wherein a value of the external capacitor is determined using:

$$C_{ext} = \frac{I_{off}}{dV_{cg}/dt} - C_{res}$$

wherein:

$C_{ext}$  is the value of the external capacitor;

$I_{off}$  is a current provided by the turn-off current source of the gate driver at turn off;

$dV_{cg}/dt$  is a desired maximum variation of the collector to gate voltage  $V_{cg}$ ; and

$C_{res}$  is a value of the parasitic capacitance between the collector and the gate.

7. The gate driver of claim 5, wherein a value of the external capacitor is in an order of magnitude of a minimum value of the parasitic capacitance between the collector and the gate of the power electronic switch.
8. The gate driver of any one of claims 1 to 7, wherein the power electronic switch is selected from an isolated gate bipolar transistor, a bipolar transistor and a metal-oxide-semiconductor field-effect transistor.

9. A circuit, comprising:
- a commutation cell including a power electronic switch having a collector, a gate and an emitter, isolation between the collector and the gate forming a parasitic capacitance, the commutation cell further including a freewheel diode, a capacitor and an inductance; and
  - a gate driver for driving the power electronic switch, the gate driver including a turn-off current source connected to the gate of the power electronic switch, the gate driver further including an additional current source in parallel to the turn-off current source and configured to control a collector to emitter voltage variation at turn off of the power electronic switch.
10. The circuit of claim 9, wherein the additional current source is configured to limit a rate of variation of a voltage across the collector to emitter of the power electronic switch.
11. The circuit of any one of claims 9 or 10, wherein the additional current source is configured to maintain a gate to emitter voltage of the power electronic switch in a linear region at turn off of the power electronic switch.
12. The circuit of any one of claims 9 to 11, wherein the additional current source comprises an external capacitor connected between the collector and the gate of the power electronic switch.
13. The circuit of claim 12, wherein the external capacitor is connected in parallel to the parasitic capacitance between the collector and the gate of the power electronic switch.

14. The circuit of claim 13, wherein a value of the external capacitor is determined using:

$$C_{ext} = \frac{I_{off}}{dV_{cg}/dt} - C_{res}$$

wherein:

$C_{ext}$  is the value of the external capacitor;

$I_{off}$  is a current provided by the turn-off current source of the gate driver at turn off;

$dV_{cg}/dt$  is a desired maximum variation of the collector to gate  $V_{cg}$  voltage; and

$C_{res}$  is a value of the parasitic capacitance between the collector and the gate.

15. The circuit of claim 13, wherein a value of the external capacitor is in an order of magnitude of a minimum value of the parasitic capacitance between the collector and the gate of the power electronic switch.
16. The circuit of any one of claims 9 to 16, wherein the power electronic switch is selected from an isolated gate bipolar transistor, a bipolar transistor and a metal-oxide-semiconductor field-effect transistor.

17. A circuit, comprising:
  - a leg having two commutation cells, each commutation cell having a power electronic switch;
  - two gate drivers including turn-on and turn-off current sources configured to turn on and then off one of the two power electronic switches while turning off and then on an other one of the two power electronic switches; and
  - two additional current sources, each additional current source being in parallel with a turn-off current source of one of the two gate drivers.
18. The circuit of claim 17, wherein the two additional current sources comprises two external capacitors having substantially equal capacitance values.
19. The circuit of any one of claims 17 or 18, wherein the two additional current sources comprise two matched current sources.
20. The circuit of any one of claims 17 or 18, wherein the two additional current sources comprise two unmatched current sources.
21. A converter, comprising:
  - the circuit of any one of claims 9 to 20;
  - wherein the converter is configured to perform a conversion selected from a DC to DC conversion, a DC to AC conversion and an AC to DC conversion.

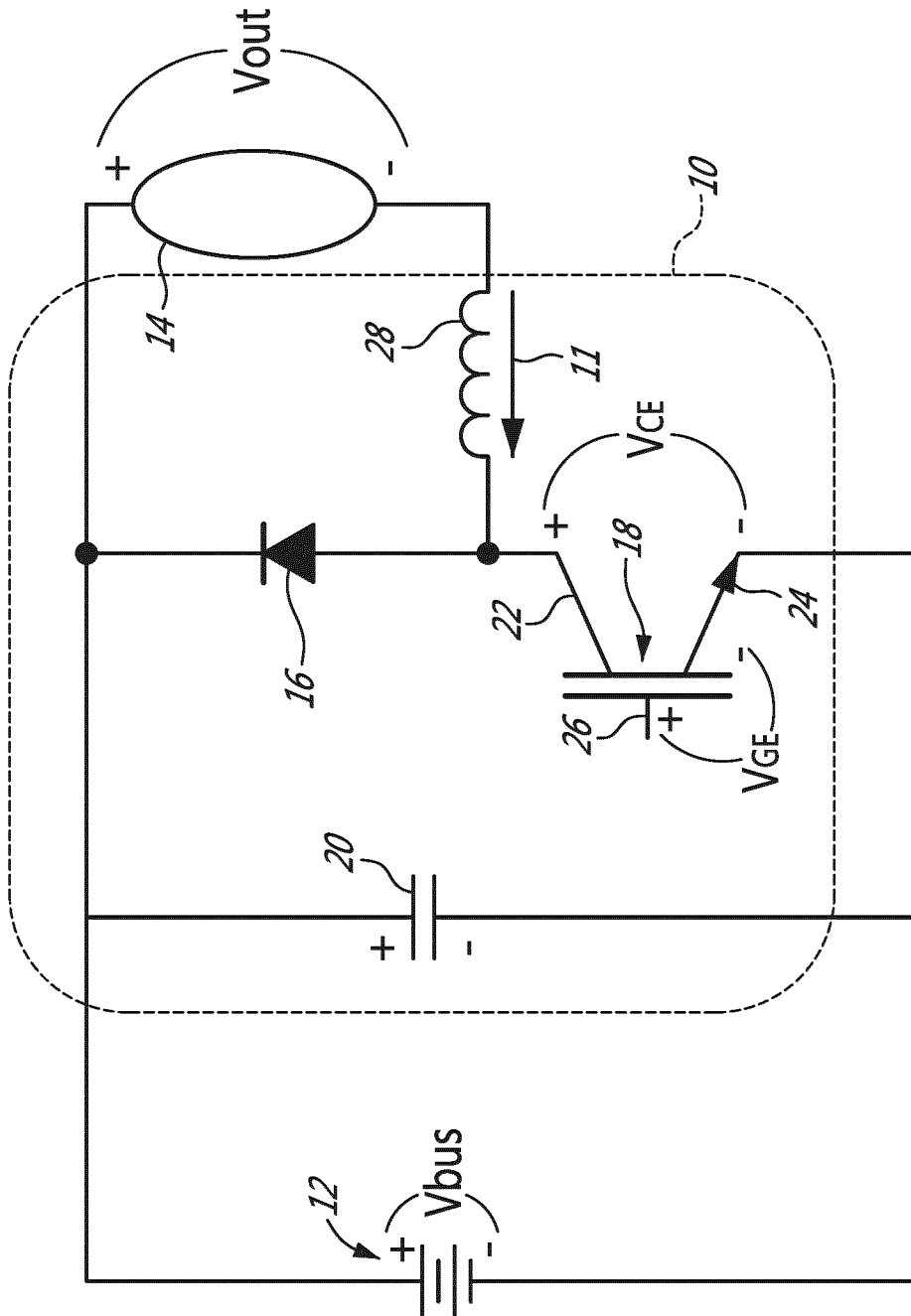


FIG. 1



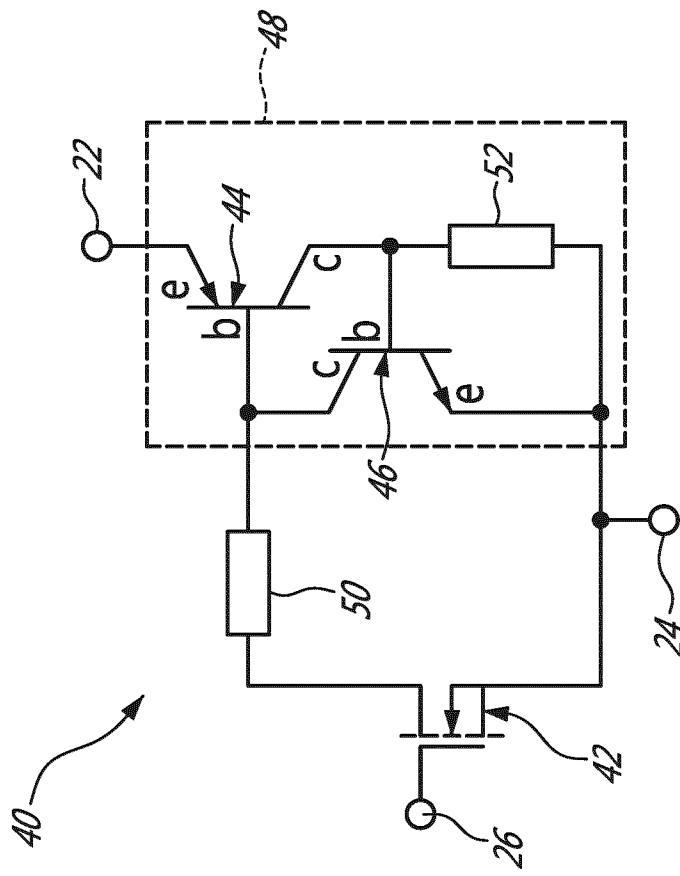


FIG. 3

switching losses IGBT-Inverter (typical)

$E_{on} = f(R_G), E_{off} = f(R_G)$

$V_{GE} = \pm 15 \text{ V}, I_c = 550 \text{ A}, V_{CE} = 300 \text{ V}$

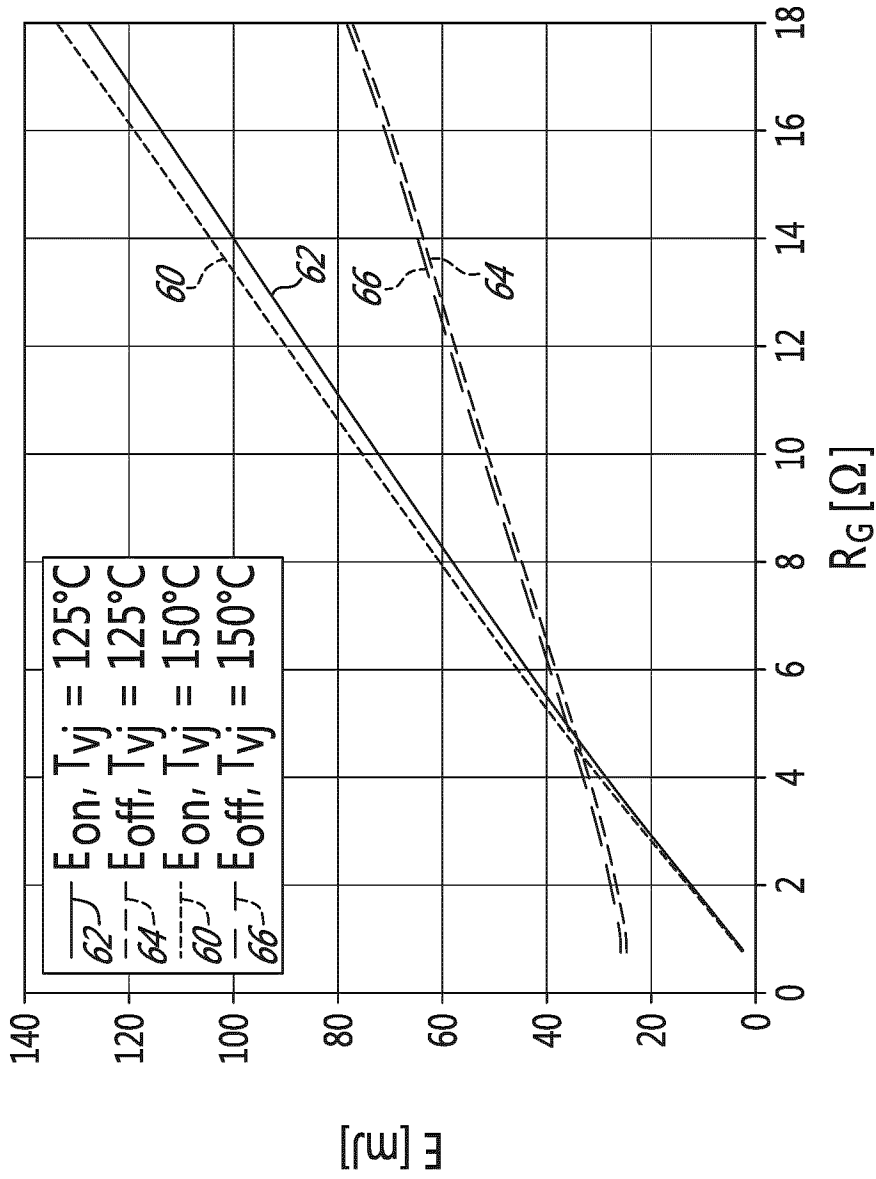


Fig. 4

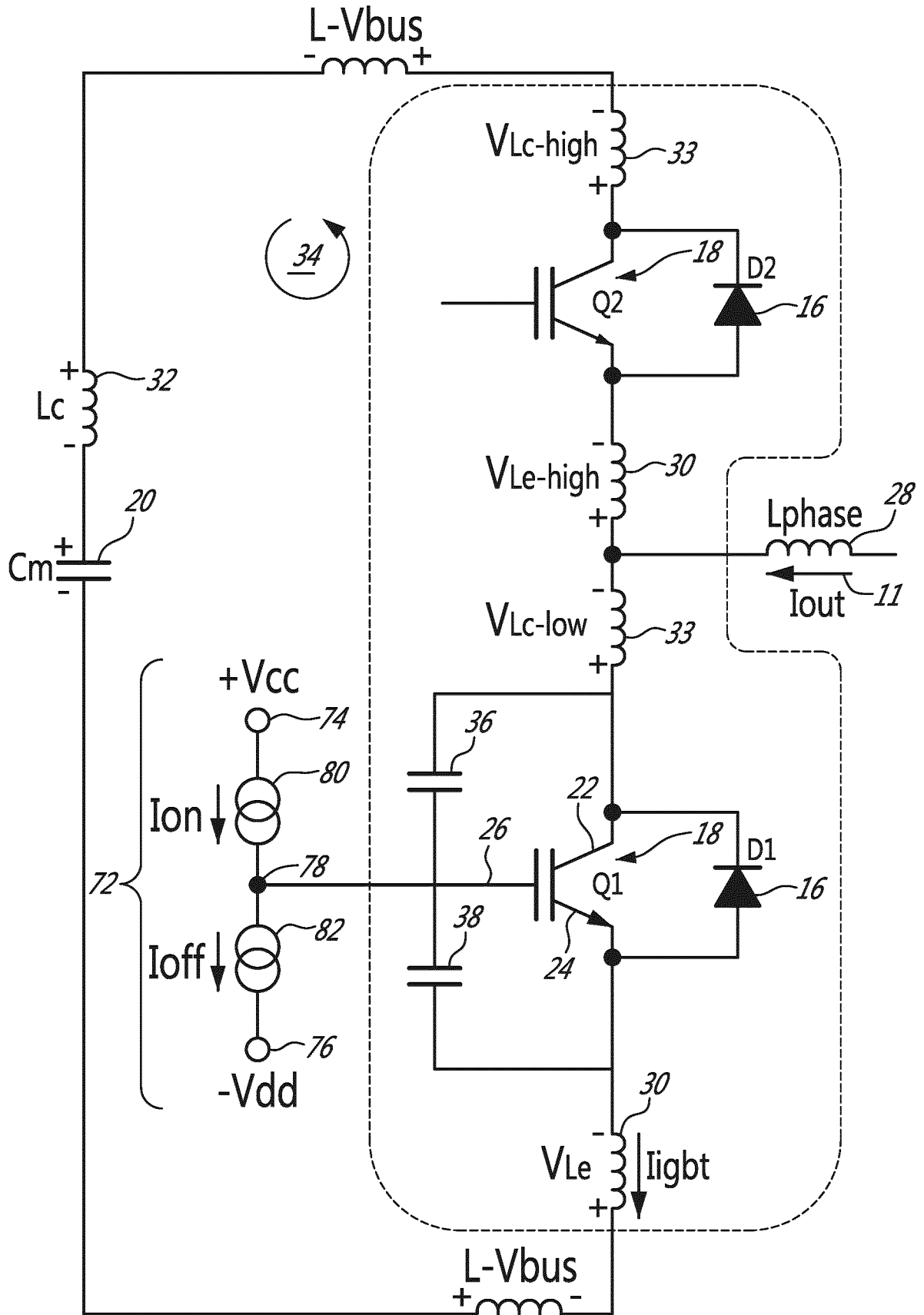


FIG. 5



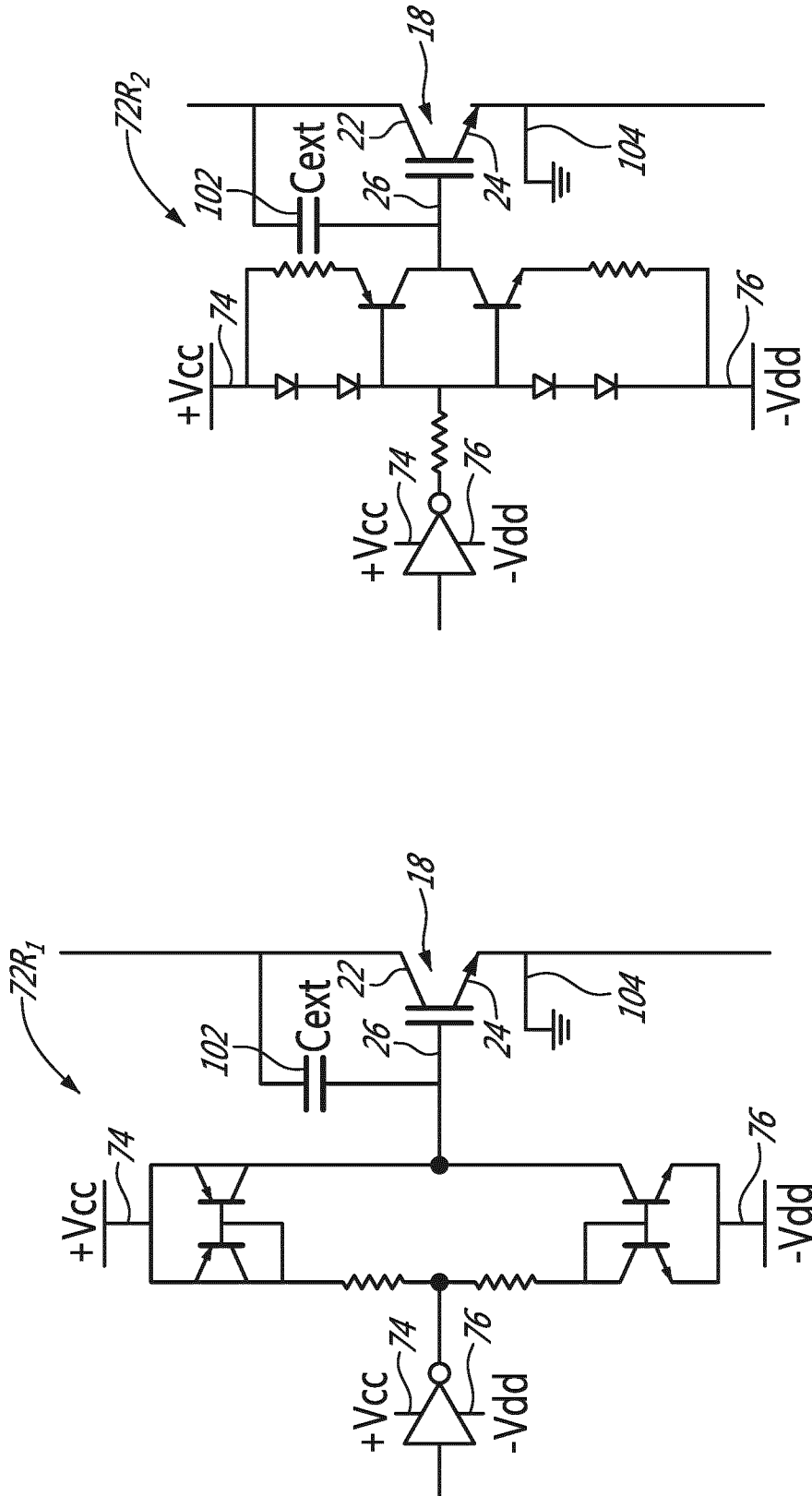


FIG - 7b

FIG - 7a

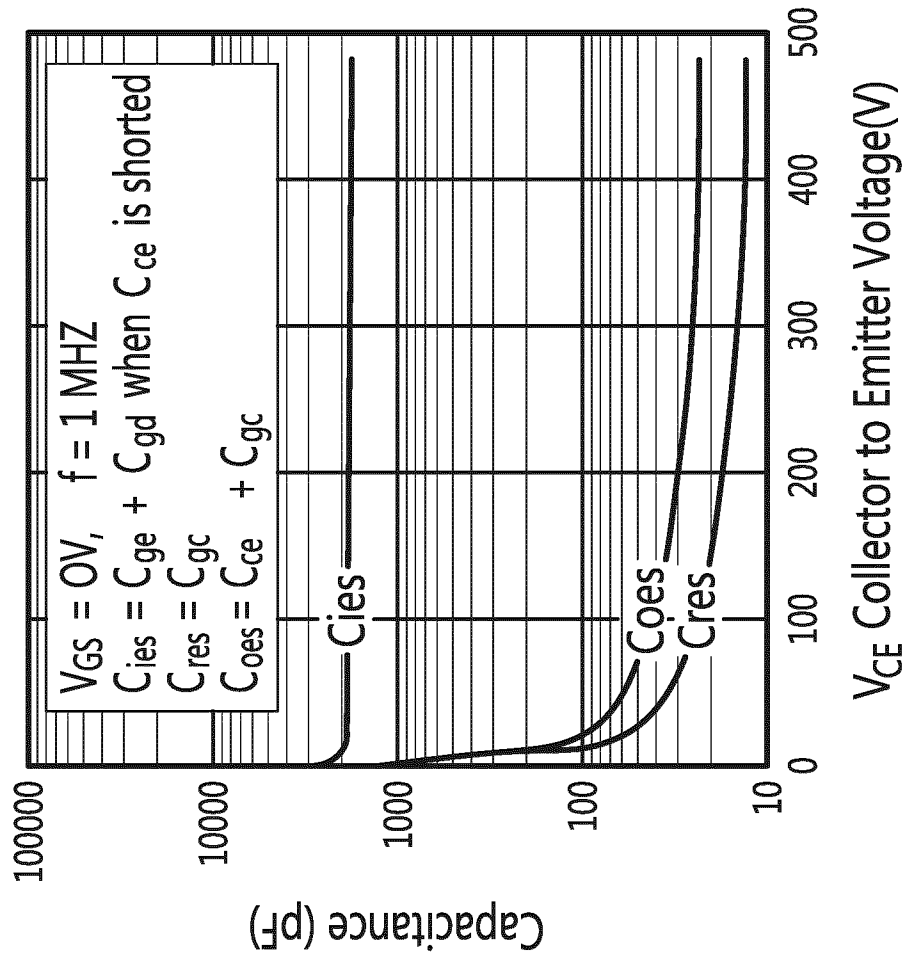


FIG. 8

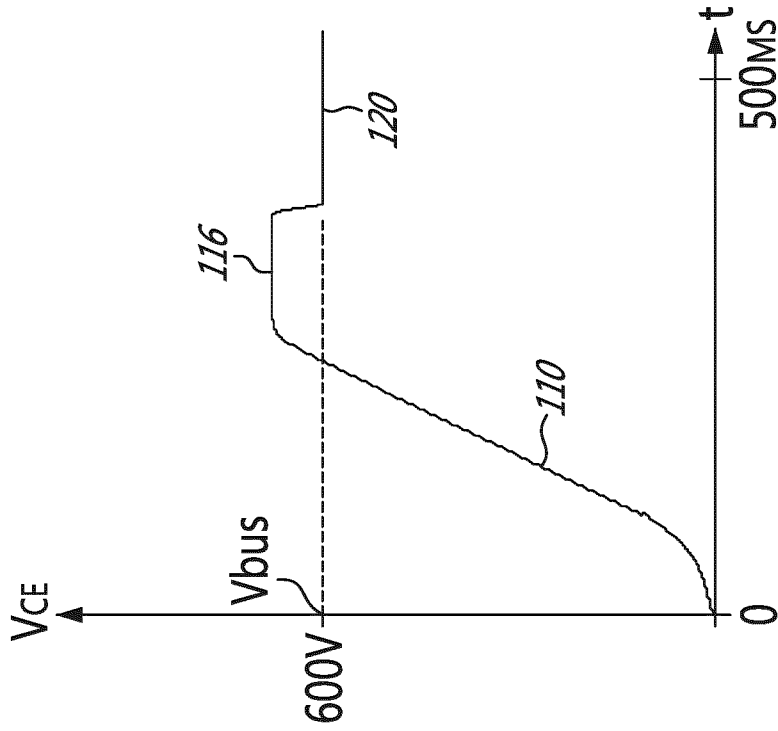


FIG. 10

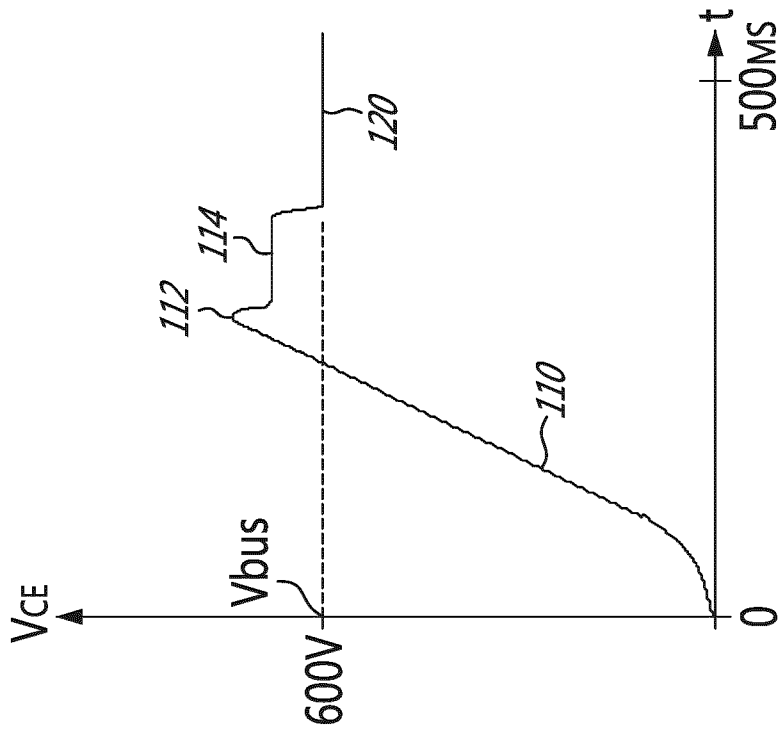


FIG. 9

## INTERNATIONAL SEARCH REPORT

International application No.  
**PCT/CA2015/050202**A. CLASSIFICATION OF SUBJECT MATTER  
IPC: **H02M 1/08** (2006.01), **H02M 3/155** (2006.01), **H02M 7/537** (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)  
IPC: **H02M 1/08** (2006.01), **H02M 3/155** (2006.01), **H02M 7/537** (2006.01)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic database(s) consulted during the international search (name of database(s) and, where practicable, search terms used)

**Databases searched:** Questel Orbit, USPTO, Esp@cenet, PatentScope®, IEEE Xplore® Digital Library, Canadian Patent Database.**Keywords:** gate, driver, switch, on/off, voltage, variation, collector, emitter, current, source, commutation, cell, parasitic, capacitance, leg, parallel, AC/DC and related terms.

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2012/0068683 (Liu et al.), 22 March 2012 (22-03-2012). Entire document.	1 to 21
A	Azeroual et al., "Limiting the Overshoot on IGBT During Turn-Off Using Stray Inductance", ATZ elektronik, May 2012, volume 7, pages 16 to 20. Entire document.	1 to 21

 Further documents are listed in the continuation of Box C. See patent family annex.

* Special categories of cited documents:	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A" document defining the general state of the art which is not considered to be of particular relevance	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E" earlier application or patent but published on or after the international filing date	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&" document member of the same patent family
"O" document referring to an oral disclosure, use, exhibition or other means	
"P" document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search  
04 June 2015 (04-06-2015)Date of mailing of the international search report  
10 June 2015 (10-06-2015)Name and mailing address of the ISA/CA  
Canadian Intellectual Property Office  
Place du Portage I, C114 - 1st Floor, Box PCT  
50 Victoria Street  
Gatineau, Quebec K1A 0C9  
Facsimile No.: 001-819-953-2476

Authorized officer

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**INTERNATIONAL SEARCH REPORT**  
Information on patent family members

International application No.  
**PCT/CA2015/050202**

<b>Patent Document Cited in Search Report</b>	<b>Publication Date</b>	<b>Patent Family Member(s)</b>	<b>Publication Date</b>
US2012068683A1	22 March 2012 (22-03-2012)	US2012068683A1 CA2714928A1	22 March 2012 (22-03-2012) 17 March 2012 (17-03-2012)

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