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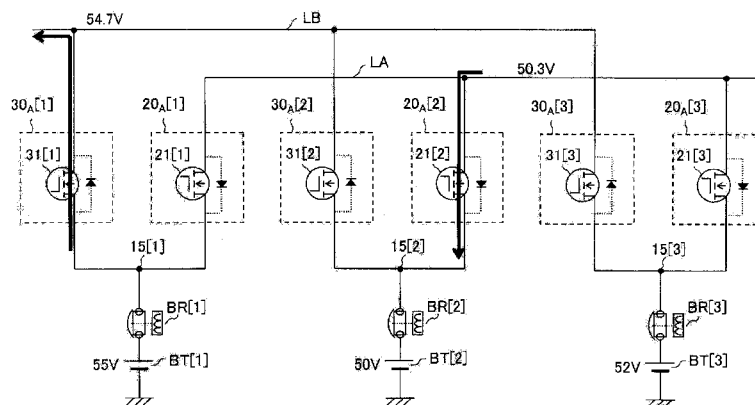
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[Continued on next page]

(54) Title: BATTERY PARALLEL-OPERATION CIRCUIT AND BATTERY SYSTEM

[Fig. 10]

FIG. 10



(57) **Abstract:** A first line electrically coupled to, in parallel to one another, a plurality of battery units that are electrically connectable to the battery parallel-operation circuit. The first line is configured to supply charging current to the plurality of battery units from a power source that is electrically connectable to the battery parallel-operation circuit. The first line connecting the plurality of battery units in parallel to one another comprises a plurality of charging backflow prevention circuits each configured to allow the charging current to flow from the first line to a corresponding one of the battery units but to prevent reverse current from flowing from the battery unit to the first line.

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Description

Title of Invention: BATTERY PARALLEL-OPERATION CIRCUIT AND BATTERY SYSTEM

Technical Field

[0001] The invention relates to a battery parallel-operation circuit used to connect plural battery units in parallel to one another. The invention also relates to a battery system using a battery parallel-operation circuit.

Background Art

[0002] JP2002-142353A discloses a system using parallel-connected plural battery units each of which includes one or more secondary batteries. Fig. 12 shows apparatus 900 using plural battery units connected in parallel to one another. In apparatus 900, battery units 901 to 903 are connected in parallel to one another. The output of battery units 901 to 903 drive load 910 in apparatus 900. Battery units 901 to 903 are charged by charging circuit 911 in apparatus 900.

[0003] The characteristics of the secondary batteries deteriorate with repeated charging and discharging. For this reason, in many cases, apparatus 900 using battery units 901 to 903 is configured so that each battery unit can be replaced. For instance, the user of apparatus 900 can change only battery unit 901 when necessary.

Summary of Invention

[0004] If battery units are not replaced at all, the battery units are substantially uniform in terms of their characteristics because all the battery units are charged and discharged equally. In contrast, if only battery unit 901 is removed from apparatus 900 and a new battery unit is attached in place of battery unit 901, the characteristics of the battery units in apparatus 900 may be non-uniform. For instance, a battery unit to be newly provided as battery unit 901 may possibly have a significantly greater open circuit voltage than battery units 902 and 903 that are not replaced with new ones. In this case, replacement of battery unit 901 with the new one may cause a relatively large current to flow from new battery unit 901 to battery units 902 and 903.

[0005] If battery units 901 to 903 are formed by using secondary batteries with relatively large internal resistances (e.g., lead-acid batteries), a large current that may deteriorate or damage the battery units is unlikely to flow even after the above-described battery-unit replacement. In contrast, if the battery units are formed by using secondary batteries with relatively small internal resistances (e.g., lithium-ion batteries and nickel-metal-hydride batteries), which are now studied actively, a large current is more likely to flow between the battery units and to deteriorate or damage the battery units after the above-described battery-unit replacement.

[0006] An aspect of the invention provides a battery parallel-operation circuit that comprises: a first line electrically coupled to, in parallel to one another, a plurality of battery units that are electrically connectable to the battery parallel-operation circuit, and configured to supply charging current to the plurality of battery units from a power source that is electrically connectable to the battery parallel-operation circuit, wherein the first line connecting the plurality of battery units in parallel to one another comprises a plurality of charging backflow prevention circuits each configured to allow the charging current to flow from the first line to a corresponding one of the battery units but to prevent reverse current from flowing from the battery unit to the first line.

[0007] Another aspect of the invention provides a battery system that comprises the battery parallel-operation circuit and a plurality of battery units.

Brief Description of Drawings

[0008] [fig.1]Fig. 1 is a schematic, overall circuit diagram illustrating a battery system according to an embodiment.

[fig.2]Fig. 2 is a diagram illustrating various examples of the internal configuration of a single battery unit.

[fig.3]Fig. 3 is a schematic diagram illustrating the configuration of an apparatus using the battery system.

[fig.4]Fig. 4 is a circuit diagram illustrating a battery parallel-connection circuit according to the first example.

[fig.5]Fig. 5 is a diagram illustrating an internal circuit and a peripheral circuit for each single driver circuit according to the first example.

[fig.6]Fig. 6 is a diagram illustrating regular charging operations in the battery parallel-connection circuit according to the first example.

[fig.7]Fig. 7 is a diagram illustrating non-uniformity charging operations in the battery parallel-connection circuit according to the first example.

[fig.8]Fig. 8 is a diagram illustrating regular discharging operations in the battery parallel-connection circuit according to the first example.

[fig.9]Fig. 9 is a diagram illustrating non-uniformity discharging operations in the battery parallel-connection circuit according to the first example.

[fig.10]Fig. 10 is a diagram illustrating non-uniformity charging and discharging operations in the battery parallel-connection circuit according to the first example.

[fig.11]Fig. 11 is a diagram illustrating a modification of the parallel-connected circuit according to the first example.

[fig.12]Fig. 12 is a diagram illustrating a parallel-connected circuit according to the second example.

[fig.13]Fig. 13 is a diagram illustrating a parallel-connected circuit according to the fourth example.

[fig.14]Fig. 14 is a diagram illustrating a parallel-connected circuit according to the fifth example.

[fig.15]Fig. 15 is a diagram illustrating operation of the parallel-connected circuit according to the fifth example

[fig.16]Fig. 16 is a diagram illustrating a modification of the parallel-connected circuit according to the fifth example.

[fig.17]Fig. 17 is a diagram related to a conventional technique and illustrating an apparatus using plural battery units.

[fig.18]Fig. 18 is a circuit diagram related to a sixth example and used in a simulation.

[fig.19]Fig. 19 is a table related to the sixth example and showing characteristics of a PTC thermistor used in the simulation.

[fig.20]Fig. 20 shows graphs related to the sixth example and describing the result of a first simulation.

[fig.21]Fig. 21 shows graphs related to the sixth example and describing the result of a second simulation.

Description of Embodiments

[0009] Embodiments of the invention are described by referring to the drawings. The same portions that appear in various drawings are denoted by the same reference numerals, and no redundant description of such portions is provided. The terms "wire" and "line" used in this specification refer to conductors with small enough resistances. Thus, the resistances of the wires and the lines are ignored. In contrast, the term "resistive element" refers to an element with significant resistance placed on a conductor. Before describing first to an eighth examples, description is provided for those things that are common to all the examples or that are referred to in the description of the examples.

[0010] Fig. 1 shows a circuit diagram illustrating schematically an overall battery system according to an embodiment. Controller 1 including an arithmetic processing unit and the like monitors the state of controlled unit 2, and controls the operations of various portions of controlled unit 2. Controlled unit 2 includes switch unit 3, power converter circuit 4, plural battery units, and plural breakers corresponding respectively to plural battery units. Switch unit 3 includes parallel-connected circuit 5 and switching elements 6 to 8. Controlled unit 2 is electrically coupled to solar cell 9, diode 10, power-supply circuit (source of AC voltage in this embodiment) 11, and load 12. Those diodes used in this embodiment are, for instance, PN-junction-type diodes, but diodes of other types may be used instead.

[0011] The plural battery units provided in controlled unit 2 are electrically coupled to

parallel-connected circuit 5 via plural breakers respectively. The plural battery units are electrically coupled in parallel to one another via parallel-connected circuit 5. Two or more battery units are to be electrically coupled in parallel to one another via parallel-connected circuit 5. That is, two, three, four, five, six, or more battery units are to be connected in that way. In this embodiment, three battery units are connected in that way unless mentioned otherwise, and the three battery units are denoted by reference numerals BT[1] to BT[3]. The breaker corresponding to battery unit BT[i] is denoted by reference numeral BR[i]. The letter i in those reference numerals represents an integer.

[0012] All the battery units BT[1] to BT[3] used in this embodiment may have identical structures, so the description of only battery unit BT[1] is provided as a representative example. Battery unit BT[1] includes one or more secondary batteries each of which may have a quite small internal resistance. If battery unit BT[1] includes plural secondary batteries, the plural secondary batteries may form any of the following circuits: a series-connected circuit of the second batteries such as one shown in Fig. 2A; a parallel-connected circuit of the second batteries such as one shown in Fig. 2B; and a combination circuit including both series-connected and parallel-connected circuits such as one shown in Fig. 2C. The secondary batteries may include rechargeable batteries. Lithium-ion batteries and nickel-metal-hydrate batteries are examples of the secondary batteries having a quite small internal resistance. Battery unit BT[1] has a negative output terminal and a positive output terminal, and outputs a positive voltage from the positive output terminal with the potential of the negative output terminal used as a reference. Voltage mentioned in this embodiment is a voltage based on the potential at a reference potential point. In the drawings of this embodiment, each battery unit is schematically shown as a single battery. However, each battery unit may include series-connected plural batteries, parallel-connected plural batteries, or a combination of both.

[0013] The positive output terminal of battery unit BT[i] is electrically coupled to branch point 15[i] via breaker BR[i]. Branch point 15[i] is electrically coupled to main line L1 via switching element 30[i] (i is 1, 2, or 3 in this embodiment). One switching element 30[i] is provided for each battery unit, and is coupled in series between the corresponding battery unit and main line L1. Branch point 15[i] is electrically coupled to sub-line L2 via resistive element 20[i] (i is 1, 2, or 3 in this embodiment). One resistive element 20[i] is provided for each battery unit, and is connected in series between the corresponding battery unit and sub-line L2. Hence, battery units BT[1] to BT[3] are electrically coupled in parallel to one another via main line L1, and are electrically coupled in parallel to one another via sub-line L2 as well. Note that resistive elements 20[1] to 20[3] used in this embodiment are identical to one another and switching

elements 30[1] to 30[3] are identical to one another.

- [0014] Charging line LA is a line through which either the charging current from solar cell 9 or the charging current from power converter circuit 4 flows. Battery unit BT[i] is charged by the charging current flowing into battery unit BT[i] through charging line LA. Discharging line LB is a line through which the electric current supplied from battery unit BT[i] to load 12 (i.e., the discharging current of battery unit BT[i]) flows. Note that the charging of battery unit BT[i] means the charging of the secondary battery included in battery unit BT[i], and the discharging of battery unit BT[i] means the discharging of the secondary battery included in battery unit BT[i].
- [0015] Charging line LA is connected to the output terminal of power converter circuit 4 via switching elements 6 and 7, and is also connected to the cathode of diode 10 via switching element 6. Discharging line LB is connected to load 12 via switching element 8. Any semiconductor switches or mechanical switches may be used as the switching elements in the battery system. In this embodiment, n-channel-type metal-oxide-semiconductor field-effect transistors (MOSFETs)-a kind of field-effect transistor-are used as the switching elements in the battery system and n-channel-type MOSFETs used as the switching elements in the battery system are expressed as FETs.
- [0016] The state of electrical continuity in FETs in switch unit 3 is controlled by controller 1. A parasitic diode is provided to each FET. This can be interpreted as either that each FET has a built-in parasitic diode, or that the parasitic diode is a circuit element electrically coupled in parallel to the FET. The parasitic diode of FET 6 is connected in parallel to FET 6 with the forward direction of the parasitic diode set in the direction from the source to drain of FET 6.
- [0017] The connection point of each of charging backflow prevention circuit 20[1] to 20[3] (hereinafter also referred simply to circuits 20[1] to 20[3]) and the charging line LA is connected to the source of FET 6 via charging line LA. The drains of FETs 6 and 7 are connected to each other at connection point 16. The source of FET 7 is connected to the output terminal of the power converter circuit 4. FET 7 is provided to prevent backflow electric current from connection point 16 toward power converter circuit 4. Without FET 7, an overcurrent caused by the output of solar cell 9 is sometimes applied to power converter circuit 4, and damages power converter circuit 4. Providing FET 7 can prevent such overcurrent applied to power converter circuit 4 from damaging power converter circuit 4. In addition, providing of FET 7 is expected to have an effect to reduce power consumption in power converter circuit 4. Connection point 16 is connected to the cathode of diode 10, and the anode of diode 10 is connected to the output terminal of solar cell 9.
- [0018] Under the control of controller 1, power converter circuit 4 converts the AC electric power supplied by AC voltage source 11 to DC electric power. Power converter circuit

4 outputs the DC voltage and DC current thus obtained out through its output terminal. Solar cell 9 converts light such as sunlight to DC electric power, and outputs the DC voltage and DC current thus obtained out through its output terminal.

[0019] If battery unit BT[i] needs charging, controller 1 turns on both FETs 6 and 7. Thus, either the output current of solar cell 9 or the output current of power converter circuit 4 is supplied to charging line LA as the charging current for battery unit BT[i]. Alternatively, controller 1 may turn on only FET 6 of the above-mentioned two FETs 6 and 7, and thus supplies the output current of solar cell 9 to charging line LA as the charging current for battery unit BT[i]. The following description assumes that if battery unit BT[i] needs charging, both FETs 6 and 7 are turned on unless mentioned otherwise. It is, however, not essential to turn FET 7 on. Similar actions to those caused by turning on only FET 6 of two FETs 6 and 7 can be caused by turning on both FETs 6 and 7. The turning on of only FET 6, however, increases power consumption. Accordingly, if battery unit BT[i] needs charging, it is desirable to turn on both of FETs 6 and 7. Both the open circuit voltage of solar cell 9 and that of power converter circuit 4 are assumed to be larger than the output voltages of battery units BT[1] to BT[3]. For the sake of descriptive simplicity, the internal resistance of each of battery units BT[1] to BT[3] is assumed to be zero unless it is necessary to assume otherwise. If controller 1 judges that the charging of battery unit BT[i] is not necessary, or if controller 1 judges that it is necessary to prohibit the charging of battery unit BT[i], controller 1 turns off FETs 6 and 7. For instance, if battery unit BT[i] is in an abnormal state (including the event of overcurrent), the charging of battery unit BT[i] is prohibited.

[0020] Solar cell 9 forms a first electric-power source whereas both source of AC voltage 11 and power converter circuit 4 together form a second electric-power source. Nevertheless, any of the two electric-power sources may be omitted.

[0021] The connection point of each of discharging backflow prevention circuits 30[1] to 30[3] (hereinafter also referred simply to circuits 30[1] to 30[3]) and the discharging line LB is connected to the drain of FET 8 via discharging line LB. The source of FET 8 is connected to load 12.

[0022] If battery unit BT[i] needs discharging, or, to put it differently, if it is necessary to supply electric power to load 12, controller 1 turns on FET 8. Thus the discharging current of battery unit BT[i] is supplied to load 12 either through main line L1 or through sub-line L2. If controller 1 judges that the discharging of battery unit BT[i] is not necessary, or if controller 1 judges that it is necessary to prohibit the discharging of battery unit BT[i], controller 1 turns off FET 8. For instance, if battery unit BT[i] is in an abnormal state (including the event of overcurrent), or if an excessively large current passes through FET 8, the discharging of battery unit BT[i] is prohibited.

- [0023] Controller 1 is capable of controlling the continuity of each of FETs 6 to 8 in accordance with the output voltages of battery units BT[1] to BT[3]. Controller 1 is capable of detecting the output voltage of battery unit BT[i] either periodically or at any timing by use of, for instance, voltage-detection sensors S[i].
- [0024] Voltage-detection sensors S[1] to S[3] output output-voltage information of battery units BT[1] to BT[3]. The output-voltage information mentioned above includes not only the information on the output voltages but also the broader information that can be used to specify the output voltages. Controller 1 receives the output-voltage information. Controller 1 may receive the output-voltage information directly from voltage-detection sensors S[1] to S[3]. Alternatively, a third apparatus may be provided to receive the output-voltage information of battery units BT[1] to BT[3]. Then, the third apparatus processes the data, and then sends the processed data to controller 1.
- [0025] Breaker BR[i] is a mechanical relay or the like that is connected in series between battery unit BT[i] and branch point 15[i]. Breaker BR[i] is capable of cutting the electrical connection between battery units BT[i] and branch point 15[i] when necessary. For instance, breaker BR[i] cuts the electrical connection between battery unit BT[i] and branch point 15[i] if either the charging current or the discharging current for battery unit BT[i] is abnormally large, or if any abnormal signal is sent from battery unit BT[i], or if a predetermined signal to cut the connection is sent from controller 1.
- [0026] Both controller 1 and controlled unit 2 may be considered as constituent elements of the battery system shown in Fig. 1. As Fig. 3 shows, battery system BS as the battery system shown in Fig. 1 may be built into apparatus AP that includes load 12. Apparatus AP is any apparatus driven by the output power of the secondary batteries in the battery system BS. Some examples of apparatus AP are electrically-driven vehicles, power tools, PCs, mobile phones, and PDAs.
- [0027] Battery units BT[1] to BT[3] are attachable to or detachable from apparatus AP independently of each other. Each battery unit can be changed from to a new one. To put it differently, the user of apparatus AP can remove, from apparatus AP, battery unit BT[1] that is currently set in apparatus AP, and attach another battery unit in apparatus AP as a new battery unit BT[1] (battery units BT[2] and BT[3] can be treated similarly). Once battery unit BT[1] is removed from apparatus AP, the electrical connection between battery unit BT[1] and battery system BS is cut off completely. If, however, another battery unit is attached to apparatus AP as a new battery unit BT[1], electrical connection is formed between the new battery unit BT[1] and battery system BS (the same happens in the cases of battery units BT[2] and BT[3]). The series of operations to remove battery unit BT[i] from apparatus AP and attach a new battery unit

in apparatus AP as a new battery unit BT[i] is referred to as battery-unit replacement.

[0028] If no battery-unit replacement occurs, battery units BT[1] to BT[3] are charged and discharged uniformly, so that the output voltages of battery units BT[1] to BT[3] are spontaneously equalized through the processes of charging and discharging. Conversely, if battery-unit replacement occurs, the output voltages of battery units BT[1] to BT[3] sometimes become different from one another. For instance, after battery-unit replacement, the output voltages of battery units BT[1] to BT[3] may be 55 V, 50 V, and 50 V respectively. Note that the expressions 55 V and 50 V mean 55 volts and 50 volts respectively (the same applies to 49 V and the like described later). In this case, if the positive output terminals of battery units BT[1] to BT[3] are directly connected to one another, an excessively large current flows from battery unit BT[1] to both battery units BT[2] and BT[3], and the large current may cause depreciation or damage of the battery units.

[0029] Circuit 20[i] is connected in series on the line connecting charging line LA to branch point 15[i]. Circuit 20[i] allows the charging current to flow from charging line LA to battery unit BT[i], but prevents the reverse current from flowing from battery unit BT[i] to charging line LA. Circuit 30[i] is connected in series on the line connecting discharging line LB to branch point 15[i]. Circuit 30[i] allows the discharging current to flow from battery unit BT[i] to discharging line LB, but prevents the reverse current from flowing from discharging line LB to battery unit BT[i]. Examples of the internal configurations of circuits 20[i] and 30[i] are described in detail later. In the following description, for the sake of descriptive convenience, FETs 6 and 7 are also referred to as charger FETs 6 and 7 whereas FET 8 is also referred to as discharger FET 8.

[0030] Specific examples of the configuration and the system based on the above-described configuration are described below as first to sixth examples.

Example 1

[0031] A first example is described. Fig. 4 illustrates the internal circuit of parallel-connection circuit 5 according to the first example. Circuit 20[i] and circuit 30[i] shown in Fig. 1 are referred to respectively as circuit 20A[i] and circuit 30A[i] in the first example.

[0032] The configurations of circuits 20A[1] to 20A[3] are identical to one another whereas the configurations of circuits 30A[1] to 30A[3] are identical to one another. Circuit 20A[i] includes FET 21[i], which is the same switching element as charger FET 6. Circuit 30B[i] includes FET 31[i], which is the same switching element as charger FET 6. Accordingly, as in the case of FET 6, a parasitic diode is provided to FET 21[i]. The parasitic diode of FET 21[i] is connected in parallel to FET 21[i] with the forward direction of the parasitic diode set in the direction from the source to the drain of FET

21[i]. Likewise, a parasitic diode is also provided to FET 31[i]. The parasitic diode of FET 31[i] is connected in parallel to FET 31[i] with the forward direction of the parasitic diode set in the direction from the source to the drain of FET 31[i]. If the parasitic diode is considered as a circuit element connected in parallel to each FET as described above, FET 21[i] and the parasitic diode of FET 21[i] together form a parallel circuit. Likewise, FET 31[i] and the parasitic diode of FET 31[i] together form a parallel circuit.

[0033] The drain of FET 21[i] is connected to the corresponding branch point 15[i] whereas the source of each FET 21[i] is connected to charging line LA. Accordingly, while both charger FETs 6 and 7 are on, turning on FET 21[i] makes FET 21[i] form a current path for the charging current from charging line LA to the corresponding battery unit BT[i]. Note that even if FET 21[i] is off, a current path for the charging current from charging line LA to battery units BT[i] is secured by the existence of the parasitic diode of FET 21[i]. The source of FET 31[i] is connected to branch point 15[i] whereas the drain of FET 31[i] is connected to discharging line LB. Accordingly, while discharger FET 8 is on, turning on FET 31[i] makes FET 31[i] form a current path for the discharging current from the corresponding battery unit BT[i] to discharging line LB. Note that even if each FET 31[i] is off, a current path for the discharging current from the corresponding battery unit BT[i] to discharging line LB is secured by the existence of the parasitic diode of FET 31[i].

[0034] Charging backflow prevention circuit 20A[i] is provided with a driver circuit (charging driver circuit) configured to control the turning on/off of FET 21[i]. Likewise, discharging backflow prevention circuit 30A[i] is provided with a driver circuit (discharging driver circuit) to control the turning on/off of FET 31[i]. Fig. 5 illustrates an internal circuit and a peripheral circuit for each single driver circuit. In Fig. 5, FET 40 is either the FET in a charging backflow prevention circuit or the FET in a discharging backflow prevention circuit. To put it differently, if driver circuit 50 shown in Fig. 5 is the driver circuit in circuit 20A[i], FET 40 is FET 21[i]. Conversely, if driver circuit 50 shown in Fig. 5 is the driver circuit in circuit 30A[i], FET 40 is FET 31[i].

[0035] The source of FET 40 is connected to connection point 41 whereas the drain of FET 40 is connected to connection point 42. If driver circuit 50 shown in Fig. 5 is the driver circuit in circuit 20A[i], connection point 41 is connected to charging line LA, and connection point 42 is connected to branch point 15[i]. If driver circuit 50 shown in Fig. 5 is the driver circuit in circuit 30A[i], connection point 41 is connected to branch point 15[i], and connection point 42 is connected to discharging line LB.

[0036] Driver circuit 50 includes: transistor 51, which is an n-type bipolar transistor; diode 52; and resistive elements 53 to 56. The emitter of transistor 51 is connected to

connection point 41, and the base thereof is connected to the anode of diode 52 via resistive element 53. In addition, collector transistor 51 is connected to the gate of FET 40 via resistive element 54, and is also connected to the anode of diode 52 via resistive elements 55 and 56 in this order. The cathode of diode 52 is connected to connection point 42.

[0037] The voltages of connection points 41 and 42 are denoted by V_i and V_o respectively. The gate voltage, the source voltage, and the drain voltage of FET 40 are denoted by V_G , V_S , and V_D respectively. The base voltage, the emitter voltage, and the collector voltage of transistor 51 are denoted by V_B , V_E , and V_C respectively. The forward voltage drop of diode 52 is denoted by V_f . The value of V_f is 0.7 V approximately. So, in the following description, the value of V_f is assumed to be 0.7 V. To turn on transistor 51, a voltage that is higher than the emitter voltage of transistor 51 by an amount of voltage V_{BEO} , i.e., a voltage ($V_i + V_{BEO}$), needs to be applied to the base of transistor 51. Voltage V_{BEO} is 0.7 V approximately. So, in the following description, voltage V_{BEO} is assumed to be 0.7 V. Note that voltage V_1 is the voltage of a connection point between resistive elements 53 and 56, and is equal to the voltage of the anode of diode 52. In addition, voltage V_x is the voltage of the connection point between resistive elements 55 and 56. Either controller 1 or controlled unit 2 always applies a voltage ($V_i + V_{UP}$), that is, a voltage that is higher than voltage V_i by an amount V_{UP} , to the connection point between resistive elements 55 and 56. To this end, a constant-voltage generating circuit (not illustrated) or the like is used. V_{UP} is a positive voltage, and is assumed to be 12 V in the following description.

[0038] Driver circuit 50 is configured to turn off FET 40 while transistor 51 is on, and to turn on FET 40 while transistor 51 is off.

[0039] To be more specific, while transistor 51 is on, collector voltage V_C of transistor 51 is approximately equal to the voltage of connection point 41 V_i (strictly, collector voltage V_C is slightly higher than voltage V_i). In the meanwhile, $V_C = V_G$ and $V_i = V_S$. Hence, FET 40 is turned off for $V_C = V_G$ approximately = $V_i = V_S$ (note that the leakage current of the gate is assumed to be zero.) To put it differently, FET 40 has a characteristic such that if transistor 51 is on and the equation " V_C approximately = V_G approximately = $V_i = V_S$ " holds true, continuity is not provided between the source and the drain.

[0040] Conversely, if transistor 51 is off, the equation " $V_C = V_x = V_i + V_{UP}$ " holds true (note that while transistor 51 is off, the collector current is assumed to be zero). In the meanwhile, $V_C = V_G$ and $V_i = V_S$. Hence, FET 40 is turned on for " $V_C = V_G = V_i + V_{UP} > V_i = V_S$ ". To put it differently, FET 40 has a characteristic such that if transistor 51 is turned off and the equation " $V_C = V_G = V_i + V_{UP} > V_i = V_S$ " holds true, continuity is provided between the source and the drain.

- [0041] When a reverse voltage is applied to FET 40, that is, if voltage V_o of connection point 42 is lower than voltage V_i of connection point 41, the circuit operates in the following way. Since the equation " $V_x = V_i + V_{UP}$ " holds true and voltage V_o is lower than the voltage V_i , a current path is formed to allow the current to flow from the connection point between resistive elements 55 and 56 to connection point 42 via resistive element 56 and diode 52, and thus diode 52 is turned on. Consequently, base voltage V_B drops. If diode 52 is on, the equation " $V_1 = V_o + V_f = V_o + 0.7 \text{ V}$ " holds true. Hence, since the voltage V_o is lower than the voltage V_i , the voltage " $V_i + V_{BEO} = V_i + 0.7 \text{ V}$ " that is needed to turn on transistor 51 is not applied to the base of transistor 51, and thus transistor 51 is turned off. Consequently, the potential of the collector of transistor 51 rises, and thus FET 40 is turned on.
- [0042] The following provides an alternative description of the above-described operations. Whether diode 52 is turned on or off depends on the value of voltage V_1 of a connection point between resistive elements 53 and 56. The threshold for voltage V_1 is " $V_o + V_f = V_o + 0.7 \text{ V}$." Whether transistor 51 is turned on or off depends on the value of base voltage V_B of transistor 51. The threshold for base voltage V_B is " $V_i + V_{BEO} = V_i + 0.7 \text{ V}$." If the voltage drop at resistive element 53 is slight, voltage V_1 is almost equal to base voltage V_B . Hence, if voltage V_o is lower than voltage V_i , electric current is drawn in from the connection point between resistive elements 53 and 56 to the side of diode 52. Consequently, as described above, diode 52 is turned on and transistor 51 is turned off. Conversely, if a forward-direction voltage is applied to FET 40, that is, if voltage V_o is higher than voltage V_i , electric current is drawn in from the connection point between resistive elements 53 and 56 to the base side of transistor 51. Consequently, diode 52 is turned off and transistor 51 is turned on. When transistor 51 is turned on, collector voltage V_c of transistor 51 is almost equal to voltage V_i . Consequently, FET 40 is turned off.
- [0043] Note that if voltage V_o is higher than voltage V_i but the difference between these voltages (i.e., $V_o - V_i$) is relatively small, the circuit may perform an intermediate operation between the circuit operations at the time when " $V_o < V_i$ " and the circuit operations at the time when " $V_o > V_i$." In this case, the state of FET 40 may be an intermediate state between the ON state and the OFF state.
- [0044] As has been described thus far, driver circuit 50 in each charging backflow prevention circuit 20A[i] operates in the following way. If the voltage of charging line LA is higher than the output voltage of the corresponding battery unit BT[i], driver circuit 50 turns on FET 21[i]. Conversely, if the voltage of charging line LA is lower than the output voltage of the corresponding battery unit BT[i], driver circuit 50 turns off FET 21[i]. If FET 21[i] is off, the function of the parasitic diode of FET 21[i] makes circuit 20A[i] function as a simple rectifier diode. Driver circuit 50 in dis-

charging backflow prevention circuit 30A[i] operates in a similar way. If the voltage of discharging line LB is lower than the output voltage of battery unit BT[i], driver circuit 50 turns on FET 31[i]. Conversely, if the voltage of discharging line LB is higher than the output voltage of battery unit BT[i], driver circuit 50 turns off FET 31[i]. If FET 31[i] is turned off, the function of the parasitic diode of FET 31[i] makes circuit 30A[i] function as a simple rectifier diode.

- [0045] Note that as long as the operations described above can be implemented, various modifications may be made in the circuit configuration of driver circuit 50 as a matter of course. In addition, the voltage of charging line LA means the potential of charging line LA. Likewise the voltage of discharging line LB means the potential of discharging line LB. The output voltage of battery unit BT[i] means the potential of the positive output terminal of battery unit BT[i].
- [0046] With the existence of circuit 20A[i] each including driver circuit 50, the following normal charging operations are performed. The normal charging operations are to charge battery unit BT[i] and are performed when the output voltages of battery units BT[1] to BT[3] are uniform (i.e., exactly or substantially the same).
- [0047] Suppose a case where the output voltages of all battery units BT[1] to BT[3] are 50 V as shown in Fig. 6. The charging operations to be performed under these conditions, for instance, are the above-mentioned normal charging operations. If, under the conditions, charger FETs 6 and 7 are turned on, a voltage that is higher than the output voltages of battery units BT[1] to BT[3] is applied to charging line LA because both the open circuit voltage of solar cell 9 and the open circuit voltage of power converter circuit 4 are equal to or higher than the output voltages of battery units BT[1] to BT[3] as described earlier. Consequently, as shown in Fig. 6, driver circuits 50 of circuits 20A[1] to 20A[3] turn on their respective FETs 21[1] to 21[3], and the charging current flows through FETs 21[1] to 21[3] into battery units BT[1] to BT[3] respectively. The charging current for battery unit BT[i] is supplied to battery unit BT[i] through FET 21[i] as described above, so that the loss at circuit 20A[i] is reduced from the case where the charging current is supplied to battery unit BT[i] through a diode.
- [0048] With the existence of circuit 20A[i] including driver circuit 50, the following non-uniform charging operations are performed. The non-uniform charging operations are to charge battery unit BT[i] and are performed when the output voltages of battery units BT[1] to BT[3] are non-uniform. There is hardly any clear distinction between the normal charging operations and the non-uniform charging operations, but the following description of the non-uniform charging operations is given on the assumption that there is a sufficiently large degree of non-uniformity.
- [0049] For instance, suppose a case where, as Fig. 7 shows, the output voltages of battery units BT[1] to BT[3] are 55 V, 50 V, and 52 V respectively due to battery-unit re-

placement or the like. The charging operations performed under these conditions are non-uniform charging operations. If, under the conditions, charger FETs 6 and 7 are turned on, charging line LA has a potential that depends on the lowest one of the output voltages of battery units BT[1] to BT[3]. As described earlier, both the open circuit voltage of solar cell 9 and the open circuit voltage of power converter circuit 4 are higher than the output voltages of battery units BT[1] to BT[3], so that FET 21[2] is turned on, and charging line LA has a potential equal to the sum of the output voltage of battery unit BT[2] and the voltage drop at FET 21[2]. In the case shown in Fig. 7, charging line LA has a potential of 50.3 V. Hence, both of FETs 21[1] and 21[3] are turned off, so that the charging current supplied from solar cell 9 or the like flows only into battery unit BT[2] through FET 21[2]. In addition, the functions of circuits 20A[1] and 20A[3] as simple diodes at this time prevent both the generation of electric current from battery units BT[1] and BT[3] to battery units BT[2] and the generation of electric current from battery unit BT[1] to battery unit BT[3].

[0050] Suppose a case where the charging of battery unit BT[2] progresses from the starting point shown in Fig. 7 until the output voltage of battery unit BT[2] reaches 52 V. At this time, FET 21[1] is still off, while not only FET 21[2] but also FET 21[3] is turned on. Hence, the charging current supplied from solar cell 9 or the like flows into battery units BT[2] and BT[3] through FETs 21[2] and 21[3] respectively. Eventually, the output voltages of all the battery units BT[1] to BT[3] become uniform, and, from then on, normal charging operations are performed.

[0051] With the existence of circuit 30A[i] including driver circuit 50, "normal discharging operations" are performed. Normal discharging operations are to discharge battery unit BT[i] and are to be performed when the output voltages of battery units BT[1] to BT[3] are uniform. Note that the voltage of the source side of FET 8-the side that the electric current is drawn in-is lower than the output voltage of battery unit BT[i].

[0052] Suppose a case where the output voltages of all the battery units BT[1] to BT[3] are 55 V as shown in Fig. 8 for example. The discharging operations performed under these conditions are normal discharging operations. If, under the conditions, discharger FET 8 is turned on, a voltage that is lower than the output voltages of battery units BT[1] to BT[3] is applied to discharging line LB. Hence, as shown in Fig. 8, driver circuits 50 of circuit 30A[1] to 30A[3] turn on their respective FETs 31[1] to 31[3], and thus the discharging current from battery units BT[1] to BT[3] are supplied to load 12 respectively through FETs 31[1] to 31[3] and discharger FET 8. The discharging current to load 12 is supplied through FET 31[i] to load 12 in the above-described way, so that the loss at circuit 30A[i] is reduced from the case where the discharging current is supplied through diodes.

[0053] With the existence of circuit 30A[i] including driver circuit 50, non-uniform dis-

charging operations are performed. The non-uniform discharging operations are to charge battery unit BT[i] and are performed when the output voltages of battery units BT[1] to BT[3] are non-uniform. There is hardly any clear distinction between the normal discharging operations and the non-uniform discharging operations, but the following description of the non-uniform discharging operations is given on the assumption that there is a sufficiently large degree of non-uniformity.

[0054] For instance, suppose a case where, as Fig. 9 shows, the output voltages of battery units BT[1] to BT[3] are 55 V, 50 V, and 52 V respectively due to battery-unit replacement or the like. The charging operations performed under these conditions are non-uniform charging operations. If, under the conditions, charger FET 8 is turned on, charging line LB has a potential that depends on the lowest one of the output voltages of battery units BT[1] to BT[3]. Specifically, FET 31[1] is turned on, and charging line LB has a potential equal to the difference between the output voltage of battery unit BT[1] and the voltage drop at FET 31[1]. In the case shown in Fig. 9, charging line LB has a potential of 54.7 V. Hence, both of FETs 31[2] and 31[3] are turned off, so that the discharging current from battery unit BT[1] is supplied to load 12 through FET 31[1] and discharger FET 8. In addition, the functions of circuits 30A[2] and 30A[3] as simple diodes at this time prevent both the generation of electric current flowing from battery units BT[1] and BT[3] to battery units BT[2] and the generation of electric current flowing from battery unit BT[1] to battery unit BT[3].

[0055] Suppose a case where the charging of battery unit BT[1] progresses from the starting point shown in Fig. 9 until the output voltage of battery unit BT[1] reaches 52 V. At this time, FET 31[2] is still off, while not only FET 31[1] but also FET 31[3] is turned on. Hence, the discharging current from battery units BT[1] and BT[3] are supplied to load 12 through FETs 31[1] and 31[3] respectively, and through discharger FET 8. Eventually, the output voltages of all the battery units BT[1] to BT[3] become uniform, and, from then on, normal discharging operations are performed.

[0056] Controller 1 is capable of turning on charger FETs 6 and 7 together with discharger FET 8 to perform simultaneously both the charging of any of battery units BT[1] to BT[3] and the discharging of any of battery units BT[1] to BT[3]. If, for instance, the output voltages of battery units BT[1] to BT[3] are 55 V, 50 V, and 52 V respectively as Fig. 10 shows, turning on FETs 6 to 8 together triggers the simultaneous execution of both the non-uniform charging operations corresponding to Fig. 7 and the non-uniform discharging operations corresponding to Fig. 9. Specifically, by turning on only FETs 21[2] and 31[1] of all the FETs 21[1] to 21[3] and 31[1] to 31[3], the charging current from solar cell 9 or the like flows into battery unit BT[2] through FET 21[2] and the discharging current only from battery unit BT[1] is supplied to load 12 through FET 31[1].

[0057] As has been described thus far, according to the first example, even if the output voltages of battery units BT[1] to BT[3] become non-uniform due to battery-unit replacement or the like, the rectifying functions of circuits 20A[i] and 30A[i] prevent excessively large electric current from flowing between battery units. Note that both the charging current from solar cell 9 or the like and the discharging current to load 12 flow through FETs included in circuits 20A[i] and 30A[i], so that the loss can be reduced from the case where simple diodes are used. In addition, when the output voltages become non-uniform, the functions of circuits 20A[i] and 30A[i] each including driver circuit 50 preferentially charge the battery units with lower output voltages and preferentially discharge the battery units with higher output voltages. Consequently, even without any special control performed by the controller system, the non-uniform output voltages caused by the battery-unit replacement or the like can be corrected automatically in the processes of the charging of or the discharging of the battery units.

[0058] Note that, as Fig. 11 shows, besides the parasitic diode, diode 23[1] with the forward direction set to be from the source to the drain of FET 21[1] may be connected in parallel to FET 21[1]. In addition, besides the parasitic diode, diode 33[1] with the forward direction set to be from the source to the drain of FET 31[1] may be connected in parallel to FET 31[1]. The same applies to FETs 21[2], 21[3], 31[2], and 31[3]. The same also applies to the second and the third examples to be described below.

Example 2

[0059] A second example is described. Fig. 12 illustrates the internal circuit of parallel-connection circuit 5 according to the second example. Circuit 20[i] and circuit 30[i] shown in Fig. 1 are referred to respectively as circuit 20B[i] and circuit 30B[i] in the second example.

[0060] Circuit 20B[i] is formed by omitting driver circuit 50 (see Fig. 5) from circuit 20A[i] described in the first example. Likewise, circuit 30B[i] is formed by omitting driver circuit 50 (see Fig. 5) from circuit 30A[i] described in the first example. Circuit 20B[i] has basically the same configuration as that of circuit 20A[i] except that no driver circuit 50 is provided whereas circuit 30B[i] has basically the same configuration as that of circuit 30A[i] except that no driver circuit 50 is provided. The elements and lines in controlled unit 2 are connected to one another in the second example in a similar manner to the one described in the first example.

[0061] In the second example, unillustrated voltage-detection sensors detect the output voltages of battery units BT[1] to BT[3]. On the basis of the detection results, controller 1 controls the continuity of each of FETs 21[1] to 21[3] included respectively in circuits 20B[1] to 20B[3] and the continuity of each of FETs 31[1] to

31[3] included respectively in circuits 30B[1] to 30B[3]. For instance, controller 1 may control the continuity of each of FETs 21[i] and 31[i] so that the continuity of FETs 21[i] and 31[i] in the second example are the same as those in the first example irrespective of whether controller 1 performs the control in the normal charging operations, the non-uniform charging operations, the normal discharging operations, or the non-uniform discharging operations (see Figs. 6 to 10).

[0062] More detailed description is provided of the controlling method performed by controller 1. In the following description, $V[i]$ means the output voltage of battery unit BT[i] detected by voltage-detection sensor S[i]. Voltage-detection sensor detects output voltages $V[1]$ to $V[3]$. Here, the detection errors are ignored. Controller 1 identifies maximum voltage V_{MAX} and minimum voltage V_{MIN} of output voltages $V[1]$ to $V[3]$, and calculates the voltage difference ($V_{MAX} - V_{MIN}$). The voltage difference ($V_{MAX} - V_{MIN}$) is an indicator of the variation in the output voltage among battery units BT[1] to BT[3]. Controller 1 compares the voltage difference ($V_{MAX} - V_{MIN}$) with a predetermined reference voltage difference V_{TH} (note that $V_{TH} > 0$). If the inequality for state determination " $V_{MAX} - V_{MIN} < V_{TH}$ " holds true, controller 1 judges that all the battery units are in the uniform voltage state. In contrast, if the inequality for state determination does not hold true, controller 1 judges that the battery units are in the non-uniform voltage state. The inequality sign "<" in the inequality for state determination may be replaced with " $\leq$." The uniform voltage state mentioned above refers to a state where battery units BT[1] to BT[3] have relatively small variation in output voltage. The non-uniform voltage state refers to a state where battery units BT[1] to BT[3] have relatively large variation in output voltage. The non-uniform voltage state corresponds to a state where there is a relatively large current flow to cause depreciation or damage of battery units BT[i] and BT[j] between battery units BT[i] and BT[j] if the positive output terminals of battery units BT[i] and BT[j] are short-circuited (both i and j are integers, and $i \neq j$).

[0063] If controller 1 judges that the battery units are in the uniform voltage state, controller 1 turns on all of FETs 21[1] to 21[3]. If, under these conditions, controller 1 turns on charger FETs 6 and 7, the normal charging operations can be performed in the same manner as in the case of the first example.

[0064] If controller 1 judges that the battery units are in the uniform voltage state, controller 1 turns on all of FETs 31[1] to 31[3]. If, under these conditions, controller 1 turns on charger FET 8, the normal discharging operations can be performed in the same manner as in the case of the first example.

[0065] If controller 1 judges that battery units are in the non-uniform voltage state, controller 1 turns on only the FET corresponding to the minimum voltage V_{MIN} among FETs 21[1] to 21[3], and turns off the other FETs. If, under these conditions,

charger FETs 6 and 7 are turned on, the non-uniform charging operations that are similar to the ones in the first example are performed. Specifically, the battery units with lower output voltages are preferentially charged to correct the non-uniformity in the output voltage. Alternatively, if controller 1 judges that the battery units are in the voltage non-uniform state, controller 1 may turn off all the FET 21[1] to 21[3]. Also in this case, the battery units with lower output voltages are charged preferentially through parasitic diodes of FETs 21[1] to 21[3]. Thus, the non-uniformity in the output voltage is gradually corrected.

[0066] Note that the above-mentioned FET corresponding to minimum voltage V_{MIN} refers specifically to FET 21[1] if $V_{MIN} = V[1]$; it refers specifically to FET 21[2] if $V_{MIN} = V[2]$; and it refers specifically to FET 21[3] if $V_{MIN} = V[3]$. In some cases, there are plural FETs corresponding to minimum voltage V_{MIN} . For instance, if $V_{MIN} = V[1] = V[2]$, both FETs 21[1] and FET 21[2] are the FETs corresponding to minimum voltage V_{MIN} . The following additional technique is applicable to the above-described method where with the judgment that the battery units are in the non-uniform voltage state, the FET corresponding to the minimum voltage V_{MIN} among FETs 21[1] to 21[3] is turned on and the other FETs are turned off. For the sake of providing more specific description, the additional technique is described on the assumption that $V_{MIN} = V[1]$. Now suppose a case where output voltage $V[1]$ is minimum voltage V_{MIN} and output voltage $V[1]$ is equal to none of output voltages $V[2]$ and $V[3]$. In this case, FET 21[1] is turned on while both of FETs 21[2] and 21[3] are turned off as described above. After that, the non-uniformity in the output voltage is gradually corrected and thus eventually output voltages $V[1]$ and $V[2]$ become equal to each other. At this point, FET 21[2] may be turned on in addition to FET 21[1] that has been on (in the same applies to a case where output voltages $V[1]$ and $V[3]$ become equal to each other). Now suppose an alternative case where output voltages $V[1]$ and $V[2]$ become equal to each other, but output voltages $V[1]$ and $V[3]$ are still different from each other. In this case, a state where FET 21[1] is on while both of FETs 21[2] and 21[3] are off may be kept. Once all the output voltages $V[1]$ to $V[3]$ become equal to one another, both of FETs 21[2] and 21[3] are switched from off to on, and thereby all of FETs 21[1] to 21[3] are on. Note that the concept of equal output voltages is used in a broader sense with a certain degree of inexactitude. For instance, if the absolute value of the difference in the output voltages of battery units $BT[i]$ and $BT[j]$ (i.e., $|V[i] - V[j]|$) is equal to or smaller than reference voltage difference V_{TH} described above, the state of such output voltages $V[i]$ and $V[j]$ can be interpreted as the state where output voltages $V[i]$ and $V[j]$ are equal to each other.

[0067] If controller 1 judges that battery units are in the non-uniform voltage state, controller 1 turns on only the FET corresponding to maximum voltage V_{MAX} among

FETs 31[1] to 31[3], and turns off the other FETs. If, under these conditions, charger FET 8 is turned on, the non-uniform discharging operations that are similar to the ones in the first example are performed. Specifically, the battery units with higher output voltages are preferentially discharged to correct the non-uniformity in the output voltage. Alternatively, if controller 1 judges that the battery units are in the voltage non-uniform state, controller 1 may turn off all the FETs 31[1] to 31[3]. Also in this case, the battery units with higher output voltages are discharged preferentially through parasitic diodes of FETs 31[1] to 31[3]. Thus, the non-uniformity in the output voltage is gradually corrected.

[0068] Note that the above-mentioned FET corresponding to maximum voltage V_{MAX} refers specifically to FET 31[1] if $V_{MAX} = V[1]$; it refers specifically to FET 31[2] if $V_{MAX} = V[2]$; and it refers specifically to FET 31[3] if $V_{MAX} = V[3]$. In some cases, there are plural FETs corresponding to minimum voltage V_{MAX} . For instance, if $V_{MAX} = V[1] = V[2]$, both FETs 31[1] and FET 31[2] are the FETs corresponding to maximum voltage V_{MAX} .

[0069] As has been described thus far, the second example has the same advantageous effects as those obtainable in the first example. Note that what distinguishes the second example from the first example is the fact that controller 1 of the second example must control the FETs so as to reflect the non-uniform output voltages of the battery units. Nevertheless, the second example needs no driver circuit 50 shown in Fig. 5, so that there is a possibility that the size of the circuit can be made smaller.

Example 3

[0070] A third example is described. The internal circuit of parallel-connection circuit 5 according to the third example is the same as the one shown in Fig. 12. The following description focuses on the differences between the second and the third examples.

[0071] Controller 1 in the third example controls the continuity of FETs 21[1] to 21[3] and 31[1] to 31[3] on the basis of the length of time passed after the last replacing of battery units without using the detected output voltages of battery unit BT[i].

[0072] This method is described in more detail. The battery unit BT[i] that is removed from apparatus AP shown in Fig. 3 during the battery-unit replacement is referred to as the old battery unit while the battery unit that is attached to apparatus AP as the new battery unit BT[i] is referred to as the new battery unit.

[0073] Suppose a state where a sufficiently long time has passed since the last battery-unit replacement in which any chosen battery unit or unit BT[i] is replaced. Such a state is referred to as the reference state. In the reference state, the output voltages of all the battery units BT[1] to [3] are equal to one another. Hence, in the reference state, controller 1 turns on all of FETs 21[1] to 21[3] and FETs 31[1] to 31[3].

- [0074] Suppose that battery unit BT[i] is removed from apparatus AP as an old battery unit and a new battery unit is attached to apparatus AP as new battery unit BT[i]. Note that two or more battery units may be replaced. Controller 1 is capable of detecting the occurrence of the replacement of battery unit BT[i], that is, the replacement of the old battery unit with a new battery unit and the attachment of the new battery unit in apparatus AP. Any method can be used for the detection.
- [0075] For instance, voltage measuring units VM[i] to measure the voltages at branch points 15[i] are provided in parallel-connected circuit 5. In the example, voltage measuring units VM[1] to VM[3] measure the voltages of branch points 15[1] to 15[3] respectively. Each measured value is output as branch-point voltage information. The branch-point voltage information mentioned above includes not only the voltage at the branch point but also broader information to be used in specifying the voltage at the branch point. Controller 1 receives the branch-point voltage information. Controller 1 may receive the branch-point voltage information directly from voltage measuring units VM[1] to VM[3]. Alternatively, a third apparatus may be provided to receive branch-point voltage information from voltage measuring units VM[1] to VM[3]. The third apparatus processes the data when necessary, and then sends the data to controller 1. On the basis of the branch-point voltage information thus received, controller 1 detects the attachment of a new battery unit in apparatus AP.
- [0076] For instance, to perform the above-mentioned detection, the casing (not illustrated) to hold battery unit BT[i] may be provided with mechanical switches or the like to detect the existence or the non-existence of battery unit BT[i].
- [0077] Upon detecting the attachment of a new battery unit in apparatus AP, controller 1 starts measuring, by use of timer 41 provided thereto, length of time TP that has passed since the new battery unit is attached to apparatus AP. When elapsed time TP does not exceed predetermined length of time TPTH, controller 1 judges that the battery units are in the non-uniform voltage state (note that $TPTH > 0$) and turns off all of FETs 21[1] to 21[3] and FETs 31[1] to 31[3]. If elapsed time TP exceeds predetermined length of time TPTH, controller 1 judges that the battery units are in the uniform voltage state and turns on all of FETs 21[1] to 21[3] and FETs 31[1] to 31[3]. If another battery-unit replacement occurs while elapsed time TP is being measured, measured elapsed time TP is reset to zero, and the measurement of elapsed time TP is resumed from the point of time at which the other new battery unit is attached to apparatus AP.
- [0078] Suppose a case where all of FETs 21[1] to 21[3] and 31[1] to 31[3] are off, and the output voltages of the battery units are in the non-uniform state. Even in this case, the non-uniformity of the output voltage is gradually corrected automatically. This is because the battery units with lower output voltages are preferentially charged through

the parasitic diodes of FETs 21[1] to 21[3] and because the battery units with higher output voltages are preferentially discharged through the parasitic diodes of FETs 31[1] to 31[3]. By the time when a certain length of time after the last changing of battery units, the non-uniformity of output voltages are presumably corrected to a certain degree or sufficiently as a result of the above-mentioned preferential charging and the above-mentioned preferential discharging. Accordingly, all of FETs 21[1] to 21[3] and 31[1] to 31[3] are turned on to reduce the loss in circuits 20B[i] and 30B[i].

[0079] The third example has the same advantageous effects as those obtainable in the first example. Note that what distinguishes the third example from the first example is the FET control performed by controller 1 of the third example on the basis of the elapsed time TP. Nevertheless, the third example needs no driver circuit 50 shown in Fig. 5, so that there is a possibility that the size of the circuit can be made smaller.

Example 4

[0080] A fourth example is described. Fig. 13 illustrates the internal circuit of parallel-connection circuit 5 according to the fourth example. Circuit 20[i] and circuit 30[i] shown in Fig. 1 are referred to respectively as circuit 20C[i] and circuit 30C[i] in the second example.

[0081] The configurations of circuits 20C[1] to 20C[3] are identical to one another whereas the configurations of circuits 30C[1] to 30C[3] are identical to one another. What distinguishes circuit 20C[i] from each of circuits 20A[i] and 20B[i] is the providing of diode 25[i] in circuit 20C[i] in place of FET 21[i] provided in each of circuits 20A[i] and 20B[i]. Likewise, what distinguishes circuit 30C[i] from each of circuits 30A[i] and 30B[i] is the providing of diode 35[i] in circuit 30C[i] in place of FET 31[i] provided in each of circuits 30A[i] and 30B[i]. The anode of diode 25[i] is connected to charging line LA whereas the cathode of diode 25[i] is connected to branch point 15[i]. The anode of diode 35[i] is connected to branch point 15[i] whereas the cathode of each diode 35[i] is connected to charging line LB.

[0082] Accordingly, even if the output voltages of battery units BT[1] to BT[3] are in the non-uniform state for reasons of the battery-unit replacement or the like, the diodes provided in circuit 20C[i] and 30C[i] prevent excessively large current from flowing between battery units. In addition, even if the output voltages of the battery units are in the non-uniform state, the functions of the diodes included in circuits 20C[i] and 30C[i] automatically correct the non-uniformity of output voltage gradually. This is because the battery units with lower output voltages are preferentially charged by the functions of the diodes while the battery units with higher output voltages are discharged preferentially by the functions of the diodes. The discharging current and the charging current always flow through the diodes, so that the configuration of this

fourth example has larger loss than in each of the cases of the first to the third examples.

Example 5

- [0083] A fifth example is described. The techniques that are described in the fifth example are modifications that are applicable to each of the first to the fourth examples. In each of the first to the fourth examples, charging line LA may be connected to each of branch points 15[1] to 15[3] via a resistive element for voltage-non-uniformity correction. Fig. 14 shows an exemplary circuit diagram of a case where resistive elements for non-voltage-uniformity correction are provided in the parallel-connection circuit of any of the first, the second, and the third examples. Resistive element 27[i], which is provided as a resistive element for voltage-non-uniformity correction, has an end connected to the source of FET 21[i] and the other end connected to the drain thereof. Resistive element 27[i] may be considered as a constituent element of circuit 20[i], or may be considered as an element provided outside of circuit 20[i]. Each of resistive elements 27[1] to 27[3] has an arbitrarily determined resistance, but the resistance is at least larger than the on-resistance of the corresponding one of FETs 21[1] to 21[3]. The resistance of each of resistive element 27[i] and 27[j] should be determined so as to prevent electric current that may deteriorate battery units BT[i] and BT[j] from flowing between battery units BT[i] and BT[j] even if the output voltages of battery units BT[i] and BT[j] differ from one another.
- [0084] If resistive element 27[i] is provided, the non-uniformity of the output voltages of the battery units can be corrected by resistive element 27[i] as well. Specifically, suppose, for instance, a case where the output voltages of battery units BT[1] to BT[3] are 55 V, 50 V, and 52 V respectively as shown in Fig. 15. In this case, if FETs 6 to 8 are turned on simultaneously, only FETs 21[2] and FET 31[1] of all the FET 21[1] to 21[3] and 31[1] to 31[3] are turned on as in the case shown in Fig. 10. Consequently, the charging current from solar cell 9 or the like flows into battery unit BT[2] through FET 21[2] while the discharging current from only battery unit BT[1] is supplied to load 12 through FET 31[1].
- [0085] On the other hand, part of output current of battery units BT[1] flows into battery unit BT[2] through resistive element 27[1] and charging line LA and through the parallel circuit of resistive element 27[2] and FET 21[2]. This current flow also contributes to the correction of the non-uniformity of the output voltages. In case where charger FETs 6 and 8 are off, electric current flows from battery unit BT[1] into battery unit BT[2] through resistive elements 27[1] and 27[2]. The current may flow from battery unit BT[1] into battery unit BT[2] through resistive element 27[1] and the parasitic diode of FET 21[2], and the current may flow from battery unit BT[3] into

battery unit BT[2] through resistive elements 27[3] and 27[2] as well as through the parasitic diode of FET 21[2]. However, the flows are not illustrated in Fig. 15 to prevent the diagram from becoming complicated.

[0086] The resistive elements for non-voltage-uniformity correction may be provided on the side of discharging line LB. Discharging line LB may be connected to each of branch points 15[1] to 15[3] via a resistive element for voltage-non-uniformity correction. Fig. 16 shows an exemplary circuit diagram of a case where resistive elements for non-voltage-uniformity correction are provided to discharging line LB of any of the first, the second, and the third examples. Resistive element 37[i], which is provided as a resistive element for voltage-non-uniformity correction, has an end connected to the source of FET 31[i] and the other end connected to the drain thereof. Resistive element 37[i] may be considered as a constituent element of circuit 30[i], or may be considered as an element provided outside of circuit 30[i]. Each of resistive elements 37[1] to 37[3] has a desired resistance, but the resistance is at least larger than the on-resistance of the corresponding one of FETs 31[1] to 31[3]. The resistance of each of resistive element 37[i] and 37[j] should be determined so as to prevent electric current that may deteriorate battery units BT[i] and BT[j] from flowing between battery units BT[i] and BT[j] even if the output voltages of battery units BT[i] and BT[j] differ from one another. The circuit shown in Fig. 16 has the same effects that are obtainable by the circuit shown in Fig. 14.

Example 6

[0087] An sixth example is described. Resistive elements with positive temperature characteristics (i.e., resistive elements with a positive temperature coefficient) may be used as resistive elements 27[1] to 27[3] or 37[1] to 37[3] (see Figs. 14 or 16), which are resistive elements for non-voltage-uniformity correction. In particular, for instance, PTC (positive temperature coefficient) thermistors can be used for this purpose. PTC thermistors are thermistors with positive temperature characteristics (i.e., thermistors with a positive temperature coefficient). As is well known, the resistance of each thermistor changes with changes in temperature to a greater degree than the resistance of each ordinary resistive element (carbon-film resistors etc) used for obtaining a constant resistance. The resistance of each PTC thermistor increases as the temperature of the PTC thermistor rises.

[0088] The effects that the use of resistive elements 27[i] or 37[i] with positive temperature characteristics has is studied through the following simulations. Fig. 18 is a diagram illustrating the circuit used in the simulations. The simulations include first and second simulations described later.

[0089] Battery unit 100 shown in Fig. 18 includes a series-connected circuit of batteries 101

and 102 whereas battery unit 110 includes a series-connected circuit of batteries 111 and 112. The output voltage of the series-connected circuit of batteries 101 and 102 appears at the positive output terminal of battery unit 100 with the negative output terminal of battery unit 100 being the reference. The output voltage of the series-connected circuit of batteries 111 and 112 appears at the positive output terminal of battery unit 110 with the negative output terminal of battery unit 110 being the reference. The positive output terminals of battery units 100 and 110 are electrically coupled to each other via resistive element 120 whereas the negative output terminals of battery units 100 and 110 are electrically coupled directly to each other.

[0090] Each of batteries 101, 102, 111, and 112 is a secondary battery with a nominal output voltage of 48 V, a maximum output voltage of 52 V, and a minimum output voltage of 39 V. Accordingly, the maximum difference between the output voltages of battery units 100 and 110 is 26 V.

[0091] In the simulations, first to fourth sample elements are individually used as resistive element 120. The first sample element is a PTC thermistor with a resistance of 6 ohm at a certain reference temperature, so that the first sample is referred to as a 6-ohm thermistor. The 6-ohm thermistor has the same temperature as the reference temperature unless the 6-ohm thermistor generates heat due to power loss. The second sample element, which always has a resistance of 6 ohm irrespective of the temperature thereof, is referred to as a 6-ohm simple resistor. The third sample element is a resistive element, which always has a resistance of 12.3 ohm irrespective of the temperature thereof, is referred to as a 12.3-ohm simple resistor. The fourth sample element is a resistive element, which always has a resistance of 240 ohm irrespective of the temperature thereof, is referred to as a 240-ohm simple resistor.

[0092] The simulations use the characteristics of 6-ohm thermistor shown in Fig. 19. Specifically, for instance, when the voltage ETM applied to the 6-ohm thermistor is 26 V, the 6-ohm thermistor has a temperature TTM of 135.5 degrees C and a resistance RTM of 236.4 ohm. At the same time, the current ITM flowing through the 6-ohm thermistor is approximately 0.11 A (amperes) because $ITM = ETM / RTM = 26 / 236.4$ approximately = 0.11. Consequently, the heating value QTM of the 6-ohm thermistor, which is the power loss of the 6-ohm thermistor, is 2.86 W (watts) because $QTM = ITM \times ITM \times RTM = 0.11 \times 0.11 \times 236.4$ approximately = 2.86. Of the above-mentioned characteristics, the current ITM and the temperature TTM are measured values. The resistance RTM and the heating value QTM are values calculated by assigning the measured values to the formulas.

[0093] As Fig. 19 shows, in the 6-ohm thermistor, the changes in the applied voltage cause less change in the heat generated amount for the following reasons. An increase in the voltage applied to a PTC thermistor such as the 6-ohm thermistor increases the current,

and the larger current in turn increases the amount of generated heat. The larger amount of generated heat in turn raises the temperature, and the higher temperature increases the resistance. The increase in the resistance reduces the current, and eventually reduces amount of generated heat. Conversely, a decrease in the applied voltage reduces the current, and the smaller current in turn reduces the amount of generated heat. The smaller amount of generated heat lowers the temperature, and the lower temperature in turn reduces the resistance. The smaller resistance increases the current and eventually increases the amount of generated heat.

- [0094] Figs. 20A and 20B show the results of a first simulation. The first simulation assumes that the difference VDIF between the output voltages of battery units 100 and 110 is 26 V at the reference point of time. On this assumption, arithmetic operations are performed to calculate, for each of the sample elements, the relationship between the time tEL elapsed from the reference point of time and the output-voltage difference VDIF. In addition, arithmetic operations are performed to calculate, for each of the sample elements, the relationship between the elapsed time tEL and the heating value Q120 generated by the sample element.
- [0095] In Fig. 20A, dotted line GA[6], dashed line GA[12.3], dashed-dotted line GA[240], and solid line GA[TM] respectively represent the relationships between the elapsed time tEL and the output-voltage difference VDIF for the cases where the 6-ohm simple resistor, the 12.3-ohm simple resistor, the 240-ohm simple resistor, and the 6-ohm thermistor are used as resistive element 120.
- [0096] In Fig. 20B, dotted line GB[6], dashed line GB[12.3], dashed-dotted line GB[240], solid line GB[TM] respectively represent the relationships between the elapsed time tEL and heating value Q120 for the cases where the 6-ohm simple resistor, the 12.3-ohm simple resistor, the 240-ohm simple resistor, and the 6-ohm thermistor are used as resistive element 120.
- [0097] It is assumed that while the output-voltage difference VDIF ranges from 26 V to 0 V, a linear relationship exists between the reserve capacity and the output voltage of each of batteries 101, 102, 111, and 112 (i.e., the reserve capacity and the output voltage are proportional to each other). Accordingly, each of batteries 101, 102, 111, and 112 is assumed to be not fully charged or nearly fully charged, and is assumed to be not fully discharged or nearly fully discharged. The unit for the elapsed time tEL is an integral multiple of second.
- [0098] As Fig. 20A shows, the elapsed time tEL till the output voltage difference VDIF reaches 0.001 V is approximately 11 units time for the case where 6-ohm simple resistor is used as resistive element 120. The corresponding elapsed time tEL for the 12.3-ohm simple resistor is approximately 24 units time, and that for the 6-ohm thermistor is also approximately 24 units time. The length of one unit time depends on

the capacity of battery 101 or the like. Hereinafter, the elapsed time t_{EL} till the output voltage difference $VDIF$ reaches 0.001 V is referred to as the voltage-balancing time. Though not shown in Fig. 20A, the voltage-balancing time for the case where 240-ohm simple resistor is used as resistive element 120 is approximately 464 unit time.

[0099] As Fig. 20B shows, the maximum value of the heating value Q_{120} is approximately 36 W (watts) for the case where 12.3-ohm simple resistor is used as resistive element 120. The corresponding value for the 240-ohm simple resistor is approximately 3 W, and that for 6-ohm thermistor is also approximately 3 W. Though not shown in Fig. 20B, the maximum value of the heating value Q_{120} for the case where 6-ohm simple resistor is used as resistive element 120 is approximately 113 W. This is because if 6-ohm simple resistor is used as resistive element 120 and t_{EL} approximately = 0, $Q_{120} = (26 \text{ V} \times 26 \text{ V}) / 6 \text{ ohm}$ approximately = 113 W holds true.

[0100] Notice that the second, the third, and the fourth sample elements are selected with the following criteria. A 6-ohm simple resistor is selected as the second sample element because the 6-ohm simple resistor is a simple resistor with a resistance that is equal to the resistance of the 6-ohm thermistor at the reference temperature. A 240-ohm simple resistor is selected as the fourth sample element because the 240-ohm simple resistor is a simple resistor with a resistance that is approximately equal to the maximum resistance of the 6-ohm thermistor (approximately 240 ohm; see Fig. 19). A 12.3-ohm simple resistor is selected as the third sample element because the 12.3-ohm simple resistor is a simple resistor with a voltage-balancing time that is approximately equal to the voltage-balancing time of the 6-ohm thermistor in the first simulation.

[0101] The results of the first simulation show that in comparison to the case where the 6-ohm thermistor is used as resistive element 120, the use of the 6-ohm simple resistor as resistive element 120 cuts the voltage-balancing time approximately in half, but increases the maximum amount of generated heat by approximately 40 (approximately = $113/3$) times. In addition, in comparison to the case where the 6-ohm thermistor is used as resistive element 120, the use of the 240-ohm simple resistor as resistive element 120 leaves the maximum amount of generated heat approximately the same (approximately 3 W), but increases the voltage-balancing time by approximately 20 (approximately = $464/24$) times. In addition, in comparison to the case where the 6-ohm thermistor is used as resistive element 120, the use of the 12.3-ohm simple resistor as resistive element 120 leaves the voltage-balancing time approximately the same, but increases the maximum amount of generated heat by approximately 10 times.

[0102] Figs. 21A and 21B show the results of a second simulation. The second simulation assumes that the difference $VDIF$ between the output voltages of battery units 100 and 110 is 13 V at the reference point of time. On this assumption, arithmetic operations

are performed to calculate, for each of the sample elements, the relationship between the time t_{EL} elapsed from the reference point of time and the output-voltage difference $VDIF$. In addition, arithmetic operations are performed to calculate, for each of the sample element, the relationship between the elapsed time t_{EL} and the heating value Q_{120} generated by the sample element.

- [0103] In Fig. 21A, dotted line $GC[6]$, dashed line $GC[12.3]$, dashed-dotted line $GC[240]$, and solid line $GC[TM]$ respectively represent the relationships between the elapsed time t_{EL} and the output-voltage difference $VDIF$ for the cases where the 6-ohm simple resistor, the 12.3-ohm simple resistor, the 240-ohm simple resistor, and the 6-ohm thermistor are used as resistive element 120.
- [0104] In Fig. 16B, dotted line $GD[6]$, dashed line $GD[12.3]$, dashed-dotted line $GD[240]$, solid line $GD[TM]$ respectively represent the relationships between the elapsed time t_{EL} and heating value Q_{120} for the cases where the 6-ohm simple resistor, the 12.3-ohm simple resistor, the 240-ohm simple resistor, and the 6-ohm thermistor are used as resistive element 120. As in the case of the first simulation, it is assumed that while the output-voltage difference $VDIF$ ranges from 13 V to 0 V, a linear relationship exists between the reserve capacity and the output voltage of each of batteries 101, 102, 111, and 112 (i.e., the reserve capacity and the output voltage are proportional to each other).
- [0105] As Fig. 21A shows, the voltage-balancing time is approximately 10 units time for the case where 6-ohm simple resistor is used as resistive element 120. The corresponding voltage-balancing time for the 12.3-ohm simple resistor is approximately 22 units time, and that for the 6-ohm thermistor is approximately 6 units time. Though not shown in Fig. 16A, the voltage-balancing time for the case where 240-ohm simple resistor is used as resistive element 120 is approximately 432 unit time.
- [0106] As Fig. 21B shows, the maximum value of the heating value Q_{120} is approximately 28 W (watts) for the case where 6-ohm simple resistor is used as resistive element 120. The corresponding value for the 12.3-ohm simple resistor is approximately 9 W, and that for 6-ohm thermistor is also approximately 3 W. The maximum value of the heating value Q_{120} for the case where 240-ohm simple resistor is used as resistive element 120 is not larger than 1 W.
- [0107] The following observations can be obtained from the first and the second simulations. The use of a simple resistor (e.g., 6-ohm simple resistor) as resistive element 120 cuts the maximum heating value of resistive element 120 in the second simulation into a quarter of its counterpart in the first simulation, but leaves the voltage-balancing time in the second simulation approximately the same as its counterpart in the first simulation. To put it differently, the use of a simple resistor as resistive element 120 increases the maximum heating value of resistive element 120 with the square of the

output voltage difference VDIF, but hardly changes the time needed for the voltage-non-uniformity correction (i.e., the voltage-balancing time) almost the same even if the degree of the non-uniformity is decreased (e.g., even if the degree of the non-uniformity is decreased from 26 V down to 13 V). As a matter of course, the increase in the maximum amount of generated heat increases the maximum rating of, the physical size of, and the cost for resistive element 120.

[0108] In contrast, the use of 6-ohm thermistor as resistive element 120 leaves little difference between the maximum amounts of heat generated by resistive element 120 in the first and the second simulations, but cuts the voltage-balancing time in the second simulation into a quarter of its counterpart in the first simulation. To put it differently, if a PTC thermistor such as the 6-ohm thermistor is used as resistive element 120, the maximum heating value of resistive element 120 can be kept down to a predetermined value or even smaller basically irrespective of the increase or the decrease in the output voltage difference VDIF. Moreover, the time needed for the voltage-non-uniformity correction (i.e., the voltage-balancing time) is reduced by an amount corresponding to the reduction in the degree of non-uniformity. Furthermore, under a restrictive condition that the maximum amount of generated heat must not be larger than a limit amount (e.g., 5 W), the use of a PTC thermistor as resistive element 120 can shorten the voltage-balancing time from the case where a simple resistor is used as resistive element 120 (see, for instance, GA[240] and GA[TM] in Fig. 20A and GB[240] and GB[TM] in Fig. 20B).

[0109] These observations testify to the utility of the use of a PTC thermistor as resistive element 27[i] or 37[i] shown in Fig. 14 or 16 and the like. The use of a PTC thermistor as resistive element 27[i] or 37[i] can keep the maximum heating value of resistive element 27[i] or 37[i] down to a predetermined value, and, at the same time, can shorten the voltage-balancing time in comparison to the case where a simple resistor is used as resistive element 20[i]. The use of a PTC thermistor as resistive element 20[i] is particularly effective for a system where the occurrence of the output-voltage non-uniformity of the battery units is unpredictable and for a system where only a part of the battery units is replaced in the battery-unit replacement. In addition, the use of a PTC thermistor as resistive element 20[i] is particularly effective when a new battery unit attached to apparatus AP (see Fig. 3) in battery-unit replacement is in the 40% to 60% capacity state. To put it differently, if a battery unit is replaced with a new one in battery-unit replacement, the voltage difference between each of those battery units not changed and the new battery unit attached to apparatus AP in the replacement has to be kept as small as possible. In this respect, it is difficult to specify the capacity states of those battery units not changed. If a new battery unit of 40% to 60% capacity state is attached to apparatus AP, it is possible to limit a maximum value of the voltage

difference between each of the battery units not changed and the new battery unit attached to apparatus AP in the replacement. Note that the battery unit of 40% to 60% capacity state means a battery unit whose actual reserve capacity is 40% to 60% of the rated reserve capacity.

Modifications

- [0110] The embodiment described above can be modified in various ways if necessary within the scope of the technical ideas shown in the claims. The embodiment is only an example of the embodiment of the invention. What the various terms of the invention and of the constituent elements of the invention mean are not limited to those described in the embodiment given above. Those specific numerical values that appear in the description given above are only for the illustrative purpose. The numerical values can be changed in various ways. The following items are some of the items applicable to the above-described examples. These items can be combined in any manner as long as they do not cause an inconsistency.
- [0111] Parallel-connection circuit 5 and the battery system described above are provided with both circuits 20[i] and 30[i]. However, parallel-connection circuit 5 and the battery system may be provided only with circuit 20[i], or alternatively may be provided only with circuit 30[i].
- [0112] The above-described embodiment assumes that each FET is an n-channel-type FET. Each FET, however, may be a p-channel-type FET.
- [0113] Alternative embodiments of the invention, for example, are conceivable as follows. In each of the second, the third, and the fifth examples, controller 1 functions both as a controller for the charging to control the states of continuity of FET 21[i] and as a controller for the discharging to control the states of continuity of FET 31[i].
- [0114] As has been described thus far, according to the embodiment, it is possible to provide a battery parallel-operation circuit and a battery system capable of electrically connecting safely plural chargeable or dischargeable battery units in parallel to one another.
- [0115] The entire contents of Japanese Patent Applications Nos. P2010-177257 entitled "BATTERY PARALLEL-OPERATION CIRCUIT AND BATTERY SYSTEM" filed on August 6, 2010 and P2010-228089 entitled "BATTERY PARALLEL-OPERATION CIRCUIT AND BATTERY SYSTEM" filed on October 8, 2010 are incorporated herein by reference.

Reference Signs List

- [0116] 1 controller
2 controlled unit
3 switch unit

4 power converter circuit
5 parallel-connected circuit
6, 7, and 8 switching element
9 solar cell
10 diode
11 power-supply circuit
12 load
15 branch point
20 charging backflow prevention circuit
30 discharging backflow prevention circuit
BT battery unit
BR breaker
LA main line
LB sub-line
BS battery system
AP apparatus
S sensor
SW mechanical switch
T timer
VM voltage measuring unit

Industrial Applicability

[0117] Some of the applications of the invention are electrically-driven vehicles (including vehicles of a single wheel, two wheels, three wheels, four wheels, or more wheels), power tools, and electronic devices (including PCs, mobile phones, PDAs, etc.).

Claims

- [Claim 1] A battery parallel-operation circuit comprising:
a first line electrically coupled to, in parallel to one another, a plurality of battery units that are electrically connectable to the battery parallel-operation circuit, and configured to supply charging current to the plurality of battery units from a power source that is electrically connectable to the battery parallel-operation circuit, wherein
the first line connecting the plurality of battery units in parallel to one another comprises a plurality of charging backflow prevention circuits each configured to allow the charging current to flow from the first line to a corresponding one of the battery units but to prevent reverse current from flowing from the battery unit to the first line.
- [Claim 2] The battery parallel-operation circuit of claim 1, wherein
each of the charging backflow prevention circuits comprises a parallel circuit comprising:
a charging switching element provided on the first line connecting the plurality of battery units in parallel to one another; and
a charging diode connected in parallel to the charging switching element with a forward direction of the charging diode set in a direction from the first line to the corresponding battery unit.
- [Claim 3] The battery parallel-operation circuit of claim 2, wherein each of the charging backflow prevention circuits comprises a charging driver circuit configured to turn on a corresponding charging switching element if a voltage of the first line is higher than an output voltage of the corresponding battery unit, and configured to turn off the corresponding charging switching element if the voltage of the first line is lower than the output voltage of the corresponding battery unit.
- [Claim 4] The battery parallel-operation circuit of claim 2, further comprising a charging controller configured to control the continuities for the respective charging switching elements in accordance with a difference among output voltages of the battery units.
- [Claim 5] The battery parallel-operation circuit of claim 2, further comprising a charging controller configured to control the continuities for the respective charging switching elements; and
a plurality of battery units attachable to and detachable from the battery parallel-operation circuit, wherein
if any of the plurality of battery units is detached, and then a different

battery unit is attached, the charging controller controls the continuities of the respective charging switching elements in accordance with a time elapsed from a time point at which the different battery unit is attached.

[Claim 6] The battery parallel-operation circuit of any one of claims 2 to 5, wherein

the charging switching element comprises a charging FET, and the charging diode comprises a parasitic diode of the charging FET.

[Claim 7] The battery parallel-operation circuit of claim 6, wherein the charging driver circuit comprises:

a bipolar transistor electrically coupled to the gate of the charging FET and the source thereof;

a diode whose cathode is electrically coupled to the drain of the charging FET; and

a first resistive element electrically coupled in series between the anode of the diode and the base of the bipolar transistor,

wherein a series-connected circuit electrically coupled in series between the gate of the charging FET and the anode of the diode comprises a second resistive element, a third resistive element, and a fourth resistive element, and

wherein a collector of the bipolar transistor is electrically coupled to the gate of the charging FET via the second resistive element, a connection point of the first and the fourth resistive elements is electrically coupled to the anode of the diode, and a voltage that is higher than a source voltage of the charging FET is applied to a connection point of the third and the fourth resistive elements.

[Claim 8] The battery parallel-operation circuit of any one of claims 1 to 7, further comprising a plurality of resistive elements connected in parallel to the charging backflow prevention circuits, respectively.

[Claim 9] The battery parallel-operation circuit of claim 8, wherein the resistive elements connected in parallel to the charging backflow prevention circuits are thermistors with a positive temperature characteristic.

[Claim 10] The battery parallel-operation circuit of any one of claims 1 to 9, further comprising:

a second line connecting, in parallel to one another, a plurality of battery units that are electrically connectable to the battery parallel-operation circuit, and configured to supply discharging current from the plurality of battery units to a load that is electrically connectable to the

battery parallel-operation circuit, wherein
the second line connecting the plurality of battery units in parallel to one another comprises a plurality of discharging backflow prevention circuits each configured to allow the discharging current from a corresponding one of the battery units to the second line but to prevent reverse current from flowing from the second line to the battery unit.

[Claim 11]

A battery parallel-operation circuit comprising:
a second line connecting, in parallel to one another, a plurality of battery units that electrically connectable to the battery parallel-operation circuit, and configured to supply discharging current from the plurality of battery units to a load that is electrically connectable to the battery parallel-operation circuit, wherein
the second line connecting the plurality of battery units in parallel to one another comprises a plurality of discharging backflow prevention circuits each configured to allow the discharging current from a corresponding one of the battery units to the second line but to prevent reverse current from flowing from the second line to the battery unit.

[Claim 12]

The battery parallel-operation circuit of claim 10 or 11, wherein each of the charging backflow prevention circuits comprises a parallel circuit comprising:
a discharging switching element provided on the second line connecting the plurality of battery units in parallel to one another; and
a discharging diode connected in parallel to the discharging switching element with a forward direction of the discharging diode set in a direction from the corresponding battery unit to the second line.

[Claim 13]

The battery parallel-operation circuit of claim 12, wherein each of the discharging backflow prevention circuits comprises a discharging driver circuit configured to turn on a corresponding discharging switching element if a voltage of the second line is lower than an output voltage of the corresponding battery unit, and configured to turn off the corresponding discharging switching element if the voltage of the second line is higher than the output voltage of the corresponding battery unit.

[Claim 14]

The battery parallel-operation circuit of claim 12, further comprising a discharging controller configured to control the continuities of the respective discharging switching elements in accordance with a difference among output voltages of the battery units.

[Claim 15]

The battery parallel-operation circuit of claim 12, further comprising

a discharging controller configured to control the continuities of the respective discharging switching elements; and
a plurality of battery units attachable to and detachable from the battery parallel-operation circuit, wherein
if any of the plurality of battery units is detached from an apparatus and then a different battery unit is attached to the apparatus, the discharging controller controls the continuities of the respective discharging switching elements in accordance with a time elapsed from a time point at which the different battery unit is attached to the apparatus.

[Claim 16] The battery parallel-operation circuit of any one of claims 12 to 15, wherein
the discharging switching element comprises a discharging FET, and
the discharging diode comprises a parasitic diode of the discharging FET.

[Claim 17] The battery parallel-operation circuit of claim 16 wherein
the charging driver circuit comprises:
a bipolar transistor electrically coupled to the gate of the discharging FET and the source thereof;
a diode whose cathode is electrically coupled to the drain of the discharging FET; and
a first resistive element electrically coupled in series between the anode of the diode and the base of the bipolar transistor,
wherein a series-connected circuit electrically coupled in series between the gate of the discharging FET and the anode of the diode comprises a second resistive element, a third resistive element, and a fourth resistive element, and
wherein a collector of the bipolar transistor is electrically coupled to the gate of the discharging FET via the second resistive element, a connection point of the first and the fourth resistive elements is electrically coupled to the anode of the diode, and a voltage that is higher than a source voltage of the discharging FET is applied to a connection point of the third and the fourth resistive elements.

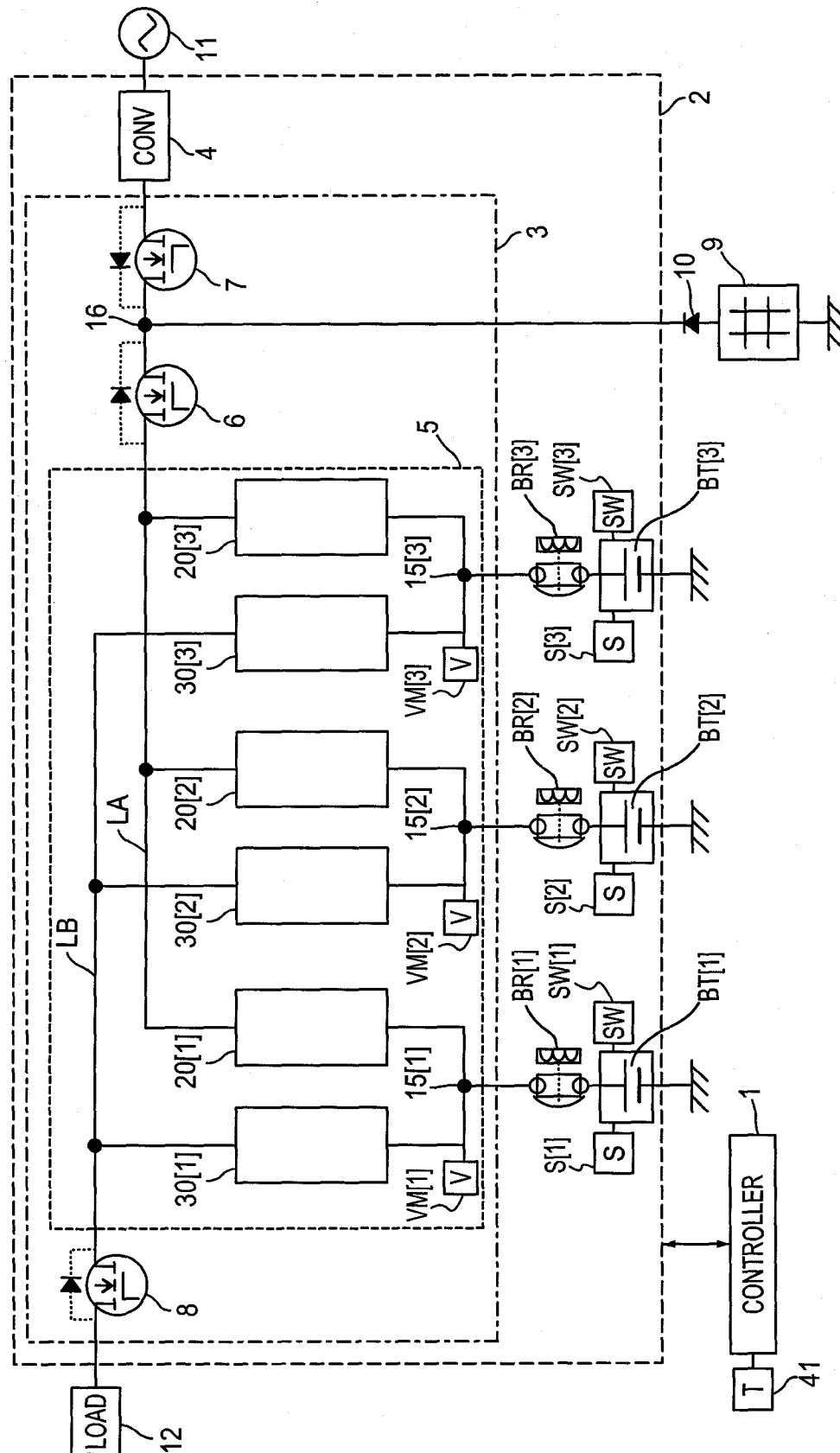
[Claim 18] The battery parallel-operation circuit of any one of claims 11 to 15, further comprising a plurality of resistive elements connected in parallel to the discharging backflow prevention circuits, respectively.

[Claim 19] The battery parallel-operation circuit of claim 18, wherein the resistive elements connected in parallel to the discharging backflow prevention circuits are thermistors with a positive temperature characteristic.

[Claim 20]

A battery system comprising:
the battery parallel-operation circuit of any of claims 1 to 19; and
a plurality of battery units.

FIG. 1



[Fig. 2]

FIG. 2A

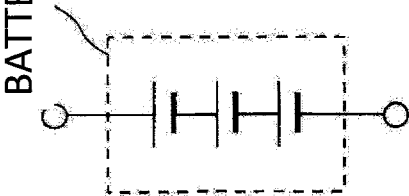


FIG. 2B

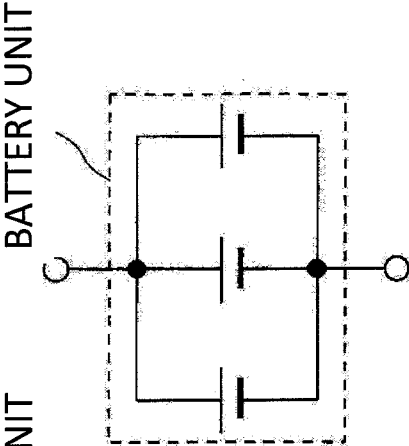
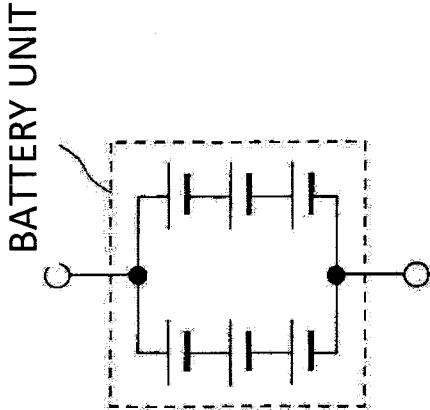
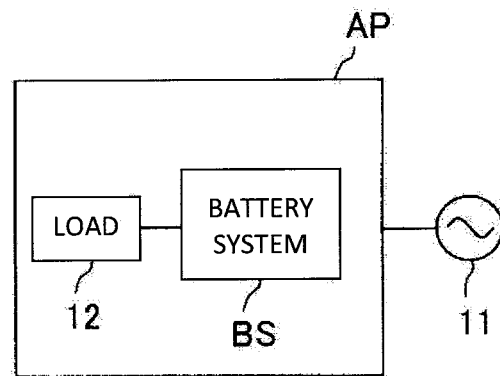


FIG. 2C



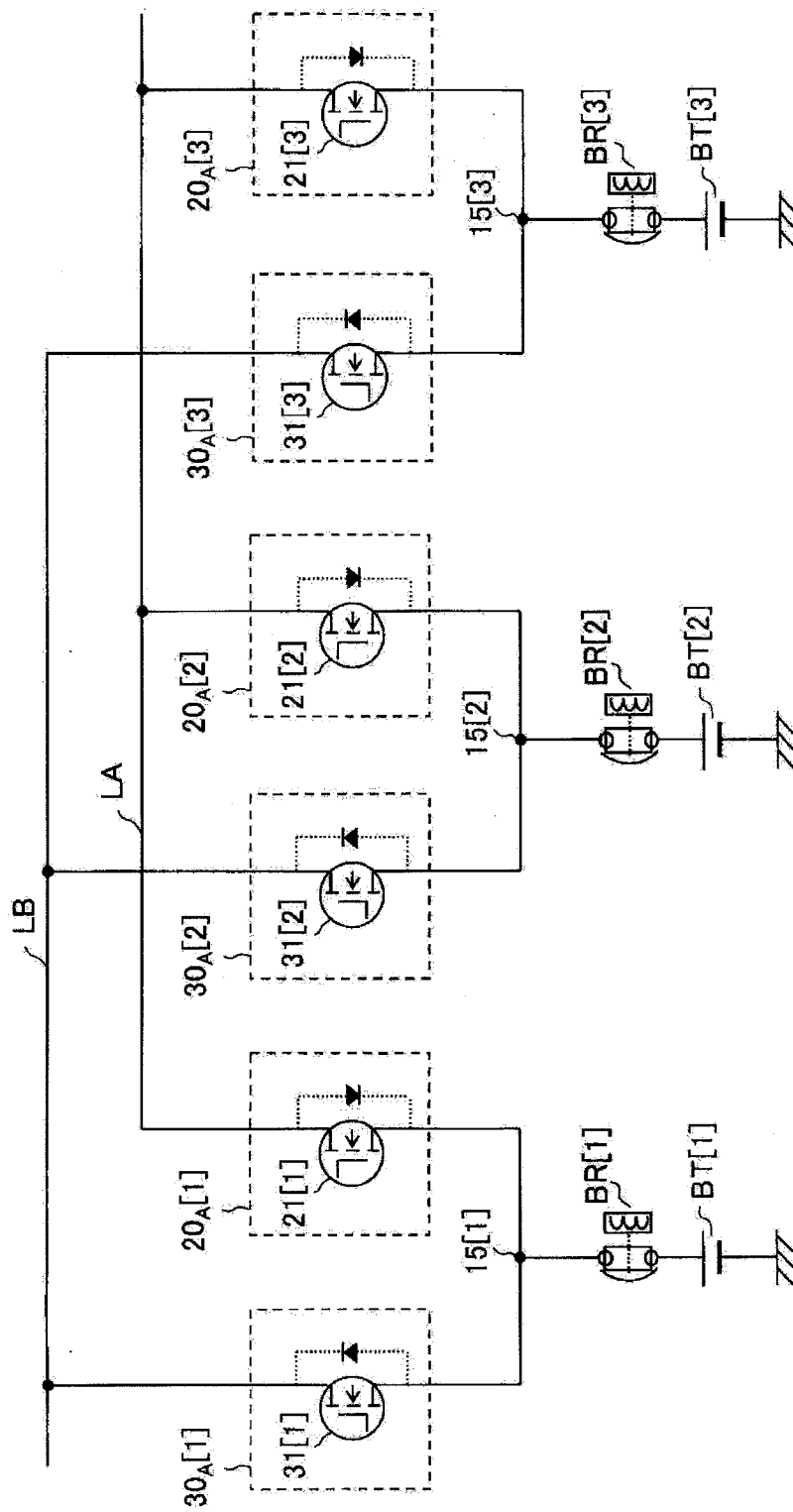
[Fig. 3]

FIG. 3



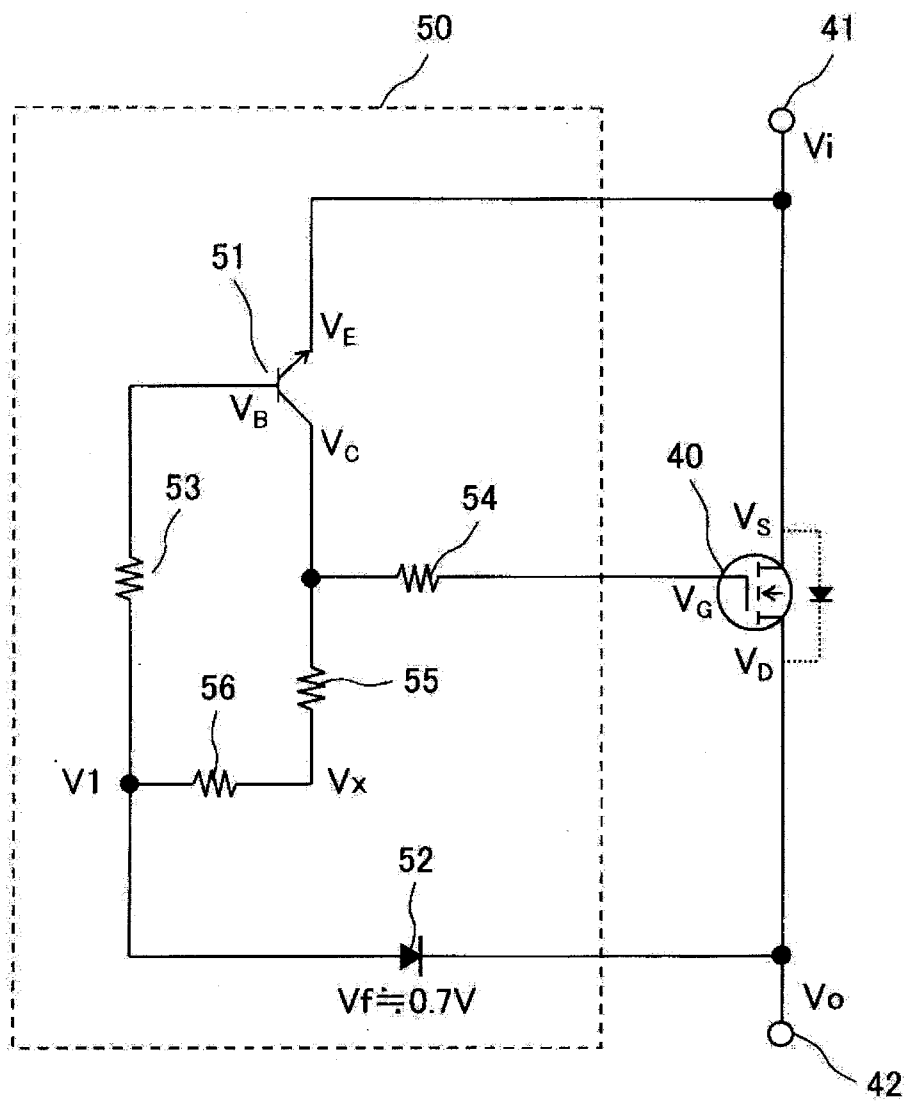
[Fig. 4]

FIG. 4



[Fig. 5]

FIG. 5



[Fig. 6]

FIG. 6

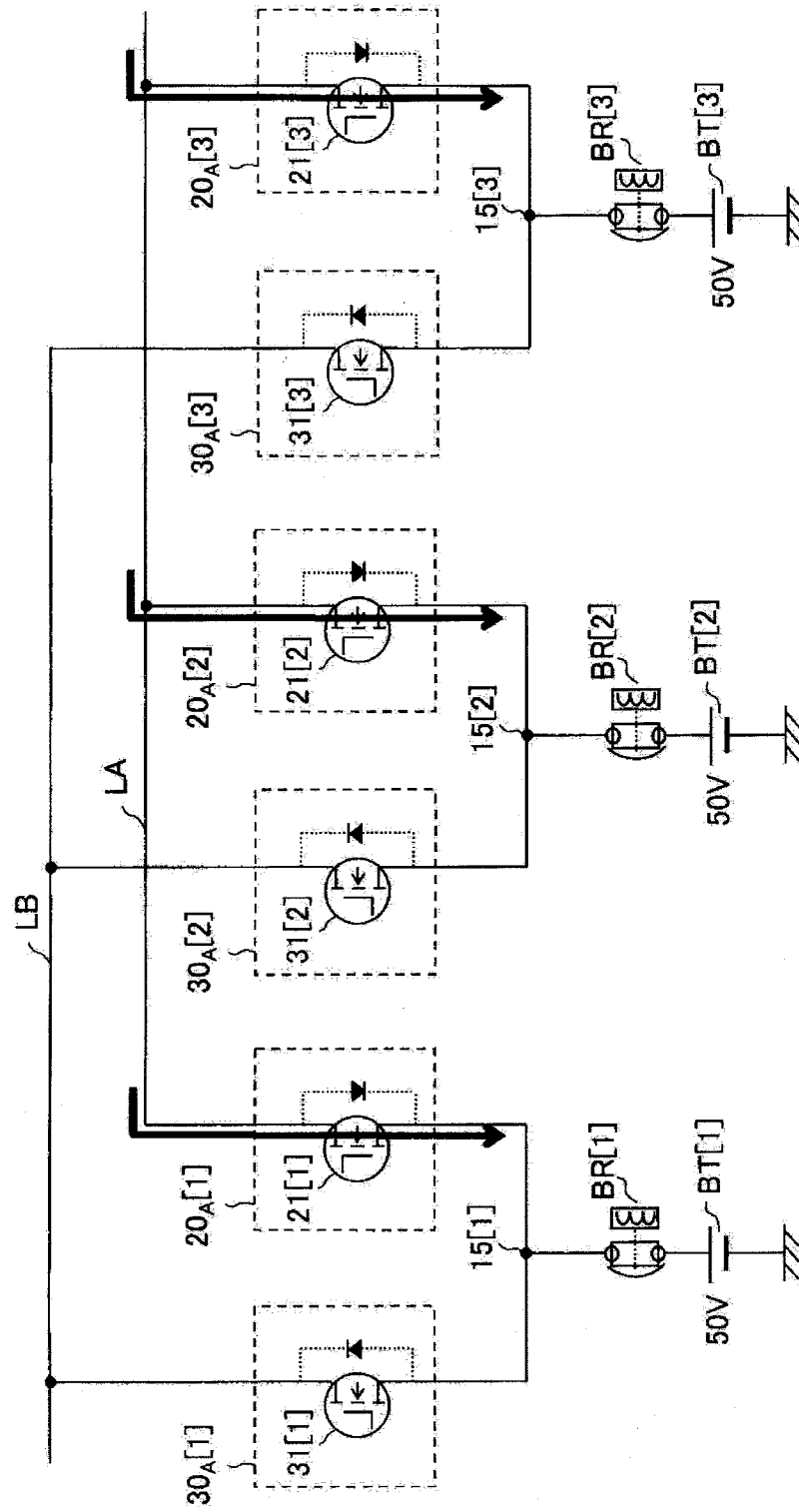


FIG. 7

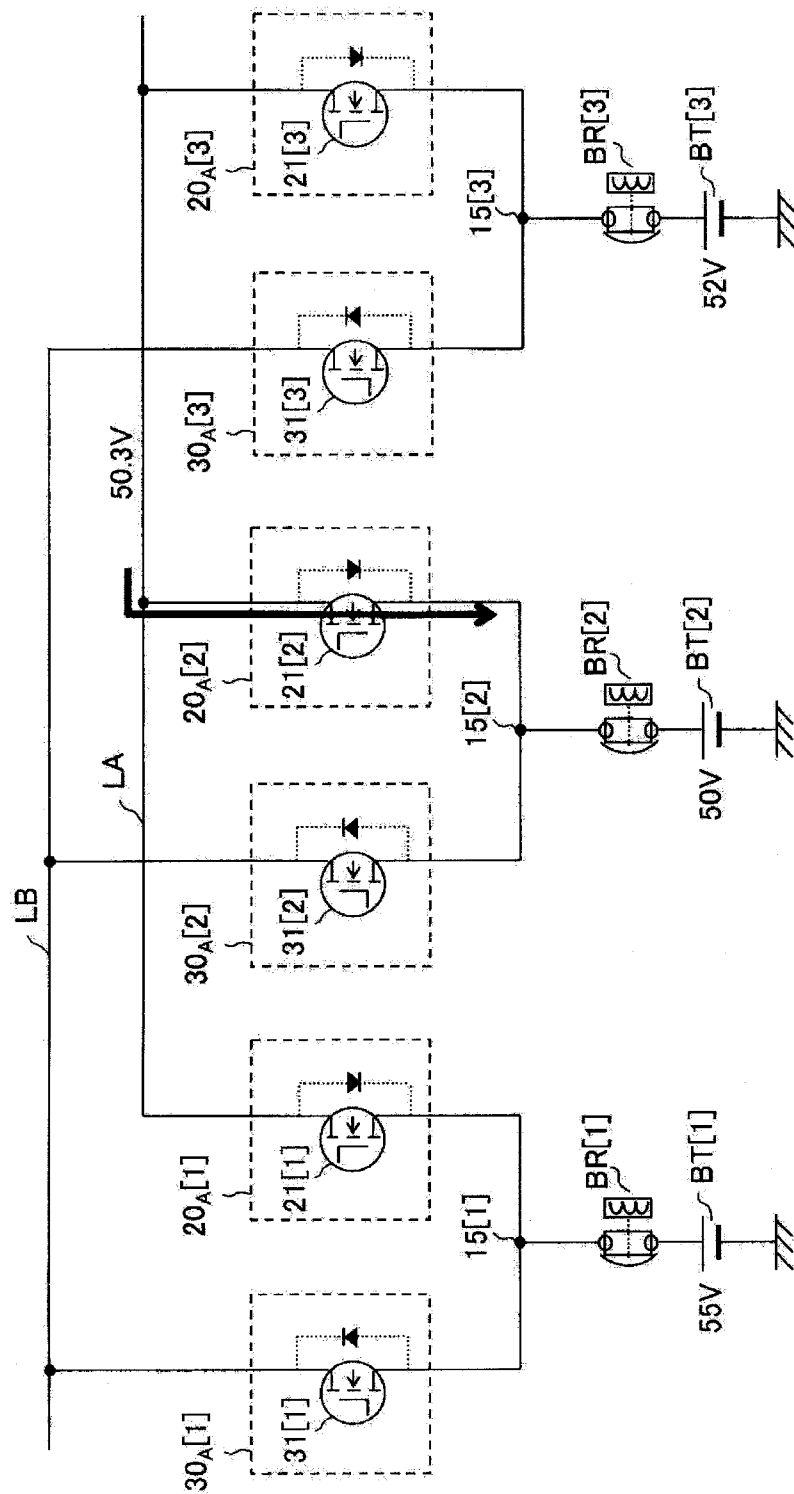
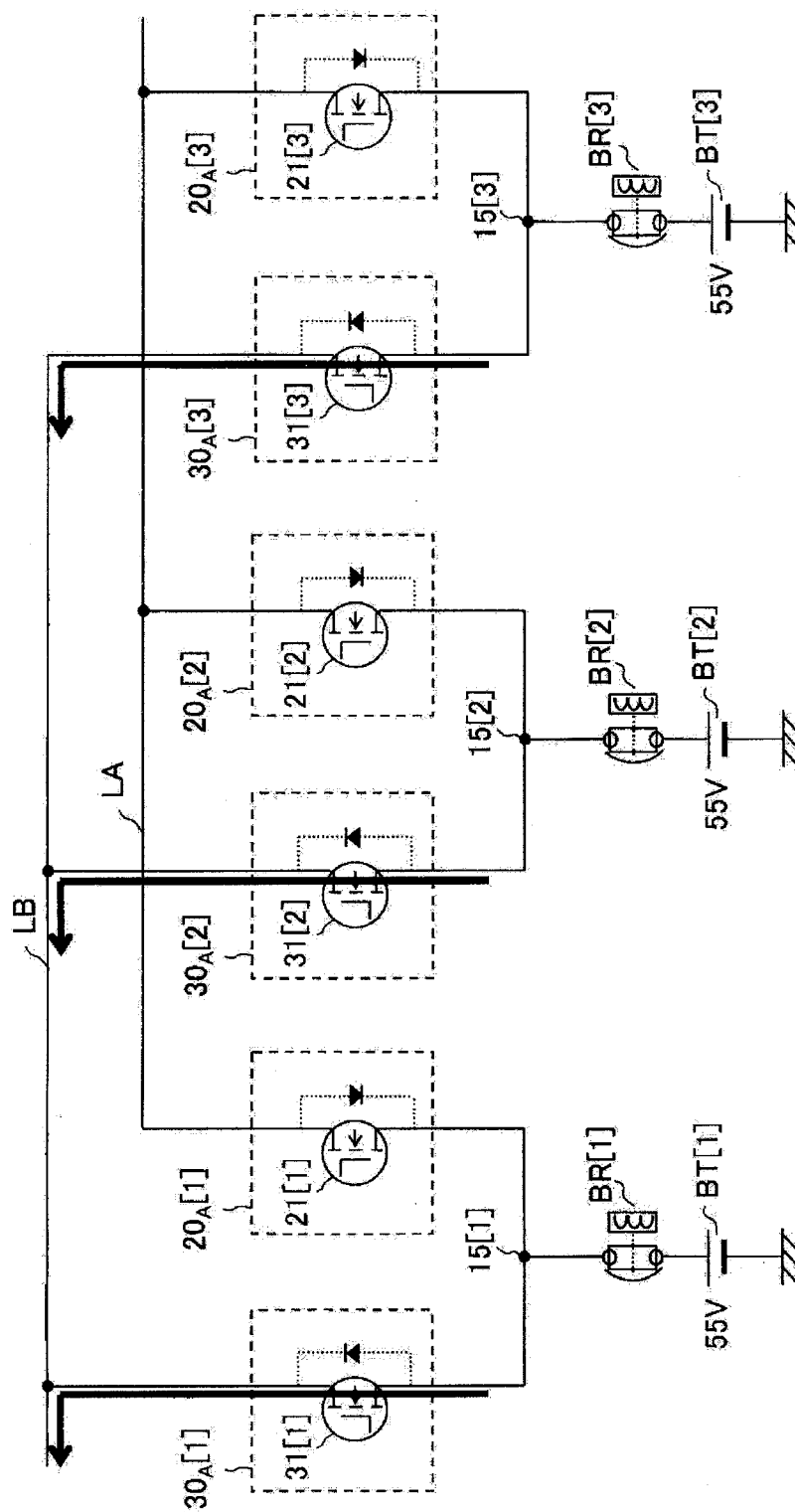
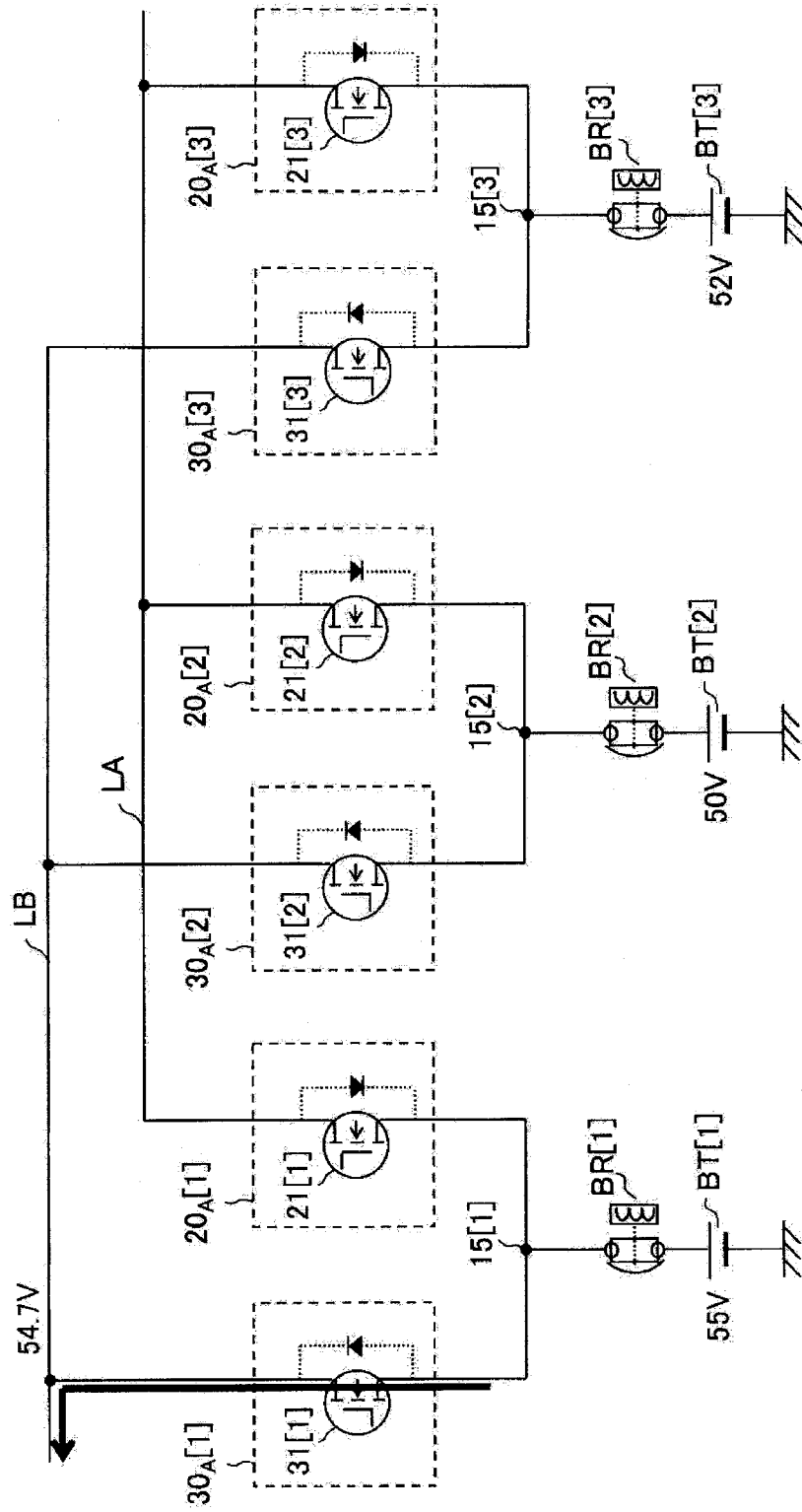


FIG. 8



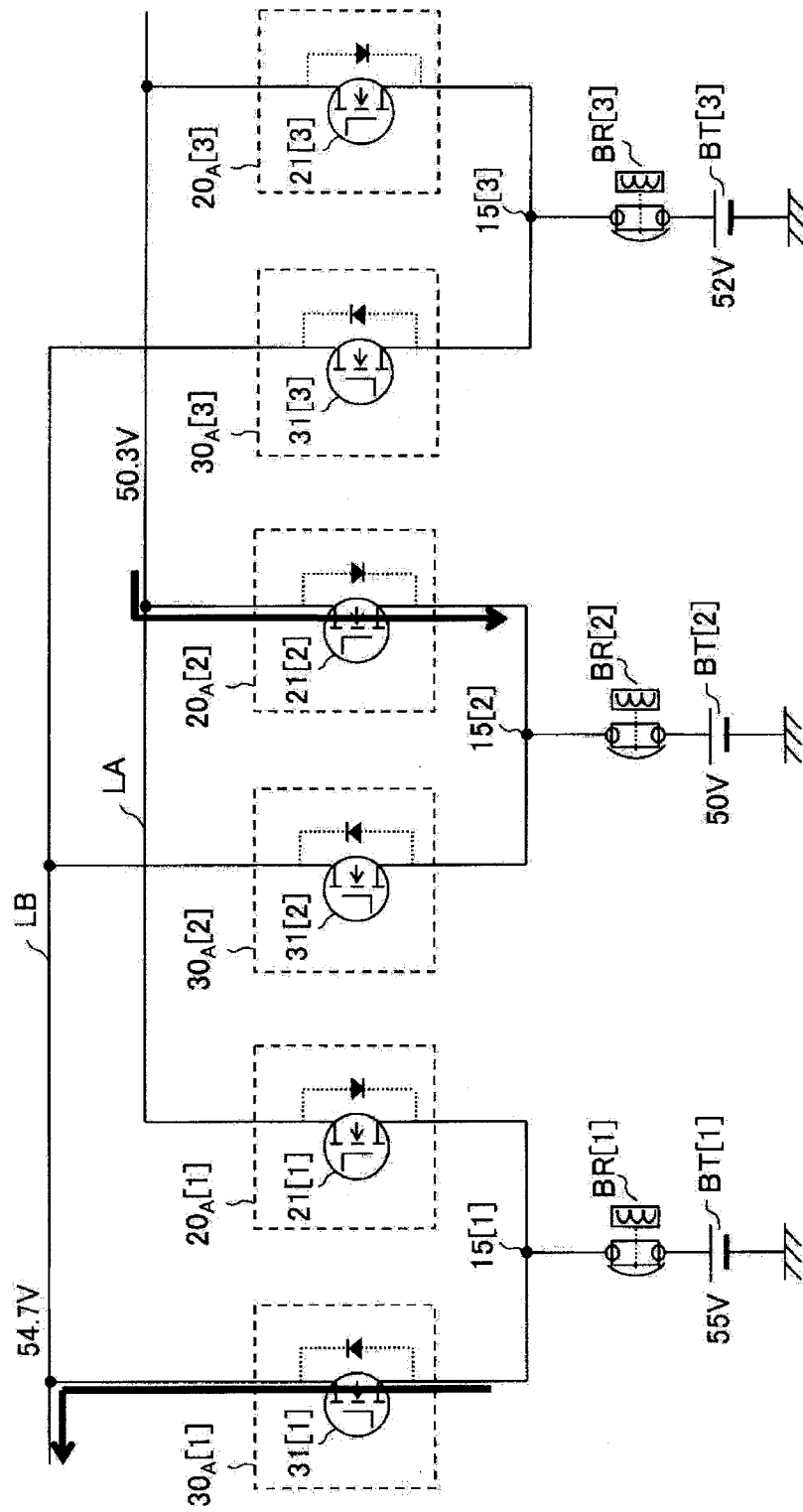
[Fig. 9]

FIG. 9



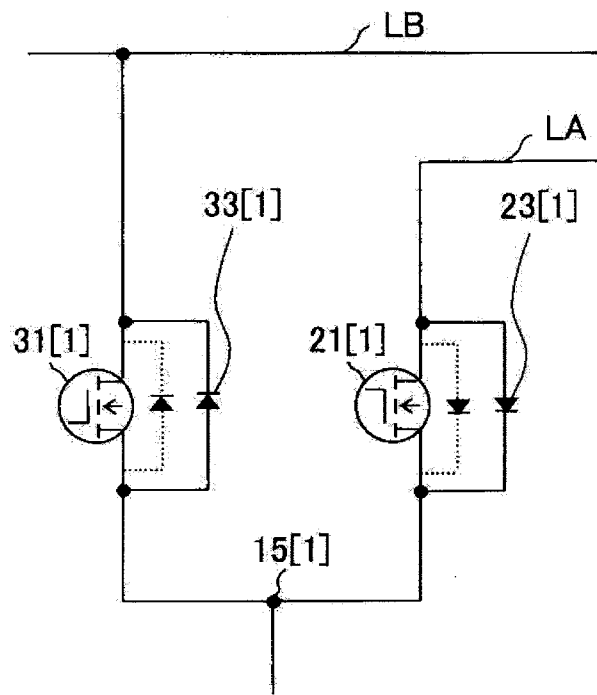
[Fig. 10]

FIG. 10



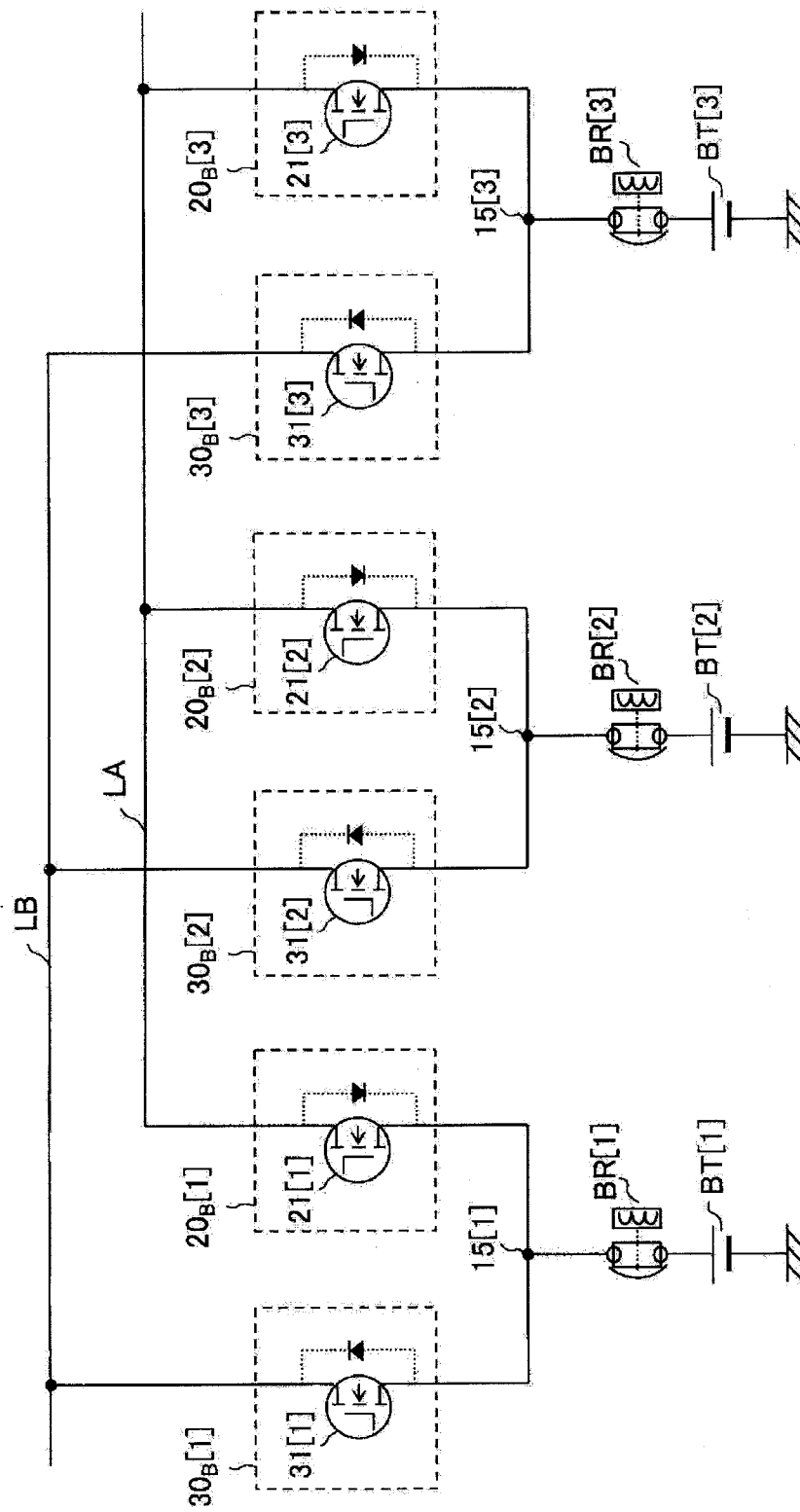
[Fig. 11]

FIG. 11



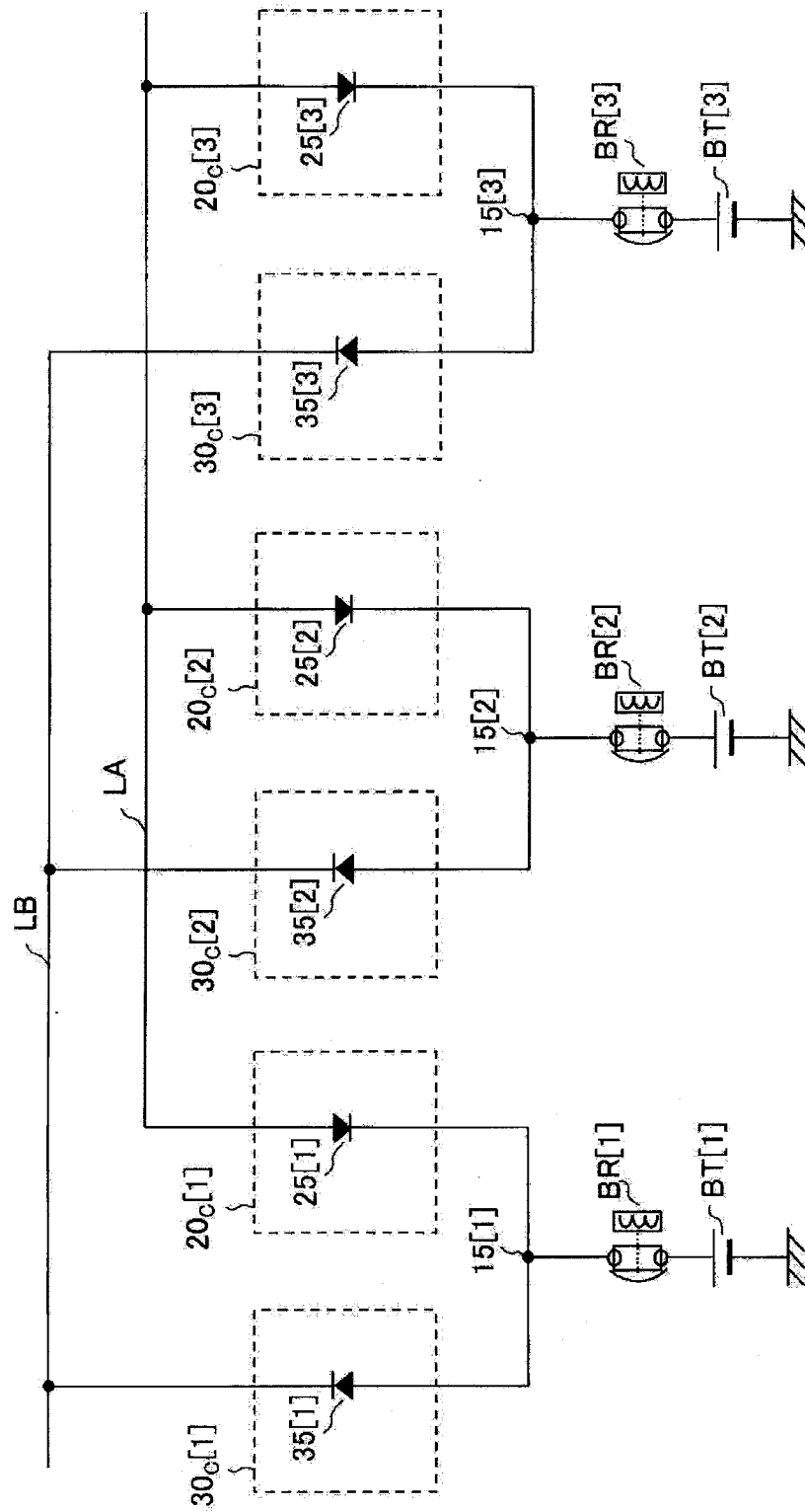
[Fig. 12]

FIG. 12



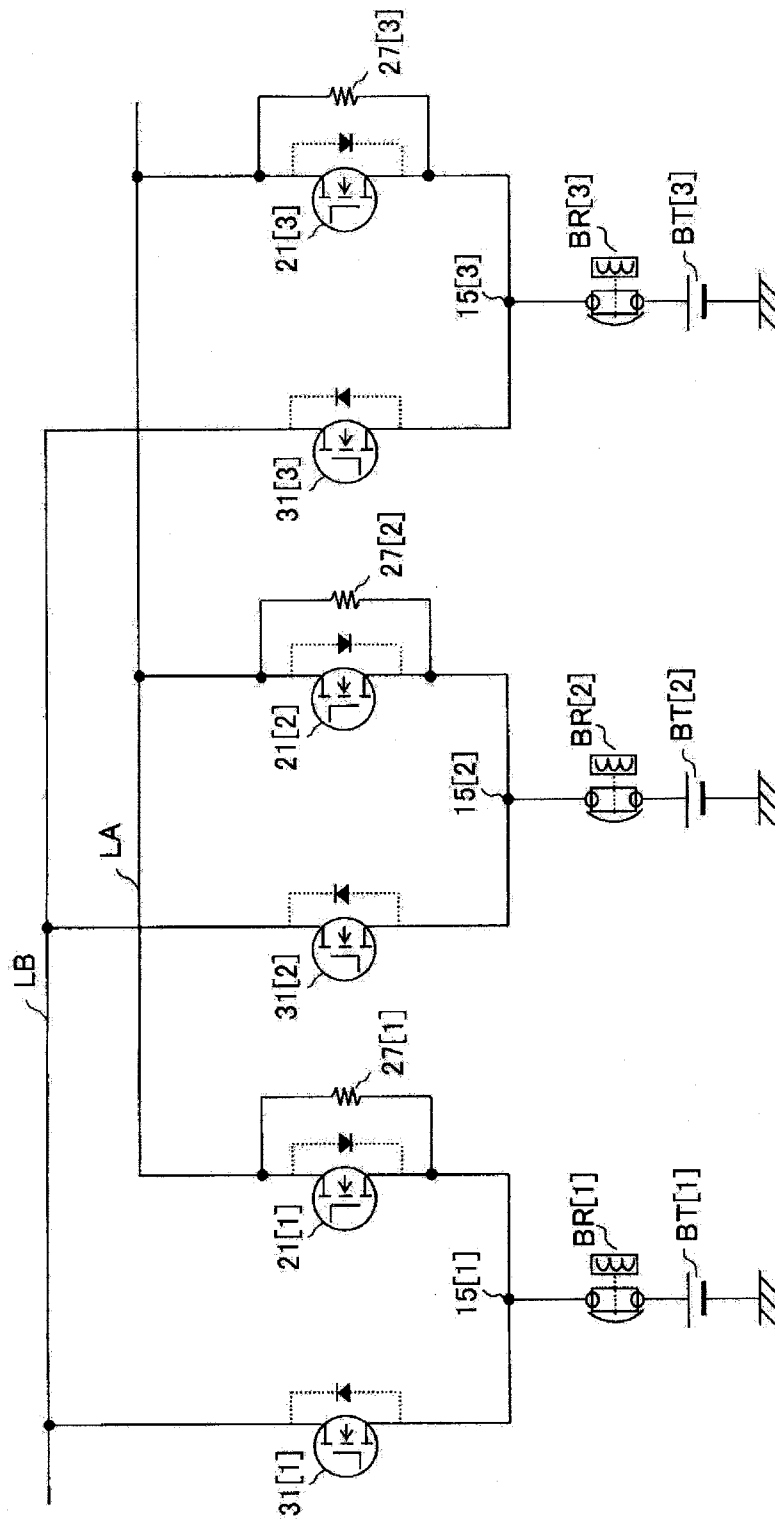
[Fig. 13]

FIG. 13



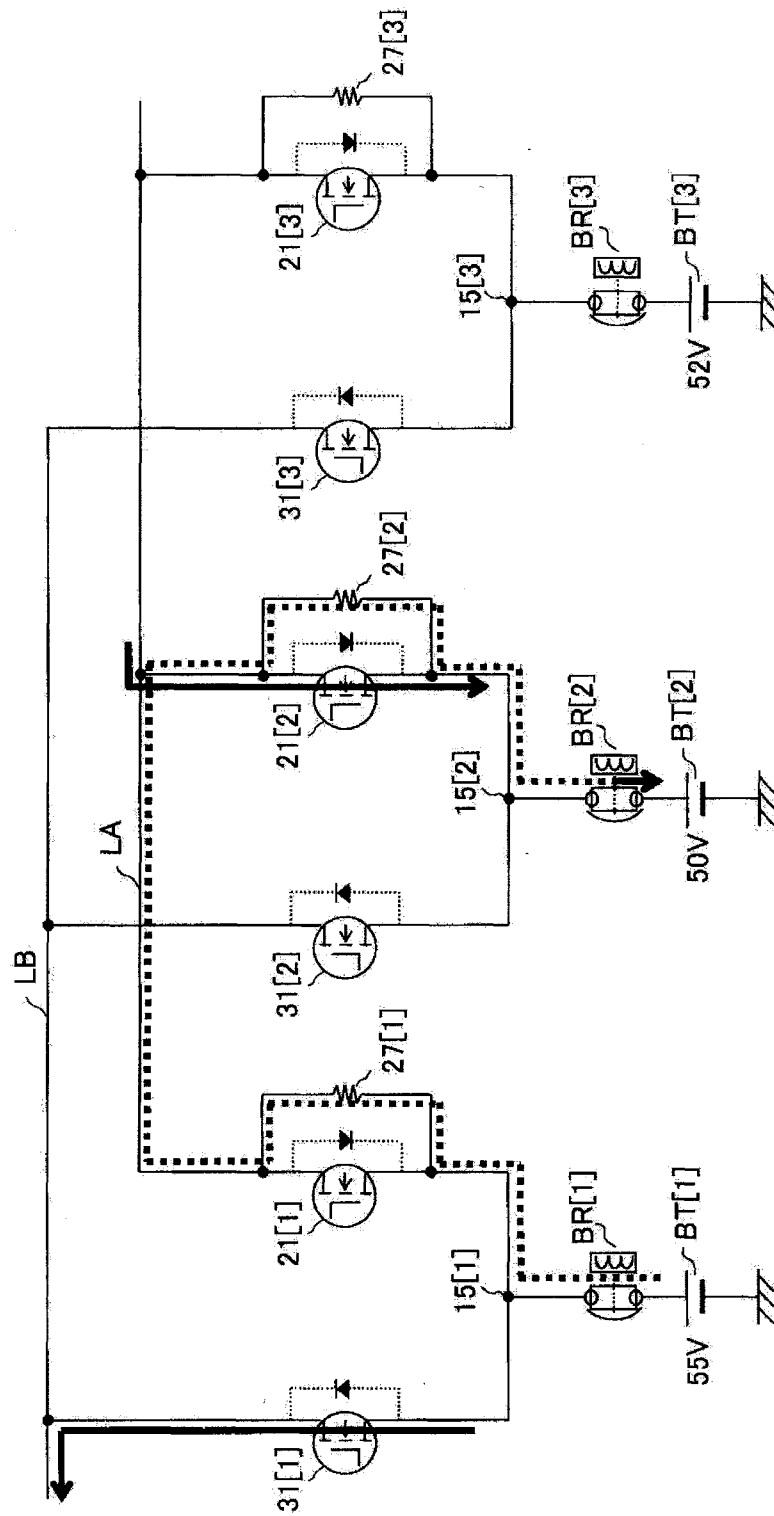
[Fig. 14]

FIG. 14



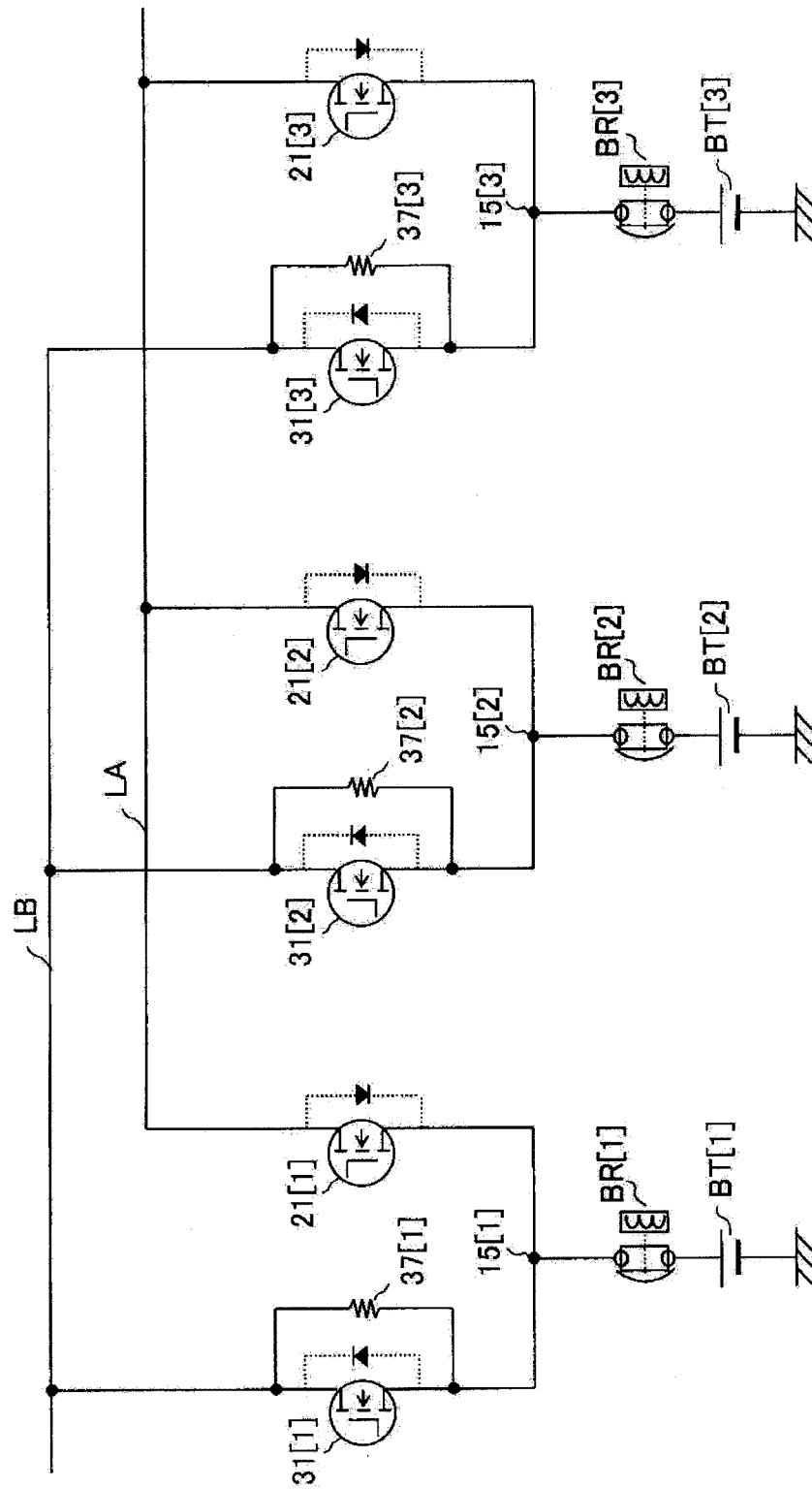
[Fig. 15]

FIG. 15



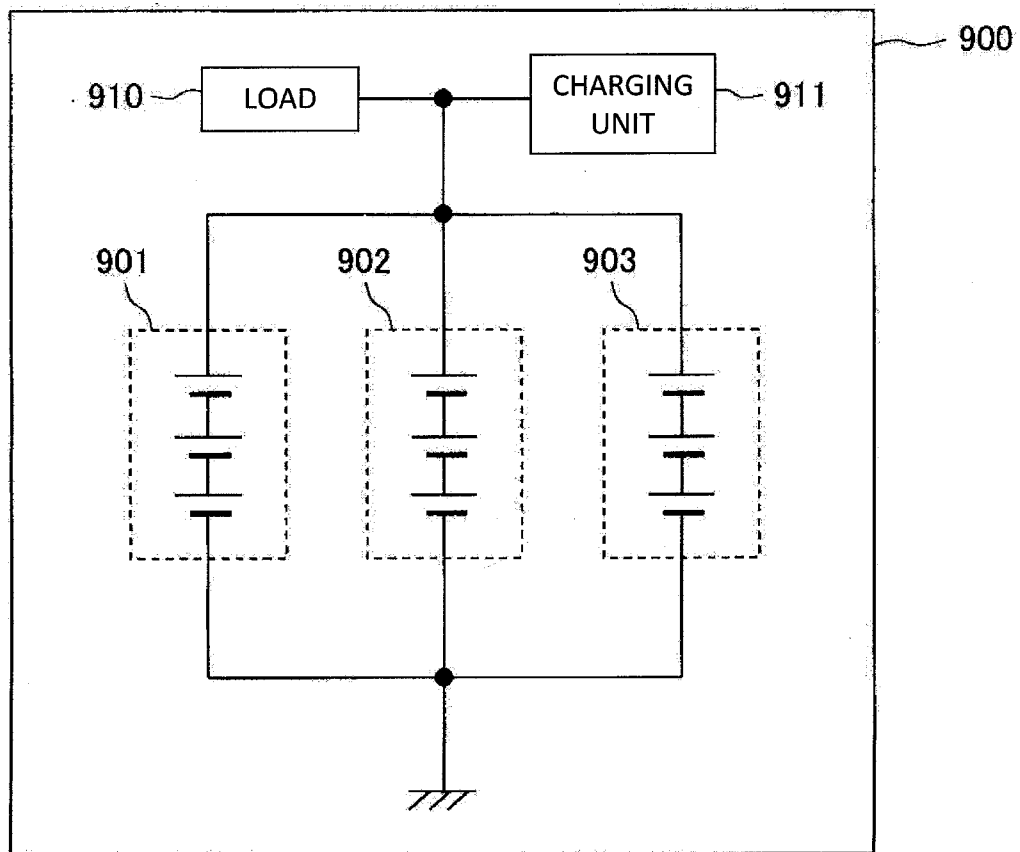
[Fig. 16]

FIG. 16



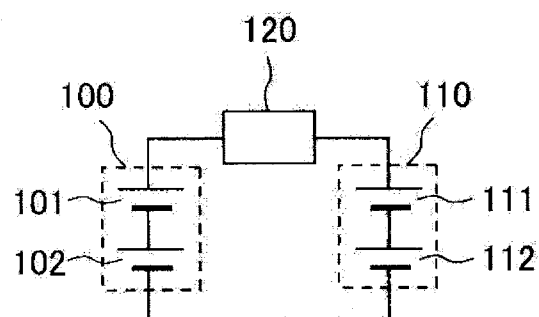
[Fig. 17]

FIG. 17



[Fig. 18]

FIG. 18



[Fig. 19]

FIG. 19

APPLIED VOLTAGE [V]	CURRENT [A]	TEMPERATURE [°C]	RESISTANCE [Ω]	HEATING VALUE [W]
26	0.11	135.5	236.4	2.86
24	0.12	134.8	200.0	2.88
22	0.13	134.2	169.2	2.86
20	0.15	133.3	133.3	3
18	0.16	132.6	112.5	2.88
16	0.18	131.8	88.9	2.88
14	0.2	130.7	70.0	2.8
12	0.24	129.7	50.0	2.88
10	0.28	128.3	35.7	2.8
8	0.34	126.2	23.5	2.72
6	0.42	121.2	14.3	2.52
4	0.52	104.6	7.7	2.08
0	0	-	6.0	0

[Fig. 20]

FIG. 20A

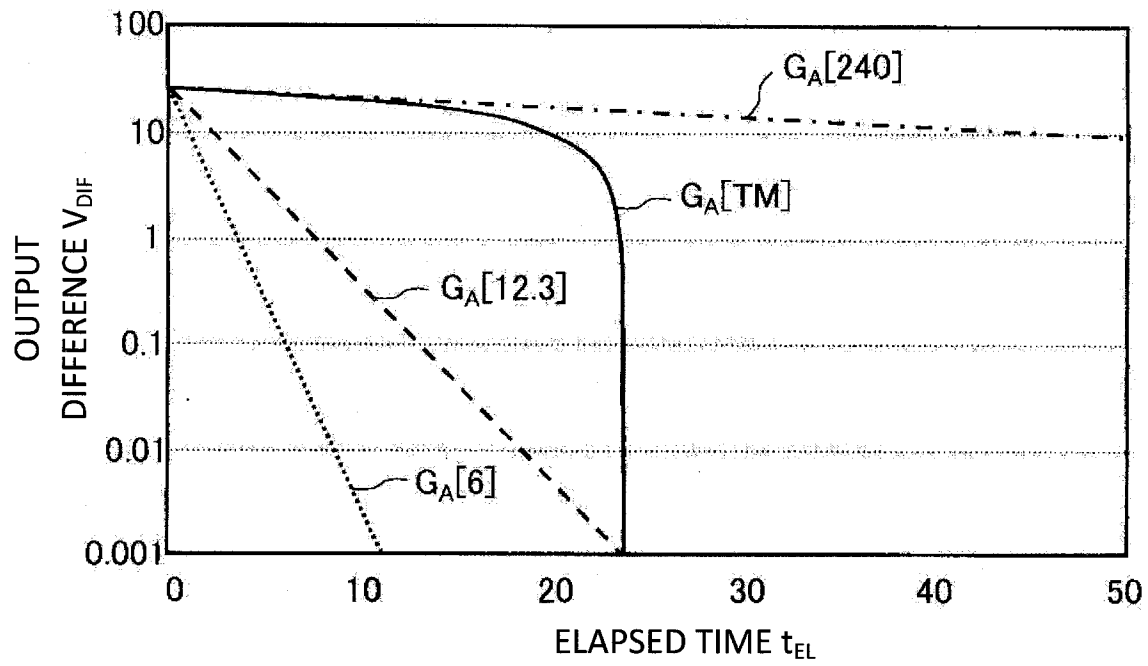
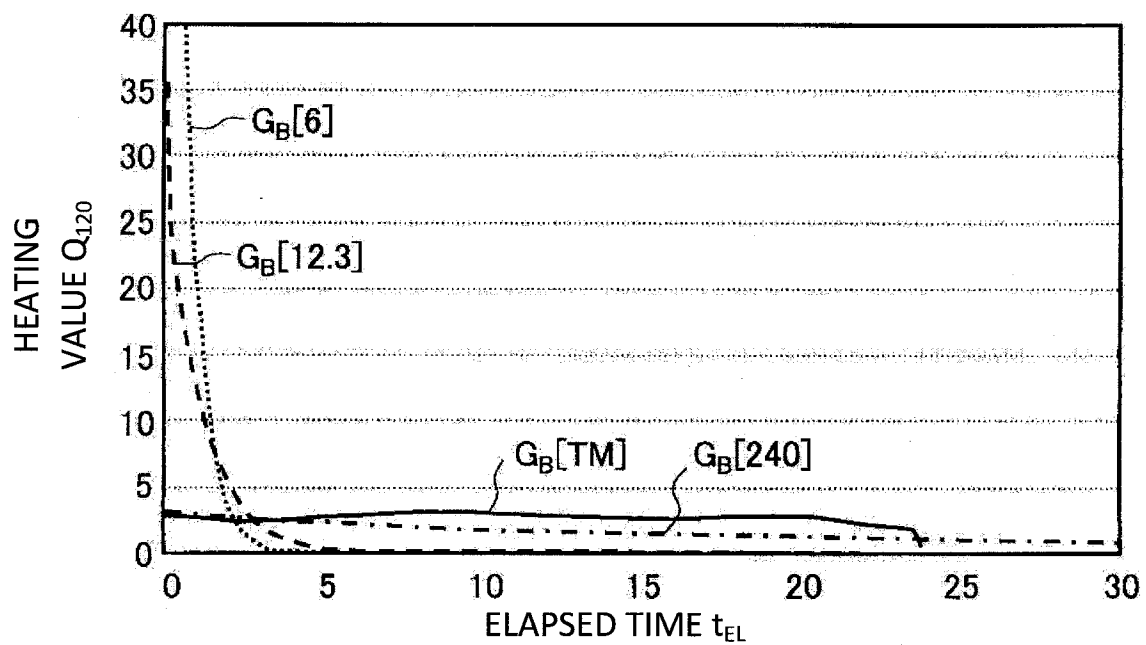


FIG. 20B



[Fig. 21]

FIG. 21A

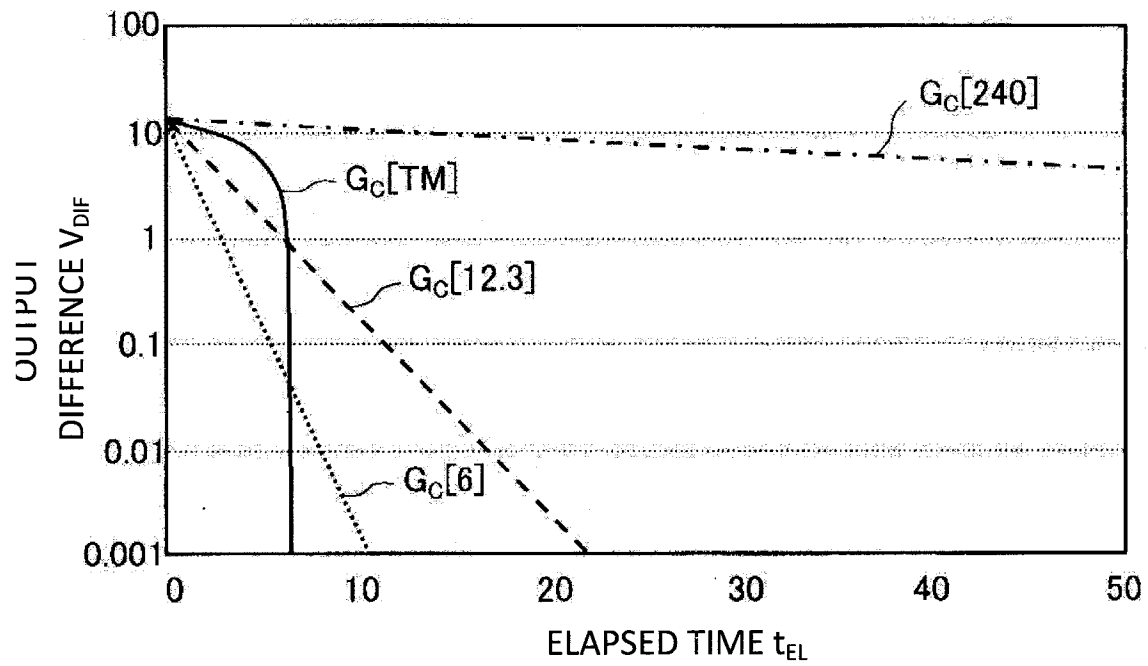
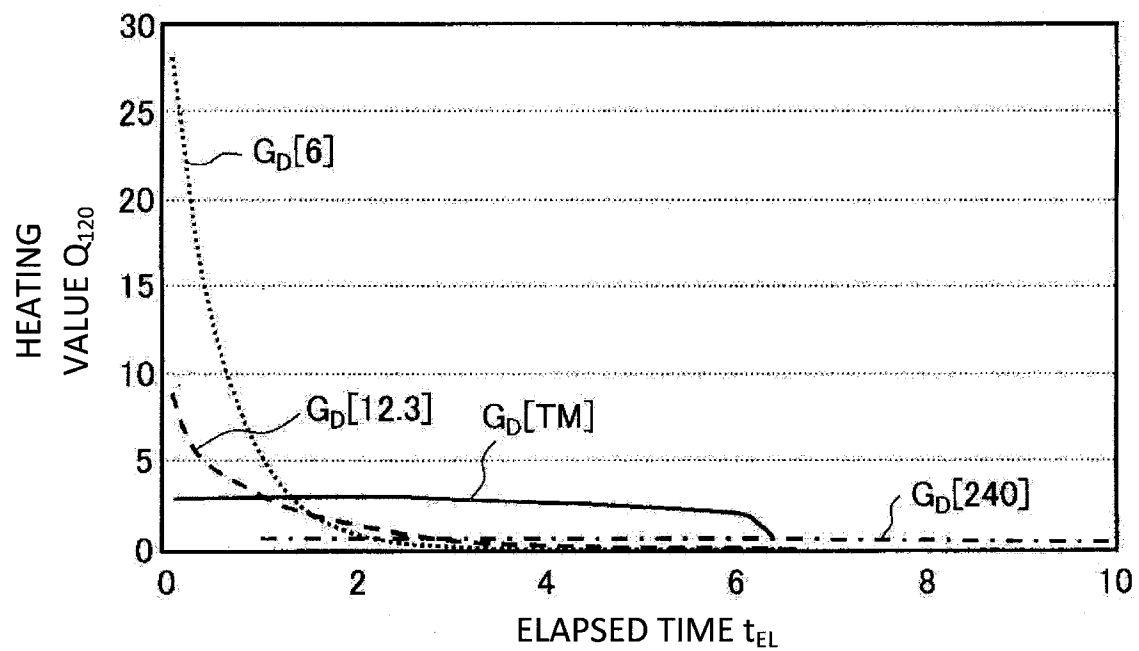


FIG. 21B



INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2011/004481

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. H02J7/02 (2006.01) i, H01M10/44 (2006.01) i, H02J7/00 (2006.01) i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. H02J7/02, H01M10/44, H02J7/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
 Published unexamined utility model applications of Japan 1971-2011
 Registered utility model specifications of Japan 1996-2011
 Published registered utility model applications of Japan 1994-2011

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y A	JP 9-140065 A (Sony Corporation) 1997.05.27, a bstract, [0017]-[0044], [0055]-[0074], Figs.1-4, 11, 12 & US 5760570 A & BR 9605505 A	1-3, 10-13, 20 4, 6 5, 7, 15, 17
X Y A	JP 2009-148099 A (Panasonic Electric Works Co., Ltd.) 2009.07.02, [0035]-[0042], Figs. 3, 4 (No Family)	11, 12, 14, 20 4 5, 7, 15, 17
X Y A A	JP 6-284589 A (NIPPON MORISERU KK) 1994.10.07, [0002]-[0004], [0026]-[0029], Figs.7, 13 (No Family)	1, 10-13, 16, 20 6 5, 7, 15, 17
A	JP 2006-136061 A (Sony Corporation) 2006.05.25, [0015], Fig.1 (No Family)	8, 9, 18, 19

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Date of the actual completion of the international search

07.11.2011

Date of mailing of the international search report

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