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(54) Title: SEMICONDUCTOR DEVICES, MAGNETIC TUNNEL JUNCTIONS, AND METHODS OF FABRICATION THEREOF

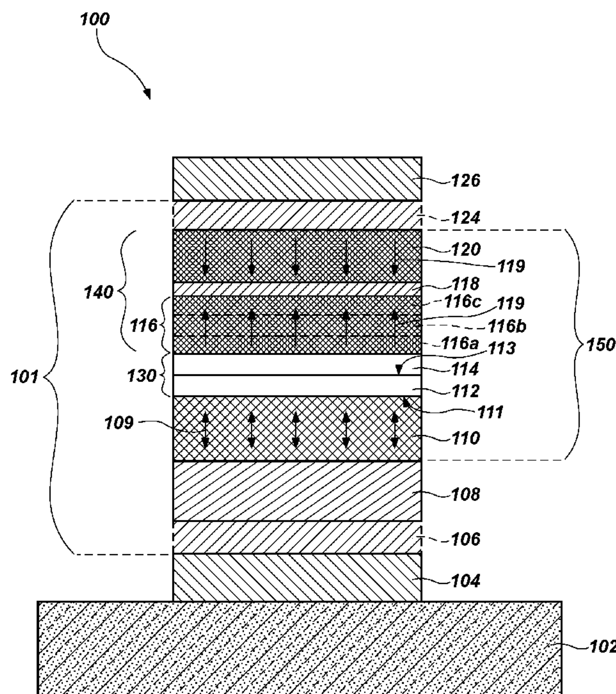

FIG. 1

(57) Abstract: A semiconductor device comprises an array of magnetic cell structures each comprising a magnetic tunnel junction over an electrode on a substrate. Each of the magnetic tunnel junctions includes a magnetic material over the substrate, a first tunnel barrier material over the magnetic material, a second tunnel barrier material over the annealed first tunnel barrier material, and another magnetic material over the second tunnel barrier material. Each magnetic tunnel junction is configured to exhibit a tunnel magnetoresistance greater than or equal to about 180% at a resistance area product of less than about 8 ohm m^2. The semiconductor device also includes another electrode over the another magnetic material. Semiconductor devices including the magnetic tunnel junctions, methods of forming the magnetic tunnel junctions, and methods of forming semiconductor devices including the magnetic tunnel junctions are disclosed.

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SEMICONDUCTOR DEVICES, MAGNETIC TUNNEL JUNCTIONS, AND METHODS OF FABRICATION THEREOF

PRIORITY CLAIM

5 This application claims the benefit of the filing date of United States Patent Application Serial No. 14/597,903, filed January 15, 2015, for "Semiconductor Devices, Magnetic Tunnel Junctions, and Methods of Fabrication Thereof."

TECHNICAL FIELD

10 Embodiments disclosed herein relate to semiconductor devices including magnetic memory cells having a magnetic tunnel junction and methods of forming such devices and magnetic tunnel junctions. More specifically, embodiments disclosed herein relate to magnetic tunnel junctions exhibiting a low resistance area product at a high tunnel magnetoresistance, semiconductor devices including the magnetic tunnel junctions, and 15 methods of forming the magnetic tunnel junctions and semiconductor devices.

BACKGROUND

Magnetic Random Access Memory (MRAM) is a non-volatile memory technology based on magnetoresistance. One type of MRAM is spin torque transfer MRAM 20 (STT-MRAM), in which a magnetic cell core includes a magnetic tunnel junction ("MTJ") sub-structure with at least two magnetic regions, for example, a "fixed region" and a "free region," with a non-magnetic region (*e.g.*, a tunnel barrier material) between. The free region and the fixed region may exhibit magnetic orientations that are either horizontally oriented ("in-plane") or perpendicularly oriented ("out-of-plane") relative to the thickness of the 25 regions. The fixed region includes a magnetic material that has a substantially fixed (*e.g.*, a non-switchable) magnetic orientation. The free region, on the other hand, includes a magnetic material that has a magnetic orientation that may be switched, during operation of the cell, between a "parallel" configuration and an "anti-parallel" configuration. In the parallel configuration, the magnetic orientations of the fixed region and the free region are directed in 30 the same direction (*e.g.*, north and north, east and east, south and south, or west and west, respectively). In the "anti-parallel" configuration, the magnetic orientations of the fixed region and the free region are directed in opposite directions (*e.g.*, north and south, east and west, south and north, or west and east, respectively). In the parallel configuration, the

STT-MRAM cell exhibits a lower electrical resistance across the magnetoresistive elements (*e.g.*, the fixed region and free region), defining a "0" logic state of the MRAM cell. In the anti-parallel configuration, the STT-MRAM cell exhibits a higher electrical resistance across the magnetoresistive elements, defining a "1" logic state of the STT-MRAM cell.

5 Switching of the magnetic orientation of the free region may be accomplished by passing a programming current through the magnetic cell core, including the fixed and free regions. The fixed region polarizes the electron spin of the programming current, and torque is created as the spin-polarized current passes through the core. The spin-polarized electron current exerts the torque on the free region. When the torque of the spin-polarized electron
10 current is greater than a critical switching current density (J_c) of the free region, the direction of the magnetic orientation of the free region is switched. Thus, the programming current can be used to alter the electrical resistance across the magnetic regions. The resulting high or low electrical resistance states across the magnetoresistive elements enable the write and read operations of the MRAM cell. After switching the magnetic orientation of the free region to
15 achieve the one of the parallel configuration and the anti-parallel configuration associated with a desired logic state, the magnetic orientation of the free region is usually desired to be maintained, during a "storage" stage, until the MRAM cell is to be rewritten to a different configuration (*i.e.*, to a different logic state).

Switching of the magnetic orientation of the free region of a magnetic memory cell
20 including a MTJ may be affected by the tunnel magnetoresistance ("TMR") and the resistance area product ("RA") of the cell. The TMR of a MTJ is a function of the resistance between a top electrode and a bottom electrode, between which the MTJ is disposed, in the high electrical resistance state and the low electrical resistance state. Specifically, the TMR measures the difference between a cell's electrical resistance in the anti-parallel configuration
25 (R_{ap}) and its electrical resistance in the parallel configuration (R_p) to R_p (*i.e.*, TMR = $(R_{ap} - R_p)/R_p$). Thus, the TMR is equivalent to the change in resistance observed by changing the magnetic state of the free layer. Generally, a MTJ with a homogeneous crystal structure (*e.g.*, a bcc (001) crystal structure), having few structural defects in the microstructure of its magnetic material, has a higher TMR than a MTJ with structural defects. A cell with high
30 TMR may have a high read-out signal, which may speed the reading of the MRAM cell during operation. A higher TMR is preferred for reliable read operation as it will generate a larger signal difference between the on and off states of the cell. In other words, the higher

the TMR, the more sensitive the device, and the easier to distinguish logic states of an associated memory cell.

Another significant characteristic of a magnetic memory cell core includes the RA. The RA of a magnetic memory cell is an indication of the voltage used to switch the magnetic orientation of the free region during programming (*e.g.*, the threshold switching voltage). An increase in the RA of a magnetic memory cell may degrade the performance of the cell by utilizing a higher threshold switching voltage, reducing the usable life of the cell. The RA may be decreased by decreasing a thickness of the tunnel barrier material. However, decreasing the thickness of the tunnel barrier material may also decrease the TMR. Thus, although a high TMR and a low RA are desired, in general, an increase in the TMR of a MTJ is obtained at the expense of a higher RA. A conventional MTJ exhibits a TMR of less than about 120% at an RA of greater than about 4 ohm μm^2.

Efforts to increase the TMR of a MTJ while maintaining a low RA include attempts to reduce structural defects in the crystal structure of the MTJ. For example, a magnesium oxide tunnel barrier material may be formed at elevated temperatures to produce the tunnel barrier material having stoichiometric proportions and minimal oxygen vacancies or interstitial oxygen. However, the elevated temperatures may undesirably cause an underlying magnetic material to crystalize in an undesired crystal orientation. A mismatch in crystal orientation of the magnetic material and the tunnel barrier material undesirably increases the RA and decreases the TMR of the MTJ. The increase in the RA increases the voltage required to switch the magnetic orientation of the free region during programming, increases the junction resistance, and increases the threshold switching voltage of the device. A decrease in the TMR reduces the effective spin-polarization of the electrons as they pass through the MTJ, reducing tunneling through the MTJ.

Alternatively, the tunnel barrier material may be formed at lower temperatures. However, when the tunnel barrier material is formed at lower temperatures, defects, such as oxygen vacancies and interstitial oxygen atoms, within the tunnel barrier material increase. The atomic defects in the tunnel barrier material may degrade device performance by causing electrons to scatter as they travel through the MTJ and reducing the TMR of the MTJ.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a simplified cross-sectional view of a magnetic cell structure according to an embodiment of the disclosure;

FIG. 2 is a simplified cross-sectional view of a magnetic material including alternating portions of a magnetic material and a conductive material;

FIG. 3 is a simplified cross-sectional view of a magnetic cell structure according to another embodiment of the disclosure;

5 FIG. 4 is a simplified cross-sectional view of a magnetic cell structure according to an embodiment of the present disclosure, wherein the fixed region and the free region exhibit in-plane magnetic orientations;

FIGS. 5A through FIG. 5C are simplified cross-sectional views illustrating different process stages for an embodiment of a method for forming the magnetic cell structure of

10 FIG. 1;

FIG. 6 is a schematic of an STT-MRAM system including a memory cell having a magnetic cell structure according to an embodiment of the disclosure;

FIG. 7 is a simplified block diagram of a semiconductor device including memory cells having a magnetic cell structure according to an embodiment of the present disclosure;

15 FIG. 8 is a simplified block diagram of a system implemented according to one or more embodiments of the present disclosure;

FIG. 9 is a graphical representation comparing the TMR vs. the RA of magnetic tunnel junctions formed according to embodiments of the present disclosure and magnetic tunnel junctions formed by conventional methods; and

20 FIG. 10 is a graphical representation of the TMR vs. the RA of magnetic tunnel junctions formed according to embodiments of the present disclosure.

MODE(S) FOR CARRYING OUT THE INVENTION

The illustrations included herewith are not meant to be actual views of any particular

25 systems or semiconductor structures, but are merely idealized representations that are employed to describe embodiments described herein. Elements and features common between figures may retain the same numerical designation.

The following description provides specific details, such as material types, material thicknesses, and processing conditions in order to provide a thorough description of

30 embodiments described herein. However, a person of ordinary skill in the art will understand that the embodiments disclosed herein may be practiced without employing these specific details. Indeed, the embodiments may be practiced in conjunction with conventional fabrication techniques employed in the semiconductor industry. In addition, the description

provided herein does not describe a complete process flow for manufacturing semiconductor devices, magnetic tunnel junctions, or magnetic memory cells, and the semiconductor devices, magnetic tunnel junctions, and magnetic memory cells described below do not form a complete semiconductor device, magnetic tunnel junction, or magnetic memory cell. Only
5 those process acts and structures necessary to understand the embodiments described herein are described in detail below. Additional acts to form a complete semiconductor device and a magnetic memory cell including the semiconductor device may be performed by conventional techniques.

According to some embodiments, a semiconductor device may include a magnetic cell
10 structure comprising a MTJ. The MTJ may include a tunnel barrier material disposed between adjacent magnetic materials. A magnetic material may overlie a substrate and the tunnel barrier material may overlie the magnetic material. Another magnetic material may overlie the tunnel barrier material. The tunnel barrier material may exhibit the same crystal orientation as the adjacent magnetic materials. The semiconductor device including the MTJ
15 may exhibit a high TMR, such as greater than about 180%, at a low RA, such as at less than about 8 ohm μm^2.

The tunnel barrier material according to embodiments of the disclosure may include at least two portions. A first portion of the tunnel barrier material may be formed over the magnetic material at a first temperature. The first portion of the tunnel barrier material and the
20 magnetic material may be annealed to crystallize the magnetic material and orient the crystal structure of the magnetic material in alignment with the crystal structure of the first portion of the tunnel barrier material. The magnetic material and the first portion of the tunnel barrier material may be annealed at a temperature between about 300°C and about 600°C for an amount of time sufficient to crystallize the magnetic material. After annealing, a second
25 portion of the tunnel barrier material may be formed over the first portion at a second temperature, which is higher than the first temperature at which the first portion of the tunnel barrier material is formed. The tunnel barrier material including the first portion and the second portion may exhibit a higher TMR, such as greater than about 180%, at a low RA, such as at less than about 8 ohm μm^2, than a conventional tunnel barrier material. The tunnel
30 barrier material may also be thicker and exhibit the higher TMR than a conventional tunnel barrier material, while maintaining the low RA. In some embodiments, the RA of the tunnel barrier material is between about 4 ohm μm^2 and about 8 ohm μm^2 and the TMR of the tunnel barrier material is between about 180% and about 205%.

Referring to FIG. 1, a magnetic memory cell 100 including a magnetic cell core 101 according to some embodiments is illustrated. The magnetic cell core 101 may include a magnetic tunnel junction 150 and may be disposed between a lower electrode 104 and an upper electrode 126 over a substrate 102. The MTJ 150 may include a magnetic region and
5 another magnetic region, for example, a "free region 110" and a "fixed region" 140, respectively. A tunnel barrier material 130 may be disposed between the free region 110 and the fixed region 140.

The substrate 102 may include a base material or other construction upon which components, such as those within memory cells, are formed. The substrate 102 may be a
10 semiconductor substrate, a base semiconductor material on a supporting substrate, a metal electrode, or a semiconductor substrate having one or more materials, structures, or regions formed thereon. The substrate 102 may be a conventional silicon substrate or other bulk substrate including semiconductor material. As used herein, the term "bulk substrate" means and includes not only silicon wafers, but also silicon-on-insulator ("SOI") substrates, such as
15 silicon-on-sapphire ("SOS") substrates or silicon-on-glass ("SOG") substrates, epitaxial layers of silicon on a base semiconductor foundation, or other semiconductor or optoelectronic materials, such as silicon-germanium ($Si_{1-x}Ge_x$, where x is, for example, a mole fraction between 0.2 and 0.8), germanium (Ge), gallium arsenide (GaAs), gallium nitride (GaN), or indium phosphide (InP), among others. Furthermore, when reference is made to a "substrate"
20 in the following description, previous process stages may have been utilized to form materials, regions, or junctions in the base semiconductor structure or foundation.

The lower electrode 104 may overlie the substrate 102. The lower electrode 104 may include a metal such as copper, tungsten, platinum, palladium, titanium, tantalum, nickel, titanium nitride (TiN), tantalum nitride (TaN), tungsten nitride (WN), polysilicon, a metal
25 silicide, a metal alloy, or combinations thereof.

One or more lower intermediary regions 106 may, optionally, be disposed under the magnetic regions (*e.g.*, the free region 110 and the fixed region 140). The lower intermediary region 106, if included, may be configured to inhibit diffusion of species between the lower electrode 104 and materials overlying the lower electrode 104. The lower intermediary
30 region 106 may include a conductive material such as one or more of copper, tantalum, titanium, tungsten, ruthenium, tantalum nitride, and titanium nitride.

A seed material 108 may overlie the lower intermediary region 106, if present, or the lower electrode 104 if the lower intermediary region 106 is not present. The seed material 108

may include tantalum, platinum, ruthenium, iron, nickel, cobalt, chromium, titanium, zirconium, vanadium, copper, zinc, rhodium, silver, hafnium, tungsten, iridium, tantalum nitride, and combinations thereof. By way of non-limiting example, the seed material 108 may include tungsten and at least one of iron, cobalt, nickel, or another suitable material. In 5 other embodiments, the seed material 108 may include iron and cobalt and may further include at least one transition element, such as tantalum, platinum, ruthenium, nickel, chromium, titanium, zirconium, vanadium, copper, zinc, rhodium, silver, hafnium, and tungsten. In yet other embodiments, the seed material 108 may include at least one of hafnium, zirconium, and tantalum and at least one of iron, cobalt, and nickel, such as FeHf. 10 The seed material 108 may be a homogeneous composition of the seed material 108 or may include distinct portions of one or more of tantalum, platinum, ruthenium, iron, nickel, cobalt, chromium, titanium, zirconium, vanadium, copper, zinc, rhodium, silver, hafnium, tungsten, and iridium adjacent to a distinct portion of another of tantalum, platinum, ruthenium, iron, nickel, cobalt, chromium, titanium, zirconium, vanadium, copper, zinc, rhodium, silver, 15 hafnium, tungsten, and iridium.

The free region 110 may overlie the seed material 108. In some embodiments, the free region 110 directly overlies and contacts the seed material 108. The free region 110 may include a magnetic material exhibiting a switchable magnetic orientation, indicated by arrows 109, during use and operation of the magnetic memory cell 100. The switchable 20 magnetic orientation may be switched between a parallel configuration and an anti-parallel configuration by the application of a current or applied field to the magnetic memory cell 100.

In some embodiments, the free region 110 may be a conventional free region. In other embodiments, the free region 110 may include alternating portions of a magnetic material and a conductive material. However, the free region 110 is not so limited and may include other 25 suitable magnetic materials that exhibit a switchable magnetic orientation.

In some embodiments, the free region 110 may include a ferromagnetic material including at least one of cobalt (Co) and iron (Fe) (*e.g.*, Co_xFe_y, wherein x = 10 to 80 and y = 10 to 80) and, in some embodiments, also boron (B) (*e.g.*, $Co_xFe_yB_z$, wherein x = 10 to 80, y = 10 to 80, and z = 0 to 50). Thus, the free region 110 may include at least one of Co, Fe, and B 30 (*e.g.*, a CoFeB material, a CoFe material, a FeB material, a CoB material, *etc.*). As used herein, the term "CoFeB material" means and includes a material comprising cobalt, iron, and boron (*e.g.*, $Co_xFe_yB_z$, wherein x = 10 to 80, y = 10 to 80, and z = 0 to 50). A CoFeB material may or may not exhibit magnetism, depending on its configuration (*e.g.*, its thickness). In

other embodiments, the free region 110 may alternatively or additionally include nickel (Ni) (*e.g.*, an NiB material). In some embodiments, the free region 110 may be substantially free of boron and may include, for example, CoFe. The CoFe may be formed as CoFeB and the boron may be diffused out of the free region 110 after formation thereof, or the CoFe may be
5 formed (*e.g.*, deposited) as CoFe, without any boron.

The free region 110 may be homogeneous, or may include one or more sub-regions (*e.g.*, a CoFeB material, with sub-regions having different relative atomic ratios of Co, Fe, and B).

A tunnel barrier material 130 may overlie the free region 110. In some embodiments,
10 the tunnel barrier material 130 directly overlies and contacts the free region 110. The tunnel barrier material 130 may include a nonmagnetic, crystalline material, such as magnesium oxide (MgO), aluminum oxide (Al_2O_3), titanium dioxide (TiO_2), tantalum oxide (Ta_2O_5), ruthenium oxide (RuO_2), boron oxide (B_2O_3), or combinations thereof. The tunnel barrier material 130 may be configured to induce interfacial magnetic anisotropy in the free
15 region 110 and the fixed region 140 and may also be configured to function as a tunnel region of the MTJ 150 effected by interaction of the free region 110, the tunnel barrier material 130, and the fixed region 140.

The tunnel barrier material 130 may include a first portion 112 and a second portion 114. The first portion 112 may overlie the free region 110. In some embodiments, the
20 first portion 112 directly overlies and contacts the free region 110. The first portion 112 may be formed over the free region 110 to form an interface 111 between the free region 110 and the tunnel barrier material 130. A crystal orientation of the MTJ 150 may not change at the interface 111 between the first portion 112 and the free region 110. By way of example and not limitation, each of the free region 110 and the first portion 112 may exhibit a bcc (001)
25 crystal structure. As described in more detail below, each of the first portion 112 and the free region 110 may be amorphous (*e.g.*, not crystalline) as formed, with the desired crystal structure occurring following an anneal. In some embodiments, the first portion 112 is an oxide material and may include MgO, Al_2O_3, TiO_2, Ta_2O_5, RuO_2, B_2O_3, or combinations thereof.

30 The second portion 114 may overlie the first portion 112. In some embodiments, the second portion 114 directly overlies and contacts the first portion 112. An interface 113 between the first portion 112 and the second portion 114 may be smooth and exhibit the same crystal orientation as the first portion 112 and the free region 110 (*e.g.*, a bcc (001) crystal

structure). The second portion 114 may be an oxide material and may include MgO, Al_2O_3, TiO_2, Ta_2O_5, RuO_2, B_2O_3, or combinations thereof. The first portion 112 and the second portion 114 may include the same material. In some embodiments, the first portion 112 and the second portion 114 include MgO. In some such embodiments, the second portion 114
5 includes a ratio of oxygen to magnesium closer to stoichiometric (*e.g.*, 1:1) than the first portion 112. Thus, the second portion 114 may have less oxygen vacancies and less interstitial oxygen and also a higher density than the first portion 112. The second portion 114 may exhibit less structural defects than the first portion 112 and, in some embodiments, may exhibit a higher TMR and a lower RA than the first portion 112.

10 The tunnel barrier material 130 may have a total thickness (*i.e.*, a sum of a thickness of the first portion 112 and a thickness of the second portion 114) of between about 10 Å and about 30 Å, such as between about 10 Å and about 15 Å, between about 15 Å and about 20 Å, between about 20 Å and about 25 Å, or between about 25 Å and about 30 Å. The tunnel barrier material 130 may have a thickness of between about 10 Å and about 20 Å. In some
15 embodiments, the thickness of the tunnel barrier material 130 is about 18 Å.

The first portion 112 and the second portion 114 may have the same thickness, the first portion 112 may have a greater thickness than the second portion 114, or the second portion 114 may have a greater thickness than the first portion 112. The RA and the TMR of the MTJ 150 may be tailored by altering the thickness of the first portion 112 relative to the
20 thickness of the second portion 114 of the tunnel junction material 130. A ratio of the thickness of the first portion 112 to the thickness of the second portion 114 may be between about 0.9 and about 2.0, such as between about 0.9 and about 1.0, between about 1.0 and about 1.25, between about 1.25 and about 1.5, between about 1.2 and about 1.8, or between about 1.5 and about 2.0. In some embodiments, the ratio is between about 1.0 and about 1.5
25 and the total thickness of the tunnel barrier material 130 is about 18 Å.

The tunnel barrier material 130 having the first portion 112 and the second portion 114 may exhibit a TMR of between about 180% and about 600%, such as between about 180% and about 200%, between about 180% and about 225%, between about 180% and about 300%, between about 200% and about 220%, between about 220% and about 250%, between
30 about 250% and about 300%, between about 300% and about 400%, or between about 400% and about 600%. In some embodiments, the TMR is between about 180% and about 300%. The tunnel barrier material 130 may exhibit a RA of between about 3 ohm μm^2 and about 8 ohm μm^2, such as between about 3 ohm μm^2 and about 4 ohm μm^2, between about 4 ohm

μm^2 and about 5 ohm μm^2, between about 5 ohm μm^2 and about 6 ohm μm^2, between about 6 ohm μm^2 and about 7 ohm μm^2, or between about 7 ohm μm^2 and about 8 ohm μm^2. In some embodiments, the RA is between about 6 ohm μm^2 and about 7 ohm μm^2. In other embodiments, the tunnel barrier material 130 exhibits an RA of between about 4 ohm μm^2 and about 8 ohm μm^2 and a TMR of between about 180% and about 205%. By way of non-limiting example, the tunnel barrier material 130 may exhibit a RA of about 4 ohm μm^2 and a TMR of about 180%, or a RA of about 8 ohm μm^2 and a TMR of about 205% at a thickness of between about 10 Å and about 20 Å.

The fixed region 140 may overlie the tunnel barrier material 130. In some embodiments, the fixed region 140 directly overlies and contacts the second portion 114 of the tunnel barrier material 130.

The fixed region 140 may include one or more magnetic materials and, optionally, one or more non-magnetic materials. For example, the fixed region 140 may be configured as a synthetic antiferromagnet including a sub-region of ruthenium or tantalum adjoined by magnetic sub-regions. The magnetic sub-regions may include a material including cobalt, and at least one of palladium and platinum, and combinations thereof, a CoFeB material, and combinations thereof. Alternatively, the fixed region 140 may be configured with structures of alternating sub-regions of magnetic material and coupler material. Each of the magnetic sub-regions may include one or more materials and one or more regions therein. As another example, the fixed region 140 may be configured as a single, homogeneous magnetic material. Accordingly, the fixed region 140 may have uniform magnetization, or sub-regions of differing magnetization that, overall, effect the fixed region 140 having a fixed magnetic orientation during use and operation of the magnetic memory cell 100.

The fixed region 140 may include a first magnetic portion 116 over the second portion 114 of the tunnel barrier material 130, a coupling material 118 over the first magnetic portion 116, and a second magnetic portion 120 over the coupling material 118. In some embodiments, the first magnetic portion 116 includes a first magnetic sub-region 116a that may include a CoFeB material overlying the second portion 114, a spacer 116b that may include a tantalum material overlying the first portion 116a, and a second magnetic sub-region 116c that may include a material including cobalt and at least one of palladium and platinum (*e.g.*, CoPd, CoPt) over the spacer 116b. The coupling material 118 may include a ruthenium material overlying the second magnetic sub-region 116c of the first magnetic portion 116. The second magnetic portion 120 may include a material including cobalt,

palladium, platinum, and combinations thereof, such as cobalt and at least one of palladium and platinum. In some embodiments, the second magnetic portion 120 includes the same material as the second magnetic sub-region 116c of the first magnetic portion 116.

In other embodiments, the first magnetic portion 116 includes an artificial superlattice structure and the second magnetic portion 120 includes another artificial superlattice structure overlying the coupling material 118. Referring to FIG. 2, the artificial superlattice structure of the first magnetic portion 116 may include alternating portions of a magnetic material 117 and a conductive material 115. The conductive material 115 may enable the magnetic material 117 to exhibit a perpendicular anisotropy (*i.e.*, a vertical magnetic orientation). The magnetic material 117 may include cobalt, iron, and combinations thereof. The conductive material 115 may include at least one of platinum, palladium, nickel, and iridium. In some embodiments, the magnetic material 117 includes cobalt and the conductive material 115 includes platinum. Although FIG. 2 depicts six regions of magnetic material 117 and six regions of conductive material 115 in the first magnetic portion 116, the artificial superlattice structure of the first magnetic portion 116 is not so limited and may include any number (*e.g.*, one, two, three, four, five, *etc.*) of alternating regions of magnetic material 117 and conductive material 115.

In some embodiments, a region of the conductive material 115 of the first magnetic portion 116 may directly overlie and contact the second portion 114 of the tunnel barrier material 130. For example, a region of the conductive material 115 may directly overlie and contact the second portion 114 of the tunnel barrier material 130. In other embodiments, a region of the magnetic material 117 may directly overlie and contact the second portion 114 of the tunnel barrier material 130.

Referring back to FIG. 1, the coupling material 118 may overlie the first magnetic portion 116. In some embodiments, the coupling material 118 directly overlies and contacts the first magnetic portion 116 (*e.g.*, the second magnetic sub-region 116c of the first magnetic portion 116). The coupling material 118 may include tantalum, ruthenium, rhodium, and combinations thereof. In some embodiments, the coupling material 118 is ruthenium. The coupling material 118 may have a thickness between about 1 Å and about 10 Å. In some embodiments, the coupling material 118 has a thickness between about 4 Å and about 5 Å.

The second magnetic portion 120 may directly overlie the coupling material 118. The second magnetic portion 120 may include the same materials and may be substantially the same as at least a portion of the first magnetic portion 116. In some embodiments, the second

magnetic portion 120 includes a material including cobalt and at least one of palladium and platinum and may include the same material as the second magnetic sub-region 116c of the first magnetic portion 116.

The first magnetic portion 116 and the second magnetic portion 120 of the fixed region 140 may include a fixed magnetic orientation, indicated by arrows 119. The fixed magnetic orientation may be north, south, east, west, *etc.* The fixed magnetic orientation of the first magnetic portion 116 and the second magnetic portion 120 may be the same or may be different.

One or more upper intermediary regions 124 may, optionally, be disposed over the fixed region 140. The upper intermediary region 124, if included, may be configured to inhibit diffusion of species between the upper electrode 126 and underlying materials during operation of the memory cell. The upper intermediary region 124 may include a conductive material (*e.g.*, one or more materials such as copper, tantalum, titanium, tungsten, ruthenium, tantalum nitride, titanium nitride) that may form a conductive capping region.

The upper electrode 126 may overlie the upper intermediary region 124. The upper electrode 126 may include copper, tungsten, platinum, palladium, titanium, tantalum, nickel, titanium nitride, tantalum nitride, tungsten nitride, polysilicon, a metal silicide, a metal alloy, or combinations thereof. In some embodiments, the upper electrode 126 includes the same materials as the lower electrode 104.

The magnetic memory cell 100 of FIG. 1 is configured as a "top pinned" memory cell (*i.e.*, a memory cell in which the fixed region 140 is disposed over the free region 110). However, in other embodiments, such as that of FIG. 3, a free region 110′ may overlie a fixed region 140′. Thus, with reference to FIG. 3, a magnetic memory cell 100′ including a MTJ 150′ may be configured as a "bottom pinned" memory cell. The magnetic memory cell 100′ may include a magnetic cell core 101′ disposed between the lower electrode 104 and the top electrode 126.

The magnetic memory cell 100′ may include a lower intermediary region 106 overlying the lower electrode 104. The seed material 108 may overlie the lower intermediary region 106, if present. In other embodiments, the seed material 108 may directly overlie and contact the lower electrode 104. The seed material 108 may be the same as described above with reference to FIG. 1.

The fixed region 140′ may directly overlie and contact the seed material 108. The fixed region 140′ may include a fixed magnetic orientation, indicated by arrows 119. The

fixed region 140′ may include the same materials described above with reference to fixed region 140. In some embodiments, the fixed region 140′ includes a second magnetic portion 120′, a coupling material 118′, and a first magnetic portion 116′. The first magnetic portion 116′ may include a first magnetic sub-region 116a′, a spacer 116b′, and a second
5 magnetic sub-region 116c′. The first magnetic sub-region 116a′, the spacer 116b′, and the second magnetic sub-region 116c′ may be the same as the first magnetic sub-region 116a, the spacer 116b, and the second magnetic sub-region 116c, respectively, described above with reference to FIG. 1. Each of the first magnetic portion 116′, the coupling material 118′, and the second magnetic portion 120′ may be the same as the first magnetic portion 116, the
10 coupling material 118, and the second magnetic portion 120, respectively, described above with reference to FIG. 1. However, the fixed region 140′ may not directly overlie the tunnel barrier material 130 as in the magnetic memory cell 100 of FIG. 1. Rather, the second magnetic portion 120′ of the fixed region 140′ may directly overlie and contact the underlying seed material 108. The coupling material 118′ may overlie the second magnetic portion 120′
15 and the first magnetic portion 116′ may overlie the coupling material 118′.

The tunnel barrier material 130 may overlie the fixed region 140′. The first portion 112 of the tunnel barrier material 130 may directly overlie and contact the fixed region 140′. The first portion 112 may be formed over the fixed region 140′ to form an interface 111′ between the fixed region 140′ and the tunnel barrier material 130. The fixed
20 region 140′ may exhibit a crystal structure that is aligned with a crystal structure of the first portion 112. By way of example and not limitation, each of the first portion 112 and the fixed region 140′ may exhibit a bcc (001) crystal structure without a change in the crystal structure of the MTJ 150′ at the interface 111′.

The tunnel barrier material 130 may include the same materials as described above
25 with reference to FIG. 1. Thus, each of the first portion 112 and the second portion 114 of the tunnel barrier material 130 may be the same as described above with reference to FIG. 1. An interface 113′ between the first portion 112 and the second portion 114 may be smooth and exhibit the same crystal orientation as the interface 111′ on which the first portion 112 is formed. The tunnel barrier material 130 may be disposed directly between the fixed
30 region 140′ and the free region 110′.

The free region 110′ may directly overlie and contact the tunnel barrier material 130. In some embodiments, the free region 110′ directly overlies and contacts the second portion 114 of the tunnel barrier material 130. The free region 110′ may include the same

materials as described above with reference to FIG. 1. The free region 110′ may include a switchable magnetic orientation, indicated by arrows 109.

The optional upper intermediary region 124 may overlie the free region 110′. The upper electrode 126 may overlie the upper intermediary region 124, if present.

5 The memory cells of embodiments of the disclosure may be configured as "out-of-plane" STT-MRAM cells. "Out-of-plane" STT-MRAM cells may include magnetic regions exhibiting a magnetic orientation that is predominately oriented in a vertical direction (*e.g.*, a direction that is perpendicular to a width and length of the respective region or a direction that is perpendicular to a primary surface of the substrate on which the STT-MRAM 10 cell is located). For example, as illustrated in FIG. 1 and FIG. 3, an STT-MRAM cell (*e.g.*, magnetic memory cell 100, magnetic memory cell 100′) may be configured to exhibit a vertical magnetic orientation in at least one of the magnetic regions (*e.g.*, the free region 110, 110′ and the fixed region 140, 140′). As indicated in FIG. 1 and FIG. 3, each of the free region 110, 110′ and the fixed region 140, 140′ may exhibit a vertical magnetic orientation as 15 indicated by the arrows 109 and the arrows 119. The magnetic orientation of the fixed region 140, 140′ may remain directed in essentially the same direction throughout use and operation of the STT-MRAM cell, for example, in the direction indicated by arrows 119. The magnetic orientation of the free region 110, 110′, on the other hand, may be switched during use and operation of the cell, between a parallel configuration and an anti-parallel 20 configuration, as indicated by the arrows 109. As another example, as illustrated in FIG. 4, an in-plane magnetic memory cell 100″ including a magnetic cell core 101″ may be configured to exhibit a horizontal magnetic orientation in at least one of the magnetic regions (*e.g.*, a free region 110″ and a fixed region 140″) of an MTJ 150″, as indicated by arrow 109′ in the free region 110″ and arrow 119′ in the fixed region 140″.

25 A semiconductor device may include at least one magnetic memory cell including the magnetic cell cores 101, 101′, 101″ of the disclosure disposed between a pair of electrodes.

Accordingly, a semiconductor device is disclosed. The semiconductor device comprises a magnetic tunnel junction over a seed material on a substrate, the magnetic tunnel junction exhibiting a tunnel magnetoresistance of between about 180% and about 300% and 30 comprising a magnetic material over the seed material, an oxide material over the magnetic material, another oxide material over the oxide material, the oxide material and the another oxide material having a thickness of between about 10 Å and about 20 Å, and another magnetic material over the another oxide material.

Referring to FIG. 5A through FIG. 5C, a method of forming the magnetic memory cell 100 of FIG. 1 is shown. The method may include forming a magnetic memory cell 200 over a substrate 202. A lower electrode material 204 may be formed over the substrate 202. The lower electrode material may include any of the materials described above with reference 5 to the lower electrode 104.

An intermediary region material 206 may, optionally, be formed over the lower electrode material 204. The lower intermediary region material 206 may be formed from any of the materials described above with reference to the lower intermediary region 106. In some embodiments, the lower intermediary region material 206 may be integral with the conductive 10 material of the lower electrode material 204. For example, the lower intermediary region material 206 may be an upper-most sub-region of the lower electrode material 204.

A seed material 208 may be formed over the lower intermediary region material 206, if present, or the lower electrode material 204. The seed material 208 may be formed as described above with reference to FIG. 1. Each portion of the seed material 208 may be 15 formed by sputter deposition, such as by magnetron sputtering (*e.g.*, high-power impulse magnetron sputtering (HIPIMS), dc magnetron sputtering, *etc.*), ion-beam sputtering, or other PVD methods. The seed material 208 may be also formed by at least one of atomic layer deposition (ALD), chemical vapor deposition (CVD), plasma enhanced chemical vapor deposition (PECVD), low pressure chemical vapor deposition (LPCVD), or other film 20 deposition processes.

A free region material 210 may be formed over the seed material 208. The free region material 210 may be formed of any of the materials described above with reference to the free region 110. For example, the free region material 210 may include a CoFeB material. In other embodiments, the free region material 210 may include an artificial superlattice structure 25 material formed of alternating portions of the magnetic material 117 and the conductive material 115, as described above with reference to the first magnetic portion 116 of FIG. 2. The free region material 210 may be amorphous when formed and may be formed at a temperature such that the free region material 210 remains in an amorphous state. The free region material 210 may exhibit a switchable magnetic orientation, indicated by arrows 209.

30 As shown in FIGs. 5A and 5B, a tunnel barrier material 230 may be formed over the free region material 210. The tunnel barrier material 230 may include a first portion 212 and a second portion 214. The first portion 212 of the tunnel barrier material 230 may be formed over the free region material 210 to form an interface 211. The first portion 212 of the tunnel

barrier material 230 may be formed from the same materials as described above with reference to the first portion 112 of the tunnel barrier material 130.

The first portion 212 may be formed by at least one of ALD, CVD, PECVD, LPCVD, PVD, or other film deposition processes. In some embodiments, the first portion 212 is formed by sputter deposition, such as by magnetron sputtering (*e.g.*, high-power impulse magnetron sputtering (HIPIMS), DC sputtering, *etc.*), RF sputtering, electron beam physical vapor deposition, ion-beam reactive sputtering, or other PVD methods. In some embodiments, the first portion 212 is formed from MgO. The first portion 212 may be formed as MgO, rather than formed as a magnesium portion that is subsequently oxidized to MgO by exposing the magnesium portion to oxidizing conditions. The source of the MgO may be a single crystal MgO or a multi-crystal MgO deposition source or sputtering target.

The first portion 212 may be formed over the free region material 210 at a first temperature such that the underlying free region material 210 is not crystallized. In other words, the free region material 210 may remain amorphous during formation of the first portion 212 of the tunnel barrier material 230. As formed, the first portion 212 may be amorphous or crystalline. In some embodiments, the free region material 210 includes a CoFeB material that remains amorphous during formation of the first portion 212. In some embodiments, the first portion 212 is crystalline when initially formed. The first portion 212 may be formed at a temperature between about -150°C and about 150°C, such as between about -150°C and about 0°C, between about 0°C and about 25°C, between about 20°C and about 25°C, between about 25°C and about 50°C, or between about 50°C and about 150°C. In some embodiments, the first portion 212 is formed at room temperature (*e.g.*, between about 20°C and about 25°C). If the first portion 212 is formed at room temperature, the underlying free region material 210 may remain in its amorphous state.

After forming the first portion 212 of the tunnel barrier material 230 over the free region material 210, the free region material 210 and the first portion 212 may be annealed, such as by thermal annealing. Exposing the free region material 210 and the first portion 212 to annealing conditions may crystallize the free region material 210 from the interface 211 through the free region material 210. After annealing the first portion 212 and the free region material 210, the free region material 210 may have a crystal structure that is aligned with (*i.e.*, matched to) a crystal structure of the first portion 212. In some embodiments, a CoFeB free region material 210 is crystallized from the interface 211 and includes the same crystal structure as the first portion 212 including MgO. Annealing the first portion 212 may also

cause any oxygen vacancies within the first portion 212 to fill with oxygen, increasing the stoichiometry of the first portion 212 of the tunnel barrier material 230. By way of non-limiting example, where the first portion 212 includes MgO, annealing the first portion 212 may attract oxygen to the first portion 212, filling any oxygen vacancies that may have been formed during the low temperature formation of the first portion 212.

To anneal the free region material 210 and the first portion 212, the free region material 210 and the first portion 212 may be exposed to a temperature sufficient to crystalize the free region material 210 and for a sufficient amount of time. Exposing the first portion 212 to annealing conditions may increase the crystal quality of the first portion 212 upon which the second portion 214 may be subsequently formed, as described in more detail below. The annealing may also form a smooth surface of the first portion 212, upon which the second portion 214 is formed. The free region material 210 and the first portion 212 may be exposed to a temperature of between about 300°C and about 600°C for between about 60 seconds and about one hour (1 hr.). The free region material 210 and the first portion 212 may be exposed to a temperature of between about 300°C and about 350°C, between about 350°C and about 400°C, between about 400°C and about 500°C, or between about 500°C and about 600°C. The exposure time may be between about 60 seconds and about five minutes, between about 5 minutes and 15 minutes, between about 15 minutes and about 30 minutes, or between about 30 minutes and about 60 minutes.

Referring to FIG. 5B, after annealing the free region material 210 and the first portion 212, the second portion 214 of the tunnel barrier material 230 may be formed. The second portion 214 may be formed directly over and in contact with the first portion 212. The second portion may be formed of the same materials described above with reference to the second portion 114. In some embodiments, the second portion 214 is formed of the same material as the first portion 212. The first portion 212 of the tunnel barrier material 230 that has been annealed may act as a seed upon which the second portion 214 is formed, such that the crystal structure of the second portion 214 matches the crystal structure of the first portion 212. An exposed surface of the first portion 212 may be a seed upon which the second portion 214 is formed to the same crystal orientation as the first portion 212 and the free region material 210. The first portion 212 and the second portion 214 may exhibit the same crystal orientation at an interface 213.

The second portion 214 of the tunnel barrier material 230 may be formed at a second temperature that is higher than the first temperature at which the first portion 212 is formed.

The second portion 214 may be formed by one of the same methods described above for forming the first portion 212. For example, the second portion 214 may be formed by sputter deposition, such as by at least one of ALD, CVD, PECVD, LPCVD, PVD, or other film deposition processes. In some embodiments, the second portion 214 is formed by sputter deposition, such as by magnetron sputtering (*e.g.*, high-power impulse magnetron sputtering (HIPIMS), DC sputtering, *etc.*), RF sputtering, electron beam physical vapor deposition, ion-beam reactive sputtering, or other PVD methods. However, the second portion 214 may be formed at a different, higher temperature than the first portion 212 is formed. For example, the second portion 214 may be formed at a temperature between about 300°C and about 600°C, as described above. The second portion 214 may be formed at the same temperature as the temperature at which the first portion 212 and the free region material 210 are annealed. In other embodiments, the second portion 214 may be formed at a different temperature than the temperature at which the first portion 212 and the free region material 210 are annealed. By way of non-limiting example, the second portion 214 may be formed at a temperature between about 300°C and about 600°C, such as between about 300°C and about 350°C, between about 350°C and about 400°C, between about 400°C and about 500°C, or between about 500°C and about 600°C. Forming the second portion 214 at an elevated temperature may form a more stoichiometric material having an increased crystal quality. For example, where the second portion 214 includes MgO, the second portion 214 may include a stoichiometric amount of oxygen with less oxygen vacancies and less interstitial oxygen than the first portion 212. In some embodiments, each of the first portion 212 and the second portion 214 have a ratio of magnesium to oxygen of approximately one to one.

The second portion 214 may be formed to the same thickness, a greater thickness, or a lesser thickness than the first portion 212. In some embodiments, the ratio is about 1.5 and the total thickness of the tunnel barrier material 130 is about 18 Å. The ratio of the thickness of the first portion 212 to the second portion 214 may be tailored to increase the TMR and decrease the RA of the tunnel barrier material 230. The tunnel barrier material 230 may be formed to exhibit a TMR of between about 180% and about 600% and an RA of between about 3 ohm μm^2 and about 8 ohm μm^2, as described above with reference to the tunnel barrier material 130. In some embodiments, the thickness of the second portion 214 is less than a thickness of the first portion 212.

With reference to FIG. 5C, a fixed region material 240 may be formed over the second portion 214 of the tunnel barrier material 230. The fixed region material 240 may include a

first magnetic material 216 over the second portion 214 of the tunnel barrier material 230, a coupling material 218 over the first magnetic material 216, and a second magnetic material 220 over the coupling material 218. The first magnetic material 216 may include a first magnetic sub-region 216a, a spacer material 216b, and a second magnetic sub-region 216c. Each of the first magnetic sub-region 216a, the spacer material 216b, and the second magnetic sub-region 216c may be formed of the same materials as the first magnetic sub-region 116a, the spacer 116b, and the second magnetic sub-region 116c, respectively, described above. Each of the first magnetic material 216, the coupling material 218, and the second magnetic material 220 may be formed of the same materials as the first magnetic portion 116, the coupling material 118, and the second magnetic portion 120, respectively, described above. The first magnetic material 216 and the second magnetic material 220 of the fixed region material 240 may include a fixed magnetic orientation, indicated by arrows 219.

The coupling material 218 may be formed over the first magnetic material 216 (*e.g.*, over the second magnetic sub-region 216c of the first magnetic material 216). The coupling material 218 may be formed between the first magnetic material 216 and the second magnetic material 220. The coupling material 218 may be formed by at least one of ALD, CVD, PVD, PECVD, LPCVD, or other film deposition processes.

The second magnetic material 220 may be formed directly over the coupling material 218. The second magnetic material 220 may be formed in the same manner and from the same materials as the first magnetic material 216.

An upper intermediary region material 224 may optionally be formed over the second magnetic material 220 and may include the same materials as the lower intermediary region material 206. An upper electrode material 226 may be formed over the upper intermediary region material 224, if present, or over the second magnetic material 220. The upper electrode material 226 may be formed of the same materials as described above with reference to the upper electrode 126.

The magnetic memory cell 200 may be processed to form the magnetic memory cell 100 as shown in FIG. 1. The magnetic memory cell 200 structure may be processed by conventional photolithography, material removal, etching, or other processes that are not described in detail herein.

Although the magnetic memory cell 200 described with reference to FIG. 5A through FIG. 5C describes forming the magnetic memory cell 100 of FIG. 1, the magnetic memory

cell 100′ of FIG. 3 may be formed by similar methods. However, the fixed region material 240 would be formed over the seed material 208, the first portion 212 of the tunnel barrier material 230 would be formed over the fixed region material 240, and the free region material 210 would be formed over the second portion 214 of the tunnel barrier material 230,
5 resulting in the magnetic memory cell of FIG. 3. In other embodiments, the magnetic memory cell 100″ of FIG. 4 may be formed by forming the free region material 210 and the fixed region material 240 to exhibit a horizontal magnetic orientation.

Forming the tunnel barrier material 230 from the first portion 212 and the second portion 214 may increase the TMR and decrease the RA of the magnetic tunnel junction. The
10 MTJ 150 may be substantially free of defects such as oxygen vacancies or interstitial oxygen within the crystal structure of the tunnel barrier material 230. The tunnel barrier material 230 may, therefore, exhibit improved tunneling characteristics at a high TMR and a low RA.

Accordingly, a method of forming a semiconductor device is disclosed. The method comprises forming a magnetic material over an electrode on a substrate, forming a first tunnel
15 barrier material over the magnetic material, annealing the magnetic material and the first tunnel barrier material, forming a second tunnel barrier material over the annealed first tunnel barrier material, forming another magnetic material over the second tunnel barrier material, and forming another electrode over the another magnetic material.

Accordingly, a method of forming a magnetic tunnel junction is disclosed. The
20 method comprises forming at a first temperature a barrier material over a magnetic material, annealing the barrier material and the magnetic material, forming at a second temperature another barrier material over the annealed barrier material, and forming another magnetic material over the another barrier material.

Accordingly, a method of forming a semiconductor device is disclosed. The method
25 comprises forming a seed material over a substrate, forming a magnetic material over the seed material, forming at a first temperature an oxide material over the magnetic material, forming at a second temperature higher than the first temperature, another oxide material over the oxide material, and forming another magnetic material over the another oxide material.

With reference to FIG. 6, illustrated is an STT-MRAM system 600 that includes
30 peripheral devices 612 in operable communication with an STT-MRAM cell 614, a grouping of which may be fabricated to form an array of memory cells in a grid pattern including a number of rows and columns, or in various other arrangements, depending on the system requirements and fabrication technology. The STT-MRAM cell 614 may include a magnetic

cell core 601, an access transistor 603, a conductive material that may function as a data/sense line 604 (*e.g.*, a bit line), a conductive material that may function as an access line 605 (*e.g.*, a word line) and a conductive material that may function as a source line 606. The peripheral devices 612 of the STT-MRAM system may include read/write circuitry 607, a bit line reference 608, and a sense amplifier 609. The magnetic cell core 601 may be any one of the magnetic cell cores 101, 101′, 101″ described above. Due to the structure of the cell core 601, the method of fabrication, or both, the STT-MRAM cell 614 may have a high TMR and a low resistance (*e.g.*, low RA product).

In use and operation, when an STT-MRAM cell 614 is selected to be programmed, a programming current is applied to the STT-MRAM cell 614, and the current is spin-polarized by the fixed region of the magnetic cell core 601 and exerts a torque on the free region of the cell core 601, which switches the magnetization of the free region to "write to" or "program" the STT-MRAM cell 614. In a read operation of the STT-MRAM cell 614, a current is used to detect the resistance state of the magnetic cell core 601.

To initiate programming of the STT-MRAM cell 614, the read/write circuitry 607 may generate a write current (*i.e.*, a programming current) to the data/sense line 604 and the source line 606. The polarity of the voltage between the data/sense line 604 and the source line 606 determines the switch in magnetic orientation of the free region in the magnetic cell core 601. By changing the magnetic orientation of the free region with the spin polarity, the free region is magnetized according to the spin polarity of the programming current and the programmed logic state is written to the STT-MRAM cell 614.

To read the STT-MRAM cell 614, the read/write circuitry 607 generates a read voltage to the data/sense line 604 and the source line 606 through the cell core 601 and the access transistor 603. The programmed state of the STT-MRAM cell 614 relates to the electrical resistance across the cell core 601, which may be determined by the voltage difference between the data/sense line 604 and the source line 606. In some embodiments, the voltage difference may be compared to the bit line reference 608 and amplified by the sense amplified 609.

FIG. 6 illustrates one example of a STT-MRAM system 600 including at least one magnetic memory cell. It is contemplated, however, that the magnetic cell cores 101, 101′, 101″ may be incorporated and utilized within any STT-MRAM system configured to incorporate a magnetic cell core having magnetic regions. It is also contemplated that the

magnetic cell cores 101, 101′, 101″ may be used in other magnetic memory cells besides STT-MRAM cells.

With reference to FIG. 7, illustrated is a simplified block diagram of a semiconductor device 700 implemented according to one or more embodiments described herein. The semiconductor device 700 includes a memory array 702 and a control logic component 704. The memory array 702 may include a plurality of STT-MRAM cells 614 (FIG. 6) including any of the magnetic cell cores (*e.g.*, the magnetic cell cores 101, 101′, 101″ of FIG. 1, FIG. 3, and FIG. 4, respectively) discussed above, which magnetic cell cores (*e.g.*, the magnetic cell cores 101, 101′, 101″) may have been formed according to a method described above and may be operated according to a method described above. The control logic component 704 may be configured to operatively interact with the memory array 702 so as to read from or write to any or all memory cells (*e.g.*, STT-MRAM cell 614 (FIG. 6)) within the memory array 702.

Accordingly, a semiconductor device is disclosed. The semiconductor device comprises an array of magnetic cell structures, each magnetic cell structure comprising a magnetic tunnel junction over an electrode on a substrate, each magnetic tunnel junction comprising a magnetic material over the substrate, a first tunnel barrier material over the magnetic material, a second tunnel barrier material over the first tunnel barrier material, and another magnetic material over the second tunnel barrier material, each magnetic tunnel junction configured to exhibit a tunnel magnetoresistance of between about 180% and about 600% at a resistance area product of less than about 8 ohm μm^2. The semiconductor device further comprises another electrode over the another magnetic material.

With reference to FIG. 8, depicted is a processor-based system 800. The processor-based system 800 may include various electronic devices manufactured in accordance with embodiments of the present disclosure. The processor-based system 800 may be any of a variety of types such as a computer, pager, cellular phone, personal organizer, control circuit, or other electronic device. The processor-based system 800 may include one or more processors 802, such as a microprocessor, to control the processing of system functions and requests in the processor-based system 800. The processor 802 and other subcomponents of the processor-based system 800 may include magnetic memory devices manufactured in accordance with embodiments of the present disclosure.

The processor-based system 800 may include a power supply 804 in operable communication with the processor 802. For example, if the processor-based system 800 is a portable system, the power supply 804 may include one or more of a fuel cell, a power

scavenging device, permanent batteries, replaceable batteries, and rechargeable batteries. The power supply 804 may also include an AC adapter; therefore, the processor-based system 800 may be plugged into a wall outlet, for example. The power supply 804 may also include a DC adapter such that the processor-based system 800 may be plugged into a vehicle cigarette
5 lighter or a vehicle power port, for example.

Various other devices may be coupled to the processor 802 depending on the functions that the processor-based system 800 performs. For example, a user interface 806 may be coupled to the processor 802. The user interface 806 may include input devices such as buttons, switches, a keyboard, a light pen, a mouse, a digitizer and stylus, a touch screen, a
10 voice recognition system, a microphone, or a combination thereof. A display 808 may also be coupled to the processor 802. The display 808 may include an LCD display, an SED display, a CRT display, a DLP display, a plasma display, an OLED display, an LED display, a three-dimensional projection, an audio display, or a combination thereof. Furthermore, an RF sub-system/baseband processor 810 may also be coupled to the processor 802. The RF
15 sub-system/baseband processor 810 may include an antenna that is coupled to an RF receiver and to an RF transmitter (not shown). A communication port 812, or more than one communication port 812, may also be coupled to the processor 802. The communication port 812 may be adapted to be coupled to one or more peripheral devices 814, such as a modem, a printer, a computer, a scanner, or a camera, or to a network, such as a local area
20 network, remote area network, intranet, or the Internet, for example.

The processor 802 may control the processor-based system 800 by implementing software programs stored in the memory. The software programs may include an operating system, database software, drafting software, word processing software, media editing software, or media playing software, for example. The memory is operably coupled to the
25 processor 802 to store and facilitate execution of various programs. For example, the processor 802 may be coupled to system memory 816, which may include one or more of spin torque transfer magnetic random access memory (STT-MRAM), magnetic random access memory (MRAM), dynamic random access memory (DRAM), static random access memory (SRAM), racetrack memory, and other known memory types. The system memory 816 may
30 include volatile memory, non-volatile memory, or a combination thereof. The system memory 816 is typically large so that it can store dynamically loaded applications and data. In some embodiments, the system memory 816 may include semiconductor devices, such as the semiconductor device 700 of FIG. 7, memory cells including any of the magnetic cell

cores 101, 101′, 101″ of FIG. 1, FIG. 3, and FIG. 4, respectively, described above, or a combination thereof.

The processor 802 may also be coupled to non-volatile memory 818, which is not to suggest that system memory 816 is necessarily volatile. The non-volatile memory 818 may include one or more of STT-MRAM, MRAM, read-only memory (ROM) such as an EPROM, resistive read-only memory (RROM), and flash memory to be used in conjunction with the system memory 816. The size of the non-volatile memory 818 is typically selected to be just large enough to store any necessary operating system, application programs, and fixed data. Additionally, the non-volatile memory 818 may include a high capacity memory such as disk drive memory, such as a hybrid-drive including resistive memory or other types of non-volatile solid-state memory, for example. The non-volatile memory 818 may include semiconductor devices, such as the semiconductor device 700 of FIG. 7, memory cells including any of the magnetic cell cores 101, 101′, 101″ of FIG. 1, FIG. 3, and FIG. 4, respectively, or a combination thereof.

EXAMPLES

Example

FIG. 9 is a graphical representation comparing the TMR vs. the RA of MTJs formed according to embodiments of the disclosure to MTJs formed by conventional methods. A MgO tunnel barrier material was formed by RF sputtering at about 20°C over a CoFeB magnetic material. The MgO and the CoFeB were annealed at a temperature of about 500°C to crystallize the CoFeB magnetic material in the same crystal orientation as the MgO. A second MgO tunnel barrier material was formed by RF sputtering at about 500°C over the annealed MgO. Another CoFeB magnetic material was formed over the second MgO tunnel barrier material. A tantalum material was formed over the CoFeB magnetic material and a cobalt/palladium magnetic material was formed over the tantalum to complete the MTJ structure. A conventional MTJ was formed by forming an MgO tunnel barrier material over a CoFeB magnetic material at room temperature. The MgO and the CoFeB were annealed at a temperature of about 500°C. Another CoFeB magnetic material was formed over the MgO. The TMR and the RA of the MTJ structures were measured using conventional techniques. The upper left line of FIG. 9 shows the TMR and the RA of MTJs formed according to embodiments of the disclosure and the lower right line shows the TMR and the RA of the MTJs formed by conventional methods. As shown in the graph, the MTJs formed by the

methods disclosed herein exhibit a higher TMR at a lower RA than MTJs formed by conventional methods.

FIG. 10 is a graphical representation of the TMR vs. the RA of MTJs formed according to the present disclosure. A first MgO tunnel barrier material was formed to a first thickness ("X") over a CoFeB magnetic material. The MgO was formed by RF sputtering at about 20°C. The MgO and the CoFeB were annealed at a temperature of about 500°C to crystallize the CoFeB in the same crystal orientation as the MgO. A second MgO tunnel barrier material was formed by RF sputtering at about 500°C over the annealed MgO. The second MgO tunnel barrier material was formed to a second thickness ("Y"). Another CoFeB magnetic material was formed over the second MgO tunnel barrier material. A tantalum material was formed over the CoFeB magnetic material and a cobalt/palladium magnetic material was formed over the tantalum to complete the MTJ structure. The TMR and RA of the MTJ structure were measured by conventional techniques. FIG. 10 graphs the TMR and the RA of MTJs having different ratios of the thickness of the first MgO tunnel barrier material to the thickness of the second MgO tunnel barrier material (*i.e.*, X/Y). Accordingly, the ratio of X/Y may be tailored to form a MTJ exhibiting a desired TMR at a desired RA.

While certain illustrative embodiments have been described in connection with the figures, those of ordinary skill in the art will recognize and appreciate that embodiments encompassed by the disclosure are not limited to those embodiments explicitly shown and described herein. Rather, many additions, deletions, and modifications to the embodiments described herein may be made without departing from the scope of embodiments encompassed by the disclosure, such as those hereinafter claimed, including legal equivalents. In addition, features from one disclosed embodiment may be combined with features of another disclosed embodiment while still being encompassed within the scope of the disclosure.

CLAIMS

What is claimed is:

5 1. A method of forming a semiconductor device, the method comprising:
forming a magnetic material over an electrode on a substrate;
forming a first tunnel barrier material over the magnetic material;
annealing the magnetic material and the first tunnel barrier material;
forming a second tunnel barrier material over the annealed first tunnel barrier material;
10 forming another magnetic material over the second tunnel barrier material; and
forming another electrode over the another magnetic material.

2. The method of claim 1, further comprising forming an array of memory cells over the substrate, each memory cell comprising the magnetic material, the first tunnel barrier
15 material, the second tunnel barrier material, and the another magnetic material.

3. The method of claim 1, wherein forming a first tunnel barrier material over the magnetic material comprises forming at least one of magnesium oxide, aluminum oxide, titanium dioxide, tantalum oxide, and ruthenium oxide over the magnetic material.
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4. The method of claim 1, wherein forming a first tunnel barrier material comprises forming magnesium oxide by sputter deposition.

5. The method of claim 1, wherein annealing the magnetic material and the first
25 tunnel barrier material comprises crystallizing the magnetic material and the first tunnel barrier material to exhibit the same crystal structure.

6. The method claim 1, wherein forming a second tunnel barrier material over the annealed first tunnel barrier material comprises forming the second tunnel barrier material at a
30 higher temperature than the first tunnel barrier material.

7. The method of claim 1, wherein forming a second tunnel barrier material over the annealed first tunnel barrier material comprises forming the second tunnel barrier material comprising the same material as the first tunnel barrier material.

5 8. The method of any one of claims 1 through 7, wherein forming a first tunnel barrier material comprises forming the first tunnel barrier material to a thickness between about 1.0 and about 1.5 times a thickness of the second tunnel barrier material.

9. The method of any one of claims 1 through 7, wherein forming a first tunnel
10 barrier material over the magnetic material comprises forming the first tunnel barrier material at a temperature between about 20°C and about 25°C.

10. The method of any one of claims 1 through 7, wherein annealing the magnetic material and the first tunnel barrier material comprises exposing the magnetic material and the
15 first tunnel barrier material to a temperature between about 300°C and about 600°C.

11. The method of any one of claims 1 through 7, wherein annealing the magnetic material and the first tunnel barrier material comprises annealing the magnetic material and the first tunnel barrier material prior to forming the second tunnel barrier material over the
20 first tunnel barrier material.

12. The method of any one of claims 1 through 7, wherein forming a second tunnel barrier material over the annealed first tunnel barrier material comprises forming the second tunnel barrier material at a temperature between about 300°C and about 600°C.

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13. The method of any one of claims 1 through 7, wherein:
forming a first tunnel barrier material comprises forming the first tunnel barrier material at a temperature between about 0°C and about 25°C; and
forming a second tunnel barrier material comprises forming the second tunnel barrier material
30 at a temperature between about 300°C and about 600°C.

14. A semiconductor device, comprising:
an array of magnetic cell structures, each magnetic cell structure comprising a magnetic tunnel junction over an electrode on a substrate, each magnetic tunnel junction comprising:
a magnetic material over the substrate;
5 a first tunnel barrier material over the magnetic material;
a second tunnel barrier material over the first tunnel barrier material; and
another magnetic material over the second tunnel barrier material, each magnetic tunnel junction configured to exhibit a tunnel magnetoresistance of between about 180% and about 600% at a resistance area product of less than
10 about 8 ohm μm^2; and
another electrode over the another magnetic material.

15. The semiconductor device of claim 14, wherein the first tunnel barrier material over the magnetic material comprises magnesium oxide.
15

16. The semiconductor device of claim 14, wherein each of the first tunnel barrier material and the second tunnel barrier material comprises magnesium oxide.

17. The semiconductor device of any one of claims 14 through 16, wherein each
20 magnetic tunnel junction is configured to exhibit a tunnel magnetoresistance of between about 180% and about 205% at a resistance area product of between about 4 ohm μm^2 and about 8 ohm μm^2.

18. The semiconductor device of any one of claims 14 through 16, wherein each
25 magnetic tunnel junction is configured to exhibit a tunnel magnetoresistance of between about 180% and about 300% at a resistance area product of between about 6 ohm μm^2 and about 7 ohm μm^2.

19. The semiconductor device of any one of claims 14 through 16, wherein a ratio
30 of a thickness of the first tunnel barrier material to a thickness of the second tunnel barrier material is between about 1.0 and about 1.5.

20. The semiconductor device of any one of claims 14 through 16, wherein the first tunnel barrier material exhibits a higher density than the second tunnel barrier material.

FIG. 1

FIG. 2

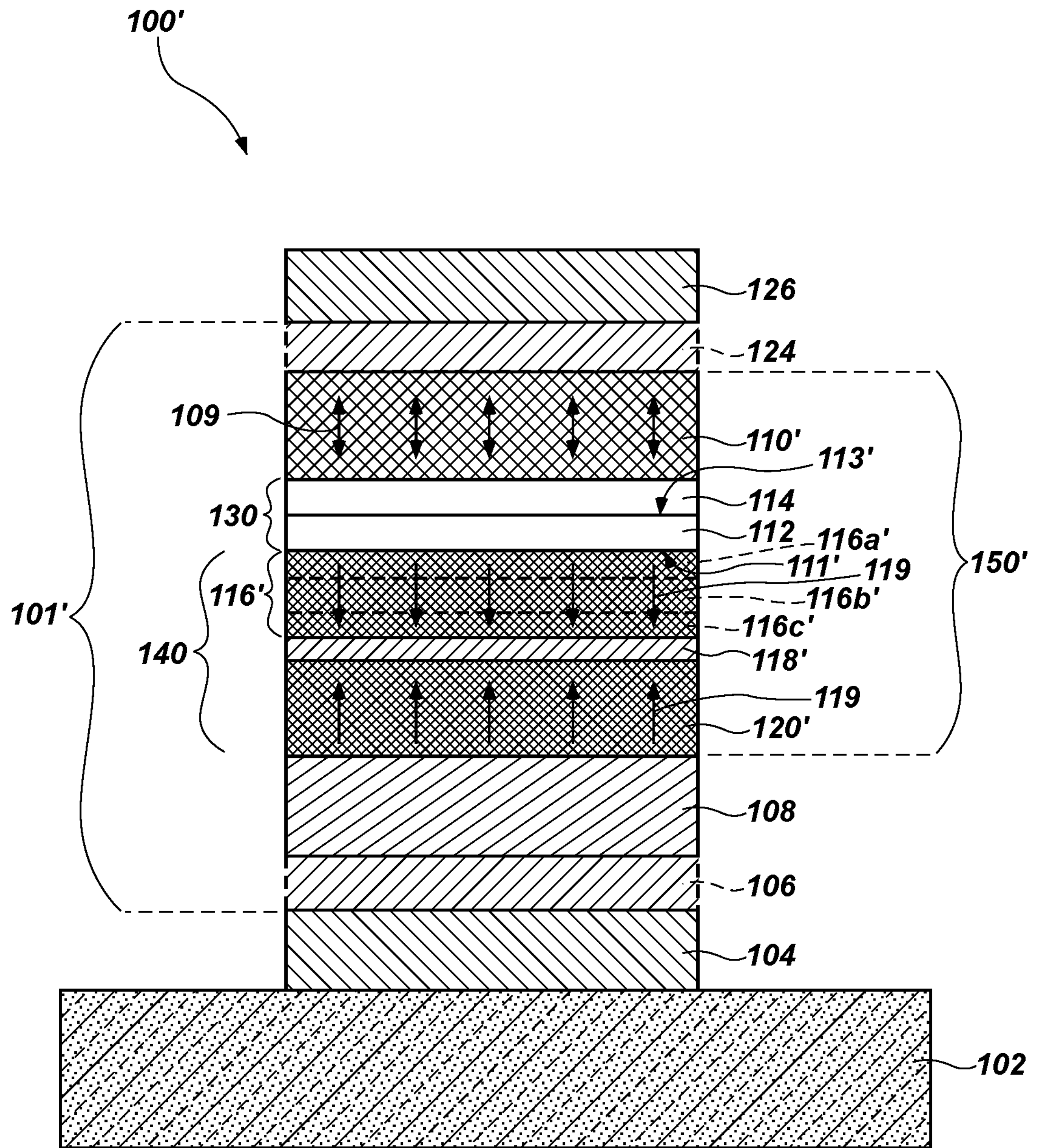

FIG. 3

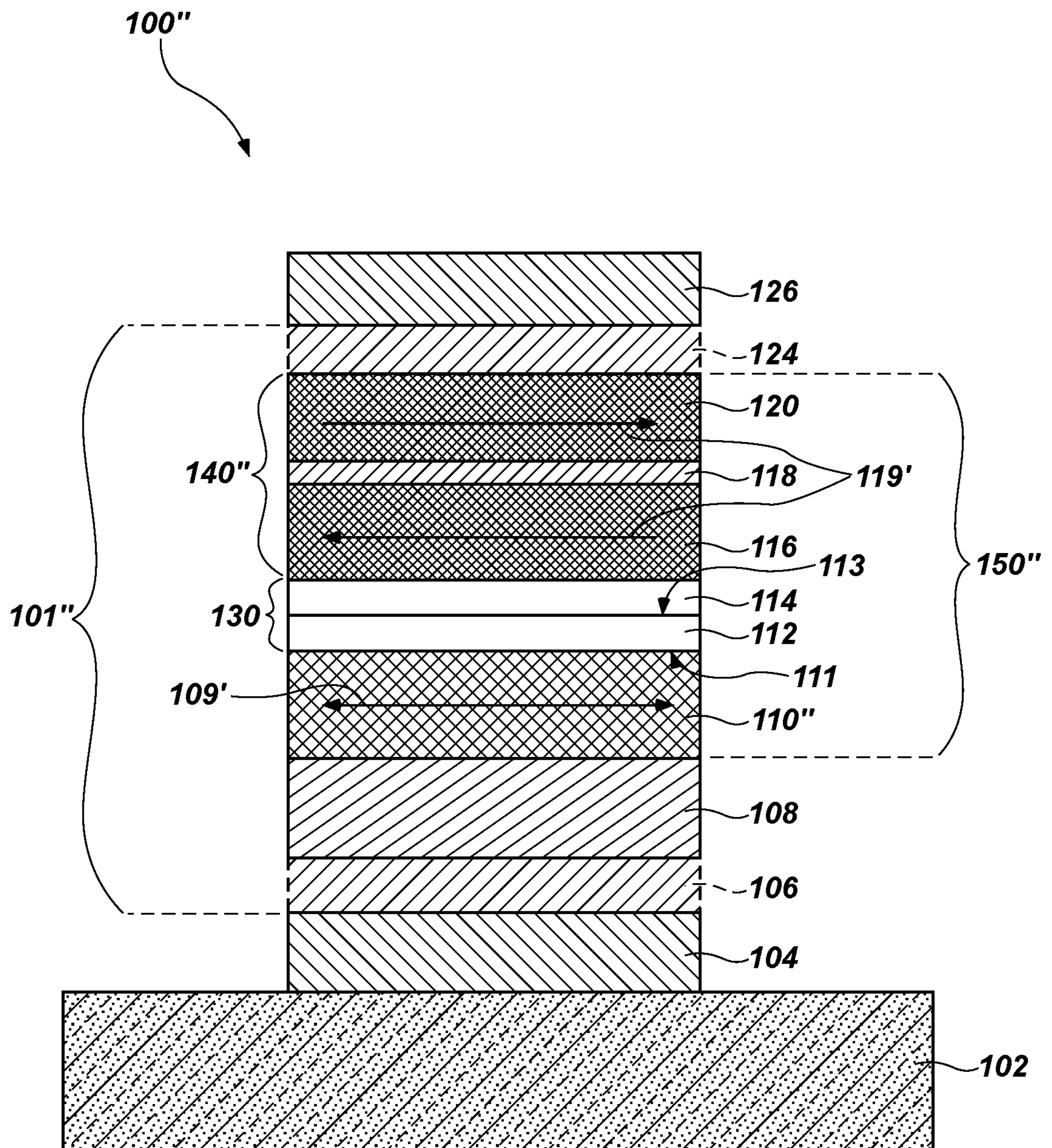

FIG. 4

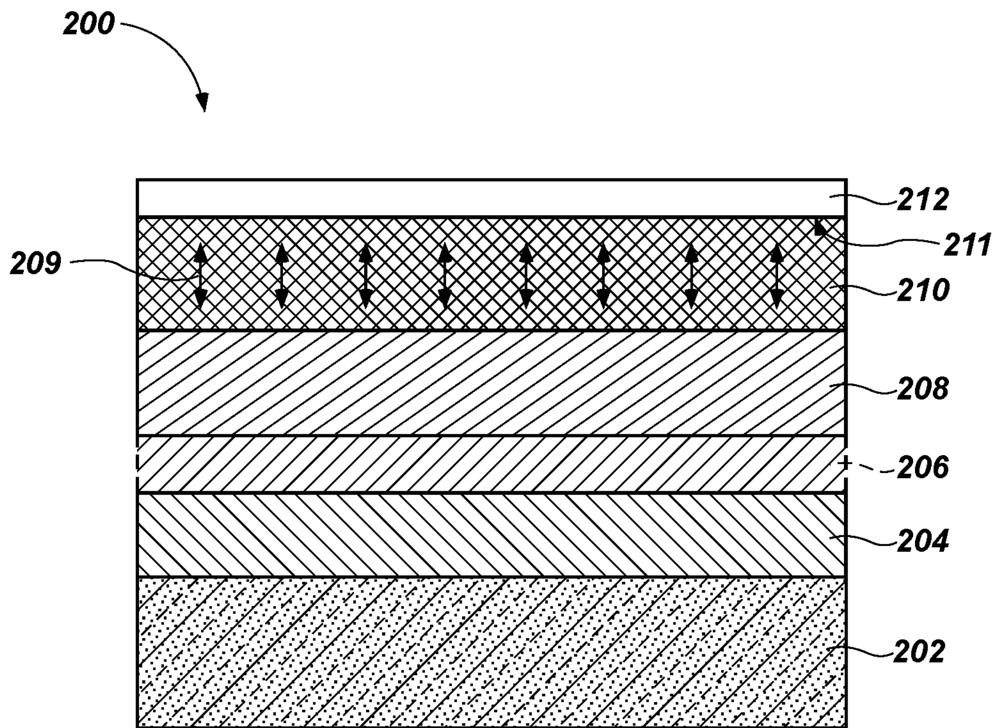

FIG. 5A

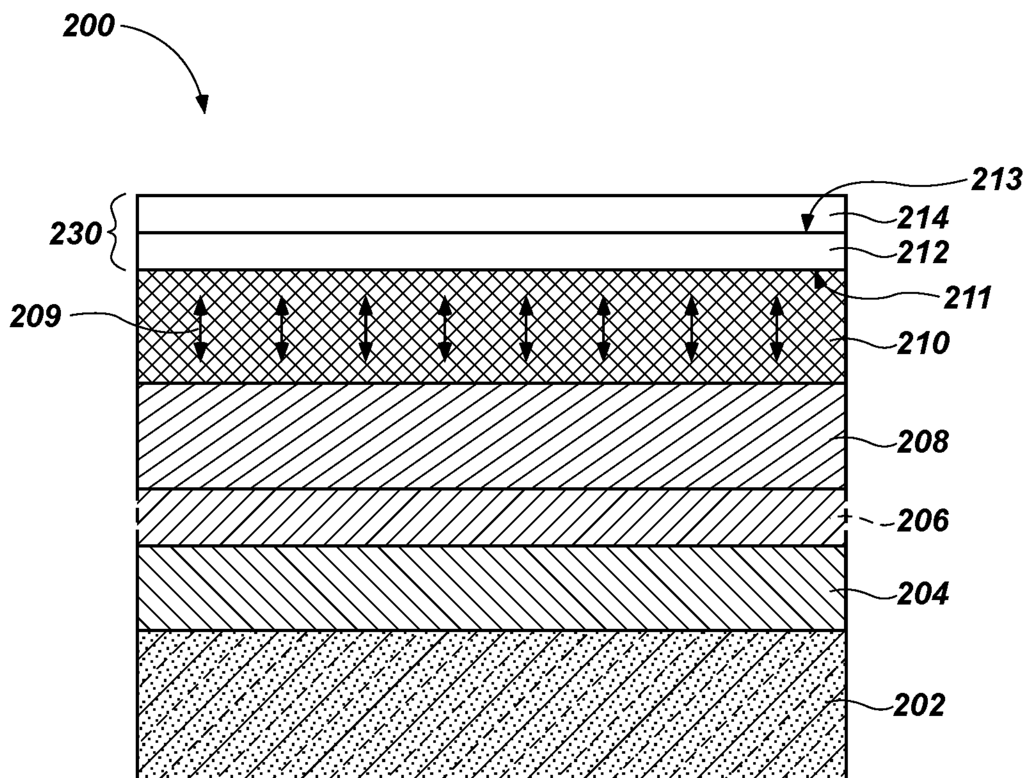

FIG. 5B

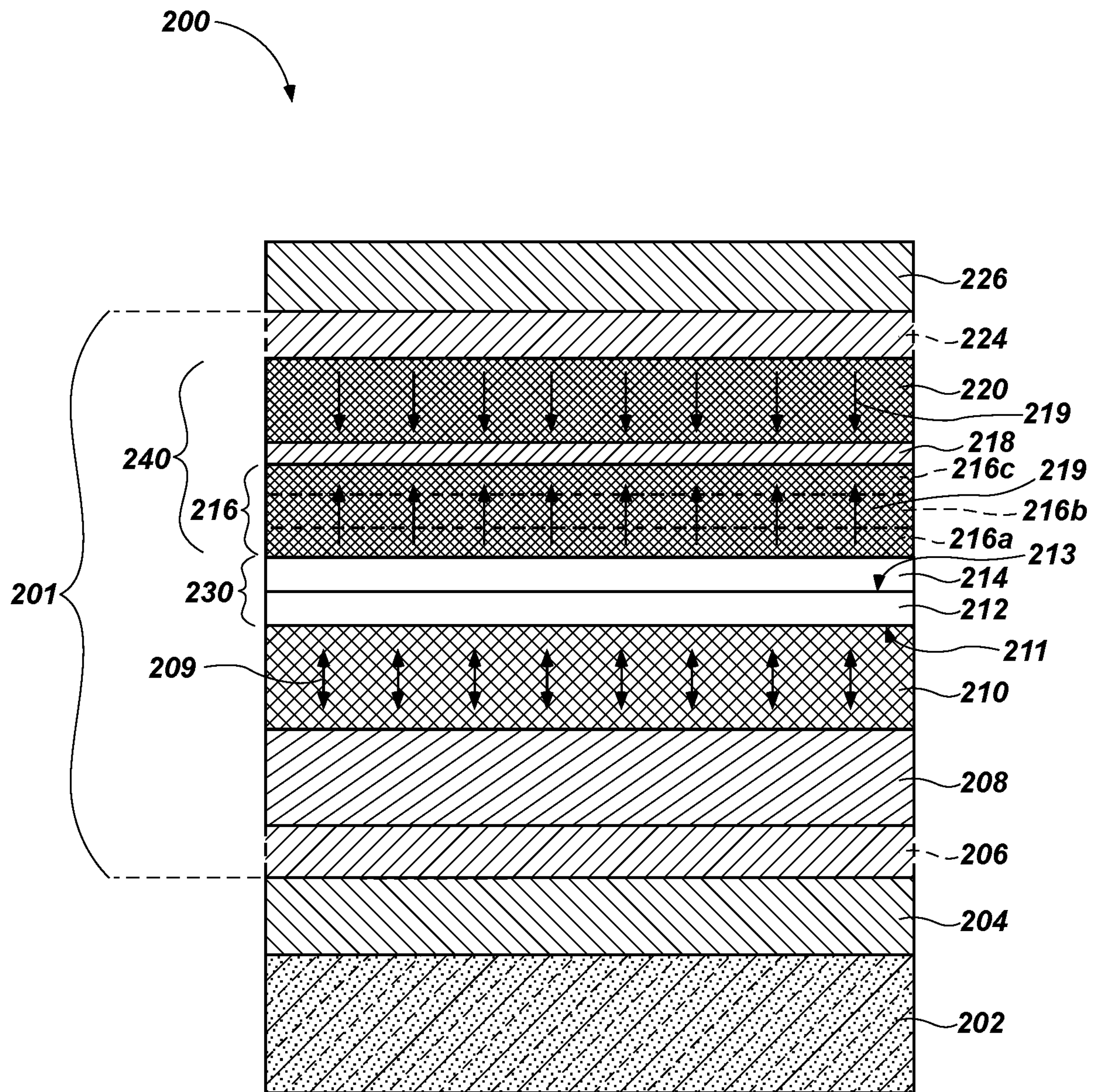

FIG. 5C

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FIG. 6

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FIG. 7

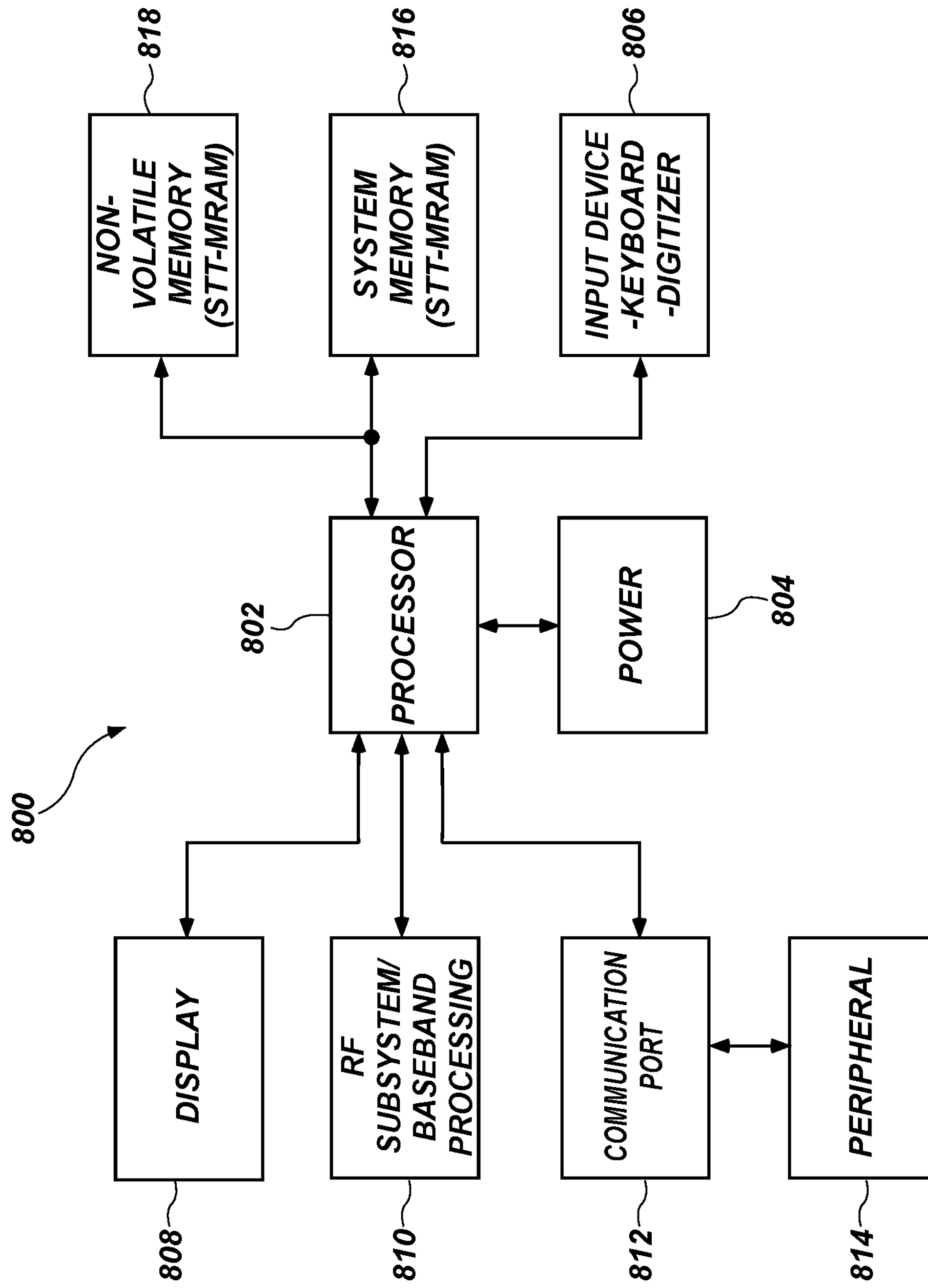

FIG. 8

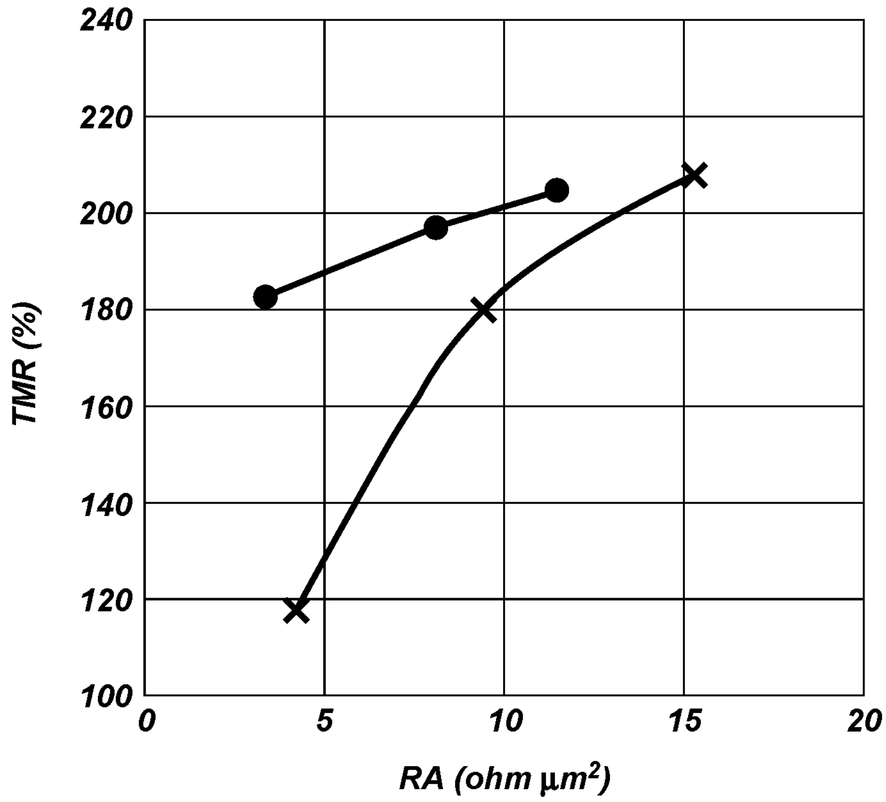

FIG. 9

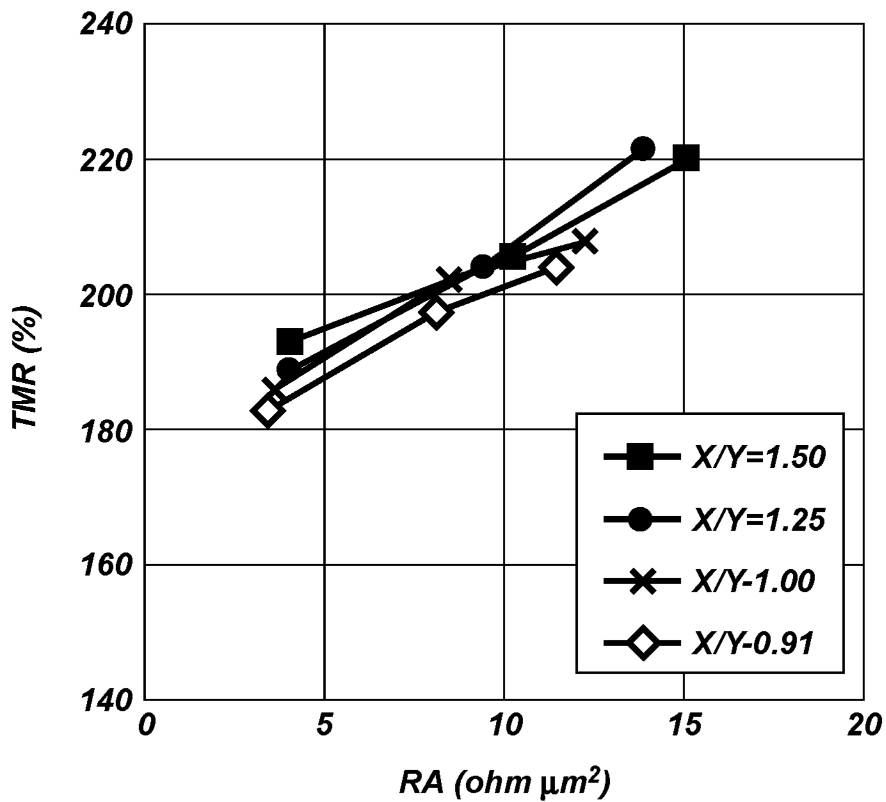

FIG. 10

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/066828

A. CLASSIFICATION OF SUBJECT MATTER

H01L 43/02(2006.01)i, H01L 43/08(2006.01)i, H01L 43/10(2006.01)i, H01L 43/12(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 43/02; H01L 43/12; G11B 5/39; H01L 29/82; G11C 11/15; H01L 43/10; G11C 11/00; H01L 43/08

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & keywords: magnetic tunnel junction, second tunnel barrier, temperature, tunnel magnetoresistance, resistance area product, and similar terms.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 2013-145846 A (ULVAC JAPAN LTD.) 25 July 2013 See paragraphs [0001]-[0041] and [0057]-[0096]; claims 1-4; and figures 1 and 4-8.	1-20
A	US 2009-0231909 A1 (BERNARD DIENY et al.) 17 September 2009 See paragraphs [0083]-[0095]; claims 1-18; and figures 10-12.	1-20
A	US 2002-0114112 A1 (EIJI NAKASHIO et al.) 22 August 2002 See paragraphs [0094]-[0120]; claim 1; and figure 5.	1-20
A	US 2002-0097534 A1 (JIJUN SUN et al.) 25 July 2002 See paragraphs [0051]-[0053] and [0078]-[0079]; claims 1-14; and figures 1A and 11A-11B.	1-20
A	US 6,347,049 B1 (JEFFREY R. CHILDRESS et al.) 12 February 2002 See column 4, lines 36-65; and figure 2.	1-20

☐ Further documents are listed in the continuation of Box C.   ☒ See patent family annex.

* Special categories of cited documents:
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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
09 April 2016 (09.04.2016)	**11 April 2016 (11.04.2016)**

Name and mailing address of the ISA/KR

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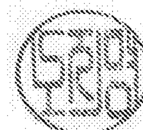

Telephone No. +82-42-481-8528

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2015/066828

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US 6347049 B1	12/02/2002	None	