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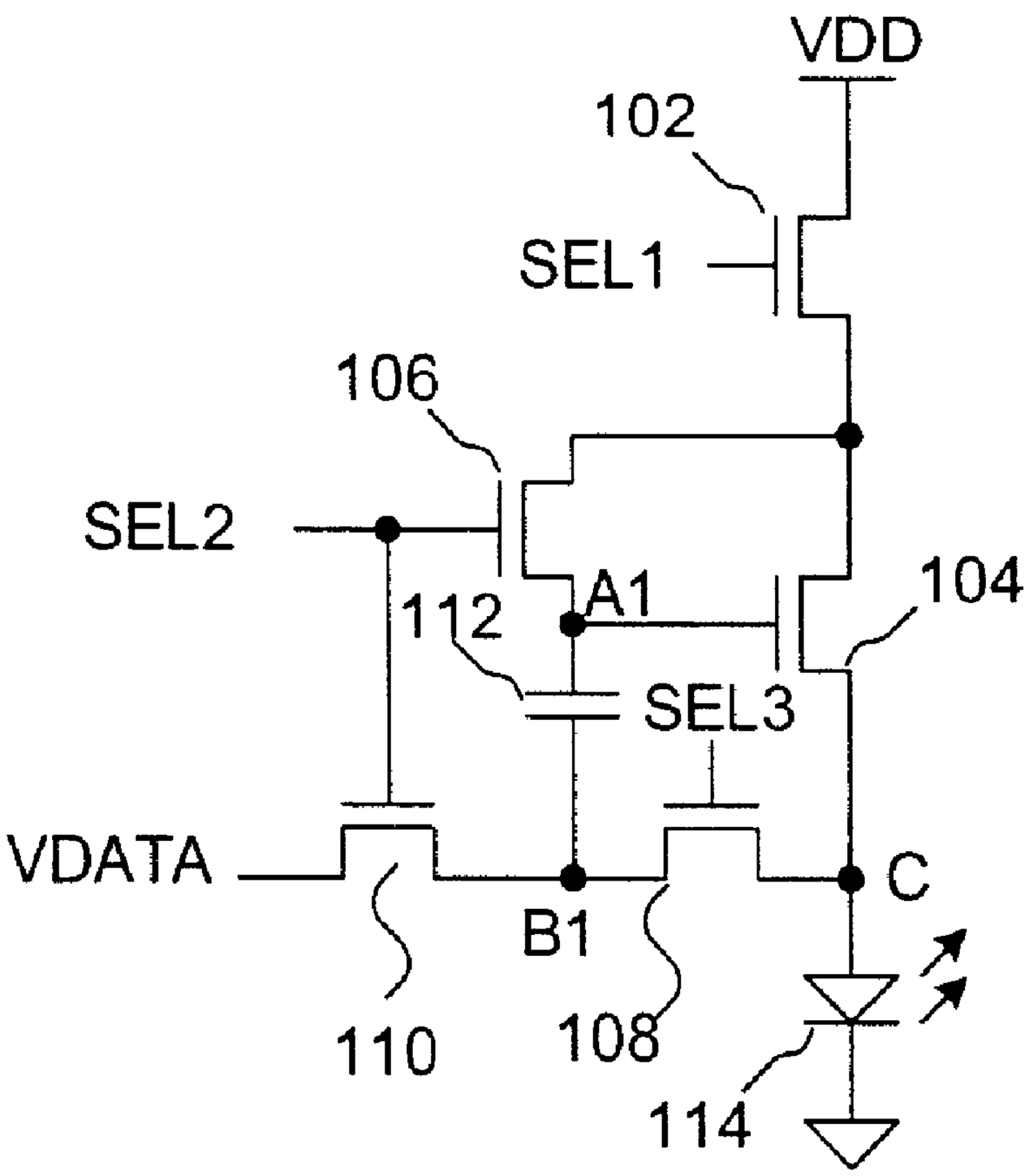
(54) Titre : TECHNIQUE DE COMPENSATION DE DEGRADATION DE LA LUMINANCE DANS LES DISPOSITIFS A ELECTRO-LUMINANCE

(54) Title: COMPENSATION TECHNIQUE FOR LUMINANCE DEGRADATION IN ELECTRO-LUMINANCE DEVICES



(57) Abrégé/Abstract:
A method and system for compensation for luminance degradation in electro-luminance devices is provided. The system includes a pixel circuit having a light emitting device, a storage capacitor, a plurality of transistors, and control signal lines to operate the pixel

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(57) Abrégé(suite)/Abstract(continued):
circuit. The storage capacitor is connected or disconnected to the transistor and a signal line(s) when programming and driving the pixel circuit.

ABSTRACT

A method and system for compensation for luminance degradation in electro-luminance devices is provided. The system includes a pixel circuit having a light emitting device, a storage capacitor, a plurality of transistors, and control signal lines to operate the pixel circuit. The storage capacitor is connected or disconnected to the transistor and a signal line(s) when programming and driving the pixel circuit.

Compensation Technique For Luminance Degradation In Electro-Luminance Devices

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority to Canadian Patent Application No. 2,518,276, filed September 13, 2005.

FIELD OF INVENTION

[0002] The present invention relates to electro-luminance device displays, and more specifically to a driving technique for the electro-luminance device displays to compensate for luminance degradation.

BACKGROUND OF THE INVENTION

[0003] Electro-luminance displays have been developed for a wide variety of devices, such as cell phones. In particular, active-matrix organic light-emitting diode (AMOLED) displays with amorphous silicon (a-Si), poly-silicon, organic, or other driving backplane have become more attractive due to advantages, such as feasible flexible displays, its low cost fabrication, high resolution, and a wide viewing angle.

[0004] An AMOLED display includes an array of rows and columns of pixels, each having an organic light-emitting diode (OLED) and backplane electronics arranged in the array of rows and columns. Since the OLED is a current driven device, the pixel circuit of the AMOLED should be capable of providing an accurate and constant drive current.

[0005] There is a need to provide a method and system that is capable of providing constant brightness with high accuracy and reducing the effect of the aging of the pixel circuit.

SUMMARY OF THE INVENTION

[0006] It is an object of the invention to provide a method and system that obviates or mitigates at least one of the disadvantages of existing systems.

[0007] In accordance with an aspect of the present invention there is provided a pixel circuit including a light emitting device and a storage capacitor having a first terminal and a second terminal. The pixel circuit includes a first transistor having a gate

terminal, a first terminal and a second terminal where the gate terminal is connected to a first select line. The pixel circuit includes a second transistor having a gate terminal, a first terminal and a second terminal where the first terminal is connected to the second terminal of the first transistor, and the second terminal is connected to the light emitting device. The pixel circuit includes a third transistor having a gate terminal, a first terminal and a second terminal where the gate terminal is connected to a second select line, the first terminal is connected to the second terminal of the first transistor, and the second terminal is connected to the gate terminal of the second transistor and the first terminal of the storage capacitor. The pixel circuit includes a fourth transistor having a gate terminal, a first terminal and a second terminal where the gate terminal is connected to a third select line, the first terminal is connected to the second terminal of the storage capacitor, and the second terminal is connected to the second terminal of the second transistor and the light emitting device. The pixel circuit includes a fifth transistor having a gate terminal, a first terminal and a second terminal where the gate terminal is connected to the second select line, the first terminal is connected to a signal line, and the second terminal is connected to the first terminal of the forth transistor and the second terminal of the storage capacitor.

[0008] In the above pixel circuit, the third select line may be the first select line.

[0009] The above pixel circuit may include a sixth transistor having a gate terminal, a first terminal and a second terminal where the gate terminal is connected to the second select line, the first terminal is connected to the first terminal of the second transistor, and the second terminal is connected to a bias current line.

[0010] In accordance with a further of the present invention there is provided a display system including a display array formed by the pixel circuit, and a driving module for programming and driving the pixel circuit.

[0011] In accordance with a further of the present invention there is provided a method for compensating for degradation of the light emitting device in the pixel circuit. The method includes the steps of charging the storage capacitor and discharging the storage capacitor. The step of charging the storage capacitor includes connecting the storage capacitor to the signal line. The method includes the step of

disconnecting the storage capacitor from the signal line and connecting the second terminal of the storage capacitor to the second terminal of the second transistor.

[0012] In accordance with a further of the present invention there is provided a method for compensating for shift in a threshold voltage of the transistor in the pixel circuit. The method includes the steps of charging the storage capacitor and discharging the storage capacitor. The step of charging the storage capacitor includes connecting the storage capacitor to the signal line. The method includes the step of disconnecting the storage capacitor from the signal line and connecting the second terminal of the storage capacitor to the second terminal of the second transistor.

[0013] In accordance with a further of the present invention there is provided a method for compensating for ground bouncing or IR drop in the pixel circuit. The method includes the steps of charging the storage capacitor and discharging the storage capacitor. The step of charging the storage capacitor includes connecting the storage capacitor to the signal line and the bias current line. The method includes the step of disconnecting the storage capacitor from the signal line and the bias current line and connecting the second terminal of the storage capacitor to the second terminal of the second transistor.

[0014] This summary of the invention does not necessarily describe all features of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] These and other features of the invention will become more apparent from the following description in which reference is made to the appended drawings wherein:

[0016] Figure 1A is a diagram illustrating an example of a pixel circuit along with its control signal lines to which a pixel driving scheme in accordance with an embodiment of the present invention is applied;

[0017] Figure 1B is a timing diagram illustrating an example of a method of operating the pixel circuit of Figure 1A;

[0018] Figure 2 is a graph illustrating a simulation result for Figures 1A-1B;

[0019] Figure 3 is a graph illustrating another simulation result for Figures 1A-1B;

[0020] Figure 4A is a diagram illustrating an example of a pixel circuit along with its control signal lines to which the pixel driving scheme in accordance with another embodiment of the present invention is applied;

[0021] Figure 4B is a timing diagram illustrating an example of a method of operating the pixel circuit of Figure 4A;

[0022] Figure 5A is a diagram illustrating an example of a pixel circuit along with its control signal lines to which the pixel driving scheme in accordance with a further embodiment of the present invention is applied;

[0023] Figure 5B is a timing diagram illustrating an example of a method of operating the pixel circuit of Figure 5A;

[0024] Figure 6 is a diagram illustrating an example of a display system with a display array having the pixel circuit of Figure 1A;

[0025] Figure 7 is a timing diagram illustrating an example of a method of operating the display array of Figure 6;

[0026] Figure 8 is a diagram illustrating an example of a display system with a display array having the pixel circuit of Figure 4A;

[0027] Figure 9 is a timing diagram illustrating an example of a method of operating the display array of Figure 8;

[0028] Figure 10 is a diagram illustrating an example of a display system with a display array having the pixel circuit of Figure 5A; and

[0029] Figure 11 is a timing diagram illustrating an example of a method of operating the display array of Figure 10.

DETAILED DESCRIPTION

[0030] Embodiments of the present invention are described using a pixel circuit having a light emitting device, such as an organic light emitting diode (OLED), and a

plurality of transistors. However, the pixel circuit may include any light emitting device other than the OLED. The transistors in the pixel circuit may be n-type transistors, p-type transistors or combinations thereof. The transistors in the pixel circuit may be fabricated using amorphous silicon, nano/micro crystalline silicon, poly silicon, organic semiconductors technologies (e.g. organic TFT), NMOS/PMOS technology or CMOS technology (e.g. MOSFET). A display having the pixel circuit may be a single color, multi-color or a fully color display, and may include one or more than one electroluminescence (EL) element (e.g., organic EL). The display may be an active matrix light emitting display. The display may be used in DVDs, personal digital assistants (PDAs), computer displays, or cellular phones.

[0031] In the description, "pixel circuit" and "pixel" may be used interchangeably. In the description below, "signal" and "line" may be used interchangeably. In the description below, "connect (or connected)"and "couple (or coupled)" may be used interchangeably, and may be used to indicate that two or more elements are directly or indirectly in physical or electrical contact with each other.

[0032] The embodiments of the present invention involve a driving method of driving the pixel circuit, which includes an in-pixel compensation technique for compensating for at least one of OLED degradation, backplane instability (e.g. TFT threshold shift), and ground bouncing (or IR drop). The driving scheme allows the pixel circuit to provide a stable luminance independent of the shift of the characteristics of pixel elements due to, for example, the pixel aging under prolonged display operation and process variation. This enhances the brightness stability of the OLED and efficiently improves the display operating lifetime.

[0033] Figure 1A illustrates an example of a pixel circuit along with its control signal lines to which a pixel driving scheme in accordance with an embodiment of the present invention is applied. The pixel circuit 100 of Figure 1A includes transistors 102-110, a storage capacitor 112 and an OLED 114. The pixel circuit 100 is connected to three select lines SEL1, SEL2, and SEL3, a signal line VDATA, a voltage line VDD, and a common ground.

[0034] The transistors 102-110 may be amorphous silicon, poly silicon, or organic thin-film transistors (TFT) or standard NMOS in CMOS technology. It would be appreciated by one of ordinary skill in the art that the pixel circuit 100 can be rearranged using p-type transistors.

[0035] The transistor 104 is a driving transistor. The source and drain terminals of the driving transistor 104 are connected to the anode electrode of the OLED 114 and the source terminal of the transistor 102, respectively. The gate terminal of the driving transistor 104 is connected to the signal line VDATA through the transistor 110 and is connected to the source terminal of the transistor 106. The drain terminal of the transistor 106 is connected to the source terminal of the transistor 102 and its gate terminal is connected to the select line SEL2.

[0036] The drain terminal of the transistor 108 is connected to the source terminal of the transistor 110, its source terminal is connected to the anode of the OLED 114, and its gate terminal is connected to the select line SEL3.

[0037] The drain terminal of the transistor 110 is connected to the signal line VDATA, and its gate terminal is connected to the select line SEL2.

[0038] The driving transistor 104, the transistor 106 and the storage capacitor 112 are connected at node A1. The transistors 108 and 110 and the storage capacitor 112 are connected at node B1.

[0039] Figure 1B illustrates an example of a method of operating the pixel circuit 100 of Figure 1A. The pixel circuit 100 of Figure 1A includes n-type transistors. However, it would be understood by one of ordinary skill in the art that the method of Figure 1B is applicable to a pixel circuit having p-type transistors.

[0040] Referring to Figures 1A-1B, the operation of the pixel circuit 100 includes two operating cycles: programming cycle 120 and driving cycle 122. At the end of the programming cycle 120, node A1 is charged to ($V_P+V_T+\Delta V_{OLED}$) where V_P is a programming voltage, V_T is the threshold voltage of the transistor 104, and ΔV_{OLED} is the OLED voltage shift under bias stress.

[0041] The programming cycle 120 includes two sub-cycles: pre-charging P11 and compensation P12, hereinafter referred to as pre-charging sub-cycle P11 and compensation sub-cycle P12, respectively.

[0042] During the pre-charging sub-cycle P11, the select lines SEL1 and SEL2 are high and SEL3 is low, resulting in turning the transistors 102, 106 and 110 on, and the transistor 108 off respectively. The voltage at VDATA is set to (V_{OLEDi}–V_P). "V_P" is a programming voltage. "i" represents initial voltage of OLED. "V_{OLEDi}" is a constant voltage and can be set to the initial ON voltage of the OLED 114. However, V_{OLEDi} can be set to other voltages such as zero. At the end of the pre-charging sub-cycle P11, the storage capacitor 112 is charged with a voltage close to (VDD+V_P-V_{OLEDi}).

[0043] During the compensation sub-cycle P12, the select line SEL2 is high so that the transistors 106 and 110 are on, and the select lines SEL1 and SEL3 are low so that the transistors 102 and 108 are off. As a result, the storage capacitor 112 starts discharging through the transistor 104 and the OLED 114 until the current through the driving transistor 104 and the OLED 114 becomes close to zero. Consequently, the voltage close to (V_T+V_P+V_{OLED}-V_{OLEDi}) is stored in the storage capacitor 112 where V_{OLED} is the ON voltage of the OLED 114.

[0044] During the driving cycle 122, the select line SEL2 is low so that the transistors 106 and 110 are off, and the select lines SEL1 and SEL3 are high so that the transistors 102 and 108 are on. As a result, the storage capacitor 112 is disconnected from the signal line VDATA and is connected to the source of the driving transistor 104.

[0045] If the driving transistor 104 is in saturation region, a current close to $K(V_P+\Delta V_{OLED})^2$ goes through the OLED 114 until the next programming cycle where K is the trans-conductance coefficient of the driving transistor 104, and $\Delta V_{OLED}=V_{OLED}-V_{OLEDi}$.

[0046] Figure 2 illustrates an example of a simulation result for the operation of Figures 1A-1B. The graph of Figure 2 represents OLED current during the driving cycle 122 as a function of shift in its voltage. Referring to Figures 1A, 1B and 2, it

can be seen that as ΔV_{OLED} increases over time, the driving current of the OLED 114 is also increased. Thus, the pixel circuit 100 compensates for luminance degradation of the OLED 114 by increasing the driving current of the OLED 114.

[0047] Figure 3 illustrates an example of another simulation result for the operation of Figures 1A-1B. The graph of Figure 3 represents OLED current during the driving cycle 122 as a function of shift in the threshold voltage of the driving transistor 104. Referring to Figures 1A, 1B and 3, the pixel circuit 100 compensates for shift in the threshold voltage of the driving transistor 104 since the driving current of the OLED 114 is independent of the threshold of the driving transistor 104. The result as shown in Figure 3 emphasizes the OLED current stability for 4-V shift in the threshold of the driving transistor.

[0048] Figure 4A illustrates an example of a pixel circuit along with its control signal lines to which the pixel driving scheme in accordance with another embodiment of the present invention is applied. The pixel circuit 130 of Figure 4A includes five transistors 132-140, a storage capacitor 142 and an OLED 144. The pixel circuit 130 is connected to two select lines SEL1 and SEL2, a signal line VDATA, a voltage line VDD, and a common ground.

[0049] The transistors 132-140 may be same or similar to the transistors 102-110 of Figure 1A. The transistors 132-140 may be amorphous silicon, poly silicon, or organic TFT or standard NMOS in CMOS technology. The storage capacitor 142 and the OLED 140 are same or similar to the storage capacitor 112 and the OLED 114 of Figure 1A, respectively.

[0050] The transistor 134 is a driving transistor. The source and drain terminals of the driving transistor 134 are connected to the anode electrode of the OLED 144 and the source of the transistor 132, respectively. The gate terminal of the driving transistor 134 is connected to the signal line VDATA through the transistor 140, and is connected to the source terminal of the transistor 136. The drain terminal of the transistor 136 is connected to the source terminal of the transistor 132 and its gate terminal is connected to the select line SEL2.

[0051] The drain terminal of the transistor 138 is connected to the source terminal of the transistor 140, its source terminal is connected to the anode of the OLED 144, and its gate terminal is connected to the select line SEL1.

[0052] The drain terminal of the transistor 140 is connected to the signal line VDATA, and its gate terminal is connected to the select line SEL2.

[0053] The driving transistor 134, the transistor 136 and the storage capacitor 142 are connected at node A2. The transistors 138 and 140 and the storage capacitor 142 are connected at node B2.

[0054] Figure 4B illustrates an example of a method of operating the pixel circuit 130 of Figure 4A. The pixel circuit 130 of Figure 4A includes n-type transistors. However, it would be understood by one of ordinary skill in the art that the method of Figure 4B is applicable to a pixel circuit having p-type transistors.

[0055] Referring to Figures 4A-4B, the operation of the pixel circuit 130 includes two operating cycles: programming cycle 150 and driving cycle 152. At the end of the programming cycle 150, node A2 is charged to ($V_P+V_T+\Delta V_{OLED}$) where V_P is a programming voltage, V_T is the threshold voltage of the transistor 134, and ΔV_{OLED} is the OLED voltage shift under bias stress.

[0056] The programming cycle 150 includes two sub-cycles: pre-charging P21 and compensation P22, hereinafter referred to as pre-charging sub-cycle P21 and compensation sub-cycle P22, respectively.

[0057] During the pre-charging sub-cycle P21, the select lines SEL1 and SEL2 are high, and VDATA goes to a proper voltage V_{OLEDi} that turns off the OLED 144. V_{OLEDi} is a predefined voltage which is less than minimum ON voltage of the OLEDs. At the end of the pre-charging sub-cycle P21, the storage capacitor 142 is charged with a voltage close to (VDD+V_{OLEDi}). The voltage at VDATA is set to (V_{OLEDi}–V_P) where V_P is a programming voltage.

[0058] During the compensation sub-cycle P22, the select line SEL2 is high so that the transistors 136 and 140 are on, and the select line SEL1 is low so that the transistors 132 and 138 are off. The voltage of VDATA at P22 is different from that

of P21 to properly charge A2 to ($V_P+V_T+\Delta V_{OLED}$) at the end of P22. As a result, the storage capacitor 142 starts discharging through the driving transistor 134 and the OLED 144 until the current through the driving transistor 134 and the OLED 144 becomes close to zero. Consequently, the voltage close to ($V_T+V_P+V_{OLED}-V_{OLEDi}$) is stored in the storage capacitor 142 where V_{OLED} is the ON voltage of the OLED 144.

[0059] During the driving cycle 152, the select SEL2 is low, resulting in turning the transistors 136 and 140 off. The select line SEL1 is high, resulting in turning the transistors 132 and 138 on. As a result, the storage capacitor 142 is disconnected from the signal line VDATA and is connected to the source terminal of the driving transistor 134

[0060] If the driving transistor 134 is in saturation region, a current close to $K(V_P+\Delta V_{OLED})^2$ goes through the OLED 144 until the next programming cycle where K is the trans-conductance coefficient of the driving transistor 134, and $\Delta V_{OLED}=V_{OLED}-V_{OLEDi}$. As a result, the driving current of the OLED 144 increases, as the ΔV_{OLED} increases over time. Thus, the pixel circuit 130 compensates for luminance degradation of the OLED 144 by increasing the driving current of the OLED 144.

[0061] Moreover, the pixel circuit 130 compensates for shift in threshold voltage of the driving transistor 134 and so the driving current of the OLED 144 is independent of the threshold V_T.

[0062] Figure 5A illustrates an example of a pixel circuit along with its control signal lines to which the pixel driving scheme in accordance with a further embodiment of the present invention is applied. The pixel circuit 160 of Figure 5A includes six transistors 162-172, a storage capacitor 174 and an OLED 176. The pixel circuit 160 is connected to two select lines SEL1 and SEL2, a signal line VDATA, a voltage line VDD, a bias current line IBIAS, and a common ground.

[0063] The transistors 162-172 may be amorphous silicon, poly silicon, or organic TFT or standard NMOS in CMOS technology. The storage capacitor 174 and the OLED 176 are same or similar to the storage capacitor 112 and the OLED 114 of Figure 1A, respectively.

[0064] The transistor 164 is a driving transistor. The source and drain terminals of the driving transistor 164 are connected to the anode electrode of the OLED 176 and the source terminal of the transistor 162, respectively. The gate terminal of the driving transistor 164 is connected to the signal line VDATA through the transistor 170 and is connected to the source terminal of the transistor 166. The drain terminal of the transistor 166 is connected to the source terminal of the transistor 162 and its gate terminal is connected to the select line SEL2.

[0065] The drain terminal of the transistor 168 is connected to the source terminal of the transistor 170, its source terminal is connected to the anode of the OLED 176, and its gate terminal is connected to the select line SEL1.

[0066] The drain terminal of the transistor 170 is connected to VDATA, and its gate terminal is connected to the select line SEL2.

[0067] The drain terminal of the transistor 172 is connected to the bias line IBIAS, its gate terminal is connected to the select line SEL2, and its source terminal is connected to the source terminal of the transistor 162 and the drain terminal of the transistor 164.

[0068] The driving transistor 164, the transistor 166 and the storage capacitor 174 are connected at node A3. The transistors 168 and 170 and the storage capacitor 174 are connected at node B3.

[0069] Figure 5B illustrates an example of a method of operating the pixel circuit 160 of Figure 5A. The pixel circuit 160 of Figure 5A includes n-type transistors. However, it would be understood by one of ordinary skill in the art that the method of Figure 5B is applicable to a pixel circuit having p-type transistors.

[0070] Referring to Figures 5A-5B, the operation of the pixel circuit 160 includes two operating cycles: programming cycle 180 and driving cycle 182. At the beginning of the second operating cycle 182, node A3 is charged to ($V_P+V_T+\Delta V_{OLED}$) where V_P is a programming voltage, V_T is the threshold voltage of the transistor 164, and ΔV_{OLED} is the OLED voltage shift under bias stress. V_T and ΔV_{OLED} are generated by large IBIAS resulting in a fast programming.

[0071] During the first operating cycle 180, the select line SEL1 is low, the select line SEL2 is high, and VDATA goes to a proper voltage (V_{OLEDi}–V_P) where V_P is a programming voltage. This proper voltage is a predefined voltage which is less than minimum ON voltage of the OLEDs. Also, the bias line IBIAS provides bias current (referred to as I_{BIAS}) to the pixel circuit 160. At the end of this cycle node A3 is charged to $V_{BIAS}+V_T+V_{OLED}(I_{BIAS})$ where V_{BIAS} is related to the bias current I_{BIAS}, and $V_{OLED}(I_{BIAS})$ is the OLED 176 voltage corresponding to I_{BIAS}. Voltage at node A3 is independent of V_P at the end of 180. Charging to ($V_P+V_T+\Delta V_{OLED}$) happens at the beginning of 182.

[0072] During the second operating cycle 182, the select line SEL1 is high and the select line SEL2 is low. As a result node B3 is charged to $V_{OLED}(I_P)$ where $V_{OLED}(I_P)$ is the OLED 176 voltage corresponding to the pixel current. Thus, the gate-source voltage of the transistor 164 becomes ($V_P+\Delta V_{OLED}+V_T$) where $\Delta V_{OLED}=V_{OLED}(I_{BIAS})-V_{OLEDi}$. Since the OLED voltage increases for a constant luminance while its luminance decreases, the gate-source voltage of the transistor 164 increases resulting in higher OLED current. Consequently, the OLED 176 luminance remains constant.

[0073] Figure 6 illustrates an example of a display system 200 including the pixel circuit 100 of Figure 1A. The display array 202 of Figure 6 includes a plurality of pixel circuit 100 arranged in rows and columns, and may form an active matrix organic light emitting diode (AMOLED) display. VDATAj (j=1, 2, ...) corresponds to VDATA of Figure 1A. SEL1k, SEL2k and SEL3k (k=1, 2, ...) correspond to SEL1, SEL2 and SEL3 of Figure 1A, respectively. The select lines SEL1k, SEL2k and SEL3k are shared among the pixels in the common row of the display array 202. The signal line VDATAj is shared among the pixels in the common column of the display array 202.

[0074] The display system 200 includes a driving module 204 having an address driver 206, a source driver 208, and a controller 210. The select lines SEL1k, SEL2k and SEL3k are driven by the address driver 206. The signal line VDATAj is driven by the source driver 208. The controller 210 controls the operation of the address driver 206 and the source driver 208 to operate the display array 202.

[0075] The waveforms shown in Figure 1B are generated by the driving module 204. The driver module 204 also generate the programming voltage. The compensation for OLED degradation, threshold voltage shift and ground bouncing occur in pixel. During the third cycle (122 of Figure 1B), the gate-source voltage of the driving transistor is defined by the voltage stored in the storage capacitor (112 of Figure 1). Therefore, the ground bouncing does not change the gate-source voltage and so the pixel current become stable.

[0076] Figure 7 illustrates an example of a method of operating the display array of Figure 6. In Figure 7, Row(i) (i=1, 2, ...) represents a row of the display array 202 of Figure 6. "120" and "122" in Figure 7 represent "programming cycle" and "driving cycle" and correspond to those of Figure 1B, respectively. "P11" and "P12" in Figure 7 represent "pre-charging sub-cycle" and "compensation sub-cycle" and correspond to those of Figure 1B, respectively. The compensation sub-cycle P11 in a row and the pre-charging sub-cycle P12 in an adjacent row are performed in parallel. Further, during the driving cycle 122 in a row, the compensation sub-cycle P22 is performed in an adjacent row. The display system 200 of Figure 6 is designed to implement the parallel operation, i.e., having capability of carrying out different cycles independently without affecting each other.

[0077] Figure 8 illustrates an example of a display system 300 including the pixel circuit 130 of Figure 4A. The display array 302 of Figure 8 includes a plurality of pixel circuit 130 arranged in rows and columns, and may form an AMOLED display. VDATAj (j=1, 2, ...) corresponds to VDATA of Figure 4A. SEL1k and SEL2k (k=1, 2, ...) correspond to SEL1 and SEL2 of Figure 4A, respectively. The select lines SEL1k and SEL2k are shared among the pixels in the common row of the display array 302. The signal line VDATAj is shared among the pixels in the common column of the display array 302.

[0078] The display system 300 includes a driving module 304 having an address driver 306, a source driver 308, and a controller 310. The select lines SEL1k and SEL2k are driven by the address driver 306. The signal line VDATAj is driven by the source driver 308. The controller 310 controls the operation of the address driver 306 and the source driver 308 to operate the display array 302.

[0079] The waveforms shown in Figure 4B are generated by the driving module 304. The driver module 304 also generates the programming voltage. The compensation for OLED degradation, threshold voltage shift and ground bouncing occur in pixel. During the third cycle (152 of Figure 4B), the gate-source voltage of the driving transistor is defined by the voltage stored in the storage capacitor (142 of Figure 4A). Therefore, the ground bouncing does not change the gate-source voltage and so the pixel current become stable.

[0080] Figure 9 illustrates an example of a method of operating the display array of Figure 8. In Figure 9, Row(i) (i=1, 2, ...) represents a row of the display array 302 of Figure 8. "150" and "152" in Figure 9 represent "programming cycle" and "driving cycle" and correspond to those of Figure 4B, respectively. "P21" and "P22" in Figure 9 represent "pre-charging sub-cycle" and "compensation sub-cycle" and correspond to those of Figure 4B, respectively. The compensation sub-cycle P21 in a row and the pre-charging sub-cycle P22 in an adjacent row are performed in parallel. Further, during the driving cycle 152 in a row, the compensation sub-cycle P22 is performed in an adjacent row. The display system 300 of Figure 8 is designed to implement the parallel operation, i.e., having capability of carrying out different cycles independently without affecting each other.

[0081] Figure 10 illustrates an example of a display system 400 including the pixel circuit 160 of Figure 5A. The display array 402 of Figure 10 includes a plurality of pixel circuit 160 arranged in rows and columns, and is an AMOLED display. The display array 402 may be an AMOLED display. VDATAj (j=1, 2, ...) corresponds to VDATA of Figure 4A. IBIASj (j=1, 2, ...) corresponds to IBIAS of Figure 4A. SEL1k and SEL2k (k=1, 2, ...) correspond to SEL1 and SEL2 of Figure 4A, respectively. The select lines SEL1k and SEL2k are shared among the pixels in the common row of the display array 402. The signal line VDATAj and the bias line IBIASj are shared among the pixels in the common column of the display array 402.

[0082] The display system 400 includes a driving module 404 having an address driver 406, a source driver 408, and a controller 410. The select lines SEL1k and SEL2k are driven by the address driver 406. The signal line VDATAj and the bias line IBIASj are driven by the source driver 408. The controller 410 controls the

operation of the address driver 406 and the source driver 408 to operate the display array 402.

[0083] The waveforms shown in Figure 5B are generated by the driving module 404. The driver module 404 also generate the programming voltage. The compensation for OLED degradation, threshold voltage shift and ground bouncing occur in pixel. During the second cycle 182 of Figure 5B, the gate-source voltage of the driving transistor is defined by the voltage stored in the storage capacitor (174 of Figure 5A). Therefore, the ground bouncing does not change the gate-source voltage and so the pixel current become stable.

[0084] Figure 11 illustrates an example of a method of operating the display array of Figure 10. In Figure 9, Row(i) (i=1, 2, ...) represents a row of the display array 402 of Figure 10. "180" and "182" in Figure 11 correspond to those of Figure 5B, respectively. For the rows of the display array 402, the programming cycle 180 is subsequently performed. During the driving cycle 182 in a row, the programming cycle 180 is performed in an adjacent row. The display system 400 of Figure 10 is designed to implement the parallel operation, i.e., having capability of carrying out different cycles independently without affecting each other.

[0085] All citations are hereby incorporated by reference.

[0086] The present invention has been described with regard to one or more embodiments. However, it will be apparent to persons skilled in the art that a number of variations and modifications can be made without departing from the scope of the invention as defined in the claims.

WHAT IS CLAIMED IS:

1. A pixel circuit comprising:

a light emitting device;

a storage capacitor having a first terminal and a second terminal;

a first transistor having a gate terminal, a first terminal and a second terminal, the gate terminal being connected to a first select line;

a second transistor having a gate terminal, a first terminal and a second terminal, the first terminal being connected to the second terminal of the first transistor, the second terminal being connected to the light emitting device;

a third transistor having a gate terminal, a first terminal and a second terminal, the gate terminal being connected to a second select line, the first terminal being connected to the second terminal of the first transistor, the second terminal being connected to the gate terminal of the second transistor and the first terminal of the storage capacitor;

a fourth transistor having a gate terminal, a first terminal and a second terminal, the gate terminal being connected to a third select line, the first terminal being connected to the second terminal of the storage capacitor, the second terminal being connected to the second terminal of the second transistor and the light emitting device; and

a fifth transistor having a gate terminal, a first terminal and a second terminal, the gate terminal being connected to the second select line, the first terminal being connected to a signal line, the second terminal being connected to the first terminal of the forth transistor and the second terminal of the storage capacitor.

2. A pixel circuit according to claim 1, wherein the first select line, the second select line and the third select line are driven to form a programming cycle and a driving cycle, the programming cycle including a pre-charge cycle and a compensation cycle.

3. A pixel circuit according to claim 2, wherein the storage capacitor is charged during the pre-charge cycle, the storage capacitor being discharged during the compensation cycle, the second terminal of the storage capacitor being disconnected from the signal line and being connected to the second terminal of the second transistor during the driving cycle.

4. A pixel circuit according to claim 3, wherein the first select line, the second select line, the signal line are driven such that during the compensation cycle, the storage capacitor stores a voltage depending on a threshold voltage of the second transistor, a voltage associated with the light emitting device and a programming voltage.

5. A pixel circuit according to claim 1, wherein the third select line is the first select tine.

6. A pixel circuit according to claim 5, wherein the first select line and the second select line are driven to form a programming cycle and a driving cycle, the programming cycle including a pre-charge cycle and a compensation cycle.

7. A pixel circuit according to claim 6, wherein the storage capacitor is charged during the pre-charge cycle, the storage capacitor being discharged during the compensation cycle, the second terminal of the storage capacitor being disconnected from the signal line and being connected to the second terminal of the second transistor during the driving cycle.

8. A pixel circuit according to claim 7, wherein the first select line, the second select line and the signal line are driven such that during the compensation cycle, the storage capacitor stores a voltage depending on a threshold voltage of the second transistor, a voltage associated with the light emitting device and a programming voltage.

9. A pixel circuit according to claim 5, further comprising a sixth transistor having a gate terminal, a first terminal and a second terminal, the gate terminal being connected to the second select line, the first terminal being connected to the first

terminal of the second transistor, the second terminal being connected to a bias current line.

10. A pixel circuit according to claim 9, wherein the first select line and the second select line are driven to form a first operating cycle and a second operating cycle.

11. A pixel circuit according to claim 10, wherein the storage capacitor is connected to the signal line and the bias current line during the first operating cycle, the storage capacitor being disconnected from the signal line and the bias current line and the second terminal of the storage capacitor being connected to the second terminal of the second transistor during the second operating cycle.

12. A pixel circuit according to claim 11, wherein the first select line, the second select line, the bias current line and the signal line are driven such that the storage capacitor stores a voltage depending on a threshold voltage of the second transistor, a voltage associated with the light emitting device, and a programming voltage.

13. A pixel circuit according to any one of claims 1-12, wherein the light emitting device is an organic light emitting diode.

14. A pixel circuit according to any one of claims 1-12, wherein the pixel circuit forms an electro-luminance device display.

15. A pixel circuit according to claim 14, wherein the pixel circuit forms an active matrix light emitting display.

16. A pixel circuit according to claim 15, wherein the display is an active matrix organic light emitting display.

17. A pixel circuit according to any one of claims 1-12, wherein at least one of the transistors includes amorphous, nano/micro crystalline, poly, organic material, n-type material, p-type material, or CMOS silicon.

18. A pixel circuit according to any one of claims 1-12, wherein the at least one of the transistors is a n-type or p-type TFT.

19. A display system comprising:

a display array formed by the pixel circuit of claim 1; and

a driving module for driving the first select line, the second select line, the third select line and the signal line and forming a programming cycle and a driving cycle, the programming cycle including a pre-charge cycle and a compensation cycle, the storage capacitor being charged during the pre-charge cycle, the storage capacitor being discharged during the compensation cycle, the second terminal of the storage capacitor being disconnected from the signal line and being connected to the second terminal of the second transistor during the driving cycle.

20. A display system comprising:

a display array formed by the pixel circuit of claim 6;

a driving module for driving the first select line, the second select line and the signal line and forming a programming cycle and a driving cycle, the programming cycle having a pre-charge cycle and a compensation cycle, the storage capacitor being charged during the pre-charge cycle, the storage capacitor being discharged during the compensation cycle. the second terminal of the storage capacitor being disconnected from the signal line and being connected to the second terminal of the second transistor during the driving cycle.

21. A display system comprising:

a display array formed by the pixel circuit of claim 9;

a driving module for driving the first select line, the second select line, the signal line and the bias current line and forming a first operating cycle and a second operating cycle, the storage capacitor being connected to the signal line and the bias current line during the first operating cycle, the storage capacitor being disconnected from the signal line and the bias current line and being connected to the second transistor during the second operating cycle.

22. A display system according to claim 19, wherein the driver module operates the pre-charging cycle and the compensation cycle so that the pre-charging cycle in a

row of the display array and the compensation cycle in an adjacent row of the display array are performed in parallel.

23. A display system according to claim 20, wherein the driver module operates the pre-charging cycle and the compensation cycle so that the pre-charging cycle in a row of the display array and the compensation cycle in an adjacent row of the display array are performed in parallel.

24. A display system according to claim 21, wherein the driver module operates the first operating cycle and the second operating cycle to subsequently perform the first operating cycle in the rows of the display array and to perform the second operating cycle after the first operating cycle.

25. A method for compensating for degradation of the light emitting device of claim 1, comprising the steps of:

charging the storage capacitor, including connecting the storage capacitor to the signal line;

discharging the storage capacitor; and

disconnecting the storage capacitor from the signal line and connecting the second terminal of the storage capacitor to the second terminal of the second transistor.

26. A method according to claim 25, a voltage depending on a threshold voltage of the second transistor, a voltage associated with the light emitting device and a programming voltage is stored in the storage capacitor to drive the pixel circuit.

27. A method for compensating for shift in a threshold voltage of the transistor in the pixel circuit of claim 1, comprising the steps of:

charging the storage capacitor, including connecting the storage capacitor to the signal line;

discharging the storage capacitor; and

disconnecting the storage capacitor from the signal line and connecting the second terminal of the storage capacitor to the second terminal of the second transistor.

28. A method according to claim 27, wherein a voltage depending on a threshold voltage of the second transistor, a voltage associated with the light emitting device and a programming voltage is stored in the storage capacitor to drive the pixel circuit.

29. A method for compensating for ground bouncing or IR drop in the pixel circuit of claim 1, comprising the steps of:

charging the storage capacitor, including connecting the storage capacitor to the signal line and the bias current line;

discharging the storage capacitor; and

disconnecting the storage capacitor from the signal line and the bias current line and connecting the second terminal of the storage capacitor to the second terminal of the second transistor.

30. A method according to claim 29, wherein a voltage depending on a threshold voltage of the second transistor, a voltage associated with the light emitting device, and a programming voltage is stored in the storage capacitor to drive the pixel circuit.

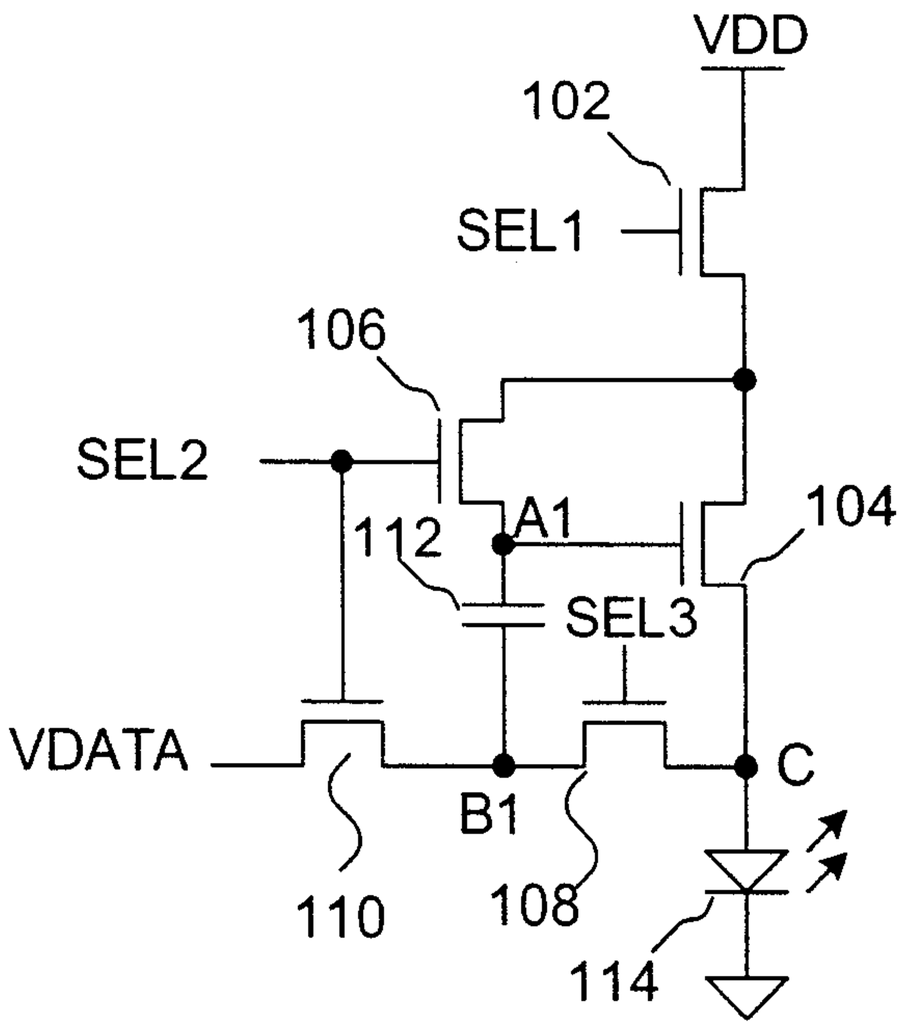


FIG.1A

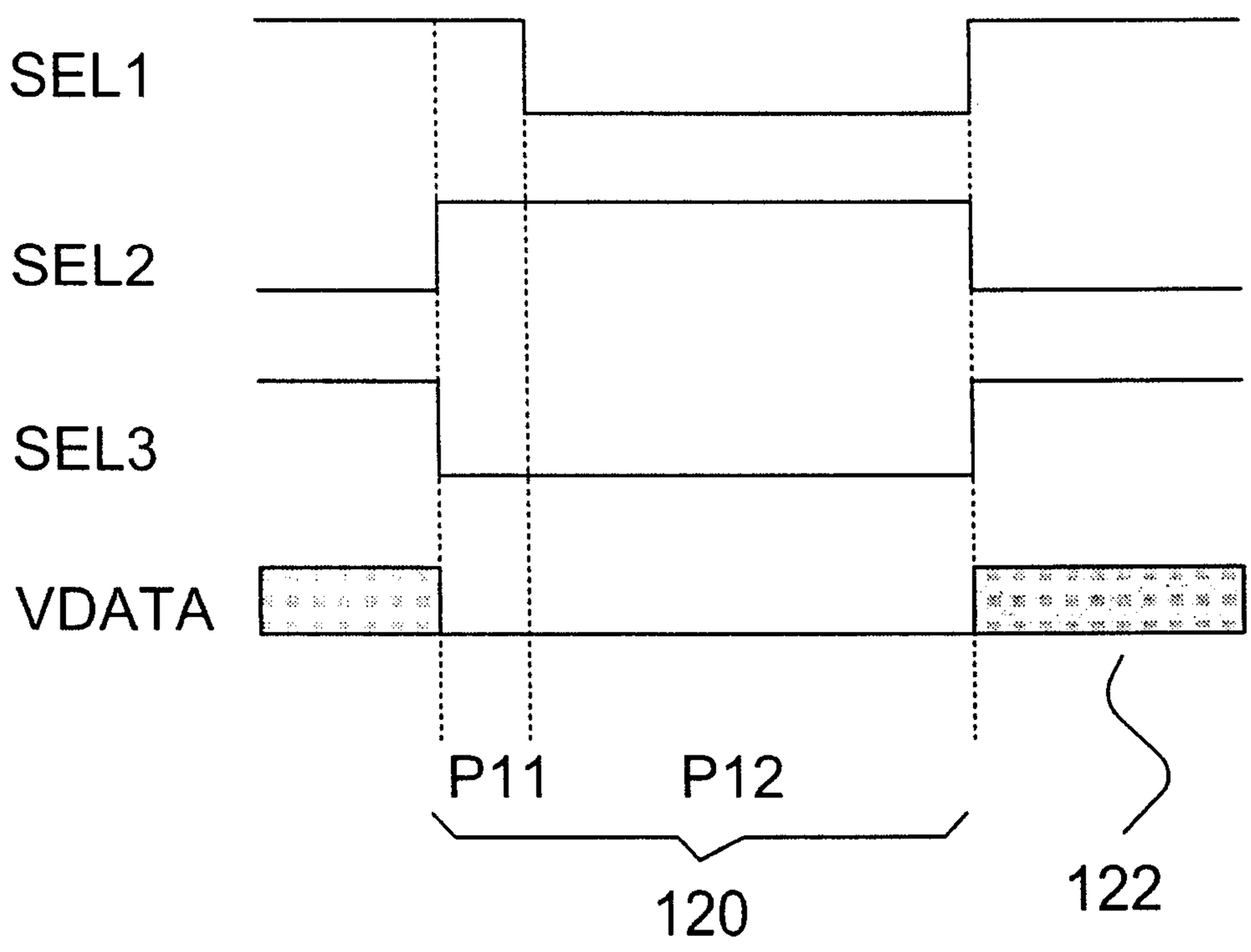


FIG.1B

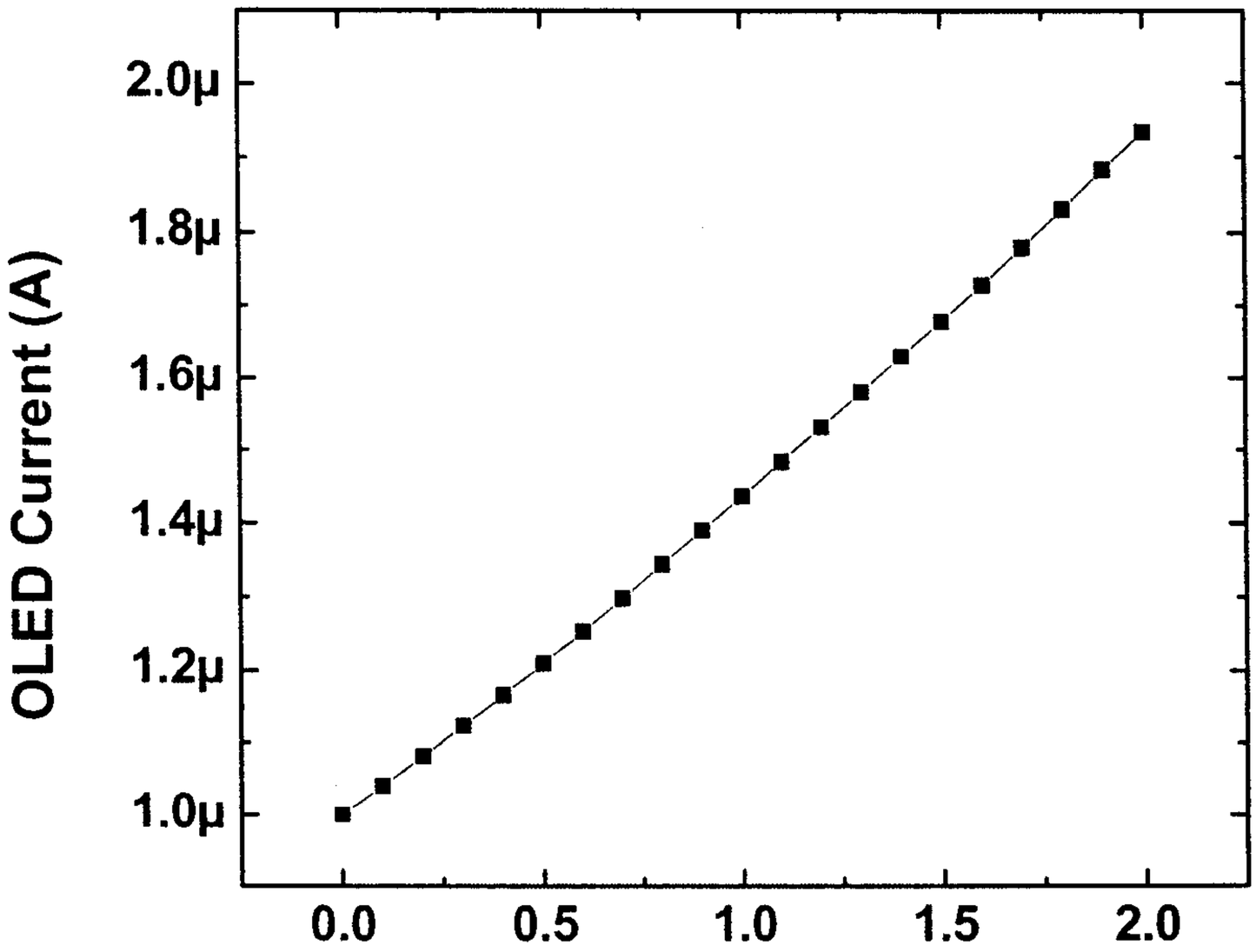

2.0µ
1.8µ
1.6µ
1.4µ
1.2µ
1.0µ
OLED Current (A)
0.0
0.5
1.0
1.5
2.0
Shift in OLED Voltage (V)

FIG.2

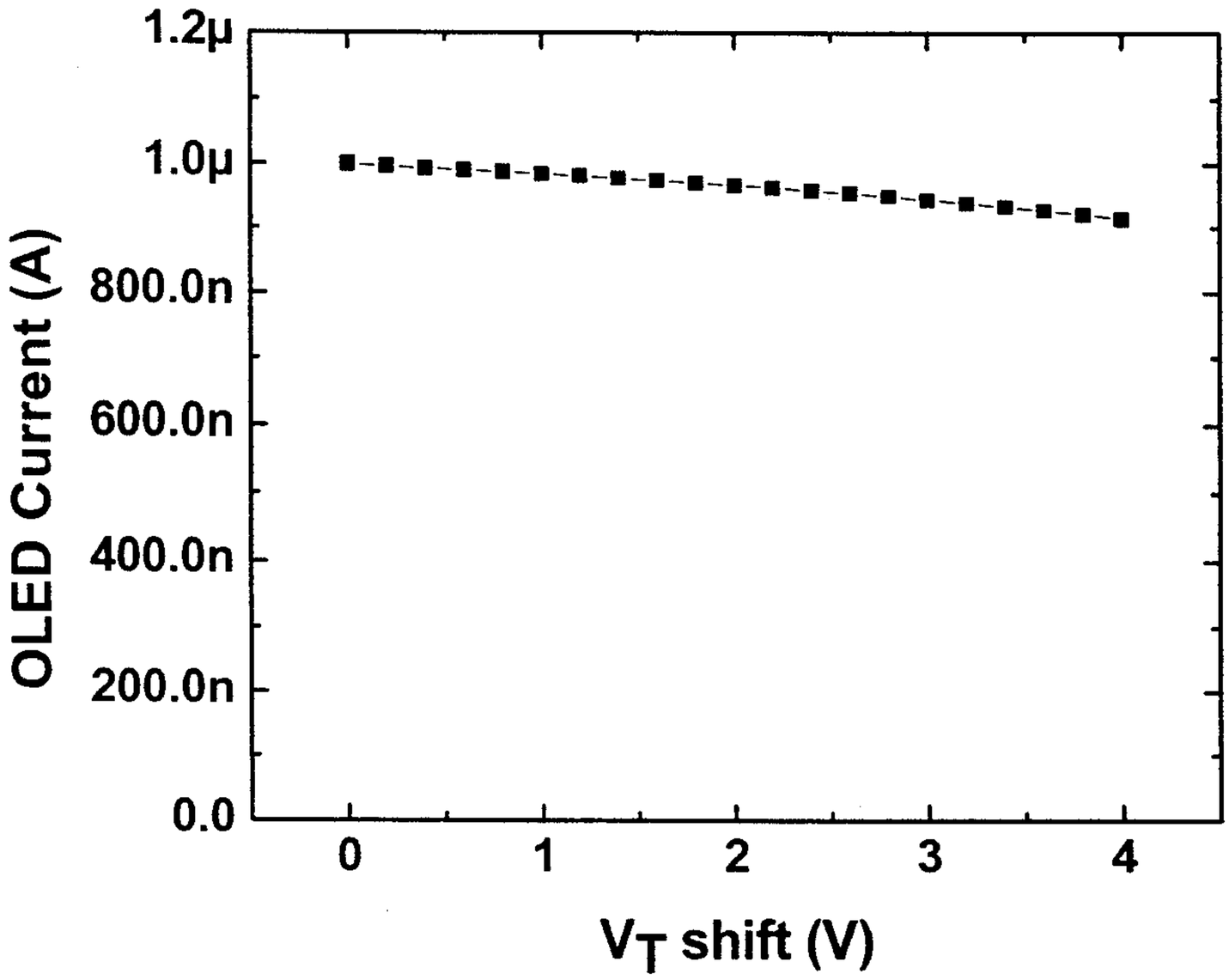

1.2µ
1.0µ
800.0n
600.0n
400.0n
200.0n
0.0
OLED Current (A)
0
1
2
3
4
V_T shift (V)

FIG.3

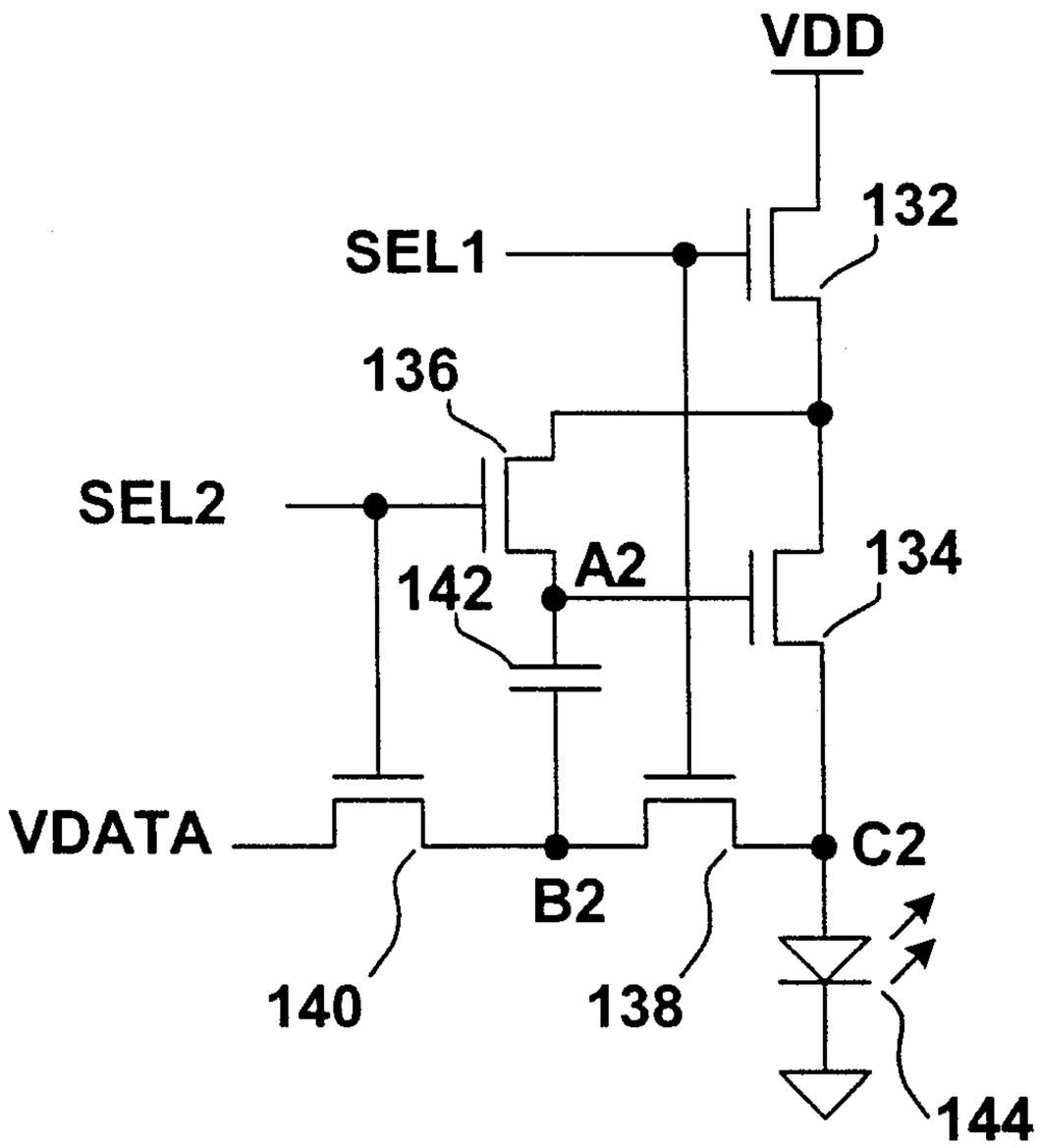

VDD
132
SEL1
136
SEL2
142
A2
134
VDATA
B2
C2
140
138
144

FIG.4A

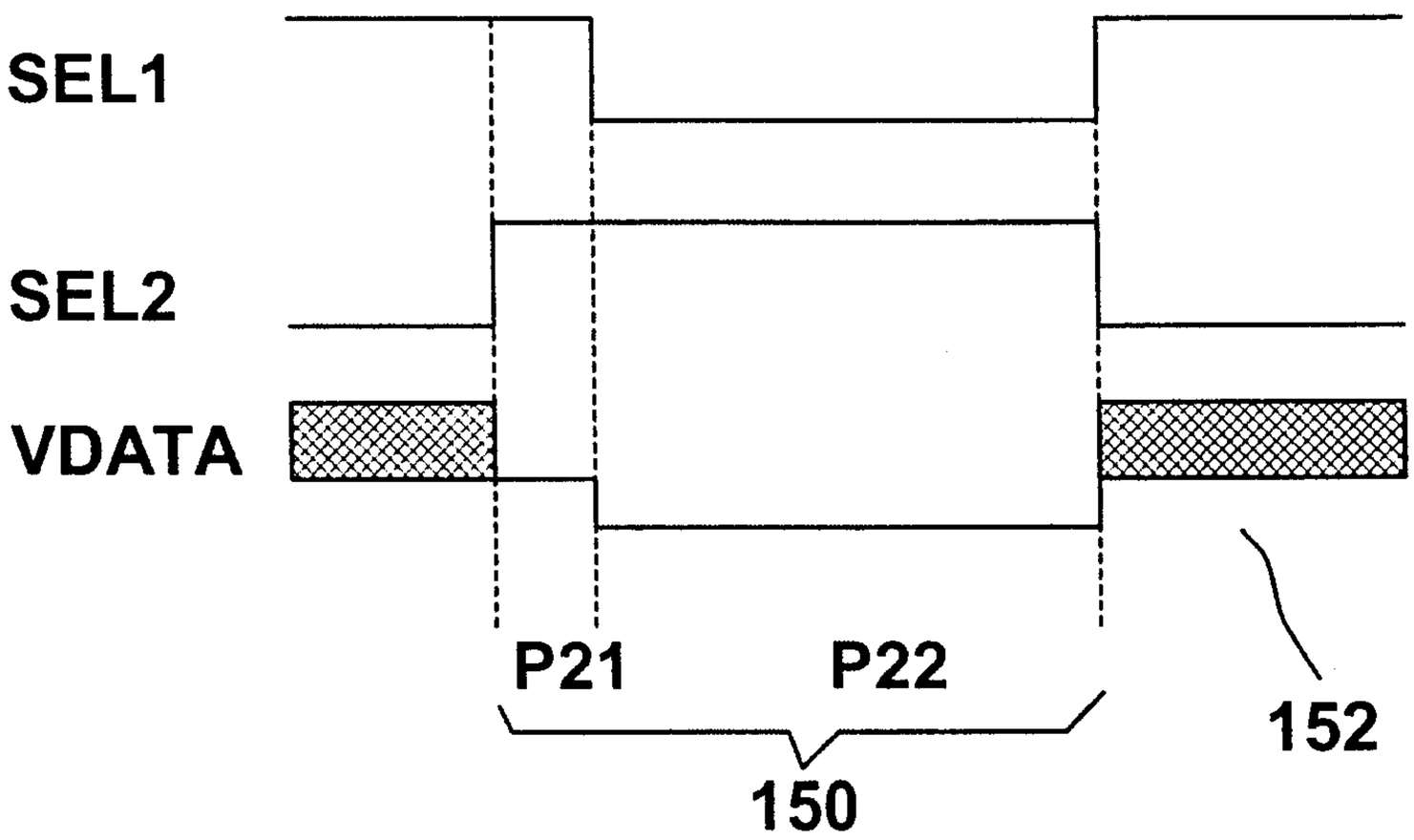

SEL1
SEL2
VDATA
P21
P22
150
152

FIG.4B

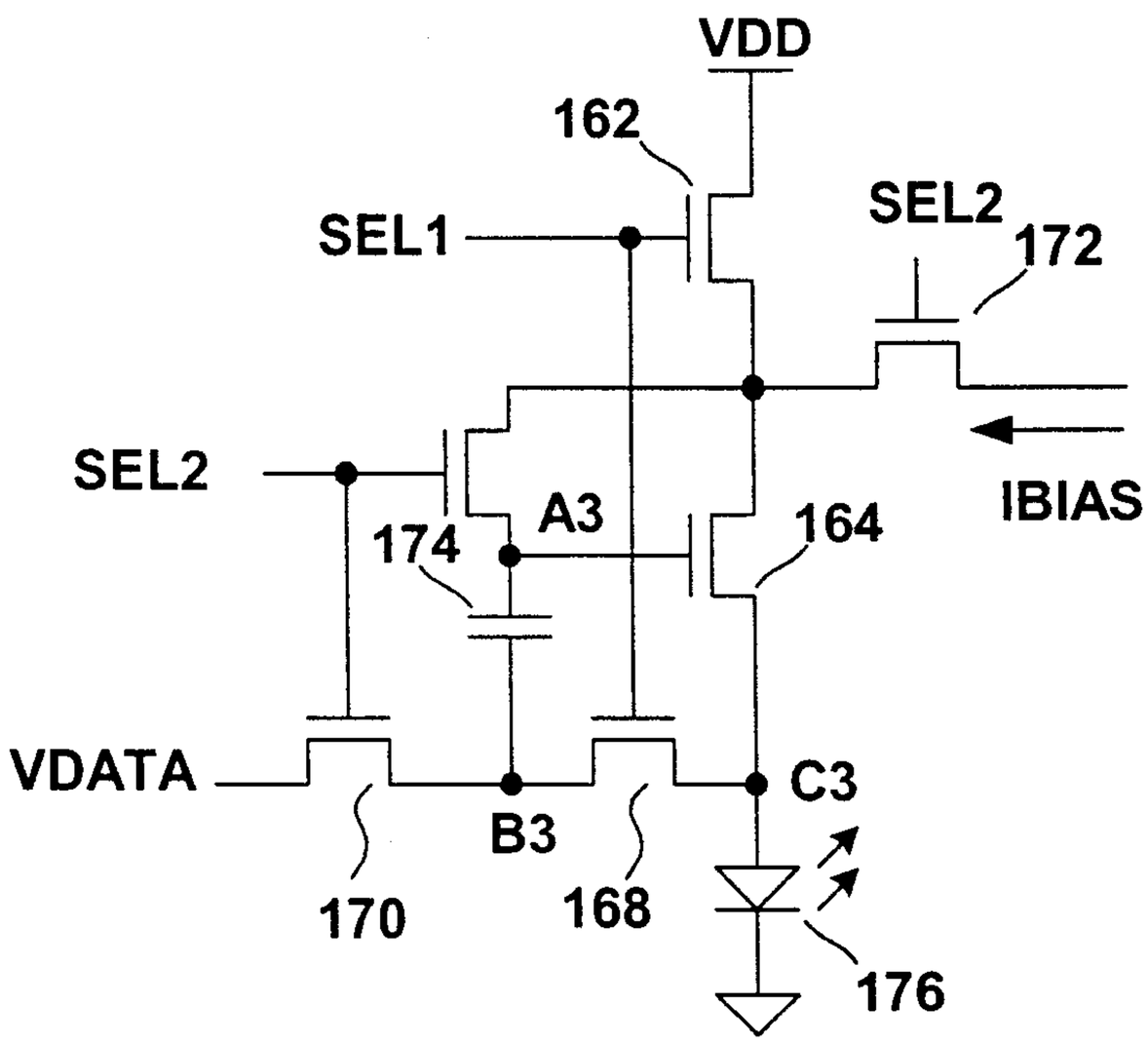

VDD
162
SEL1
SEL2
172
SEL2
IBIAS
174
A3
164
VDATA
C3
B3
170
168
176

FIG.5A

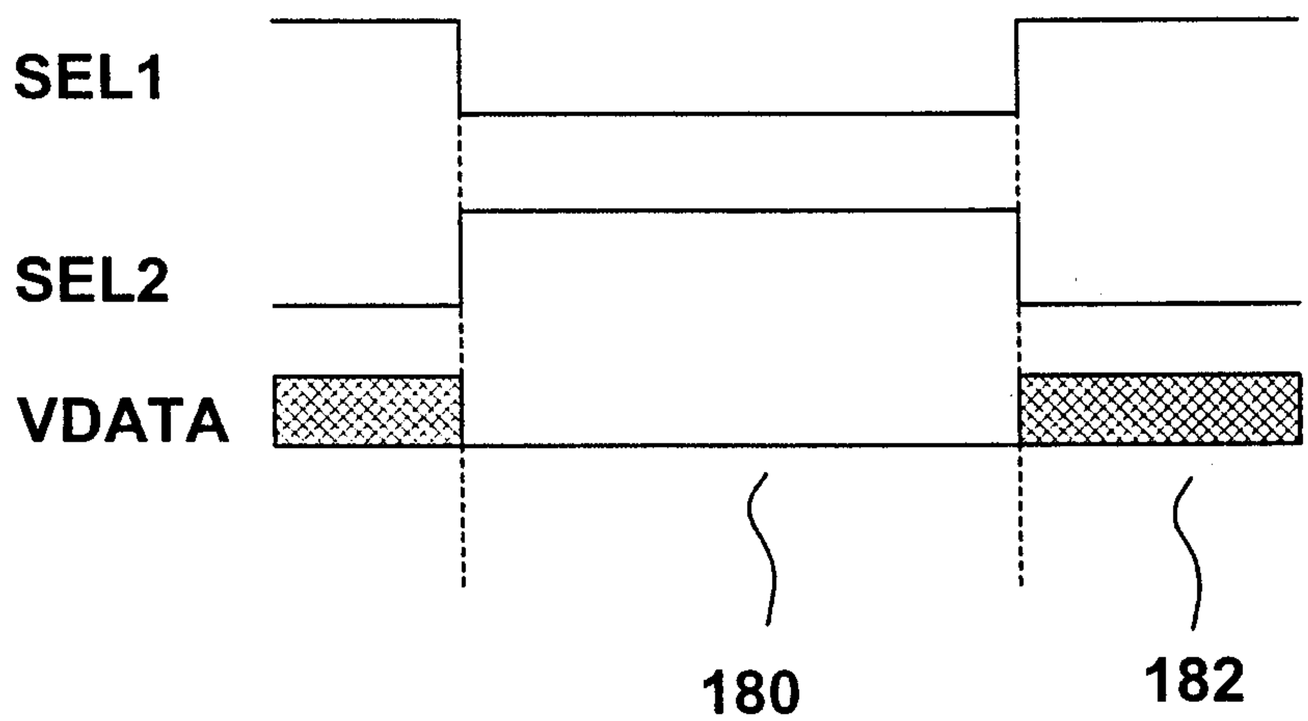

SEL1
SEL2
VDATA
180
182

FIG.5B

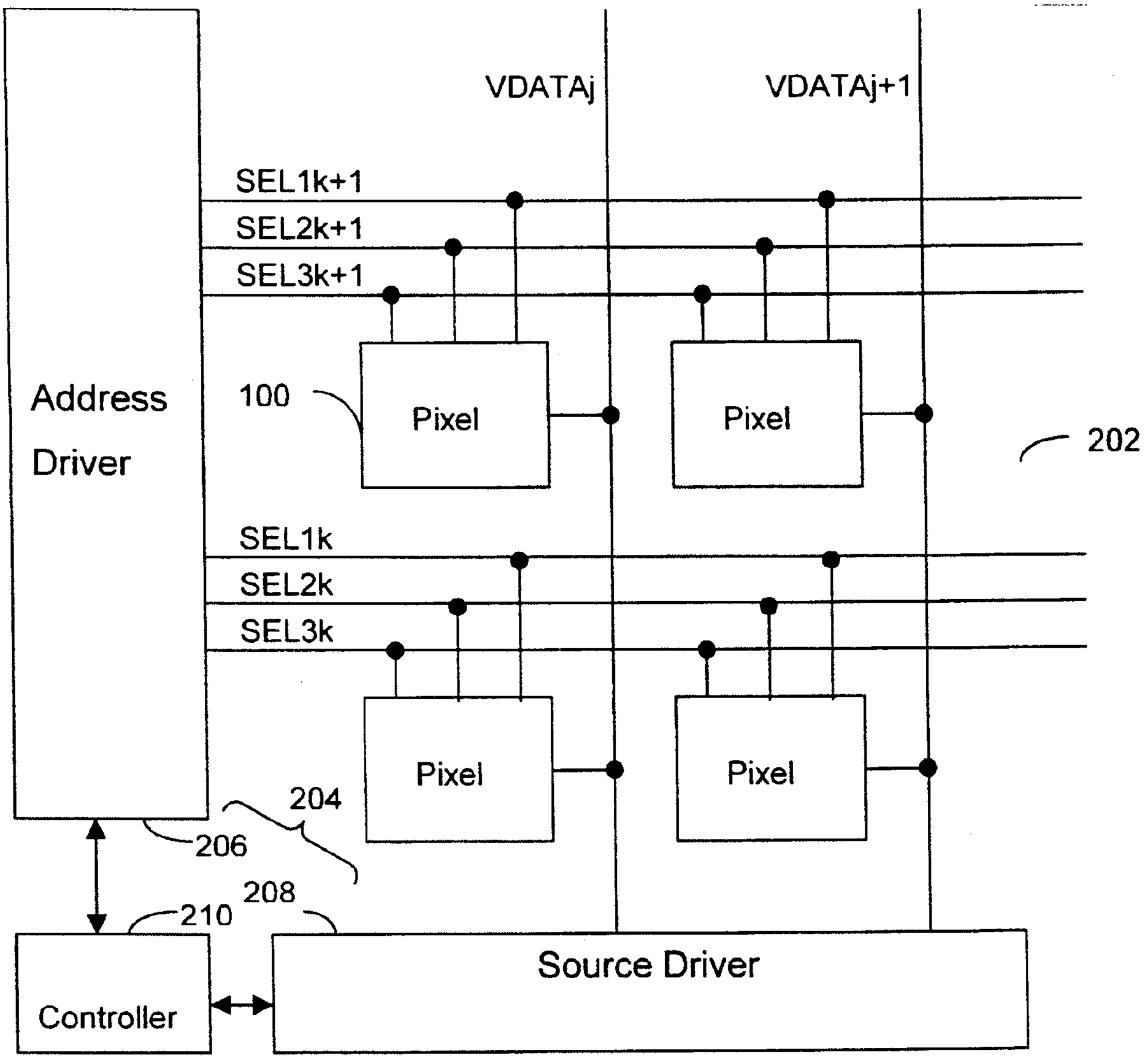

VDATAj
VDATAj+1
SEL1k+1
SEL2k+1
SEL3k+1
Address
Driver
100
Pixel
Pixel
202
SEL1k
SEL2k
SEL3k
Pixel
Pixel
204
206
208
210
Controller
Source Driver

FIG.6

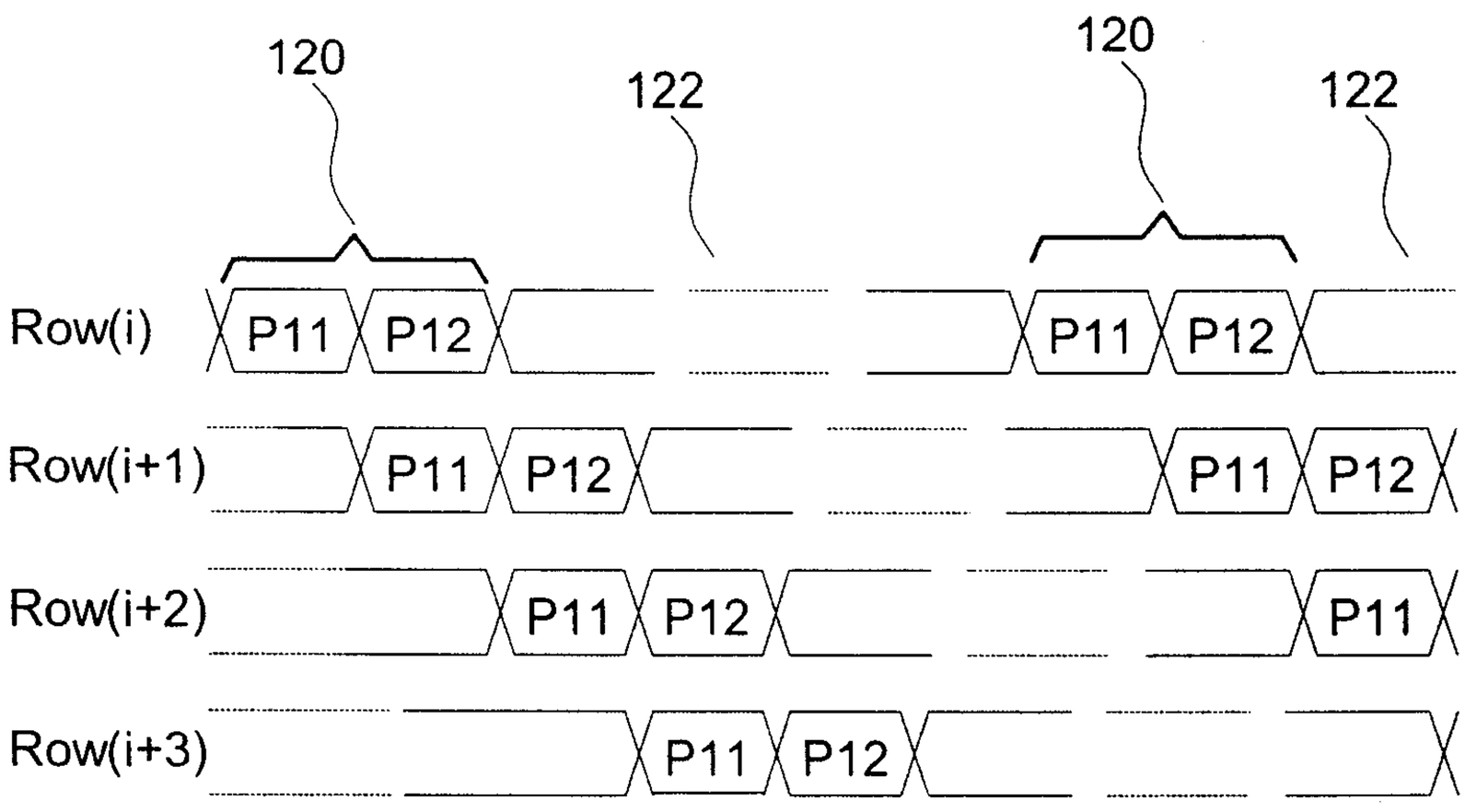

120
122
120
122
Row(i)
Row(i+1)
Row(i+2)
Row(i+3)
P11
P12
P11
P12
P11
P12
P11
P12
P11
P12
P11
P12

FIG.7

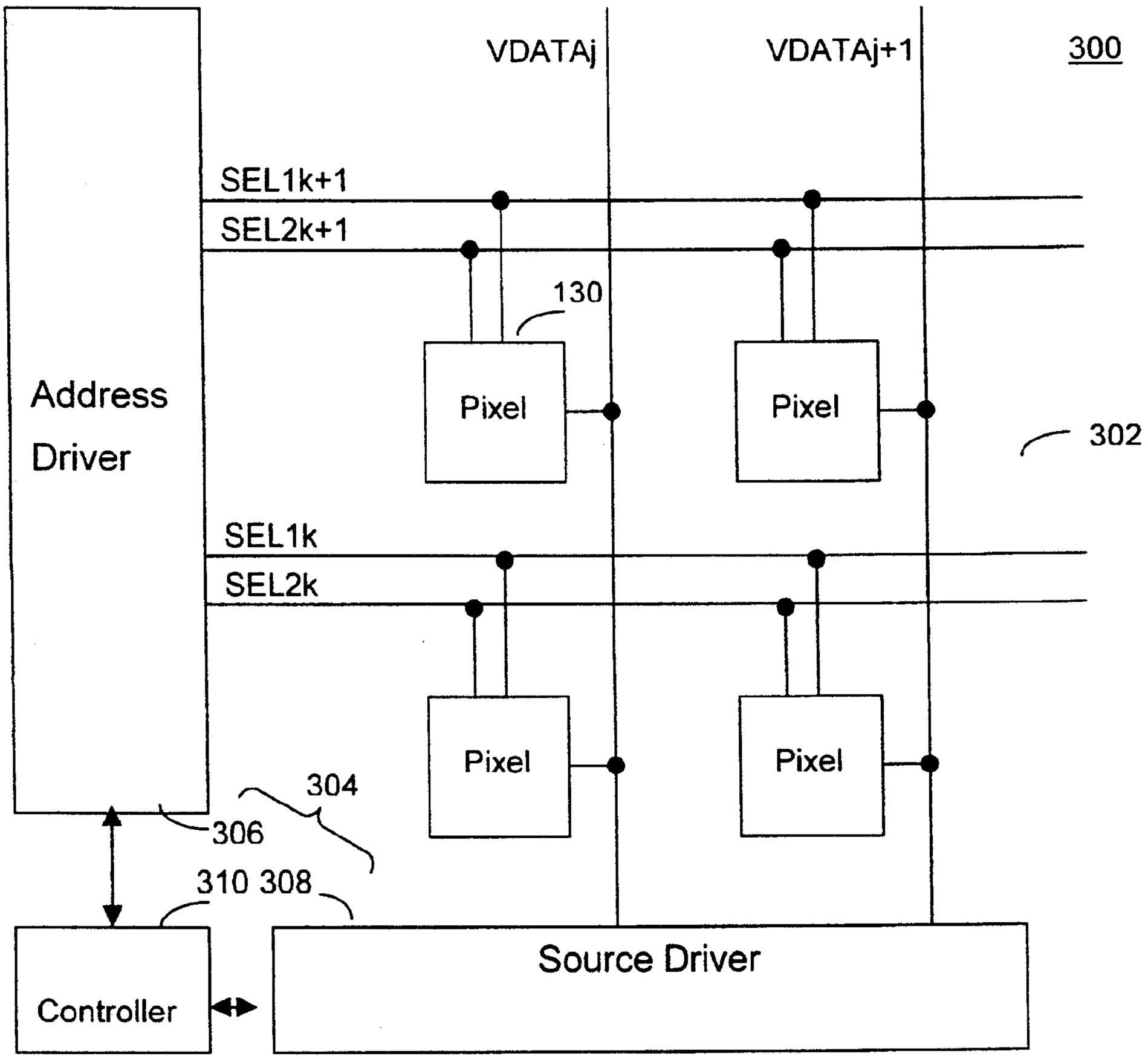

VDATAj
VDATAj+1
300
SEL1k+1
SEL2k+1
130
Address
Driver
Pixel
Pixel
302
SEL1k
SEL2k
Pixel
Pixel
304
306
310 308
Controller
Source Driver

FIG.8

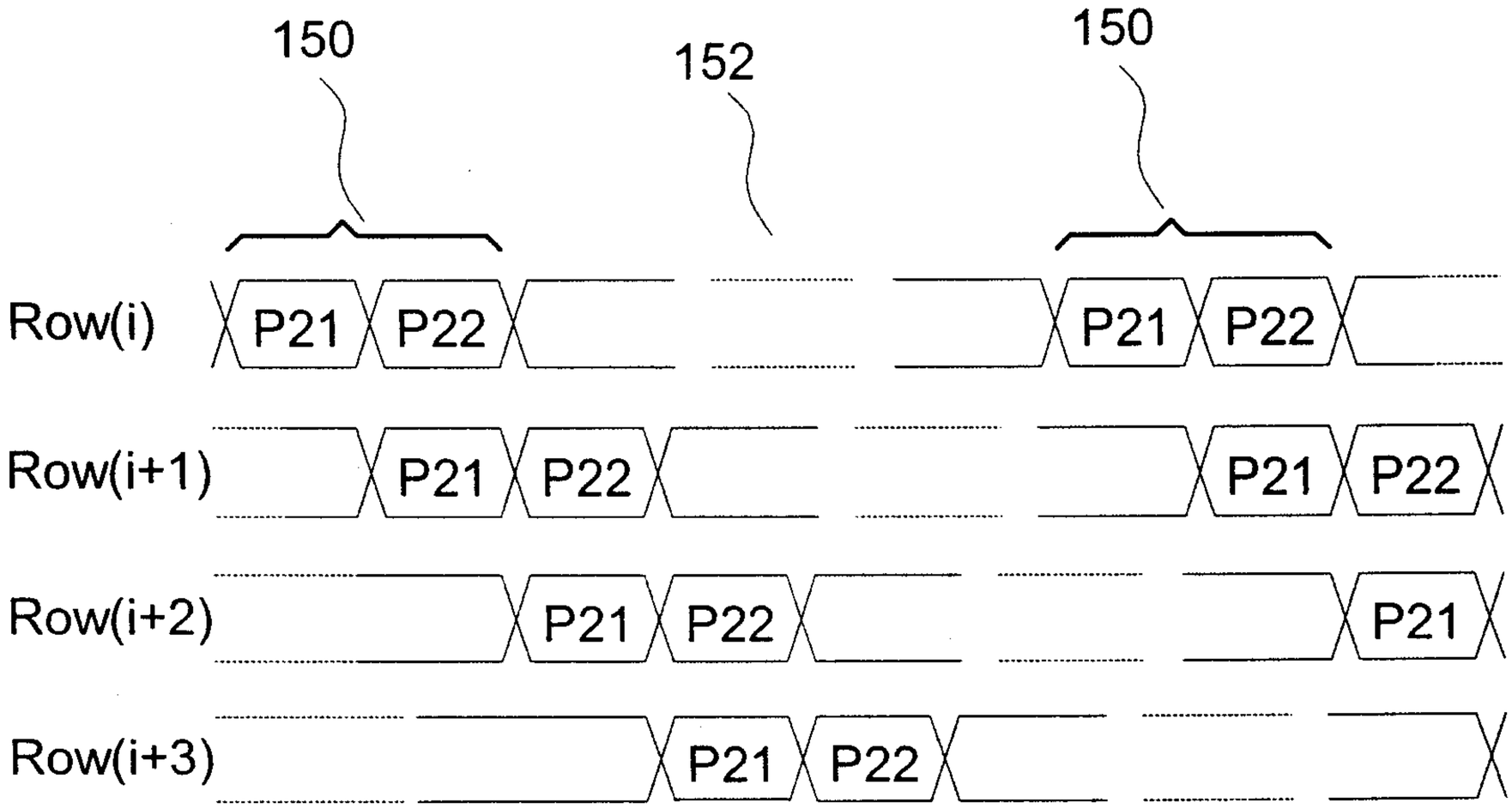

150
152
150
Row(i)
P21
P22
P21
P22
Row(i+1)
P21
P22
P21
P22
Row(i+2)
P21
P22
P21
Row(i+3)
P21
P22

FIG.9

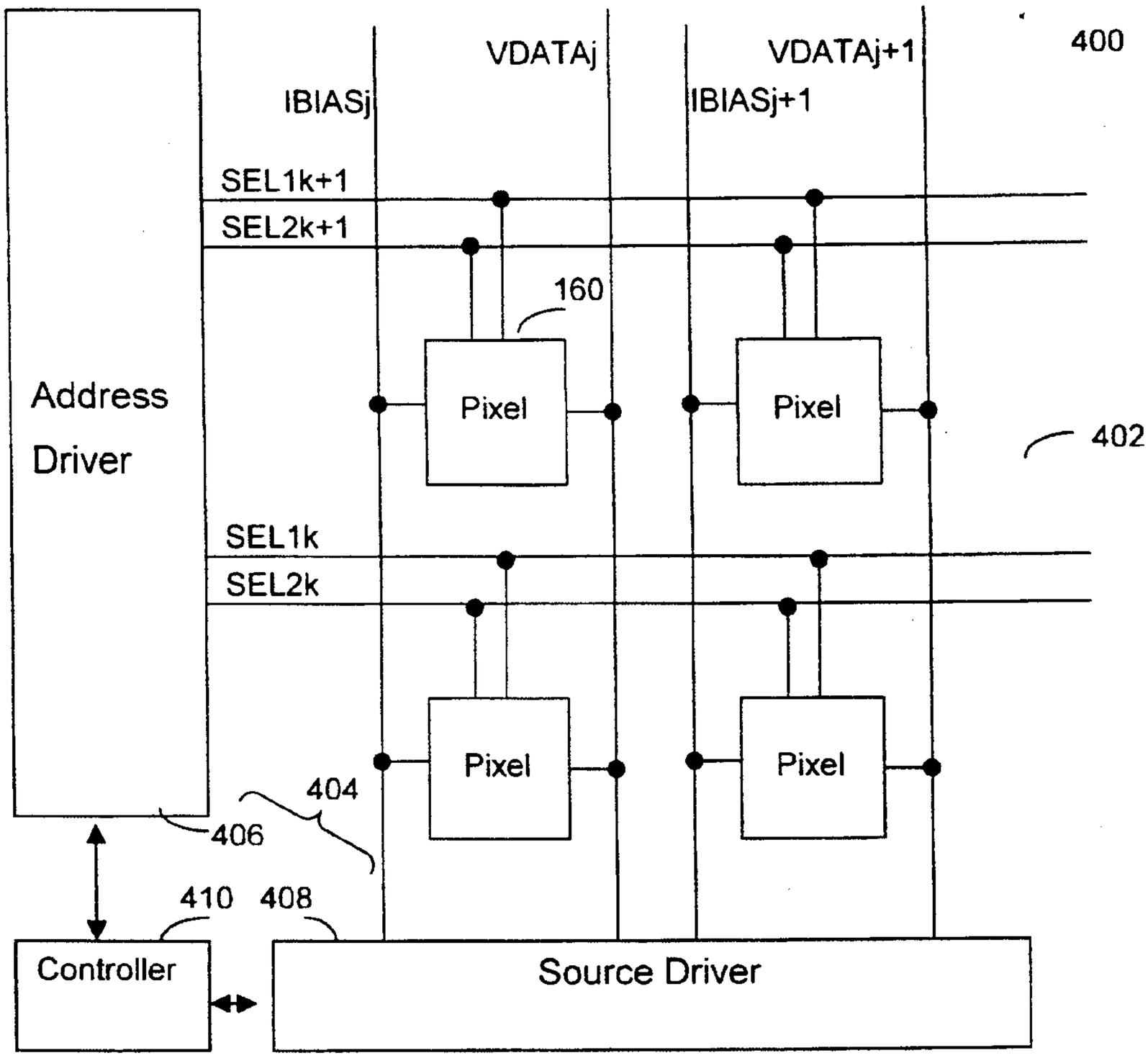

VDATAj
VDATAj+1
400
IBIASj
IBIASj+1
SEL1k+1
SEL2k+1
160
Pixel
Pixel
Address
Driver
402
SEL1k
SEL2k
Pixel
Pixel
404
406
410
408
Controller
Source Driver

FIG.10

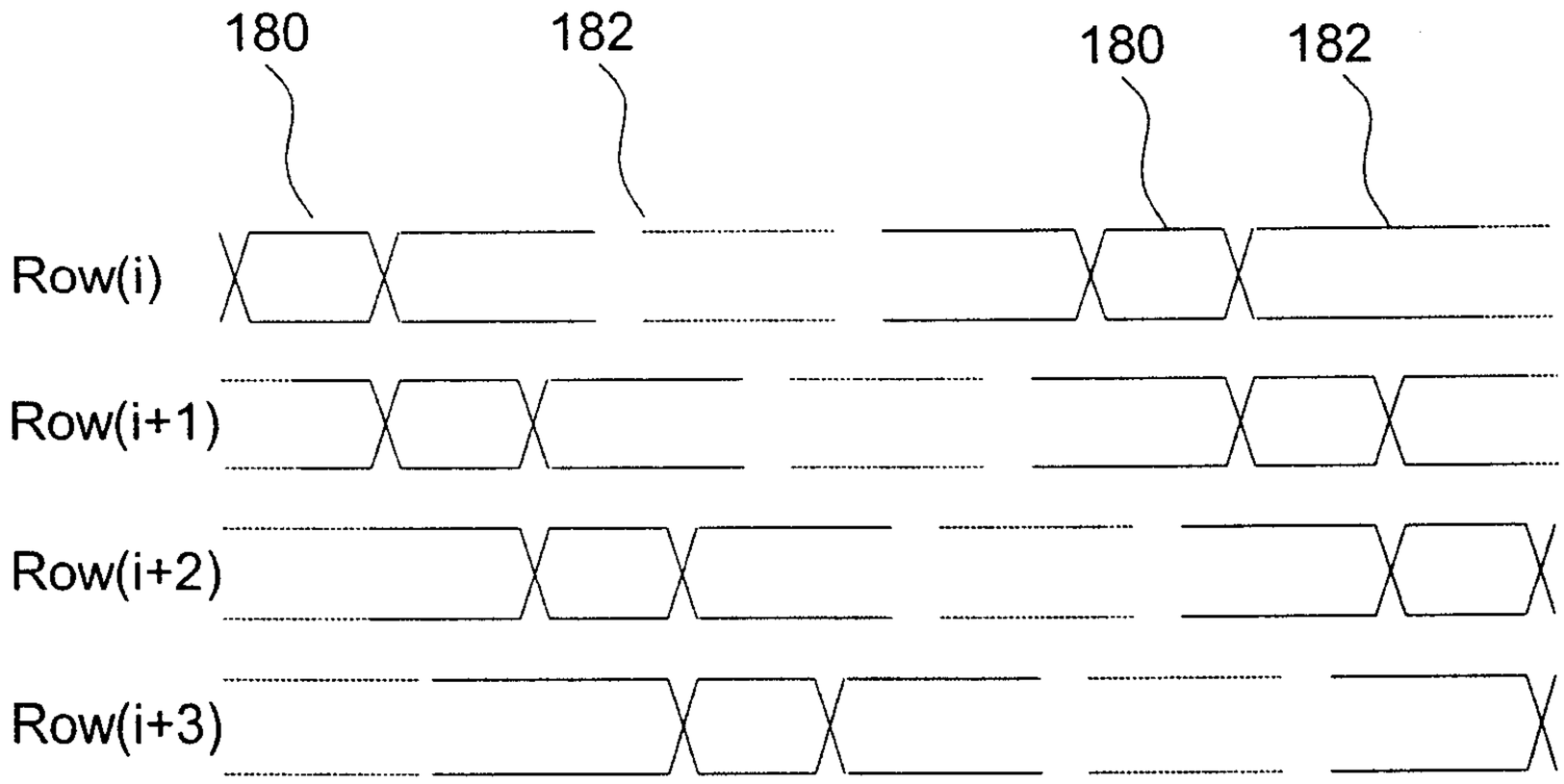
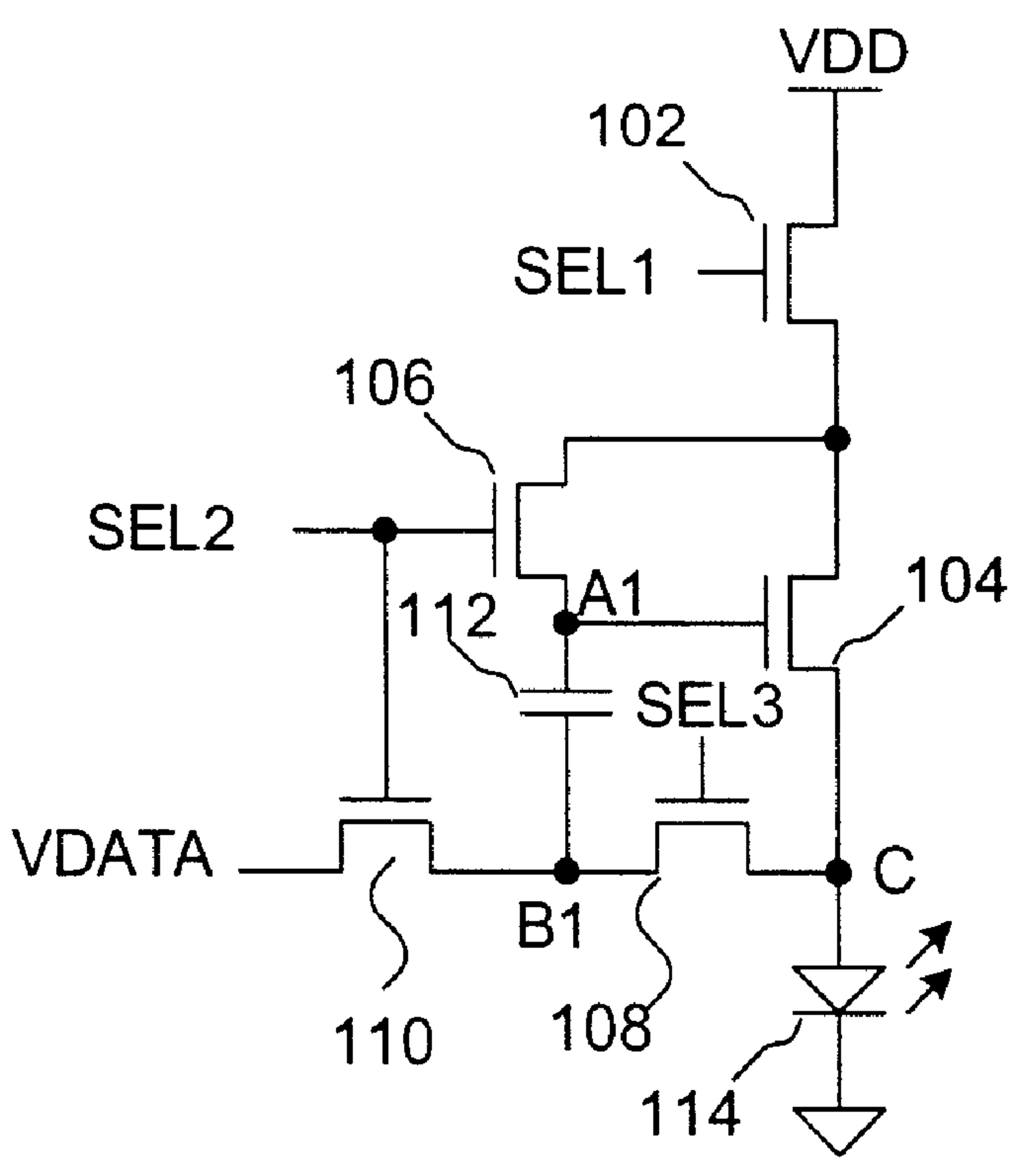


FIG. 11


VDD
102
SEL1
106
SEL2
112
A1
104
SEL3
VDATA
C
B1
110
108
114