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(54) **Title:** ARRAY TESTING METHOD USING ELECTRIC BIAS STRESS FOR TFT ARRAY

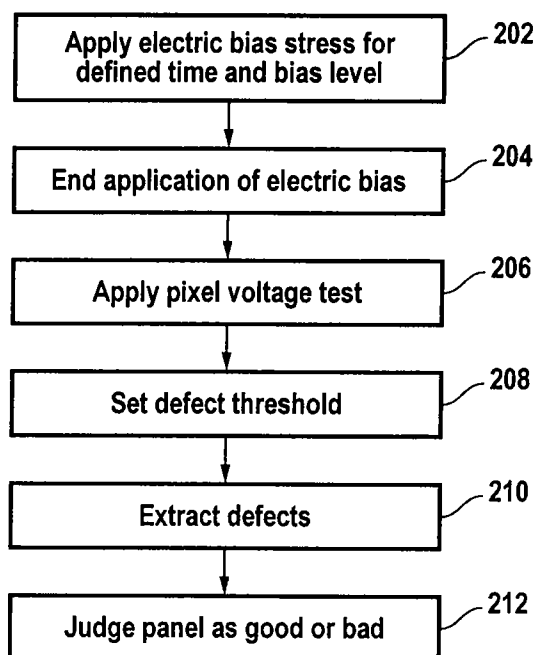


FIG. 10

(57) **Abstract:** A method of detecting thin film transistor (TFT) defects in a TFT-liquid crystal display (LCD) panel (10), includes, in part, applying a stress bias to the TFTs disposed on the panel (10); and detecting a change in electrical characteristics of the TFTs. The change in the electrical characteristics of the TFTs may be detected using a voltage imaging optical system or a electron beam. The panel (10) temperature may be varied while the bias stress is being applied. The change in the electric characteristics is optionally detected across an array of the TFTs.

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INTERNATIONAL SEARCH REPORT

International application No.

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A. CLASSIFICATION OF SUBJECT MATTER

IPC: **G01R 31/00**(2006.01);**G01R 31/26**(2006.01)

USPC: 324/765,770

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 324/760, 765, 769-770; 327/118

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US PGPub 2003/0137318 A1 (ENACHESCU et al) 24 July 2003 (24.06.2003), figures 3, 6A-B, paragraphs [0031-0035, 0052]	1-2, 4-10
X	US PGPub 2004/0032280 A1 (CLARK et al) 19 February 2004 (19.02.2004), figure 4, paragraphs [0030-0031, 0035-0036].	1, 3, 10
A	US PGPub 2004/0246015 A1 (CHUNG et al) 9 December 2004 (09.12.2004), paragraphs [0034-0039].	



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