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[Continued on next page]

(54) Title: FIELD EFFECT TRANSISTOR

FIG. 1A

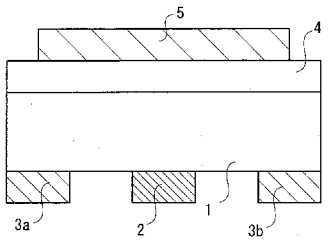


FIG. 1B

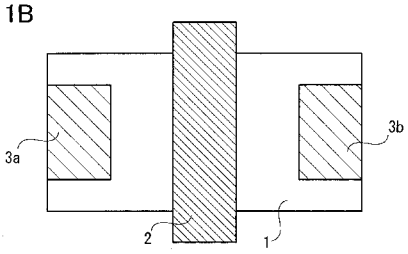
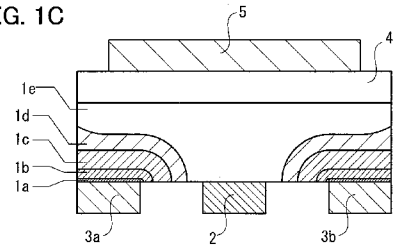


FIG. 1C



(57) Abstract: An object is to provide a structure with which the off-state current of a field effect transistor including a conductor-semiconductor junction can be reduced. A semiconductor layer is provided in contact with a first conductor electrode and a second conductor electrode which include a material with a work function that is at the same level as or lower than the electron affinity of the semiconductor layer. A third conductor electrode is formed using a material whose work function is higher than the electron affinity of the semiconductor layer to be in contact with a surface of the semiconductor layer opposite to a surface provided with a gate and to cross the semiconductor layer, so that a Schottky barrier junction is formed in the semiconductor layer. The carrier concentration of the portion including the Schottky barrier junction is extremely low; thus, the off-state current can be reduced.

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DESCRIPTION

FIELD EFFECT TRANSISTOR

TECHNICAL FIELD

[0001]

The present invention relates to a field effect transistor (FET) including a semiconductor.

BACKGROUND ART

[0002]

A field effect transistor (FET) is a device in which regions called a source and a drain are provided in a semiconductor, each of the regions is provided with an electrode, potentials are supplied to the electrodes, and an electric field is applied to the semiconductor with the use of an electrode called a gate through an insulating film or a Schottky barrier so that the state of the semiconductor is controlled, whereby current flowing between the source and the drain is controlled. As the semiconductor, Group IV elements (Group 14 elements) such as silicon and germanium, Group III-V compounds such as gallium arsenide, indium phosphide, and gallium nitride, Group II-VI compounds such as zinc sulfide and cadmium telluride, and the like can be given.

[0003]

In recent years, FETs in which an oxide such as zinc oxide or an indium gallium zinc oxide-based compound is used as a semiconductor have been reported (Patent Document 1 and Patent Document 2). In an FET including such an oxide semiconductor, relatively high mobility can be obtained, and such a material has a wide bandgap of greater than or equal to 3 electron volts; therefore, application of the FET including an oxide semiconductor to displays, power devices, and the like is discussed.

[0004]

The fact that the bandgap of such a material is greater than or equal to 3 electron volts means that the material transmits visible light, for example; thus, in the case where the material is used in a display, even an FET portion can transmit light and the aperture ratio is expected to be improved.

[0005]

Further, such a wide bandgap is common to silicon carbide, which is used in power devices; therefore, the oxide semiconductor is also expected to be applied to a power device.

[0006]

Furthermore, a wide bandgap means few thermally excited carriers. For example, silicon has a bandgap of 1.1 electron volts at room temperature and thus thermally excited carriers exist therein at approximately 10^{11} /cm^3, while in a semiconductor with a bandgap of 3.2 electron volts, thermally excited carriers exist at approximately 10^{-7} /cm^3 according to calculation.

[0007]

In the case of silicon, carriers generated by thermal excitation exist as described above even in silicon including no impurities, and thus the resistivity of the silicon cannot be higher than or equal to 10^5 Ωcm. In contrast, in the case of the semiconductor with a bandgap of 3.2 electron volts, a resistivity of higher than or equal to 10^{20} Ωcm can be obtained in theory. When an FET is manufactured using such a semiconductor and its high resistivity in an off state (a state where the potential of a gate is the same as the potential of a source) is utilized, it is expected that electric charge can be retained semipermanently.

[0008]

Meanwhile, there are few reports on an oxide semiconductor which includes zinc or indium in particular and has p-type conductivity. Accordingly, an FET of an oxide semiconductor using a PN junction like an FET of silicon has not been reported, and a conductor-semiconductor junction as disclosed in Patent Document 1 and Patent Document 2, where a conductor electrode is in contact with an n-type oxide semiconductor, has been used for forming a terminal corresponding to a source or a drain.

[0009]

Note that in general academic books about semiconductors, the "conductor-semiconductor junction" is expressed as a "metal-semiconductor junction." In this case, metal means a conductor. For example, a semiconductor such as silicon (a

degenerated semiconductor in particular) which is doped at a high concentration and whose resistivity is significantly lowered, metal nitrides such as titanium nitride and tungsten nitride, metal oxides such as indium tin oxide and aluminum zinc oxide, and the like are also regarded as metal in "metal-semiconductor junctions." However, in such a case, the term "metal" might cause misunderstanding; therefore, the term "conductor-semiconductor junction" is used instead of the term "metal-semiconductor junction" in this specification.

[0010]

In an FET where terminals corresponding to a source and a drain are formed with the use of a conductor-semiconductor junction, when the carrier concentration of the semiconductor is high, current (off-state current) flows between the source electrode and the drain electrode even in an off state. Thus, the off-state current needs to be reduced by lowering the concentration of a donor or an acceptor in the semiconductor so that an i-type semiconductor is obtained. Note that in this specification, an i-type semiconductor is a semiconductor whose carrier concentration derived from a donor or an acceptor is lower than or equal to 10^{12} /cm^3. However, it is apparent from the following that such an attempt does not work when the channel length of an FET is short and a semiconductor layer is thick.

[0011]

In a conductor-semiconductor junction, in general, an ohmic junction or a Schottky barrier junction is formed depending on the relation between a work function of a conductor and an electron affinity (or a Fermi level) of a semiconductor. For example, if an ideal conductor-semiconductor junction (i.e., a junction where a compound, a trap level, or the like does not exist at the interface) is formed by making a conductor with a work function of 3.9 electron volts in contact with a semiconductor with an electron affinity of 4.3 electron volts, electrons flow from the conductor into a region which is in the semiconductor and has a certain width.

[0012]

In that case, a region closer to a junction interface between the conductor and the semiconductor has a higher electron concentration, and the electron concentrations are 10^{20} /cm^3 at several nanometers from the interface of the conductor-semiconductor junction, 10^{18} /cm^3 at several tens of nanometers from the interface, 10^{16} /cm^3 at several

hundreds of nanometers from the interface, and 10^{14} /cm^3 even at several micrometers from the interface according to rough calculation. That is, even when the semiconductor itself is an i-type semiconductor, contact with a conductor produces a region with a high carrier concentration. As a result of formation of such a region including many carriers in the vicinity of the interface of the conductor-semiconductor junction, the conductor-semiconductor junction becomes an ohmic junction.

[0013]

In contrast, for example, if an ideal conductor-semiconductor junction is formed by making a conductor with a work function of 4.9 electron volts in contact with a semiconductor with an electron affinity of 4.3 electron volts, electrons existing in a region which is in the semiconductor and has a certain width move to the conductor. In a region which the electrons have left, the electron concentration is, as is obvious, extremely low. The width of the region of the semiconductor to which electrons move depends on the electron concentration of the semiconductor; for example, when an original electron concentration of the semiconductor is 10^{18} /cm^3, the width is several tens of nanometers.

[0014]

The electron concentration in this portion becomes significantly low; accordingly, a barrier is formed at a junction interface between the conductor and the semiconductor in a band diagram. A conductor-semiconductor junction including such a barrier is referred to as a Schottky barrier junction. Electrons easily flow from the semiconductor to the conductor, whereas electrons are less likely to flow from the conductor to the semiconductor owing to the barrier. Therefore, rectification action is observed in the Schottky barrier junction.

[0015]

A similar phenomenon occurs even when a conductor is not in direct contact with a semiconductor. For example, even in the case where an insulating film is provided between a semiconductor and a conductor, the electron concentration of the semiconductor is influenced by the conductor. Needless to say, the degree of the influence of the conductor depends on the thickness or the dielectric constant of the insulating film. When the thickness of the insulating film is increased or when the dielectric constant thereof is lowered, the influence of the conductor is reduced.

[0016]

In an FET, since it is preferable that a junction between a source electrode and a semiconductor or between a drain electrode and the semiconductor be formed so that current flows easily, a material of the source electrode or the drain electrode is selected so that an ohmic junction is formed. For example, titanium and titanium nitride are given. When a junction between an electrode and a semiconductor is an ohmic junction, there are advantages of stable characteristics of an FET to be obtained and of high percentage of non-defective products.

[0017]

As a material of a gate, a material having action that eliminates electrons from a semiconductor is selected. For example, tungsten and platinum are given. When such a material is used and a ratio L/T, where L is the size of a semiconductor (typically, the distance between a source electrode and a drain electrode) and T is the sum of the effective thicknesses of a gate insulating film and the semiconductor, is greater than or equal to 10, an FET having an extremely small off-state current of less than or equal to 1×10^{-18} A can be manufactured. Here, T is calculated by the following formula: T = (the thickness of a gate insulating film × the dielectric constant of a semiconductor / the dielectric constant of the gate insulating film) + the thickness of the semiconductor.

[0018]

The ratio L/T is required to be low because of a need to increase current in an on state (on-state current), a limit of a technique of forming a thin film, miniaturization, or the like. When a semiconductor layer is made thicker, for example, the cross-sectional area thereof is increased; thus, larger current can flow. Further, when the thickness of a semiconductor layer or a gate insulating layer is reduced to the limit of mass production and a channel (the distance between the source electrode and the drain electrode) is shortened, L becomes small relative to T. In addition, for an application to a power device, the thickness of the gate insulating film needs to be increased in order to increase withstand voltage.

[0019]

With such a structure, however, it is impossible to keep the off-state current low when the ratio L/T is less than or equal to 4. A similar phenomenon can be

observed when L is less than 100 nm or when T is greater than or equal to 1 μm. A cause of that phenomenon is described with reference to FIGS. 7A and 7B. FIG. 7A illustrates a typical structure of an FET including a conductor-semiconductor junction. Specifically, a source electrode 13a and a drain electrode 13b are provided on one surface of a semiconductor layer 11. Further, a gate insulating film 14 and a gate 15 are provided over an opposite surface of the semiconductor layer 11.

[0020]

As the source electrode 13a and the drain electrode 13b, a conductor is selected so that a junction between the source electrode 13a and the semiconductor layer 11 and a junction between the drain electrode 13b and the semiconductor layer 11 are ohmic junctions. By using a material whose work function is higher than the electron affinity of the semiconductor for the gate 15, electrons flowing from the source electrode 13a or the drain electrode 13b are eliminated.

[0021]

In order to simplify the explanation, it is assumed that a force of the source electrode 13a or the drain electrode 13b for injecting electrons into the semiconductor layer 11 is equal to a force of the gate 15 for eliminating electrons from the semiconductor layer 11. The forces are thought to depend on respective distances from the source electrode 13a (or the drain electrode 13b) and the gate 15 to a point.

[0022]

In a portion of the semiconductor layer 11 where the distances from the source electrode 13a (or the drain electrode 13b) and the gate 15 are equal, the opposing forces are balanced; therefore, it can be thought that the electron concentration therein is equal to an original value. When the distance from the source electrode 13a is shorter than the distance from the gate 15 in a position, the force of the source electrode 13a is stronger than that of the gate 15; thus, the electron concentration is higher at the position. In contrast, when the former distance is longer than the latter distance in another position, the force of the gate 15 is stronger than that of the source electrode 13a; thus, the electron concentration is lower at the position.

[0023]

Here, it should be noted that the distance in this case means not a spatial distance but an electromagnetic distance; therefore, the comparison needs to be made on

the basis of a value obtained by multiplying a spatial distance by a dielectric constant.

[0024]

FIG. 7B illustrates conceptual isoconcentration lines of the electron concentration in the semiconductor layer 11 of the FET in FIG. 7A, which is based on the above premise. In order to simplify the explanation, the dielectric constant of the gate insulating film 14 is assumed to be equal to the dielectric constant of the semiconductor layer 11. In addition, the potentials of the source electrode 13a and the drain electrode 13b are equal to the potential of the gate 15.

[0025]

There are regions 1a where the electron concentration is high in the vicinity of an interface between the semiconductor layer 11 and the source electrode 13a and the drain electrode 13b. Further, regions 1b where the electron concentration is lower than the electron concentration in the regions 1a by approximately one order of magnitude, regions 1c where the electron concentration is lower than that in the regions 1b by approximately one order of magnitude, a region 1d where the electron concentration is lower than that in the regions 1c by approximately one order of magnitude, and a region 1e where the electron concentration is lower than that in the region 1d exist outside the regions 1a in this order.

[0026]

It should be noted that the region 1d is not divided on a side opposite to the gate 15 in the semiconductor layer 11. This is because the force of the gate 15 does not reach that region and electrons are injected by the forces of the source electrode 13a and the drain electrode 13b.

[0027]

In the drawing, the ratio L/T is a little less than 2. Assuming that the distance between the source electrode 13a and the drain electrode 13b is 120 nm, the thickness of the semiconductor layer 11 is 50 nm; thus, the electron concentration on the isoconcentration line between the region 1a and the region 1b is approximately 10^{20} /cm^3, and the electron concentration on the isoconcentration line between the region 1d and the region 1e is approximately 10^{17} /cm^3.

[0028]

Assuming that the distance between the source electrode 13a and the drain

electrode 13b is 1.2 μm, the thickness of the semiconductor layer 11 is 0.5 μm; thus, the electron concentration on the isoconcentration line between the region 1a and the region 1b is approximately 10^{18} /cm^3, and the electron concentration on the isoconcentration line between the region 1d and the region 1e is approximately 10^{15} /cm^3.

[0029]

Although an electron concentration of 10^{15} /cm^3 seems low enough, the value is approximately 1 kΩcm in resistivity. As illustrated in the drawing, in one third or more part of the semiconductor layer, the electron concentration is higher than or equal to 10^{15} /cm^3. Accordingly, in an FET in which the channel length and the channel width are equal, the resistance is approximately 10 MΩ and the off-state current is as large as 0.1 μA in the case where the potential difference between the source electrode 13a and the drain electrode 13b is 1 V.

[0030]

In short, in order to reduce the off-state current, the electron concentration on the side opposite to the gate needs to be prevented from being such an unignorable value. For that purpose, a method in which the thickness of the semiconductor layer 11 is reduced can be considered. In other words, a region which is not influenced by the gate 15 may be reduced. In the case of the FET in the drawing, calculation results indicate that the off-state current can be reduced to one hundred-thousandth when the thickness of the semiconductor layer 11 is reduced by half, for example.

[0031]

However, in an extremely small device in which the distance between the source electrode 13a and the drain electrode 13b is 24 nm, for example, the thickness of the semiconductor layer 11 needs to be less than or equal to 2.5 nm and thus it is technically difficult to uniformly form the semiconductor layer 11 with such a small thickness. Moreover, reduction in the thickness of the semiconductor layer 11 leads to smaller on-state current.

[0032]

A second method is to make the gate insulating film 14 thinner. When the thickness of the gate insulating film 14 in the drawing is reduced to one sixth or less, the influence of the gate 15 can reach the back surface of the semiconductor layer 11.

However, as in the above example, when the distance between the source electrode 13a and the drain electrode 13b is 24 nm, the gate insulating film 14 needs to have a thickness of less than or equal to 0.8 nm.

[0033]

A gate insulating film is formed over an oxide semiconductor by a sputtering method or a CVD method. It is difficult to form, by these methods, an insulating film having high quality and a uniform thickness like an insulating film of silicon formed by a thermal oxidation method; therefore, these methods are not realistic.

[0034]

The above consideration is based on the premise that the force of the source electrode 13a or the drain electrode 13b for injecting electrons into the semiconductor layer 11 is equal to the force of the gate 15 for eliminating electrons from the semiconductor layer 11. When the former force is stronger than the latter force, more electrons are injected from the source electrode 13a or the drain electrode 13b into the semiconductor layer 11.

[Reference]

[Patent Document]

[0035]

[Patent Document 1] United States Published Patent Application No. 2005/0199879

[Patent Document 2] United States Published Patent Application No. 2007/0194379

DISCLOSURE OF INVENTION

[0036]

An object of the present invention is to provide at least one of the following: a novel semiconductor device including a conductor-semiconductor junction; a novel field effect transistor including a conductor-semiconductor junction; a method for manufacturing the novel semiconductor device; and a method for manufacturing the novel field effect transistor. Another object of the present invention is to provide a method which is effective to the above-described problem in that the off-state current of an FET including a conductor-semiconductor junction is increased by changing the size of the FET. In particular, it is an object to provide a novel structure with which the off-state current of an FET, where the ratio L/T is less than or equal to 2, L is less than

100 nm, or T is greater than or equal to 1 μm, is small enough for practical use. According to the present invention, at least one of the above objects is achieved.

[0037]

Before the present invention is described, terms used in this specification will be briefly explained. First, as for a source and a drain of a transistor in this specification, a terminal supplied with a higher potential is referred to as a drain and the other terminal is referred to as a source in an n-channel FET, and a terminal supplied with a lower potential is referred to as a drain and the other terminal is referred to as a source in a p-channel FET. In the case where the same potential is supplied to the two terminals, one of them is referred to as a source and the other is referred to as a drain. In addition, the terms "first conductor electrode" and "second conductor electrode" are used instead of the terms "source electrode" and "drain electrode" in some cases. In that case, the names are not changed depending on the level of a potential.

[0038]

An embodiment of the present invention is an FET including a semiconductor layer, first and second conductor electrodes provided in contact with one surface of the semiconductor layer, and a gate provided over an opposite surface of the semiconductor layer. The FET further includes a third conductor electrode provided between the first conductor electrode and the second conductor electrode so as to cross the semiconductor layer. Another embodiment of the present invention is an FET including a semiconductor layer, first and second conductor electrodes provided in contact with one surface of the semiconductor layer, and a gate provided over the one surface of the semiconductor layer. The FET further includes a third conductor electrode provided on an opposite surface of the semiconductor layer so as to cross the semiconductor layer. In the above structure, the third conductor electrode is preferably formed so as to hinder current flow from the first conductor electrode to the second conductor electrode. Alternatively, the third conductor electrode is preferably formed between the first conductor electrode and the second conductor electrode. Further alternatively, the third conductor electrode is preferably provided so that a portion where the third conductor electrode is in contact with the semiconductor layer is positioned between a portion where the first conductor electrode is in contact with the semiconductor layer and a portion where the second conductor electrode is in contact with the semiconductor

layer.

[0039]

In the above structure, it is preferable that the third conductor electrode be in contact with only one of the first and second conductor electrodes or be kept at the same potential as only one of the first and second conductor electrodes.

[0040]

In addition to the above structure, a fourth conductor electrode may be provided on the surface where the third conductor electrode is provided, so as to cross the semiconductor layer. The fourth conductor electrode is preferably provided to be apart from the third conductor electrode. In that case, it is preferable that the third conductor electrode be in contact with one of the first and second conductor electrodes or be kept at the same potential as one of the first and second conductor electrodes, and that the fourth conductor electrode be in contact with the other of the first and second conductor electrodes or be kept at the same potential as the other of the first and second conductor electrodes.

[0041]

Further, the semiconductor layer may be doped to have a first doped region and a second doped region which include a donor or an acceptor at a high concentration, and the first doped region and the second doped region may be in contact with the first conductor electrode and the second conductor electrode, respectively. The concentration of a donor or an acceptor in the first and second doped regions may be set to higher than or equal to 1×10^{18} /cm^3 and lower than 1×10^{21} /cm^3, preferably higher than or equal to 1×10^{19} /cm^3 and lower than 1×10^{20} /cm^3.

[0042]

In the above structure, it is preferable that the portions of the first and second conductor electrodes, which are in contact with the semiconductor layer, have a work function of lower than the sum of the electron affinity of the semiconductor layer and 0.3 electron volts (i.e., the electron affinity + 0.3 electron volts). Alternatively, it is preferable that ohmic junctions be formed between the first and second conductor electrodes and the semiconductor layer.

[0043]

Further, it is preferable that one or both of portions of the third and fourth conductor electrodes, which are in contact with the semiconductor layer, have a work function of higher than the sum of the electron affinity of the semiconductor layer and 0.6 electron volts (i.e., the electron affinity + 0.6 electron volts). Alternatively, it is preferable that a Schottky barrier junction be formed between one or both of the third and fourth conductor electrodes and the semiconductor layer. In addition, the work function of the gate is preferably higher than the electron affinity of the semiconductor layer.

[0044]

Furthermore, a gate insulating film may be provided between the semiconductor layer and the gate. Alternatively, a Schottky barrier junction may be formed between the semiconductor layer and the gate. In addition, it is not necessary that the first conductor electrode and the second conductor electrode are formed using the same material.

[0045]

Note that the kind of the semiconductor layer is not limited to an oxide, and a Group II-VI compound such as a sulfide may be used. In addition, the bandgap of the semiconductor is preferably greater than or equal to 2 electron volts and less than 4 electron volts, further preferably greater than or equal to 2.9 electron volts and less than 3.5 electron volts.

[0046]

An FET of the present invention will be described below with reference to drawings. The terms used herein are basically the same as the terms used in the above description. Therefore, conditions for the components denoted by the terms used in the above description may be applied to components denoted by the same terms. For example, in the case where a first conductor electrode is described below, the work function thereof may be in the range given in the above description.

[0047]

FIGS. 1A to 1C illustrate an example of the FET of the present invention. The FET in FIG. 1A includes a semiconductor layer 1; a first conductor electrode 3a, a second conductor electrode 3b, and a third conductor electrode 2 on one surface of the semiconductor layer 1; and a gate 5 over an opposite surface of the semiconductor layer

1 with a gate insulating film 4 provided therebetween.

[0048]

FIG. 1B schematically illustrates the FET in FIG. 1A seen from the below. The FET in FIG. 1A may be formed over a substrate. The substrate is not illustrated here in order to facilitate understanding. As illustrated in FIG. 1B, the third conductor electrode 2 is provided so as to cross the semiconductor layer 1.

[0049]

The third conductor electrode 2 is not in contact with the first conductor electrode 3a and the second conductor electrode 3b in the FET, but may be configured to have the same potential as one of the first conductor electrode 3a and the second conductor electrode 3b through a wiring or the like. With such a structure, carriers (electrons in the case of an n-channel FET) flowing into the third conductor electrode 2 while in use for some reasons can be easily eliminated.

[0050]

FIG. 2A illustrates another example of the FET of the present invention. The FET in FIG. 2A includes the semiconductor layer 1; the first conductor electrode 3a and the second conductor electrode 3b on one surface of the semiconductor layer 1; and the gate 5 over the one surface of the semiconductor layer 1 with the gate insulating film 4 provided therebetween. Further, the third conductor electrode 2 is provided on an opposite surface of the semiconductor layer.

[0051]

A first doped region 6a and a second doped region 6b in which the donor concentration is high as a result of doping are provided in the semiconductor layer 1 so as to be in contact with the first conductor electrode 3a and the second conductor electrode 3b, respectively. The first doped region 6a and the second doped region 6b are preferably formed in a self-aligned manner with the use of the gate 5 as a mask. The first doped region 6a and the second doped region 6b are formed to be apart from each other.

[0052]

FIG. 2B illustrates another example of the FET of the present invention. The FET in FIG. 2B includes the semiconductor layer 1; and the first conductor electrode 3a, the second conductor electrode 3b, and the third conductor electrode 2 on one surface of

the semiconductor layer 1. Further, the gate 5 is provided over an opposite surface of the semiconductor layer 1 with the gate insulating film 4 provided therebetween. The semiconductor layer 1 has the first doped region 6a and the second doped region 6b. The first doped region 6a and the second doped region 6b are formed to be apart from each other and in contact with the first conductor electrode 3a and the second conductor electrode 3b, respectively.

[0053]

FIG. 2C illustrates another example of the FET of the present invention. The FET in FIG. 2C includes the semiconductor layer 1; the first conductor electrode 3a, the second conductor electrode 3b, and the third conductor electrode 2 on one surface of the semiconductor layer 1; and the gate 5 over an opposite surface of the semiconductor layer 1 with the gate insulating film 4 provided therebetween. Here, the third conductor electrode 2 is formed so as to be in contact with the first conductor electrode 3a. The third conductor electrode 2 may be formed so as to be in contact with the second conductor electrode 3b instead of the first conductor electrode 3a.

[0054]

FIG. 2D illustrates another example of the FET of the present invention. The FET in FIG. 2D includes the semiconductor layer 1; the first conductor electrode 3a, the second conductor electrode 3b, a third conductor electrode 2a, and a fourth conductor electrode 2b on one surface of the semiconductor layer 1; and the gate 5 over an opposite surface of the semiconductor layer 1 with the gate insulating film 4 provided therebetween. Here, the third conductor electrode 2a and the fourth conductor electrode 2b are formed so as to be in contact with the first conductor electrode 3a and the second conductor electrode 3b, respectively.

[0055]

FIG. 3A illustrates another example of the FET of the present invention. The FET in FIG. 3A includes the semiconductor layer 1; the first conductor electrode 3a and the second conductor electrode 3b on one surface of the semiconductor layer 1; and the gate 5 over the one surface of the semiconductor layer 1 with the gate insulating film 4 provided therebetween. Further, the third conductor electrode 2 is provided on an opposite surface of the semiconductor layer.

[0056]

The first doped region 6a and the second doped region 6b are formed to be apart from each other in the semiconductor layer 1, and are in contact with the first conductor electrode 3a and the second conductor electrode 3b, respectively. The third conductor electrode 2 is formed so as to be in contact with the first doped region 6a. The third conductor electrode 2 may be formed so as to be in contact with the second doped region 6b instead of the first doped region 6a.

[0057]

FIG. 3B illustrates another example of the FET of the present invention. The FET in FIG. 3B includes the semiconductor layer 1; and the first conductor electrode 3a, the second conductor electrode 3b, and the third conductor electrode 2 on one surface of the semiconductor layer 1. Further, the gate 5 is provided over an opposite surface of the semiconductor layer with the gate insulating film 4 provided therebetween.

[0058]

The first doped region 6a and the second doped region 6b are formed to be apart from each other in the semiconductor layer 1, and are in contact with the first conductor electrode 3a and the second conductor electrode 3b, respectively. The third conductor electrode 2 is formed so as to be in contact with the first doped region 6a and the first conductor electrode 3a. The third conductor electrode 2 may be formed so as to be in contact with the second doped region 6b and the second conductor electrode 3b instead.

[0059]

FIG. 3C illustrates another example of the FET of the present invention. The FET in FIG. 3C includes the semiconductor layer 1; the first conductor electrode 3a and the second conductor electrode 3b on one surface of the semiconductor layer 1; and the gate 5 over the one surface of the semiconductor layer 1 with the gate insulating film 4 provided therebetween. Further, the third conductor electrode 2a and the fourth conductor electrode 2b are provided on an opposite surface of the semiconductor layer.

[0060]

The first doped region 6a and the second doped region 6b are formed to be apart from each other in the semiconductor layer 1, and are in contact with the first conductor electrode 3a and the second conductor electrode 3b, respectively. The third conductor electrode 2a is formed so as to be in contact with the first doped region 6a,

and the fourth conductor electrode 2b is formed so as to be in contact with the second doped region 6b.

[0061]

FIG. 3D illustrates another example of the FET of the present invention. The FET in FIG. 3D includes the semiconductor layer 1; and the first conductor electrode 3a, the second conductor electrode 3b, the third conductor electrode 2a, and the fourth conductor electrode 2b on one surface of the semiconductor layer 1. Further, the gate 5 is provided over an opposite surface of the semiconductor layer with the gate insulating film 4 provided therebetween.

[0062]

The first doped region 6a and the second doped region 6b are formed to be apart from each other in the semiconductor layer 1, and are in contact with the first conductor electrode 3a and the second conductor electrode 3b, respectively. The third conductor electrode 2a is formed so as to be in contact with the first doped region 6a and the first conductor electrode 3a, and the fourth conductor electrode 2b is formed so as to be in contact with the second doped region 6b and the second conductor electrode 3b.

[0063]

By employing any of the above structures, at least one of the above objects can be achieved. An effect of an embodiment of the present invention will be described with reference to FIGS. 1A to 1C. FIG. 1A illustrates a cross section of the FET which is an example of the present invention. Specifically, in the FET including the semiconductor layer 1, the first and second conductor electrodes 3a and 3b provided in contact with one surface of the semiconductor layer 1, and the gate 5 provided over the opposite surface of the semiconductor layer with the gate insulating film 4 provided therebetween, the third conductor electrode 2 is provided between the first conductor electrode 3a and the second conductor electrode 3b so as to cross the semiconductor layer 1.

[0064]

The reason why the off-state current is small in an FET having such a structure will be described with reference to FIG. 1C. In FIG. 1C, the gate 5, the first conductor electrode 3a, the second conductor electrode 3b, and the third conductor electrode 2 are

kept at the same potential. Here, for simplicity, conditions of the gate 5, the first conductor electrode 3a, the second conductor electrode 3b, the semiconductor layer 1, and the gate insulating film 4 are the same as those used in the description of FIGS. 7A and 7B. The work function of the third conductor electrode 2 is the same as the work function of a material used for the gate 5.

[0065]

As in the case illustrated in FIG. 7B, electrons are injected into the semiconductor layer 1 from the first conductor electrode 3a and the second conductor electrode 3b; accordingly, regions with an extremely high electron concentration are formed in the vicinity of the first conductor electrode 3a and the second conductor electrode 3b, and a region located more distant from the first conductor electrode 3a or the second conductor electrode 3b has a lower electron concentration. In addition, electrons in the vicinity of the gate insulating film 4 are eliminated by action between the gate 5 and the semiconductor layer 1, and the electron concentration in the vicinity of the gate insulating film 4 is lowered.

[0066]

However, unlike the case illustrated in FIG. 7B, the electron concentration in the vicinity of the third conductor electrode 2 is also extremely low. This is because a Schottky barrier junction is formed between the third conductor electrode 2 and the semiconductor layer 1. As a result, a region with a relatively high electron concentration is divided in a central portion of the FET, which is different from the case of FIG. 7B. Thus, the off-state current can be significantly reduced as compared to the FET illustrated in FIGS. 7A and 7B.

[0067]

The above effect is remarkable when the force of the third conductor electrode 2 for absorbing electrons from the semiconductor layer 1 is stronger than the force of the first conductor electrode 3a or the second conductor electrode 3b for injecting electrons into the semiconductor layer 1. The strength of the forces depends on the work function or the electron affinity. Specifically, it is preferable that the work function of the third conductor electrode 2 be higher than the work function of the first conductor electrode 3a or the second conductor electrode 3b by 0.3 electron volts or more.

[0068]

Alternatively, it is preferable that the work function of the first conductor electrode 3a or the second conductor electrode 3b be lower than the sum of the electron affinity of the semiconductor layer 1 and 0.3 electron volts (i.e., the electron affinity + 0.3 electron volts) or that ohmic junctions be formed between the first and second conductor electrodes and the semiconductor layer.

[0069]

Further alternatively, it is preferable that the work function of the third conductor electrode 2 be higher than the sum of the electron affinity of the semiconductor layer and 0.6 electron volts (i.e., the electron affinity + 0.6 electron volts) or that a Schottky barrier junction be formed between the third conductor electrode 2 and the semiconductor layer 1. In addition, the work function of the gate is preferably higher than the electron affinity of the semiconductor layer.

[0070]

Since a Schottky barrier junction is formed between the third conductor electrode 2 and the semiconductor layer 1, it is relatively easy for electrons to move from the semiconductor layer 1 to the third conductor electrode 2 but difficult to move inversely. In that case, electrons are accumulated in the third conductor electrode 2 and the action of the third conductor electrode 2 that eliminates electrons is enhanced; accordingly, the operation of the FET becomes unstable.

[0071]

In order to avoid this phenomenon, the third conductor electrode 2 may be in contact with one of the first conductor electrode 3a and the second conductor electrode 3b through a wiring or the like or may be set at the same potential as one of the first conductor electrode 3a and the second conductor electrode 3b.

[0072]

It is interesting that even in the case where the thickness of the semiconductor layer is increased in the FET illustrated in FIG. 1A, the distribution pattern of the electron concentration is basically the same as that illustrated in FIG. 1C.

[0073]

In order to simplify the explanation, it is assumed that the force of the third

conductor electrode 2 for eliminating electrons from the semiconductor layer 1 is equal to the force of the first conductor electrode 3a or the second conductor electrode 3b for injecting electrons into the semiconductor layer 1. In that case, as described with reference to FIGS. 7A and 7B, the strength of each of the forces depends on the distance from a point.

[0074]

Here, a perpendicular line drawn from the third conductor electrode 2 to the gate 5 is assumed. The distance from any point on the line to the third conductor electrode 2 is shorter than that to the first conductor electrode 3a or the second conductor electrode 3b. Therefore, the influence of the third conductor electrode 2 is larger than that of the first conductor electrode 3a and the second conductor electrode 3b; as a result, the force for eliminating electrons is stronger than the force for injecting electrons. Consequently, the electron concentration becomes lower than an original electron concentration.

[0075]

That is to say, the present invention is also suitable for a device in which the semiconductor layer 1 is stacked to be thick and larger current is generated. Although the case where the semiconductor layer 1 is made thick is considered above, a similar effect can also be observed in the present invention by increasing the thickness of the gate insulating film 4. In that case, the withstand voltage of the gate of the FET can be increased.

[0076]

Here, when only the gate is kept at a positive potential for example, a region with a high electron concentration is formed in accordance with the potential in the vicinity of the gate insulating film 4 in the semiconductor layer 1 and is connected to a region with a high electron concentration (i.e., a region with low resistance) in the vicinity of the first conductor electrode 3a and the second conductor electrode 3b; thus, the FET is turned on.

[0077]

Further, when the potential of the gate 5 is increased, the electron concentration of the semiconductor layer in the vicinity of the gate insulating film 4 is further increased. In addition, a region with a high electron concentration is formed also in a

portion distant from the gate insulating film 4 and is connected to the region with a high electron concentration in the vicinity of the first conductor electrode 3a and the second conductor electrode 3b, so that the resistance of the FET is further lowered and larger current flows. However, if the semiconductor layer 1 is thin, the amount of flowing current is saturated at a certain stage even when the potential of the gate 5 is increased.

[0078]

In contrast, when the semiconductor layer 1 is thick, a region with a high electron concentration can be formed in a region that is more distant from the gate insulating film as well by further increasing the potential of the gate 5; accordingly, larger current can be obtained. When the thickness of a semiconductor layer is increased in a conventional FET, the off-state current is increased owing to the reason described above; according to the present invention, the off-state current can be sufficiently low even when the thickness of a semiconductor layer is increased.

[0079]

In order to obtain sufficiently low off-state current in accordance with the present invention, the carrier concentration derived from a donor or an acceptor is preferably lower than or equal to 10^{12} /cm^3. This point should be noted particularly when the thickness of the semiconductor layer is increased. Note that a concentration of a donor (or an acceptor) in this specification is a concentration of an element, a chemical group, or the like which could be a donor (or an acceptor) multiplied by an ionization rate thereof. For example, in the case where a donor element is included at 2 % and the ionization rate thereof is 0.005 %, the donor concentration is 1 ppm (= 0.02 × 0.00005).

[0080]

Although the force for eliminating electrons is stronger than the force for injecting electrons at any point on the perpendicular line drawn from the third conductor electrode 2 to the gate 5 as described above, the difference between the distance between the third conductor electrode 2 and the point and the distance between the first conductor electrode 3a or the second conductor electrode 3b and the point is smaller as the point is distant from the third conductor electrode 2.

[0081]

Therefore, there is a limit on reduction in the electron concentration and the electron concentration is close to an original electron concentration (i.e., an electron concentration derived from a donor or an acceptor) of the semiconductor layer 1. In such a case, the off-state current is determined by the original electron concentration of the semiconductor layer 1; therefore, if the value is not small enough, reduction in the off-state current is limited.

[0082]

As for the above description, in the case where the semiconductor layer 1 is an oxide semiconductor, oxygen vacancies and the hydrogen concentration therein are preferably reduced as much as possible. This is because an oxygen vacancy or hydrogen serves as a donor. Further, inclusion of hydrogen causes unstable operation of an FET. The hydrogen concentration is preferably lower than or equal to 10^{18} /cm^3.

[0083]

Although an FET including a conductor-semiconductor junction is discussed above, an embodiment of the present invention can also be applied to an FET in which the donor concentration has a gradient. Especially in an FET in which a PN junction cannot be used for insulation, a source and a drain can be separated in accordance with the present invention.

[0084]

In a junction between a conductor and a semiconductor, as described above, electrons are supplied from the conductor to the semiconductor or electrons are absorbed by the conductor from the semiconductor owing to a work function, an electron affinity, or the like. A similar phenomenon occurs in a junction between a region including a donor at a high concentration and a region including a donor at a low concentration.

[0085]

For example, it is assumed that the donor concentration in a first region is 1×10^{20} /cm^3 and the donor concentration in a second region is 1×10^{12} /cm^3. In that case, electrons in the first region exist in the vicinity of a lower end of the conduction band in a band diagram, while electrons in the second region exist in the vicinity of the center of the bandgap. That is, the electrons in the first region have a higher energy potential

than the electrons in the second region.

[0086]

If the first region and the second region are joined, the electrons in the first region flow into the second region owing to a difference in the energy potential. Assuming that the electron concentration in the first region is as relatively high as 1×10^{20} /cm^3, electrons are thought to be supplied in a manner similar to that in the case where the second region is in contact with a conductor; thus, the electrons flow into a considerably deep portion of the second region.

[0087]

The depth to which the electrons flow depends on a ratio between the level of the energy potential of an electron in the second region and the level of the energy potential of an electron in the first region, that is, a ratio between the electron concentration in the second region and the electron concentration in the first region. When the electron concentration in the second region is lower, electrons are injected from the first region into a deeper portion of the second region. Needless to say, electrons injected in such a manner cause increase in off-state current.

[0088]

In particular, when the case of silicon and the case of a semiconductor having a wider bandgap are compared, electrons are injected into a deeper portion of the second region in the latter case. This is because, in the latter case, the bandgap is wider and thus the difference in the energy potential between an electron in the first region and an electron in the second region is larger.

[0089]

In order to prevent such flow of carriers from a region including a donor at a high concentration, the third conductor electrode described above may be provided so that a Schottky barrier junction is formed and a region with an extremely low electron concentration as illustrated in FIG. 1C is formed in the semiconductor layer.

[0090]

Note that in the above FET, when the third conductor electrode 2 is kept at the same potential as the first conductor electrode 3a and, in addition, when a potential supplied to the first conductor electrode 3a is higher than a potential supplied to the second conductor electrode 3b, the area of such a Schottky barrier junction is reduced

and electrons flow from the second conductor electrode 3b into the semiconductor layer 1.

[0091]

For prevention of such a phenomenon, a circuit may be designed so that the potential of the first conductor electrode 3a is always higher than the potential of the second conductor electrode 3b, or a fourth conductor electrode may be provided in addition to the third conductor electrode so as to have the same potential as the second conductor electrode 3b as illustrated in FIG. 2D, FIG. 3C, or FIG. 3D.

[0092]

Such a structure is effective for a transistor in a circuit where current flows back and forth between a first conductor electrode and a second conductor electrode, such as a memory cell of a dynamic random access memory (DRAM) or the like, or for a switching transistor in an active matrix display device.

[0093]

The work function of a conductor is discussed in the above description. The work function of a conductor may be a value determined by an interface with a semiconductor in a simplest assumption; however, a complex physical property such as generation of a compound of the semiconductor and the conductor due to chemical reaction or a trap of electric charge or another element is often observed at the interface in reality.

[0094]

In the case where a first conductor layer with an extremely small thickness of less than or equal to several nanometers and a second conductor layer with a relatively large thickness are stacked over a semiconductor layer in this order, for example, the influence of the work function of the first conductor layer is considerably reduced. Therefore, in application of the present invention, the design may be performed so that the work function or the like of each material at a position that is 5 nm away from an interface with the semiconductor layer satisfies favorable conditions of the present invention.

[0095]

As a material of the third conductor electrode, a material which is chemically stable to the semiconductor layer, for example, noble metal such as platinum or

palladium is preferably used. When an oxide is used for the semiconductor layer, an oxide conductor may be used as the material of the third conductor electrode.

[0096]

The present invention is particularly effective for a semiconductor material in which substantially only one of an electron and a hole can be used as a carrier. In other words, a favorable result can be obtained in accordance with the present invention, for example, in the case where the mobility of one of the electron and the hole is higher than or equal to 1 cm^2/Vs whereas the mobility of the other is lower than or equal to 0.01 cm^2/Vs, the other does not exist as a carrier, or the effective mass of the other is 100 times or more as large as that of a free electron.

BRIEF DESCRIPTION OF DRAWINGS

[0097]

In the accompanying drawings:

FIGS. 1A to 1C illustrate an example of a field effect transistor of the present invention and a principle of operation thereof;

FIGS. 2A to 2D illustrate examples of a field effect transistor of the present invention;

FIGS. 3A to 3D illustrate examples of a field effect transistor of the present invention;

FIGS. 4A to 4F illustrate a manufacturing process of a field effect transistor of Embodiment 1;

FIGS. 5A to 5G illustrate a manufacturing process of a field effect transistor of Embodiment 2;

FIGS. 6A to 6E illustrate a manufacturing process of a field effect transistor of Embodiment 3; and

FIGS. 7A and 7B illustrate an example of a conventional field effect transistor and operation thereof.

BEST MODE FOR CARRYING OUT THE INVENTION

[0098]

Hereinafter, embodiments will be described with reference to the drawings.

Note that the embodiments can be implemented in various modes, and it is easily understood by those skilled in the art that modes and details can be changed in various ways without departing from the spirit and scope of the present invention. Therefore, the present invention is not construed as being limited to the description of the embodiments. Note that in structures described below, the same portions or portions having similar functions are denoted by the same reference numerals in different drawings, and detailed description thereof is not repeated.

[0099]

(Embodiment 1)

In this embodiment, a method for manufacturing the FET illustrated in FIG. 1A will be described with reference to FIGS. 4A to 4F. First, as illustrated in FIG. 4A, a third conductor electrode 102 is formed over a substrate 101. A variety of substrates can be given as examples of the substrate 101, but the substrate 101 needs to have such a property as to withstand the subsequent treatment. Further, it is preferable that a surface of the substrate 101 has an insulating property. Accordingly, the substrate 101 is preferably a single insulator; an insulator, conductor, or semiconductor whose surface is provided with an insulating layer; or the like.

[0100]

In the case of using an insulator for the substrate 101, various kinds of glasses, sapphire, quartz, ceramics, or the like can be used. In the case of using a conductor, aluminum, copper, stainless steel, silver, or the like can be used. In the case of using a semiconductor, silicon, germanium, silicon carbide, gallium nitride, or the like can be used. In this embodiment, barium borosilicate glass is used as the substrate 101.

[0101]

As a material of the third conductor electrode 102, metal with a high work function, such as platinum, gold, or tungsten, can be used. Alternatively, a compound with an electron affinity of higher than or equal to 5 electron volts, such as indium nitride, may be used. The third conductor electrode 102 may include a single material of any of the above-described materials or may have a multilayer structure where a portion in contact with a semiconductor layer provided later includes any of the above-described materials. In this embodiment, the third conductor electrode 102 is formed in such a manner that a 100-nm-thick platinum film is formed by a sputtering

method and then etched.

[0102]

Next, as illustrated in FIG. 4B, a conductor film 103 is formed. The conductor film 103 serves as first and second conductor electrodes later. Therefore, the conductor film 103 is formed using a material suitable for the purpose. For example, titanium, molybdenum, titanium nitride, and molybdenum nitride are given. The conductor film 103 may include a single material of any of the above-described materials or may have a multilayer structure where a portion in contact with the semiconductor layer provided later includes any of the above-described materials.

[0103]

Further, the conductor film 103 is formed to overlap with the third conductor electrode 102 and then patterned into a predetermined shape; therefore, it is preferable that the etching rate of a material included in the conductor film 103 be different from that of a material included in the third conductor electrode 102. In this embodiment, a 100-nm-thick titanium film is formed and then a surface thereof is nitrided so that titanium nitride is formed; this titanium nitride is used as the conductor film 103.

[0104]

Next, the conductor film 103 is etched, so that a first conductor electrode 103a and a second conductor electrode 103b are formed. Further, a first insulating film 104 is formed by a sputtering method (see FIG. 4C). As a material of the first insulating film 104, silicon oxide, aluminum oxide, aluminum nitride, or the like can be used. In this embodiment, 100-nm-thick silicon oxide formed by a sputtering method is used as the first insulating film 104.

[0105]

Next, the first insulating film 104 is etched by a chemical mechanical polishing method or the like, so that a surface of the substrate 101 is planarized. This etching is performed until the first conductor electrode 103a, the second conductor electrode 103b, and the third conductor electrode 102 are exposed as illustrated in FIG. 4D. As a result, a structure is obtained in which insulators 104a and 104b are embedded between the first conductor electrode 103a and the third conductor electrode 102 and between the second conductor electrode 103b and the third conductor electrode 102, respectively.

[0106]

After that, an oxide semiconductor layer including indium and zinc is formed and then patterned, so that a semiconductor layer 105 is obtained. Other than the above oxide semiconductor, a variety of oxide semiconductors can be used. In this embodiment, the semiconductor layer 105 is formed in the following manner: an indium zinc oxide film having a thickness of 200 nm is formed by a sputtering method using an oxide target including equal amounts of indium and zinc.

[0107]

Further, a second insulating film 106 is formed by a sputtering method (see FIG. 4E). The second insulating film 106 is used as a gate insulating film. As a material of the second insulating film 106, silicon oxide, aluminum oxide, aluminum nitride, hafnium oxide, lanthanum oxide, yttrium oxide, or the like can be used. In this embodiment, aluminum oxide having a thickness of 100 nm is formed by a sputtering method as the second insulating film 106.

[0108]

Appropriate heat treatment is preferably performed either after formation of the semiconductor layer 105 or after formation of the second insulating film 106 or at both of the timings. This heat treatment is for reducing the hydrogen concentration or oxygen vacancies in the semiconductor layer 105, and if possible, the heat treatment is preferably performed right after formation of the semiconductor layer 105.

[0109]

After that, a gate 107 is formed. The gate 107 is preferably formed so as to overlap with the third conductor electrode 102 and partly overlap with the first conductor electrode 103a and the second conductor electrode 103b as illustrated in FIG. 4F.

[0110]

A material of the gate 107 can be metal having a high work function such as platinum, gold, or tungsten. The gate 107 may include a single material of any of the above-described materials or may have a multilayer structure where a portion in contact with the second insulating film 106 includes any of the above-described materials. In this embodiment, a 100-nm-thick platinum film and a 100-nm-thick aluminum film are formed by a sputtering method and then etched, so that the gate 107 is formed. In this manner, the FET is manufactured.

[0111]

(Embodiment 2)

In this embodiment, a method for manufacturing the FET illustrated in FIG. 2D will be described with reference to FIGS. 5A to 5G. First, as illustrated in FIG. 5A, a third conductor electrode 102a and a fourth conductor electrode 102b are formed over the substrate 101. In this embodiment, barium borosilicate glass is used as the substrate 101. As a material of the third conductor electrode 102a and the fourth conductor electrode 102b, 100-nm-thick platinum formed by a sputtering method is used. The platinum is etched, so that the third conductor electrode 102a and the fourth conductor electrode 102b are formed.

[0112]

Next, as illustrated in FIG. 5B, the conductor film 103 is formed. In this embodiment, a 100-nm-thick titanium film is formed and then a surface thereof is nitrided so that titanium nitride is formed; this titanium nitride is used as the conductor film 103.

[0113]

Next, the conductor film 103 is etched by a chemical mechanical polishing method or the like, so that a surface of the substrate 101 is planarized. This etching is performed until the third conductor electrode 102a and the fourth conductor electrode 102b are exposed as illustrated in FIG. 5C. As a result, a structure is obtained in which a conductor film 103c is embedded between the third conductor electrode 102a and the fourth conductor electrode 102b.

[0114]

Then, as illustrated in FIG. 5D, the conductor film 103c is etched away, so that a space is formed between the third conductor electrode 102a and the fourth conductor electrode 102b. Further, as illustrated in FIG. 5E, the first insulating film 104 is formed by a sputtering method. In this embodiment, 100-nm-thick silicon oxide formed by a sputtering method is used as the first insulating film 104.

[0115]

Next, the first insulating film 104 is etched by a chemical mechanical polishing method or the like, so that the surface of the substrate 101 is planarized. This etching is performed until the first conductor electrode 103a, the second conductor electrode

103b, the third conductor electrode 102a, and the fourth conductor electrode 102b are exposed as illustrated in FIG. 5F. As a result, a structure is obtained in which the insulator 104a is embedded between the third conductor electrode 102a and the fourth conductor electrode 102b.

[0116]

After that, the semiconductor layer 105 is formed in the following manner: an indium zinc gallium oxide film having a thickness of 200 nm is formed by a sputtering method using an oxide target including equal amounts of indium, zinc, and gallium and then the film is patterned. Further, the second insulating film 106 is formed from 100-nm-thick aluminum oxide formed by a sputtering method.

[0117]

Then, a 100-nm-thick platinum film and a 100-nm-thick titanium film are formed by a sputtering method and then etched, so that the gate 107 is formed. The gate 107 is preferably formed so as to overlap with the third conductor electrode 102a and the fourth conductor electrode 102b and partly overlap with the first conductor electrode 103a and the second conductor electrode 103b as illustrated in FIG. 5G. In this manner, the FET is manufactured.

[0118]

(Embodiment 3)

In this embodiment, a method for manufacturing the FET illustrated in FIG. 2A will be described with reference to FIGS. 6A to 6E. First, the third conductor electrode 102 is formed over the substrate 101. In this embodiment, barium borosilicate glass is used as the substrate 101. The third conductor electrode 102 is formed in such a manner that a 100-nm-thick platinum film is formed by a sputtering method and then etched.

[0119]

Next, as illustrated in FIG. 6A, the first insulating film 104 is formed. In this embodiment, 100-nm-thick silicon oxide formed by a sputtering method is used as the first insulating film 104.

[0120]

Next, the first insulating film 104 is etched by a chemical mechanical polishing method or the like, so that a surface of the substrate 101 is planarized. This etching is

performed until the third conductor electrode 102 is exposed as illustrated in FIG. 6B. As a result, a structure is obtained in which the third conductor electrode 102 is embedded between the insulator 104a and an insulator 104b.

[0121]

After that, as the semiconductor layer 105, a 200-nm-thick indium zinc gallium oxide film is formed by a sputtering method using an oxide target including indium, zinc, and gallium at a ratio of 2:2:1. Further, the second insulating film 106 is formed using 100-nm-thick aluminum oxide formed by a sputtering method.

[0122]

Then, a 50-nm-thick platinum film and a 150-nm-thick aluminum film are formed by a sputtering method and then etched, so that the gate 107 is formed. As illustrated in FIG. 6C, the gate 107 is preferably formed so as to overlap with the third conductor electrode 102.

[0123]

Then, with the use of the gate 107 as a mask, an ion having an effect of reducing the indium zinc gallium oxide, such as a phosphorus ion, a boron ion, or a titanium ion, is introduced into the semiconductor layer 105 by an ion implantation method.

[0124]

In this embodiment, a phosphorus ion is used. A phosphorus ion is used also in a silicon semiconductor process and the ion does not travel in an FET owing to its large ionic radius; therefore, the use of a phosphorus ion is advantageous in terms of stability and reliability of the characteristics of the FET. In this manner, a first doped region 108a and a second doped region 108b are formed as illustrated in FIG. 6D.

[0125]

After that, a 300-nm-thick silicon oxide film is formed by a CVD method as a third insulating film 109. A surface of the third insulating film 109 is planarized by a chemical mechanical polishing method or the like. Then, contact holes that reach the first doped region 108a and the second doped region 108b are formed in the third insulating film 109 and the second insulating film 106, and the first conductor electrode 103a and the second conductor electrode 103b are formed.

[0126]

In this embodiment, a 50-nm-thick titanium nitride film and a 150-nm-thick titanium film are successively formed by a sputtering method and then patterned, so that the first conductor electrode 103a and the second conductor electrode 103b are formed. In this manner, the FET illustrated in FIG. 6E is manufactured.

[0127]

(Embodiment 4)

The semiconductor devices described in Embodiments 1 to 3 can be used in a variety of electronic devices, for example, in driver circuits for display devices such as liquid crystal displays, electro luminescent (EL) displays, and field emission (FE) displays, driver circuits for image sensors, semiconductor memories, and the like. Further, the semiconductor devices described in Embodiments 1 to 3 can be used in electronic devices including the above-described electronic devices, for example, in television sets, personal computers, communication devices such as mobile phones, electronic notebooks, portable music players, and the like.

This application is based on Japanese Patent Application serial no. 2010-027835 filed with Japan Patent Office on February 10, 2010, the entire contents of which are hereby incorporated by reference.

CLAIMS

1. A field effect transistor comprising:

a semiconductor layer including a first surface and a second surface opposed to the first surface;

a first conductor electrode in contact with the first surface of the semiconductor layer;

a second conductor electrode in contact with the first surface of the semiconductor layer;

a gate provided over the second surface of the semiconductor layer; and

a third conductor electrode in contact with the first surface of the semiconductor layer and between the first conductor electrode and the second conductor electrode so as to cross the semiconductor layer.

2. The field effect transistor according to claim 1, further comprising a fourth conductor electrode provided in contact with the first surface, so as to cross the semiconductor layer and be apart from the third conductor electrode.

3. The field effect transistor according to claim 1,

wherein the third conductor electrode is in contact with one of the first conductor electrode and the second conductor electrode.

4. The field effect transistor according to claim 1,

wherein the third conductor electrode is kept at the same potential as one of the first conductor electrode and the second conductor electrode.

5. The field effect transistor according to claim 2,

wherein the third conductor electrode is in contact with one of the first conductor electrode and the second conductor electrode, and

wherein the fourth conductor electrode is in contact with the other of the first conductor electrode and the second conductor electrode.

6. The field effect transistor according to claim 2,

wherein the third conductor electrode is kept at the same potential as one of the first conductor electrode and the second conductor electrode, and

wherein the fourth conductor electrode is kept at the same potential as the other of the first conductor electrode and the second conductor electrode.

7. The field effect transistor according to claim 1,

wherein the semiconductor layer comprises a first doped region and a second doped region that include a donor or an acceptor at a high concentration .

8. The field effect transistor according to claim 7,

wherein concentrations of the donor or the acceptor in the first doped region and the second doped region are higher than or equal to 1×10^{18} /cm^3 and lower than 1×10^{21} /cm^3.

9. The field effect transistor according to claim 1,

wherein work functions of portions of the first conductor electrode and the second conductor electrode, which are in contact with the semiconductor layer, are lower than a sum of an electron affinity of the semiconductor layer and 0.3 electron volts.

10. The field effect transistor according to claim 1,

wherein a junction between the first conductor electrode and the semiconductor layer and a junction between the second conductor electrode and the semiconductor layer are each an ohmic junction.

11. The field effect transistor according to claim 1,

wherein a work function of a portion of the third conductor electrode, which is in contact with the semiconductor layer, is higher than a sum of an electron affinity of the semiconductor layer and 0.6 electron volts.

12. The field effect transistor according to claim 1,

wherein a junction between the third conductor electrode and the semiconductor layer is a Schottky barrier junction.

13. The field effect transistor according to claim 1, further comprising a gate insulating film between the semiconductor layer and the gate.

14. The field effect transistor according to claim 1, wherein a material of the semiconductor layer is an oxide semiconductor.

15. A field effect transistor comprising:

a semiconductor layer including a first surface and a second surface opposed to the first surface;

a first conductor electrode in contact with the first surface of the semiconductor layer;

a second conductor electrode provided in contact with the first surface of the semiconductor layer;

a gate over the first surface of the semiconductor layer; and

a third conductor electrode in contact with the second surface of the semiconductor layer so as to cross the semiconductor layer.

16. The field effect transistor according to claim 15, further comprising a fourth conductor electrode provided in contact with the second surface, so as to cross the semiconductor layer and be apart from the third conductor electrode.

17. The field effect transistor according to claim 15,

wherein the third conductor electrode is in contact with one of the first conductor electrode and the second conductor electrode.

18. The field effect transistor according to claim 15,

wherein the third conductor electrode is kept at the same potential as one of the first conductor electrode and the second conductor electrode.

19. The field effect transistor according to claim 16,

wherein the third conductor electrode is in contact with one of the first conductor electrode and the second conductor electrode, and

wherein the fourth conductor electrode is in contact with the other of the first conductor electrode and the second conductor electrode.

20. The field effect transistor according to claim 16,

wherein the third conductor electrode is kept at the same potential as one of the first conductor electrode and the second conductor electrode, and

wherein the fourth conductor electrode is kept at the same potential as the other of the first conductor electrode and the second conductor electrode.

21. The field effect transistor according to claim 15,

wherein the semiconductor layer comprises a first doped region and a second doped region that include a donor or an acceptor at a high concentration .

22. The field effect transistor according to claim 21,

wherein concentrations of the donor or the acceptor in the first doped region and the second doped region are higher than or equal to 1×10^{18} /cm^3 and lower than 1×10^{21} /cm^3.

23. The field effect transistor according to claim 15,

wherein work functions of portions of the first conductor electrode and the second conductor electrode, which are in contact with the semiconductor layer, are lower than a sum of an electron affinity of the semiconductor layer and 0.3 electron volts.

24. The field effect transistor according to claim 15,

wherein a junction between the first conductor electrode and the semiconductor layer and a junction between the second conductor electrode and the semiconductor layer are each an ohmic junction.

25. The field effect transistor according to claim 15,

wherein a work function of a portion of the third conductor electrode, which is in contact with the semiconductor layer, is higher than a sum of an electron affinity of the semiconductor layer and 0.6 electron volts.

26. The field effect transistor according to claim 15,

wherein a junction between the third conductor electrode and the semiconductor layer is a Schottky barrier junction.

27. The field effect transistor according to claim 15, further comprising a gate insulating film between the semiconductor layer and the gate.

28. The field effect transistor according to claim 15, wherein a material of the semiconductor layer is an oxide semiconductor.

FIG. 1A

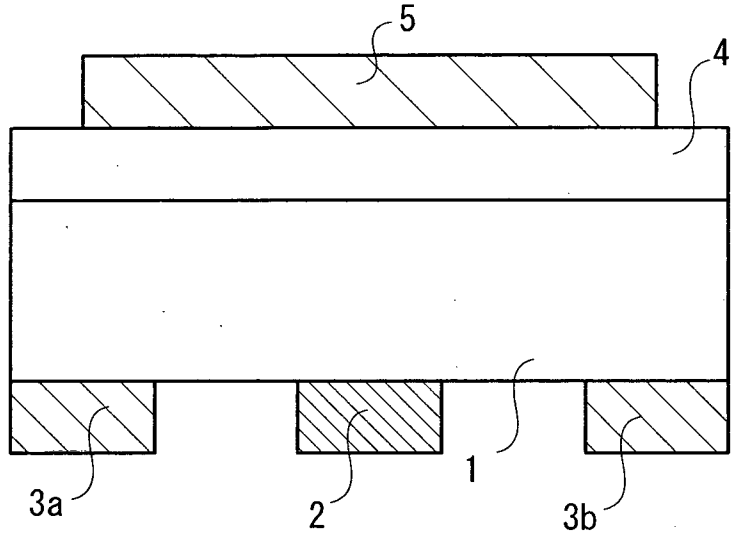


FIG. 1B

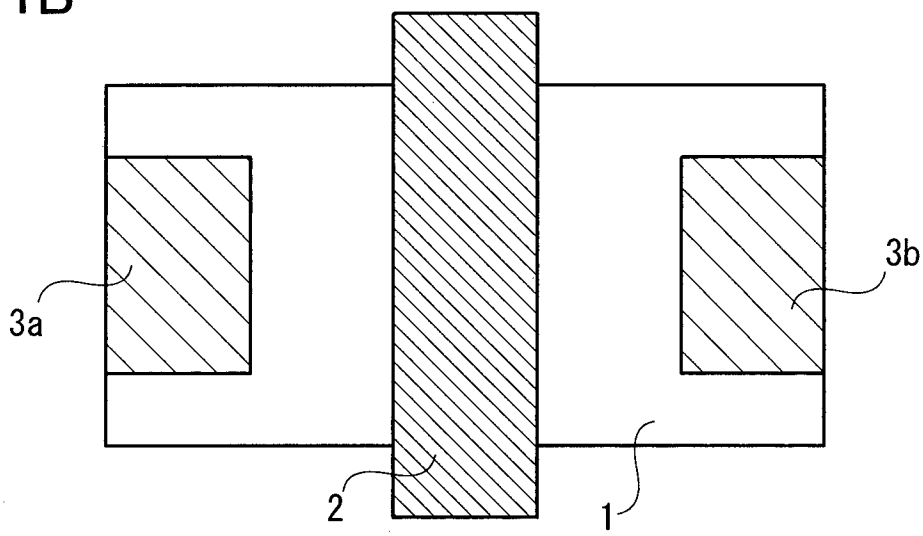


FIG. 1C

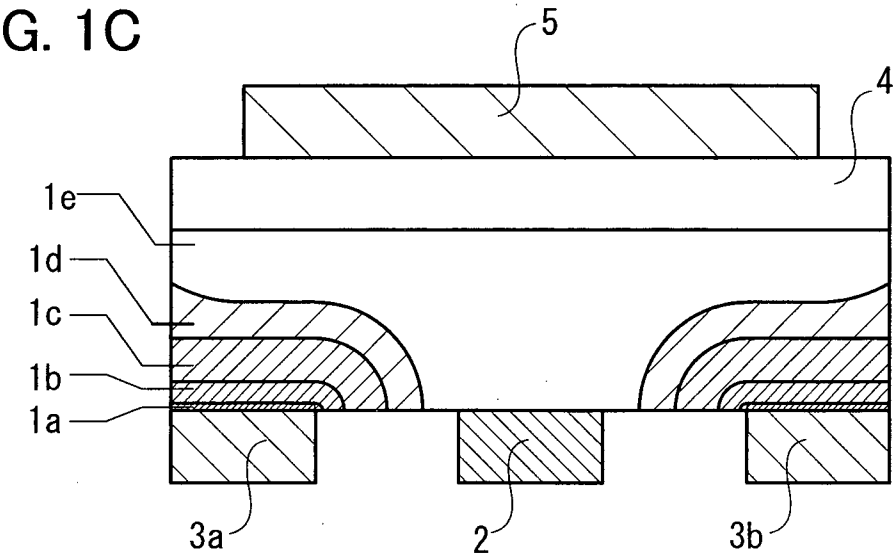


FIG. 2A

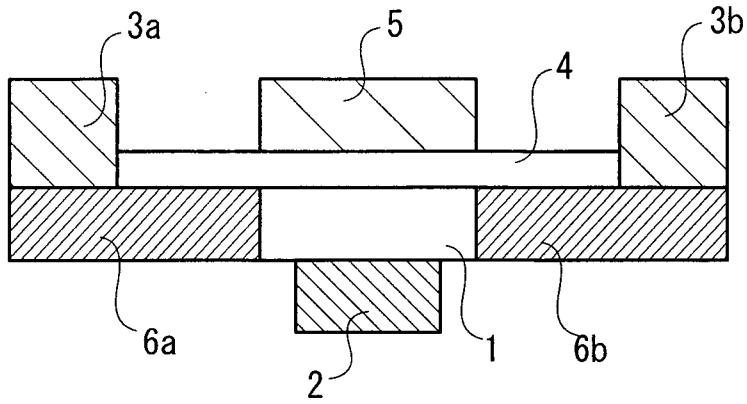


FIG. 2B

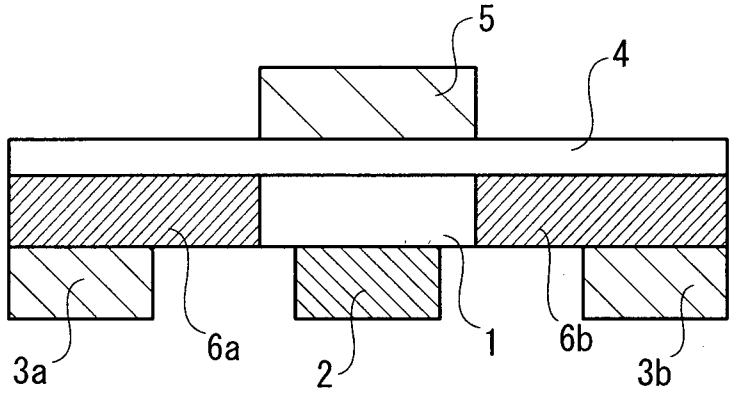


FIG. 2C

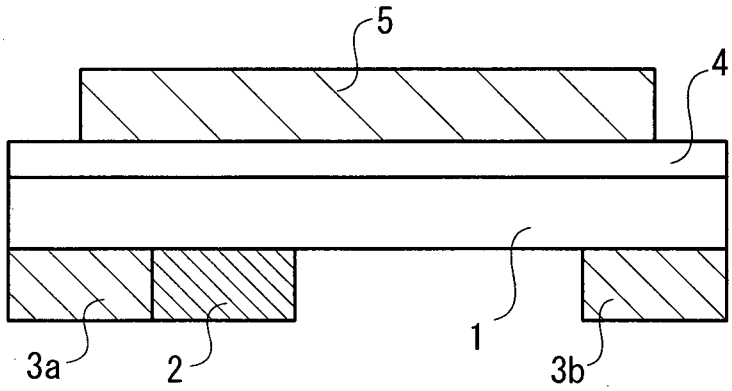


FIG. 2D

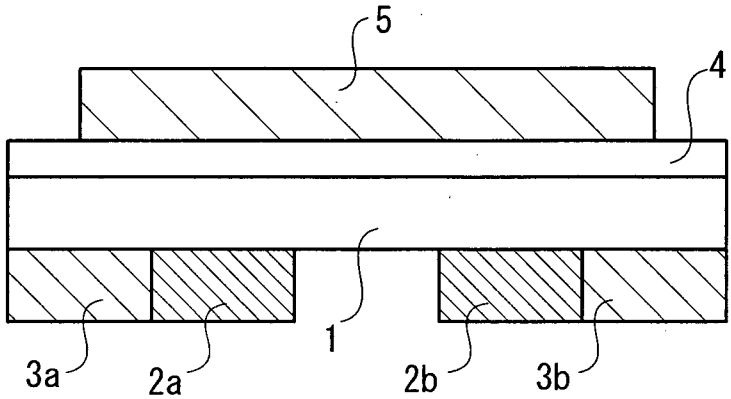


FIG. 3A

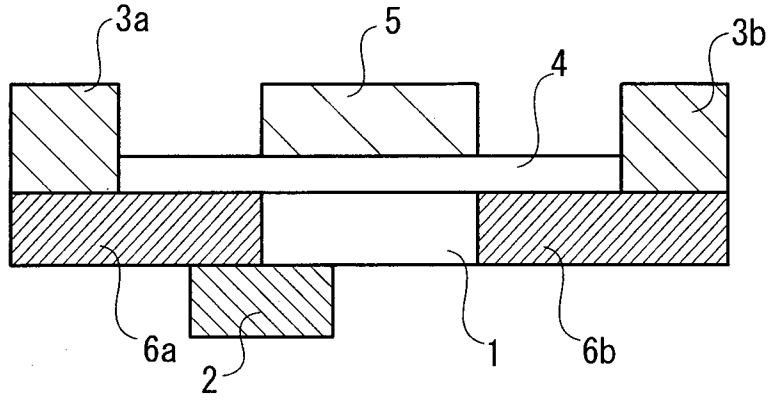


FIG. 3B

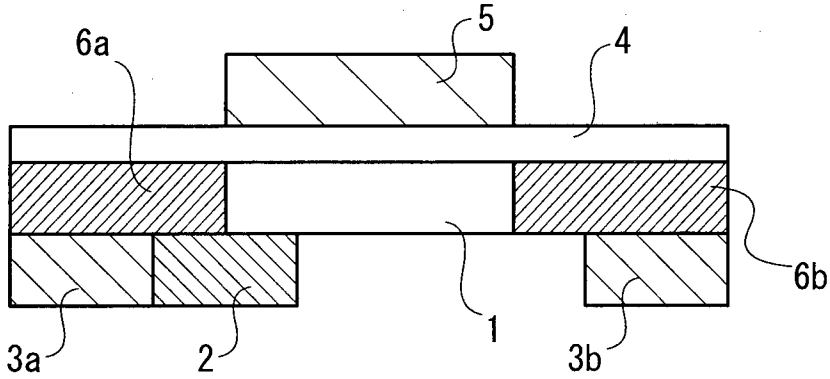


FIG. 3C

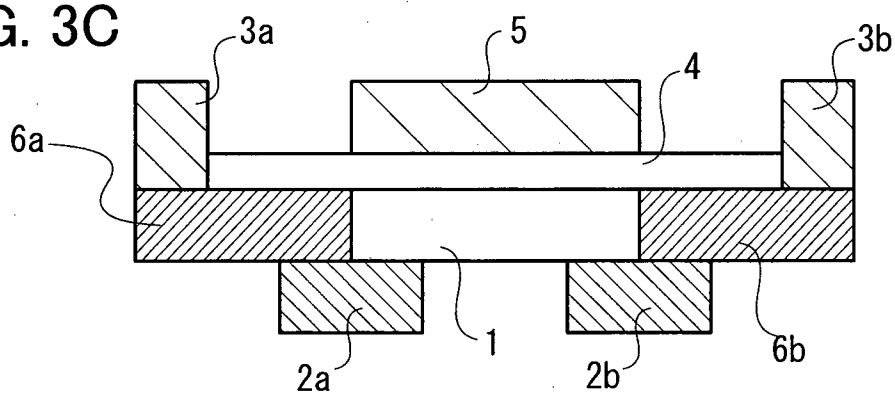


FIG. 3D

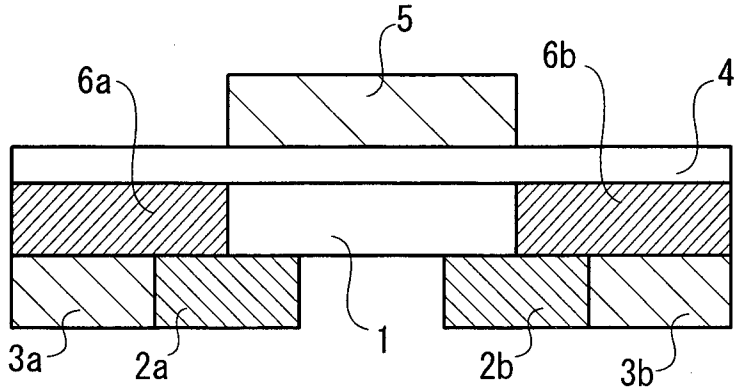


FIG. 4A

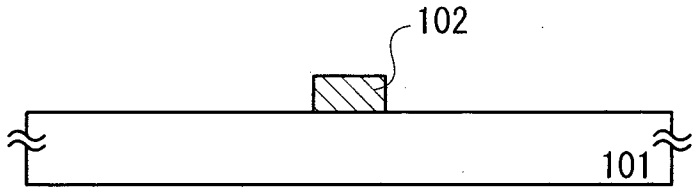


FIG. 4B

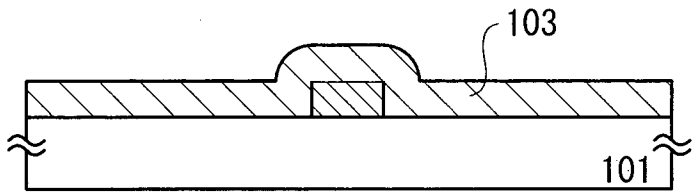


FIG. 4C

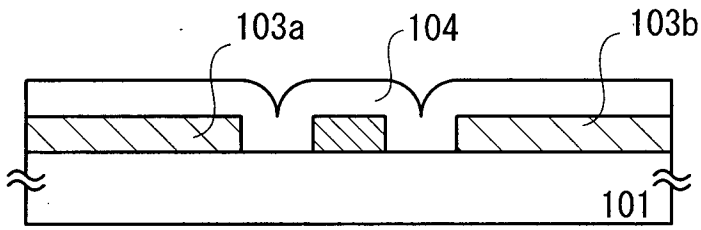


FIG. 4D

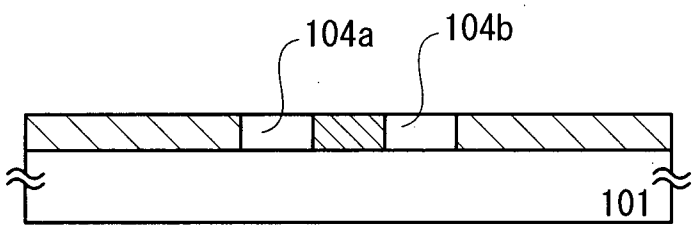


FIG. 4E

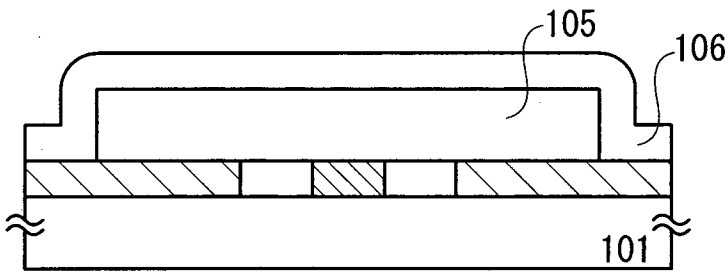


FIG. 4F

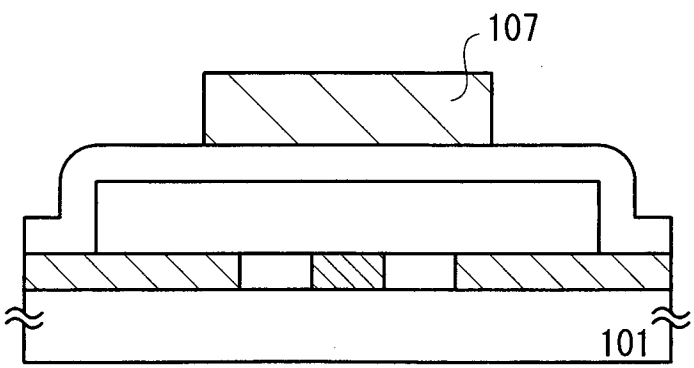


FIG. 5A

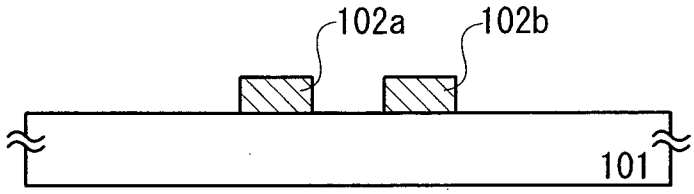


FIG. 5B

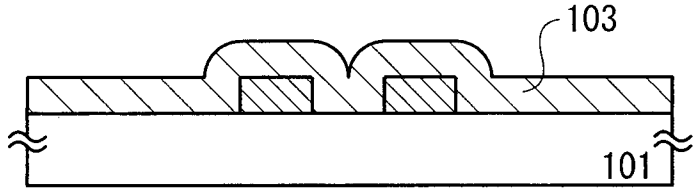


FIG. 5C

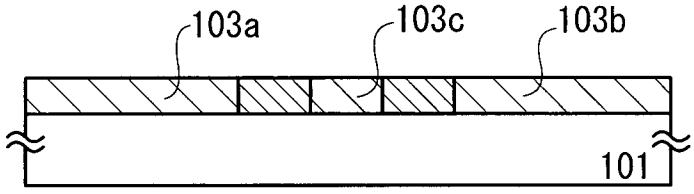


FIG. 5D

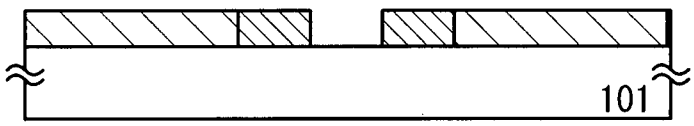


FIG. 5E

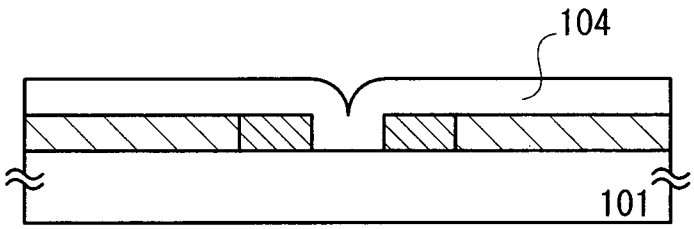


FIG. 5F

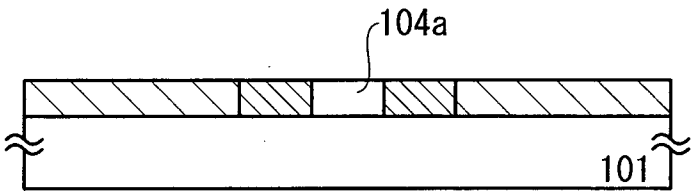


FIG. 5G

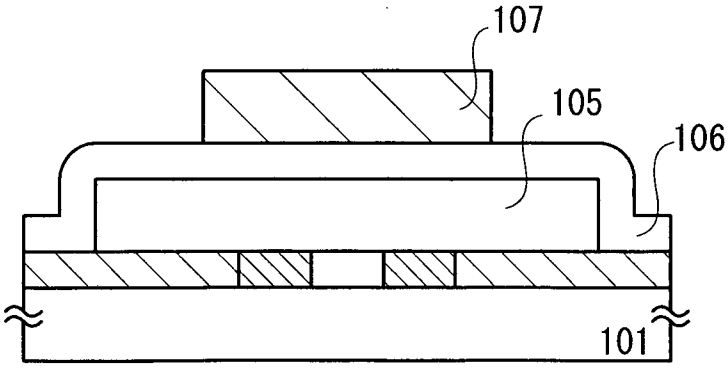


FIG. 6A

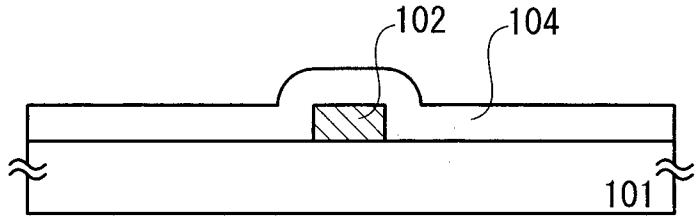


FIG. 6B

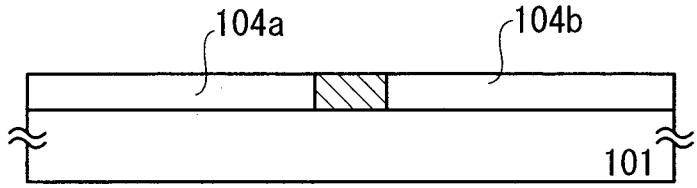


FIG. 6C

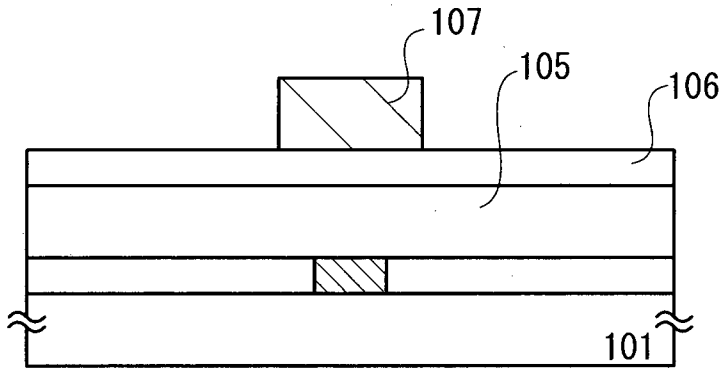


FIG. 6D

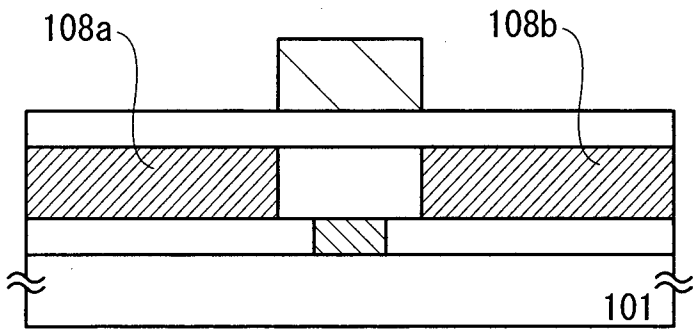


FIG. 6E

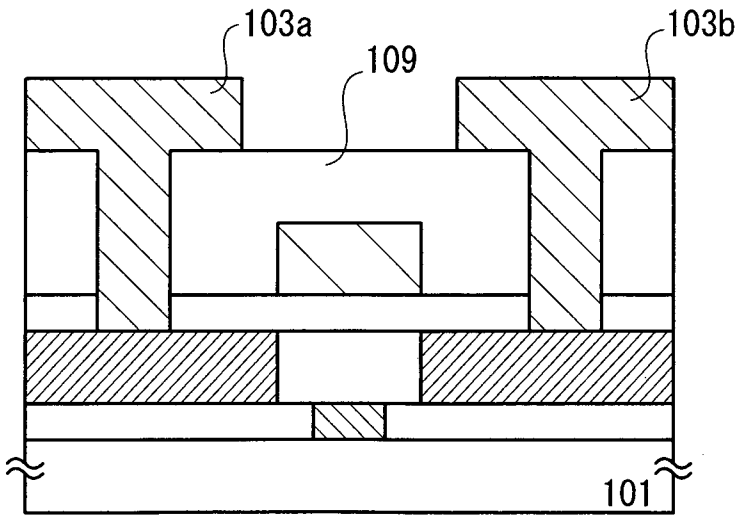


FIG. 7A

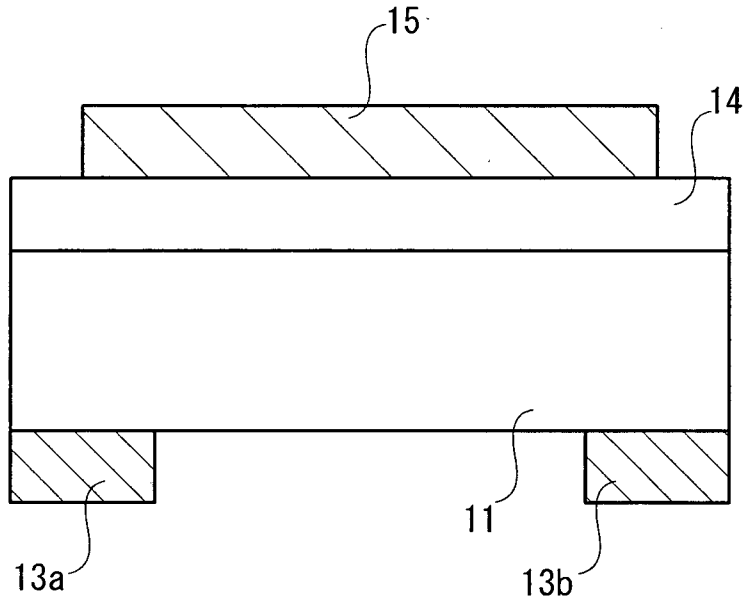
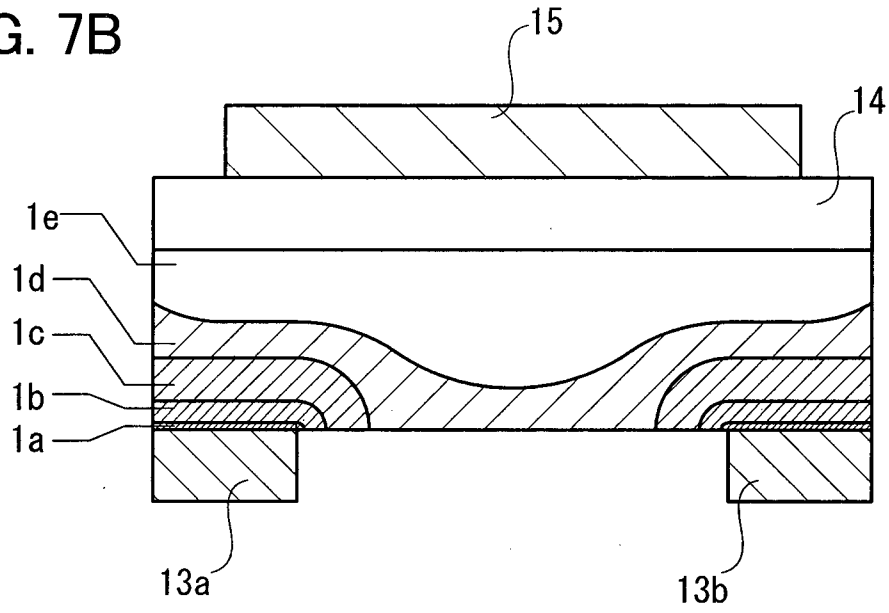


FIG. 7B



EXPLANATION OF REFERENCE

1: semiconductor layer, 1a: region, 1b: region, 1c: region, 1d: region, 1e: region, 2: third conductor electrode, 2a: third conductor electrode, 2b: fourth conductor electrode, 3a: first conductor electrode, 3b: second conductor electrode, 4: gate insulating film, 5: gate, 6a: first doped region, 6b: second doped region, 11: semiconductor layer, 13a: source electrode, 13b: drain electrode, 14: gate insulating film, 15: gate, 101: substrate, 102: third conductor electrode, 102a: third conductor electrode, 102b: fourth conductor electrode, 103: conductor film, 103a: first conductor electrode, 103b: second conductor electrode, 103c: conductor film, 104: first insulating film, 104a: insulator, 104b: insulator, 105: semiconductor layer, 106: second insulating film, 107: gate, 108a: first doped region, 108b: second doped region, and 109: third insulating film.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2011/051033

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. See extra sheet

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. H01L29/786, H01L21/28, H01L21/338, H01L21/8234, H01L27/088, H01L29/423, H01L29/812

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
Published unexamined utility model applications of Japan 1971-2011
Registered utility model specifications of Japan 1996-2011
Published registered utility model applications of Japan 1994-2011

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	JP 2005-236180 A (RENESAS TECHNOLOGY) 2005.09.02, [0014]-[0028], Fig.1-Fig.3 (No Family)	1,7-15,21-28 2-6,16-20
X A	JP 2006-253490 A (SHARP KABUSHIKI KAISHA) 2006.09.21, [0007]-[0010], Fig.1-Fig.2 (No Family)	1,7-15,21-28 2-6,16-20
A	JP 4-367265 A (CANON KABUSHIKI KAISHA) 1992.12.18, whole document (No Family)	1-28
A	JP 9-8317 A (Casio Computer Co., Ltd.) 1997.01.10, whole document (No Family)	1-28

☑ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15.02.2011	01.03.2011

Name and mailing address of the ISA/JP	Authorized officer
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INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2011/051033

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6104040 A (Hitachi, Ltd.) 2000.08.15, whole document & JP 10-73845 A & EP 816903 A1 & DE 69708981 D & SG 73573 A	1-28

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2011/051033

CLASSIFICATION OF SUBJECT MATTER
H01L29/786(2006.01)i, H01L21/28(2006.01)i, H01L21/338(2006.01)i,
H01L21/8234(2006.01)i, H01L27/088(2006.01)i, H01L29/423(2006.01)i,
H01L29/812(2006.01)i