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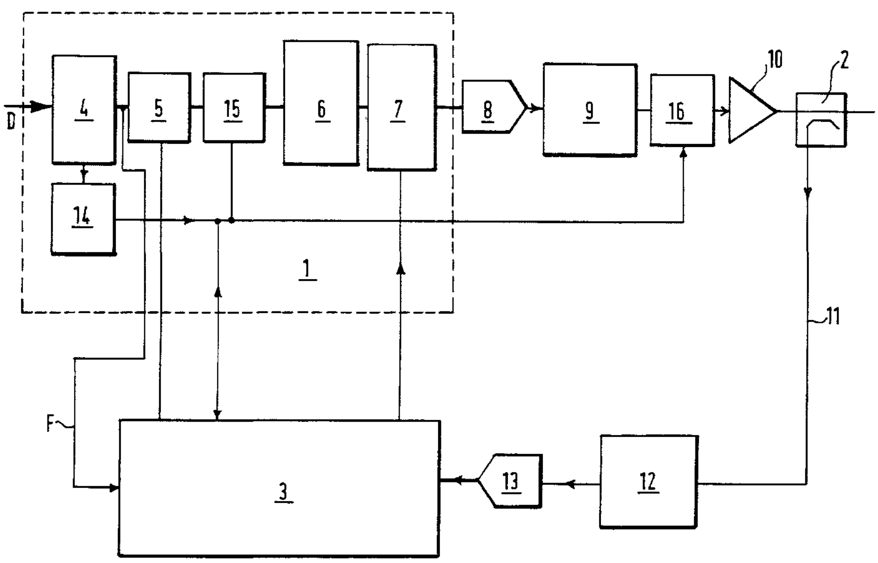
(54) Title: LINEARISED RADIO TRANSMITTER



(57) Abstract: A linearised radio transmitter comprises a fixed digital signal processor (1), an output element (2), and a programmable digital signal processor (3). The fixed digital signal processor (1) includes a pre-distorter (5) which is controlled by the programmable digital signal processor (3) in dependence upon signals received by the programmable digital signal processor from the output element (2). The transmitter further comprises a digital amplitude control (15) and an analogue amplitude control (16) positioned between the pre-distorter (5) and the output element (2). Control means (14) are provided for simultaneously controlling the setting of the digital amplitude control (15) and the setting of the analogue amplitude control (16) such that their combined gain is constant.

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LINEARISED RADIO TRANSMITTER

This invention relates to a linearised radio transmitter, and in particular to a linearised radio transmitter which incorporates adaptive pre-distortion linearisation. Such a transmitter would be suitable for use in a third generation mobile phone base station.

Linearised radio transmitters employing adaptive pre-distortion are known. A typical known transmitter is shown in the block circuit diagram of Figure 1, which shows a dedicated digital signal processor (DSP) 1, an output sampling block 2, and a programmable DSP 3. The dedicated DSP 1 includes a coding and power control block 4 , a digital pre-distorter 5, a digital frequency up-converter 6, and an IQ and DC error corrector 7. Input data signals (indicated by the reference D) are processed by the block 4 which performs channel coding, power control and filtering functions for a multiplicity of channels. The digital pre-distorter 5 typically produces distortion of the signal amplitude and phase, and is controlled by a set of coefficients provided by the programmable DSP3. The up-converter and error corrector blocks 6 and 7 provide frequency conversion and correction for hardware inaccuracies in the analogue processing and are optional. The output of the dedicated DSP 1 is fed to a digital-to-analogue (DAC) converter 8, whose output is fed to an RF up-converter 9. The output of the RF up-converter 9 is fed to the output sampling block 2 via a high power output amplifier 10. A feedback line 11 from the output sampling block 2 leads to the programmable DSP 3 via an RF down-converter 12, and an analogue-to-digital converter 13. The programmable DSP 3 is connected to the digital pre-distorter 5 and the error corrector 7 of the dedicated DSP 1, thereby to provide error estimation and adaptation. A feedback link F is also provided so that the programmable DSP 3 can compare the signal from the analogue-to-digital converter 13 with the ideal signal.

The purpose of using pre-distortion is to reduce the power consumption requirements of the transmitter. The majority of the power consumption is within the amplifier 10, and is determined mainly by the bias current and voltage of the amplifier transistors. The bias levels are typically chosen to ensure that the amplifier 10 is able to deliver the required peak envelope power (PEP) into the load. If the bias levels are reduced, then signals at the peak power level will be distorted, resulting in a loss of system data transmission capacity. Distortion of the output signal peaks can be eliminated by pre-distorting the baseband digital signal in such a way that subsequent non-linearity in the RF processing and the amplifier 10 results in a signal free from distortion. To achieve optimum reduction of the output distortion, the parameters of the pre-distorter 5 must be accurately matched to that of the amplifier 10 and the RF processing characteristics. In practice, the system characteristics will change. The RF down-converter 12 and the analogue-to-digital converter 13 provide means for measuring the output signal. The programmable DSP 3 compares the measured output signal with the desired optimum output signal to estimate the required pre-distortion parameters to obtain perfect cancellation. The calculated optimum distortion parameters are then fed back to the pre-distorter 5. This distortion adaptation loop, tracks changes in the system with time, temperature and output load.

The transmitter of Figure 1, as with many practical transmitters, requires means for controlling the output power , this being accomplished by the coding and power control block 4. For the system to operate without distortion, however, the digital-to-analogue converter 8, the RF up-converter 9, the amplifier 10 and the output sampling block 2 must accommodate the total signal dynamic range, which will be the sum of the required output signal-to-noise ratio (SNR), the power control dynamic range, and a head room allowance for the pre-distortion. It is normal practice when designing such systems to ensure that the dominant source of non-linearity is within the amplifier 10, and hence the digital-to-analogue converter 8 and the RF up-converter 9 are relatively linear. Thus, to achieve the dynamic range and linearity requirements within these two elements, requires a high level of power supply consumption, which reduces the overall efficiency gains resulting from the use of pre-distortion to linearise the amplifier 10.

The aim of the invention is to improve power consumption within a linearised radio transmitter using adaptive pre-distortion linearisation.

The present invention provides a linearised radio transmitter comprising digital signal processor means, and an output sampling means, the digital signal processor means including a digital pre-distorter which is controlled by the digital signal processor means in dependence upon signals received from the output sampling means, the transmitter further comprising a digital-to-analogue converter at the output of the digital pre-distorter, an amplifier positioned between the digital-to-analogue converter and the output sampling means, a digital amplitude control positioned between the digital pre-distorter and the digital-to-analogue converter, an analogue amplitude control positioned between the digital-to-analogue converter and the amplifier, and an analogue-to-digital converter positioned between the output sampling means and the digital signal processor means, wherein control means are provided for simultaneously controlling the setting of the digital amplitude control and the setting of the analogue amplitude control such that their combined gain is constant.

Advantageously, the transmitter further comprises an RF up-converter positioned between the analogue-to-digital converter and the analogue gain control, and an RF down-converter positioned between the output sampling means and the amplifier.

Preferably, the digital signal processor means is constituted by first and second digital signal processors, the first digital signal processor including the digital pre-distorter, the second digital signal processor controlling the digital pre-distorter in dependence upon signals received by the second digital signal processor from the output sampling means, the digital-to-analogue converter being positioned at the output of the first digital signal processor, and the analogue-to-digital converter being positioned between the output sampling means and the second digital signal processor.

In a preferred embodiment, the first digital signal processor includes a coding and power control element for modifying incoming signals to the first digital signal processor. Preferably, the control means is a power detection and range control element which receives output signals from the coding and power control element, and feeds output signals to the digital amplitude control, the analogue amplitude control and the second digital signal processor.

Advantageously, the arrangement is such that distortion coefficients applied to the digital pre-distorter are adapted in accordance with the signals received by the second digital signal processor from the output sampling means.

In a preferred embodiment, the control means operates in accordance with an algorithm such that:

a) if P1 is greater than or equal to P2, the analogue amplitude control is adjusted for maximum amplitude, and the second digital signal processor is controlled such that the adaptation process is enabled to apply optimised distortion coefficients to the digital pre-distorter in response to measurement of the output sampling means;

b) if P1 is less than P2 but greater than or equal to P3, the analogue amplitude control is adjusted for maximum amplitude, and the second digital signal processor is controlled so that the adaptation process is disabled so that new distortion coefficients are not applied to the digital pre-distorter; and

c) if P1 is less than P3, the analogue amplitude control is adjusted to provide a level less than the maximum amplitude, and the second digital signal processor is controlled such that the adaptation process is disabled so that new distortion coefficients are not applied to the digital pre-distorter;

where P1 is the power measured by the control means, P2 is a first reference level, and P3 is a second reference level and less than P2.

Advantageously, step c) is such that the pre-distorter is forced to a linear state by modifying the distortion coefficients.

Preferably, P1 is the sum of the individual power settings within the transmit coding and power control element. Alternatively, P1 is the peak power at the output of the transmit coding and power control element measured over a predetermined period of time.

Conveniently, the control means operates in accordance with a modified form of said algorithm, where P2 and P3 are each replaced by two parameters $P2_{high}$, $P2_{low}$, and $P3_{high}$, $P3_{low}$, and the modified algorithm is such that:

a) if P1 is increasing $P2_{high}$ and $P3_{high}$ are used; and

b) if P1 is decreasing, $P2_{low}$ and $P3_{low}$ are used;

$P2_{high}$ being greater than $P2_{low}$,, $P3_{high}$ being greater than $P3_{low}$, and $P2_{low}$ being greater than $P3_{high}$.

A linearised radio transmitter constructed in accordance with the invention will now be described in greater detail, by way of example, with reference to Figure 2 of the drawings which is a block circuit diagram of the transmitter.

The transmitter of Figure 2 is a modified version of the transmitter of Figure 1, so like reference numerals will be used for like parts, and only the modifications will be described in detail. Thus, the transmitter of Figure 2 includes a power detection and range control block 14 associated with the coding and power control block 4 within the dedicated DSP 1, a digital amplitudecontrol block 15 positioned at the output of the digital pre-distorter 5, and an analogue amplitude control block (typically an analogue attenuator) 16 between the RF up-converter 9, and the amplifier 10.

The power detection and range control block 14 controls the digital amplitudecontrol block 15 and the analogue amplitude control16 simultaneously and in tandem. This control is such that the amplitude setting of the digital control block 15 is matched by the amplitude settingof the analogue amplitude control 16, such that the combined gain of the two blocks is constant regardless of individual settings.

The power detection and range control block 14 measures the total output power level of the coding and power control block 4, and adjusts the digital amplitudecontrol block 15, the analogue amplitude control16, and the programmable DSP 3 with respect to the measured power and in accordance with the algorithm described below.
In this algorithm, P1 is the power measured by the power detection and range control block 14, P2 and P3 are reference levels where P2 is greater than or equal to P3. The

value of P1 may be found by summing the individual channel power settings present within the block 4, or from the peak power at the output of the block 4 measured over a period. Typically, P2 is set to a level at which the amplifier 10 is operating relatively linearly compared to at the maximum output power. For a given maximum level of output distortion, the values of the parameters of the pre-distorter 5 become less critical as the degree of correction is significantly lower. Below the level P2, the adaptation process is consequently no longer useful and is disabled. The level P3 is chosen such that the characteristics of the amplifier 10 are sufficiently linear that the pre-distortion can be disabled entirely, or such that the gain mismatches introduced due to imperfections of the analogue attenuator 16 will not cause unacceptable output distortion due to the resulting mismatch of the pre-distortion and amplifier characteristics. The parameters P2 and P3 will be dependent on the specific implementation, and must be determined by simulation or empirically for any given system.

Where P1 is greater than or equal to P2, the analogue amplitude control 16 is adjusted for a maximum amplitude, and the programmable DSP 3 is controlled such that the adaptation process is enabled to apply optimised distortion coefficients to the digital pre-distorter 5 in response to measurements of the output 2.

Where P1 is less than P2 but greater than or equal to P3, the analogue amplitude control 16 is adjusted for a maximum amplitude, and the programmable DSP 3 is controlled such that the adaptation process is disabled so that new distortion coefficients are not applied to the digital pre-distorter 5.

Where P1 is less than P3, the analogue amplitude control 16 is adjusted to provide a level less than the maximum amplitude, and the programmable DSP 3 is controlled such that the adaptation process is disabled so that new distortion coefficients are not applied to the digital pre-distorter 5. This lesser setting of amplitude may be fixed or variable. Where a variable amplitude setting is used, the setting will also be adjusted in accordance with P1, such that the level of power at the output of the RF up-converter 9 is maintained at a nominal operating level. This nominal level is chosen such that the

RF up-conversion linearity and the SNR are optimised for a given level of power supply consumption. In the case where a fixed level of amplitude reduction is used, this is chosen such that the level of power at the output of the RF up-converter 9 is maintained within a minimal deviation of the nominal operating level. An option within this operating range is that the digital pre-distorter 5 is forced to a linear state, either by by-passing the element entirely, or by appropriately modifying the parameters. In this case, the digital gain control block 15 may be logically implemented within the transmit coding and power control block 4, by simultaneously modifying the level control of all the multiplicity of channels by the equivalent amount.

In a modified version of the algorithm, each of the levels P2 and P3 is replaced by two parameters $P2_{high}$ and $P2_{low}$ and $P3_{high}$ and $P3_{low}$. The algorithm is such that, if P1 is increasing $P2_{high}$ and $P3_{high}$ are used; and, if P1 is decreasing, then $P2_{low}$ and $P3_{low}$ are used. Thus, by setting $P2_{high}$ to be larger than $P2_{low}$ and $P3_{high}$ to be greater than $P3_{low}$, hysteresis is achieved. In this case, the value of $P2_{low}$ must be greater than the value of $P3_{high}$, to ensure that the adaptation process is disabled when the amplitude control 16 is not set to provide a maximum amplitude.

The invention has a number of advantages. Firstly, the dynamic range requirements of the DAC converter 8 and the up-converter 9 are reduced, so that the power supply consumption of the transmitter is reduced. Moreover, by reducing the dynamic range requirements of the DAC 8, a cheaper device with less resolution may be employed. Secondly, the RF up-converter local oscillator leakage is attenuated by the analogue attenuator 16 as the output level is reduced, and the requirement for filtering or for oscillator leakage suppression is also reduced.

Claims

1. A linearised radio transmitter comprising digital signal processor means, and an output sampling means, the digital signal processor means including a digital pre-distorter which is controlled by the digital signal processor means in dependence upon signals received from the output sampling means, the transmitter further comprising a digital-to-analogue converter at the output of the digital pre-distorter, an amplifier positioned between the digital-to-analogue converter and the output sampling means, a digital amplitude control positioned between the digital pre-distorter and the digital-to-analogue converter, an analogue amplitude control positioned between the digital-to-analogue converter and the amplifier, and an analogue-to-digital converter positioned between the output sampling means and the digital signal processor means, wherein control means are provided for simultaneously controlling the setting of the digital amplitude control and the settingof the analogue amplitude control such that their combined gain is constant.

2. A transmitter as claimed in claim 1, further comprising an RF up-converter positioned between the digital-to-analogue converter and the amplifier, and an RF down-converter positioned between the output sampling means and the analogue-to-digital converter.

3. A transmitter as claimed in claim 1 or claim 2, wherein the digital signal processor means is constituted by first and second digital signal processors, the first digital signal processor including the digital pre-distorter, the second digital signal processor controlling the digital pre-distorter in dependence upon signals received by the second digital signal processor from the output sampling means, the digital-to-analogue converter being positioned at the output of the first digital signal processor, and the analogue-to-digital converter being positioned between the output sampling means and the second digital signal processor.

4. A transmitter as claimed in claim 3, wherein the first digital signal processor includes a coding and power control element for modifying incoming signals to the first digital signal processor.

5. A transmitter as claimed in claim 4, wherein the control means is a power detection and range control element which receives output signals from the coding and power control element, and feeds output signals to the digital amplitude control, the analogue amplitude control and the second digital signal processor.

6. A transmitter as claimed in claim 4 or claim 5, wherein the arrangement is such that distortion coefficients applied to the digital pre-distorter are adapted in accordance with the signals received by the second digital signal processor from the output sampling means.

7. A transmitter as claimed in claim 6, wherein the control means operates in accordance with an algorithm such that:

a) if P1 is greater than or equal to P2, the analogue amplitude control is adjusted for maximum amplitude, and the second digital signal processor is controlled such that the adaptation process is enabled to apply optimised distortion coefficients to the digital pre-distorter in response to measurement of the output sampling means;

b) if P1 is less than P2 but greater than or equal to P3, the analogue amplitude control is adjusted for maximum amplitude, and the second digital signal processor is controlled so that the adaptation process is disabled so that new distortion coefficients are not applied to the digital pre-distorter; and

c) if P1 is less than P3, the analogue amplitude control is adjusted to provide a level less than the maximum amplitude, and the second digital signal processor is controlled such that the adaptation process is disabled so that new distortion coefficients are not applied to the digital pre-distorter;

where P1 is the power measured by the control means, P2 is a first reference level, and P3 is a second reference level and less than P2.

8. A transmitter as claimed in claim 7, wherein step c) is such that the pre-distorter is forced to a linear state by modifying the distortion coefficients.

9. A transmitter as claimed in claim 8 when appendant to claim 6, wherein P1 is the sum of the individual power settings within the transmit coding and power control element.

10. A transmitter as claimed in claim 8 when appendant to claim 6, wherein P1 is the peak power at the output of the transmit coding and power control element measured over a predetermined period of time. 11. A transmitter as claimed in any one of claims 7 to 10, wherein the control means operates in accordance with a modified form of said algorithm, where P2 and P3 are each replaced by two parameters $P2_{high}$, $P2_{low}$, and $P3_{high}$, $P3_{low}$, and the modified algorithm is such that:

a) if P1 is increasing $P2_{high}$ and $P3_{high}$ are used; and

b) if P1 is decreasing, $P2_{low}$ and $P3_{low}$ are used;

$P2_{high}$ being greater than $P2_{low}$,, $P3_{high}$ being greater than $P3_{low}$, and $P2_{low}$ being greater than $P3_{high}$

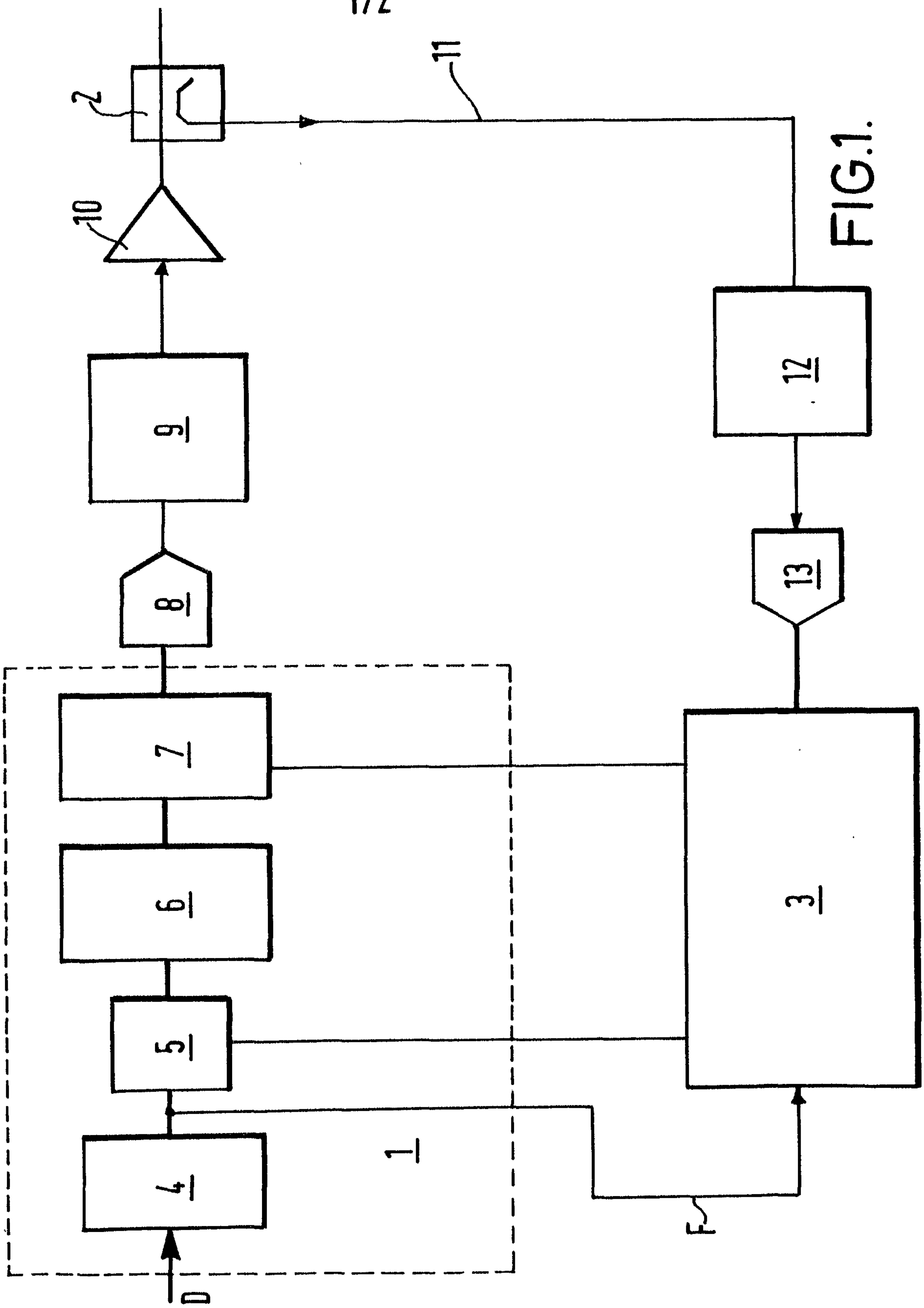

FIG.1.

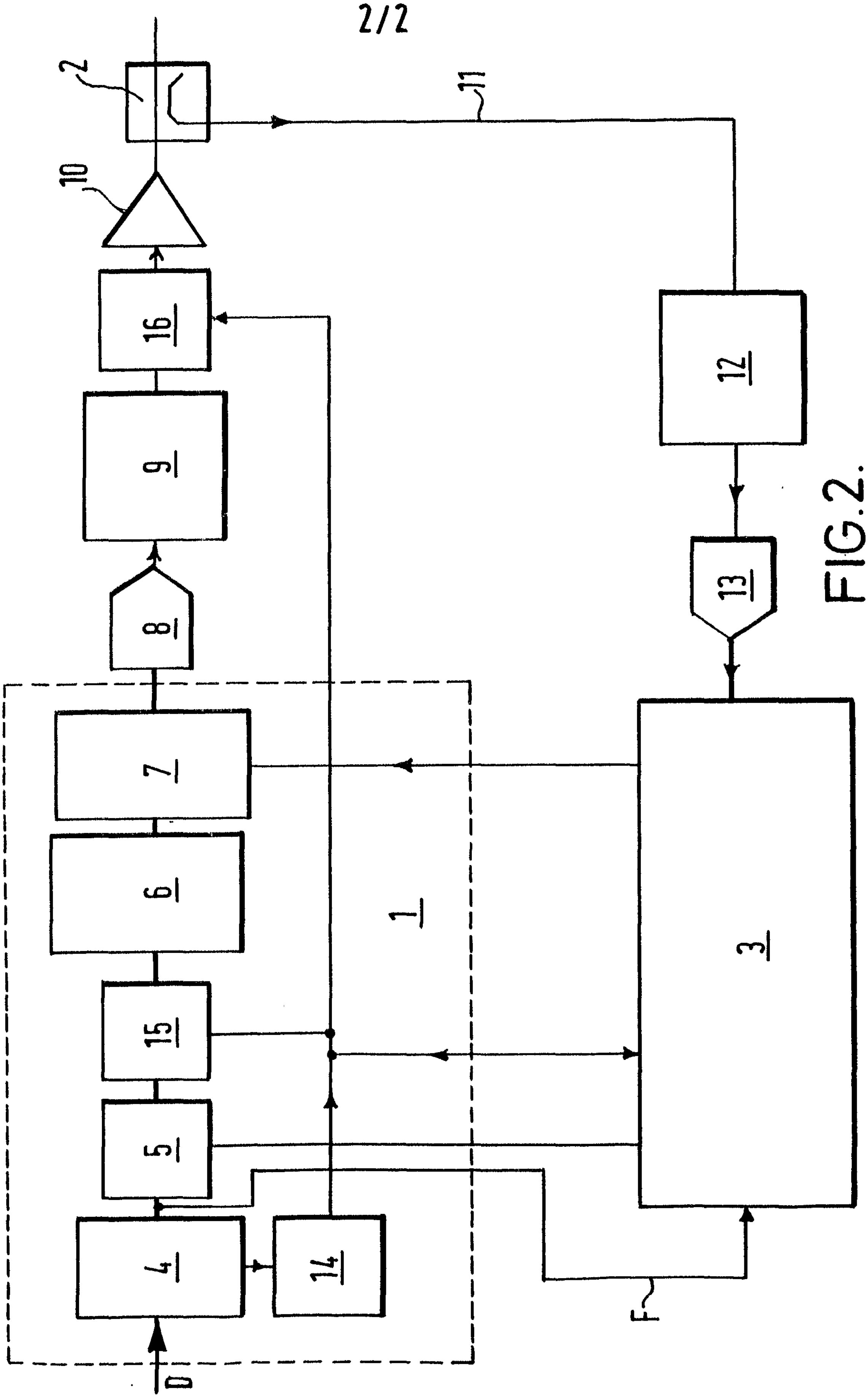

FIG.2.

INTERNATIONAL SEARCH REPORT

International Application No
PCT/GB 02/03824

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03F1/32 H03G3/20 H03G3/30

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03F H03G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 961 402 A (NOKIA MOBILE PHONES LTD) 1 December 1999 (1999-12-01) column 16, line 31 -column 19, line 11; figure 5	1-11
A	US 5 959 499 A (KHAN ANDREW MERRITT ET AL) 28 September 1999 (1999-09-28) column 2, line 35 -column 5, line 17; figure 1	1-11

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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Date of the actual completion of the international search	Date of mailing of the international search report
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Name and mailing address of the ISA	Authorized officer
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INTERNATIONAL SEARCH REPORT

Information on patent family members

Int. onal Application No
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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0961402 A	01-12-1999	EP 0961402 A2	01-12-1999
		JP 2000049630 A	18-02-2000
US 5959499 A	28-09-1999	FR 2769152 A1	02-04-1999
		WO 9917439 A1	08-04-1999