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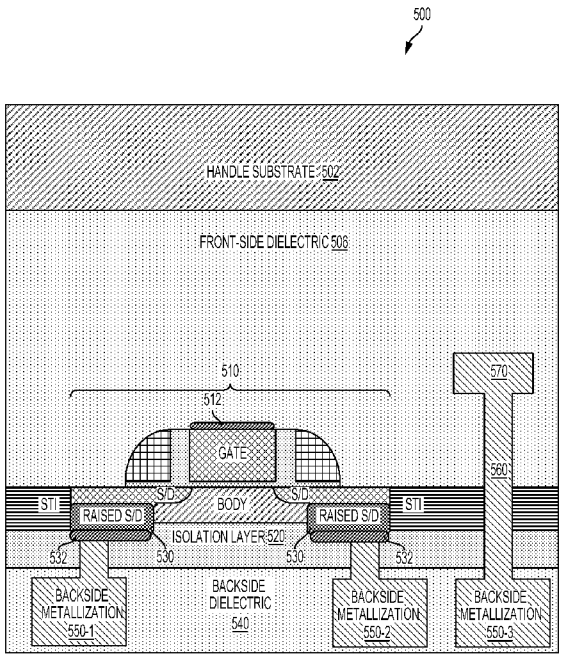

FIG. 5A

(57) Abstract: An integrated circuit structure may include a transistor on a front-side semiconductor layer supported by an isolation layer. The transistor is a first source/drain/body region. The integrated circuit structure may also include a raised source/drain/body region coupled to a backside of the first source/drain/body region of the transistor. The transistor is a raised source/drain/body region extending from the backside of the first source/drain/body region toward a backside dielectric layer supporting the isolation layer. The integrated circuit structure may further include a backside metallization coupled to the raised source/drain/body region.

WO 2018/031175 A1

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BACKSIDE SEMICONDUCTOR GROWTH

TECHNICAL FIELD

[0001] The present disclosure generally relates to integrated circuits (ICs). More specifically, the present disclosure relates to a method and apparatus for backside semiconductor growth.

BACKGROUND

[0002] Mobile radio frequency (RF) chip designs (e.g., mobile RF transceivers), including high performance diplexers have migrated to a deep sub-micron process node due to cost and power consumption considerations. The design of such mobile RF transceivers becomes complex at this deep sub-micron process node. The design complexity of these mobile RF transceivers is further complicated by added circuit functions to support communication enhancements, such as carrier aggregation. Further design challenges for mobile RF transceivers include analog/RF performance considerations, including mismatch, noise and other performance considerations. The design of these mobile RF transceivers includes the use of additional passive devices, for example, to suppress resonance, and/or to perform filtering, bypassing and coupling.

[0003] The design of these mobile RF transceivers may include the use of silicon on insulator (SOI) technology. SOI technology replaces conventional silicon substrates with a layered silicon–insulator–silicon substrate to reduce parasitic device capacitance and improve performance. SOI-based devices differ from conventional, silicon-built devices because the silicon junction is above an electrical isolator, typically a buried oxide (BOX) layer. A reduced thickness BOX layer, however, may not sufficiently reduce the parasitic capacitance caused by the proximity of an active device on the silicon layer and a substrate supporting the BOX layer.

[0004] The active devices on the SOI layer may include complementary metal oxide semiconductor (CMOS) transistors. Unfortunately, successful fabrication of transistors using SOI technology may involve the use of raised source/drain regions. Conventionally, a raised source/drain is specified to enable contact between the raised source/drain region and subsequent metallization layers. In addition, a raised

source/drain region provides a channel for carriers to travel. As a result, conventional transistors having raised source/drain regions generally suffer from the raised source/drain region problem. The source/drain region problem is characterized by unwanted, parasitic capacitance in the form of fringe capacitance and overlap capacitance between a gate and the source/drain regions of a transistor.

SUMMARY

[0005] An integrated circuit structure may include a transistor on a front-side semiconductor layer supported by an isolation layer. The transistor includes a first source/drain/body region. The integrated circuit structure may also include a raised source/drain/body region coupled to a backside of the first source/drain/body region of the transistor. The raised source/drain/body region may extend from the backside of the first source/drain/body region toward a backside dielectric layer supporting the isolation layer. The integrated circuit structure may further include a backside metallization coupled to the raised source/drain/body region.

[0006] A method of constructing an integrated circuit structure may include fabricating a transistor using a front-side semiconductor layer supported by an isolation layer. The transistor includes a first source/drain/body region. The method may also include exposing a backside of the first source/drain/body region. The method may further include fabricating a raised source/drain/body region coupled to the backside of the first source/drain/body region of the transistor. The raised source/drain/body region may extend from the backside of the first source/drain/body region toward a first backside dielectric layer supporting the isolation layer. The method may also include fabricating a backside metallization coupled to the raised source/drain/body region.

[0007] An integrated circuit structure may include a transistor on a front-side semiconductor layer supported by an isolation layer. The transistor includes a first source/drain/body region. The integrated circuit structure may also include a means for extending a backside of the first source/drain/body region of the transistor from the isolation layer toward a backside dielectric layer supporting the isolation layer. The integrated circuit structure may further include a backside metallization coupled to the backside of first source/drain/body region through the extending means.

[0008] A radio frequency (RF) front end module may include an integrated RF circuit structure. The integrated RF circuit structure may include a switch transistor on a front-side semiconductor layer supported by an isolation layer. The switch transistor includes a first source/drain/body region and a raised source/drain/body region coupled to a backside of the first source/drain/body region of the switch transistor. The raised source/drain/body region extends from the backside of the first source/drain/body region toward a backside dielectric layer supporting the isolation layer. The switch transistor also includes a backside metallization coupled to the raised source/drain/body region. The RF front end module may further include an antenna coupled to an output of the switch transistor.

[0009] This has outlined, rather broadly, the features and technical advantages of the present disclosure in order that the detailed description that follows may be better understood. Additional features and advantages of the disclosure will be described below. It should be appreciated by those skilled in the art that this disclosure may be readily utilized as a basis for modifying or designing other structures for carrying out the same purposes of the present disclosure. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the teachings of the disclosure as set forth in the appended claims. The novel features, which are believed to be characteristic of the disclosure, both as to its organization and method of operation, together with further objects and advantages, will be better understood from the following description when considered in connection with the accompanying figures. It is to be expressly understood, however, that each of the figures is provided for the purpose of illustration and description only and is not intended as a definition of the limits of the present disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] For a more complete understanding of the present disclosure, reference is now made to the following description taken in conjunction with the accompanying drawings.

[0011] FIGURE 1A is a schematic diagram of a radio frequency (RF) front end (RFFE) module employing a diplexer according to an aspect of the present disclosure.

[0012] FIGURE 1B is a schematic diagram of a radio frequency (RF) front end (RFFE) module employing diplexers for a chipset to provide carrier aggregation according to aspects of the present disclosure.

[0013] FIGURE 2A is a diagram of a diplexer design according to an aspect of the present disclosure.

[0014] FIGURE 2B is a diagram of a radio frequency (RF) front end module according to an aspect of the present disclosure.

[0015] FIGURES 3A to 3E show cross-sectional views of an integrated radio frequency (RF) circuit structure during a layer transfer process according to aspects of the present disclosure.

[0016] FIGURE 4 is a cross-sectional view of an integrated radio frequency (RF) circuit structure fabricated using a layer transfer process according to aspects of the present disclosure.

[0017] FIGURES 5A and 5B illustrate integrated circuit structures, in which a post-layer transfer process forms backside raised source/drain regions of an active device according to aspects of the present disclosure.

[0018] FIGURES 6A to 6E are cross-sectional views illustrating a process for fabricating an integrated circuit structure, including backside raised source/drain regions according to aspects of the present disclosure.

[0019] FIGURES 7A to 7E are cross-sectional views illustrating a process for fabricating an integrated circuit structure, including backside extended source/drain/body regions according to aspects of the present disclosure.

[0020] FIGURES 8A to 8E are cross-sectional views illustrating a process for self-alignment between the source/drain/body regions of an active device and the backside extended source/drain/body regions of the active device according to aspects of the present disclosure.

[0021] FIGURE 9 is a process flow diagram illustrating a method of constructing an integrated circuit structure including an active device having backside extended source/drain/body regions according to an aspect of the present disclosure.

[0022] FIGURE 10 is a block diagram showing an exemplary wireless communication system in which a configuration of the disclosure may be advantageously employed.

[0023] FIGURE 11 is a block diagram illustrating a design workstation used for circuit, layout, and logic design of a semiconductor component according to one configuration.

DETAILED DESCRIPTION

[0024] The detailed description set forth below, in connection with the appended drawings, is intended as a description of various configurations and is not intended to represent the only configurations in which the concepts described herein may be practiced. The detailed description includes specific details for the purpose of providing a thorough understanding of the various concepts. It will be apparent to those skilled in the art, however, that these concepts may be practiced without these specific details. In some instances, well-known structures and components are shown in block diagram form in order to avoid obscuring such concepts. As described herein, the use of the term "and/or" is intended to represent an "inclusive OR", and the use of the term "or" is intended to represent an "exclusive OR".

[0025] Mobile radio frequency (RF) chip designs (e.g., mobile RF transceivers) have migrated to a deep sub-micron process node due to cost and power consumption considerations. The design complexity of mobile RF transceivers is further complicated by added circuit functions to support communication enhancements, such as carrier aggregation. Further design challenges for mobile RF transceivers include analog/RF performance considerations, including mismatch, noise and other performance considerations. The design of these mobile RF transceivers includes the use of passive devices, for example, to suppress resonance, and/or to perform filtering, bypassing and coupling.

[0026] Successful fabrication of modern semiconductor chip products involves interplay between the materials and the processes employed. In particular, the formation of conductive material plating for semiconductor fabrication in back-end-of-line (BEOL) processes is an increasingly challenging part of the process flow. This is particularly true in terms of maintaining a small feature size. The same challenge of maintaining a small feature size also applies to passive on glass (POG) technology, where high performance components such as inductors and capacitors are built upon a highly insulative substrate that may also have a very low loss to support mobile RF transceiver design.

[0027] The design of these mobile RF transceivers may include the use of silicon on insulator (SOI) technology. SOI technology replaces conventional silicon substrates with layered silicon–insulator–silicon substrates to reduce parasitic device capacitance and improve performance. SOI-based devices differ from conventional, silicon-built devices because the silicon junction is above an electrical isolator, typically a buried oxide (BOX) layer, in which a thickness of the BOX layer may be reduced. A reduced thickness BOX layer, however, may not sufficiently reduce the parasitic capacitance caused by the proximity of an active device on the silicon layer and a substrate supporting the BOX layer. In addition, the active devices on an SOI layer may include complementary metal oxide semiconductor (CMOS) transistor.

[0028] Unfortunately, successful fabrication of transistors using SOI technology may involve the use of raised source/drain regions. Conventionally, a raised source/drain enables contact between the raised source/drain region and subsequent metallization layers. In addition, a raised source/drain region provides a channel for carriers to travel. Conventional transistors with raised source/drain regions generally suffer from the raised source/drain region problem. The raised source/drain region problem is characterized by unwanted, parasitic capacitance in the form of fringe capacitance and overlap capacitance between a gate and the source/drain regions. In addition, conventional CMOS technology is limited to epitaxial growth on the front-side of the active devices. As a result, aspects of the present disclosure include a post-layer transfer process to enable backside semiconductor deposition/growth to eliminate the raised source/drain region problem.

[0029] Various aspects of the disclosure provide techniques for integrated circuit structures including transistors having backside extended (raised) source/drain/body regions. The process flow for semiconductor fabrication of the integrated circuit structure may include front-end-of-line (FEOL) processes, middle-of-line (MOL) (also referred to as middle end of line (MEOL)) processes, and back-end-of-line (BEOL) processes. The front-end-of-line processes may include the set of process steps that form the active devices, such as transistors, capacitors, diodes. The FEOL processes include ion implantation, anneals, oxidation, chemical vapor deposition (CVD) or atomic layer deposition (ALD), etching, chemical mechanical polishing (CMP), epitaxy. The middle-of-line processes may include the set of process steps that enable connection of the transistors to BEOL interconnect. These steps include silicidation and contact formation as well as stress introduction. The back-end-of-line processes may include the set of process steps that form the interconnect that ties the independent transistors and form circuits. Currently, copper and aluminum provide the interconnects, but with further development of the technology other conductive material may be used.

[0030] It will be understood that the term "layer" includes film and is not to be construed as indicating a vertical or horizontal thickness unless otherwise stated. As described herein, the term "substrate" may refer to a substrate of a diced wafer or may refer to a substrate of a wafer that is not diced. Similarly, the terms chip and die may be used interchangeably unless such interchanging would tax credulity.

[0031] Aspects of the present disclosure describe integrated circuit structures including transistors having backside raised source/drain/body regions that may be used as antenna switch transistors in integrated radio frequency (RF) circuit structures for high quality (Q)-factor RF applications. In one configuration, a post layer-transfer process forms the backside raised source/drain/body regions of a transistor. The post-layer transfer process may form a backside semiconductor layer on a backside of the source/drain regions of a transistor. The backside semiconductor layer may extend from a first surface to a second surface of an isolation layer, in which the first surface of the isolation layer supports the transistor.

[0032] In this configuration, the post-layer transfer process may include a post-layer deposition process or a post-layer growth process for forming the backside semiconductor layers on the backside of the source/drain regions of the transistor. The raised source/drain/body region is composed of an epitaxially grown, backside semiconductor material. Alternatively, the raised source/drain region may be formed using chemical vapor deposition (CVD), atomic layer deposition (ALD), or other like front-end-of-line fabrication process. In this configuration, the backside raised source/drain regions of the transistor may reduce the parasitic capacitance associated with front-side raised source/drain regions fabricated using conventional CMOS processes. That is, extension of the source/drain regions into a backside of the transistor helps prevent the formation of parasitic capacitance between the body of the transistor and conventional front-side raised source/drain regions.

[0033] One goal driving the wireless communication industry is providing consumers with increased bandwidth. The use of carrier aggregation in current generation communications provides one possible solution for achieving this goal. Carrier aggregation enables a wireless carrier, having licenses to two frequency bands (e.g., 700 MHz and 2 GHz) in a particular geographic area, to maximize bandwidth by simultaneously using both frequencies for a single communication stream. While an increased amount of data is provided to the end user, carrier aggregation implementation is complicated by noise created at the harmonic frequencies due to the frequencies used for data transmission. For example, 700 MHz transmissions may create harmonics at 2.1 GHz, which interfere with data broadcast at 2 GHz frequencies.

[0034] For wireless communication, passive devices are used to process signals in a carrier aggregation system. In carrier aggregation systems, signals are communicated with both high band and low band frequencies. In a chipset, a passive device (e.g., a diplexer) is usually inserted between an antenna and a tuner (or a radio frequency (RF) switch) to ensure high performance. Usually, a diplexer design includes inductors and capacitors. Diplexers can attain high performance by using inductors and capacitors that have a high quality (Q)-factor. High performance diplexers can also be attained by reducing the electromagnetic coupling between components, which may be achieved through an arrangement of the geometry and direction of the components.

[0035] FIGURE 1A is a schematic diagram of a radio frequency (RF) front end (RFFE) module 100 employing a diplexer 200 according to an aspect of the present disclosure. The RF front end module 100 includes power amplifiers 102, duplexer/filters 104, and a radio frequency (RF) switch module 106. The power amplifiers 102 amplify signal(s) to a certain power level for transmission. The duplexer/filters 104 filter the input/output signals according to a variety of different parameters, including frequency, insertion loss, rejection or other like parameters. In addition, the RF switch module 106 may select certain portions of the input signals to pass on to the rest of the RF front end module 100.

[0036] The RF front end module 100 also includes tuner circuitry 112 (e.g., first tuner circuitry 112A and second tuner circuitry 112B), the diplexer 200, a capacitor 116, an inductor 118, a ground terminal 115 and an antenna 114. The tuner circuitry 112 (e.g., the first tuner circuitry 112A and the second tuner circuitry 112B) includes components such as a tuner, a portable data entry terminal (PDET), and a house keeping analog to digital converter (HKADC). The tuner circuitry 112 may perform impedance tuning (e.g., a voltage standing wave ratio (VSWR) optimization) for the antenna 114. The RF front end module 100 also includes a passive combiner 108 coupled to a wireless transceiver (WTR) 120. The passive combiner 108 combines the detected power from the first tuner circuitry 112A and the second tuner circuitry 112B. The wireless transceiver 120 processes the information from the passive combiner 108 and provides this information to a modem 130 (e.g., a mobile station modem (MSM)). The modem 130 provides a digital signal to an application processor (AP) 140.

[0037] As shown in FIGURE 1A, the diplexer 200 is between the tuner component of the tuner circuitry 112 and the capacitor 116, the inductor 118, and the antenna 114. The diplexer 200 may be placed between the antenna 114 and the tuner circuitry 112 to provide high system performance from the RF front end module 100 to a chipset including the wireless transceiver 120, the modem 130 and the application processor 140. The diplexer 200 also performs frequency domain multiplexing on both high band frequencies and low band frequencies. After the diplexer 200 performs its frequency multiplexing functions on the input signals, the output of the diplexer 200 is fed to an optional LC (inductor/capacitor) network including the capacitor 116 and the inductor 118. The LC network may provide extra impedance matching components for the

antenna 114, when desired. Then a signal with the particular frequency is transmitted or received by the antenna 114. Although a single capacitor and inductor are shown, multiple components are also contemplated.

[0038] FIGURE 1B is a schematic diagram of a wireless local area network (WLAN) (e.g., WiFi) module 170 including a first diplexer 200-1 and an RF front end module 150 including a second diplexer 200-2 for a chipset 160 to provide carrier aggregation according to an aspect of the present disclosure. The WiFi module 170 includes the first diplexer 200-1 communicably coupling an antenna 192 to a wireless local area network module (e.g., WLAN module 172). The RF front end module 150 includes the second diplexer 200-2 communicably coupling an antenna 194 to the wireless transceiver (WTR) 120 through a duplexer 180. The wireless transceiver 120 and the WLAN module 172 of the WiFi module 170 are coupled to a modem (MSM, e.g., baseband modem) 130 that is powered by a power supply 152 through a power management integrated circuit (PMIC) 156. The chipset 160 also includes capacitors 162 and 164, as well as an inductor(s) 166 to provide signal integrity. The PMIC 156, the modem 130, the wireless transceiver 120, and the WLAN module 172 each include capacitors (e.g., 158, 132, 122, and 174) and operate according to a clock 154. The geometry and arrangement of the various inductor and capacitor components in the chipset 160 may reduce the electromagnetic coupling between the components.

[0039] FIGURE 2A is a diagram of a diplexer 200 according to an aspect of the present disclosure. The diplexer 200 includes a high band (HB) input port 212, a low band (LB) input port 214, and an antenna 216. A high band path of the diplexer 200 includes a high band antenna switch 210-1. A low band path of the diplexer 200 includes a low band antenna switch 210-2. A wireless device including an RF front end module may use the antenna switches 210 and the diplexer 200 to enable a wide range band for an RF input and an RF output of the wireless device. In addition, the antenna 216 may be a multiple input, multiple output (MIMO) antenna. Multiple input, multiple output antennas will be widely used for the RF front end of wireless devices to support features such as carrier aggregation.

[0040] FIGURE 2B is a diagram of an RF front end module 250 according to an aspect of the present disclosure. The RF front end module 250 includes the antenna

switch (ASW) 210 and diplexer 200 (or triplexer) to enable the wide range band noted in FIGURE 2A. In addition, the RF front end module 250 includes filters 230, an RF switch 220 and power amplifiers 218 supported by a substrate 202. The filters 230 may include various LC filters, having inductors (L) and capacitors (C) arranged along the substrate 202 for forming a diplexer, a triplexer, low pass filters, balun filters, and/or notch filters to prevent high order harmonics in the RF front end module 250. The diplexer 200 may be implemented as a surface mount device (SMD) on a system board 201 (e.g., printed circuit board (PCB) or package substrate). Alternatively, the diplexer 200 may be implemented on the substrate 202.

[0041] In this configuration, the RF front end module 250 is implemented using silicon on insulator (SOI) technology, which helps reduce high order harmonics in the RF front end module 250. SOI technology replaces conventional silicon substrates with a layered silicon-insulator-silicon substrate to reduce parasitic device capacitance and improve performance. SOI-based devices differ from conventional silicon-built devices because the silicon junction is above an electrical insulator, typically a buried oxide (BOX) layer. A reduced thickness BOX layer, however, may not sufficiently reduce the parasitic capacitance caused by the proximity between an active device (on the silicon layer) and a substrate supporting the BOX layer. As a result, aspects of the present disclosure include a layer transfer process to further separate the active device from the substrate, as shown in FIGURES 3A to 3E.

[0042] FIGURES 3A to 3E show cross-sectional views of an integrated radio frequency (RF) circuit structure 300 during a layer transfer process according to aspects of the present disclosure. As shown in FIGURE 3A, an RF silicon on insulator (SOI) device includes an active device 310 on a buried oxide (BOX) layer 320 supported by a sacrificial substrate 301 (e.g., a bulk wafer). The RF SOI device also includes interconnects 350 coupled to the active device 310 within a first dielectric layer 306. As shown in FIGURE 3B, a handle substrate 302 is bonded to the first dielectric layer 306 of the RF SOI device. In addition, the sacrificial substrate 301 is removed. Removal of the sacrificial substrate 301 using the layer transfer process enables high-performance, low-parasitic RF devices by increasing the dielectric thickness. That is, a parasitic capacitance of the RF SOI device is proportional to the dielectric thickness, which determines the distance between the active device 310 and the handle substrate 302.

[0043] As shown in FIGURE 3C, the RF SOI device is flipped once the handle substrate 302 is secured and the sacrificial substrate 301 is removed. As shown in FIGURE 3D, a post layer transfer metallization process is performed using, for example, a regular complementary metal oxide semiconductor (CMOS) process. As shown in FIGURE 3E, an integrated RF circuit structure 300 is completed by depositing a passivation layer, opening bond pads, depositing a redistribution layer, and forming conductive bumps/pillars to enable bonding of the integrated RF circuit structure 300 to a system board (e.g., a printed circuit board (PCB)).

[0044] Referring again to FIGURE 3A, the RF SOI device may include a trap rich layer between the sacrificial substrate 301 and the BOX layer 320. In addition, the sacrificial substrate 301 may be replaced with the handle substrate, and a thickness of the BOX layer 320 may be increased to improve harmonics. Although this arrangement of the RF SOI device may provide improved harmonics relative to a pure silicon or SOI implementation, the RF SOI device is limited by the non-linear responses from the handle substrate, especially when a silicon handle substrate is used. That is, in FIGURE 3A, the increased thickness of the BOX layer 320 does not provide sufficient distance between the active device 310 and the sacrificial substrate 301 relative to the configurations shown in FIGURES 3B to 3E. Moreover, a body of the active device 310 in the RF SOI device may not be tied.

[0045] FIGURE 4 is a cross-sectional view of an integrated RF circuit structure 400 fabricated using a layer transfer process according to aspects of the present disclosure. Representatively, the integrated RF circuit structure 400 includes an active device 410 having a gate, a body, and source/drain regions formed on an isolation layer 420. In silicon on insulator (SOI) implementations, the isolation layer 420 is a buried oxide (BOX) layer, and the body and source/drain regions are formed from an SOI layer including shallow trench isolation (STI) regions supported by the BOX layer.

[0046] The integrated RF circuit structure 400 also includes middle-end-of-line (MEOL)/back-end-of-line (BEOL) interconnects coupled to the source/drain regions of the active device 410. As described herein, the MEOL/BEOL layers are referred to as front-side layers. By contrast, the layers supporting the isolation layer 420 may be referred to herein as backside layers. According to this nomenclature, a front-side

interconnect 450 is coupled to the source/drain regions of the active device 410 through front-side contact 412, and arranged in a front-side dielectric layer 406. In addition, a handle substrate 402 is directly coupled to the front-side dielectric layer 406. In this configuration, a backside dielectric 440 is adjacent to and possibly supports the isolation layer 420. In addition, a backside metallization 430 is coupled to the front-side interconnect 450.

[0047] As shown in FIGURE 4, a layer transfer process provides increased separation between the active device 410 and the handle substrate 402 to improve the harmonics of the integrated RF circuit structure 400. While the layer transfer process enables high-performance, low-parasitic RF devices, the integrated RF circuit structure 400 may suffer from the floating body effect. Accordingly, the performance of the integrated RF circuit structure 400 may be further improved by using a post transfer metallization to provide access to a backside of the active device 410 to tie the body region of the active device 410.

[0048] Various aspects of the disclosure provide techniques for a post layer transfer deposition/growth process on a backside of active devices of an integrated radio frequency (RF) integrated structure. By contrast, access to active devices, formed during a front-end-of-line (FEOL) process, is conventionally provided during middle-end-of-line (MEOL) processing that provides contacts between the gates and source/drain regions of the active devices and back-end-of-line (BEOL) interconnect layers (e.g., M1, M2, etc.). Aspects of the present disclosure involve a post layer transfer growth/deposition process for forming backside extended (raised) source/drain/body regions of transistors that may be used as antenna switch transistors in integrated radio frequency (RF) circuit structures for high quality (Q)-factor RF applications. Other applications include an active device in a low power amplifier module, a low noise amplifier, and an antenna diversity switch.

[0049] FIGURE 5A is a cross-sectional view of an integrated circuit structure 500, in which a post-layer transfer process is performed on a backside of source/drain (S/D) regions of an active device (e.g., a transistor) according to aspects of the present disclosure. Representatively, the integrated circuit structure 500 includes an active device 510 having a gate, a body, and source/drain (S/D) regions formed on an isolation

layer 520. The isolation layer 520 may be a buried oxide (BOX) layer for silicon on insulator (SOI) implementation, in which the body and source/drain regions are formed from an SOI layer. In this configuration, shallow trench isolation (STI) regions are also supported by the BOX layer.

[0050] The integrated RF circuit structure 500 includes a front-side metallization 570 (e.g., a first BEOL interconnect (M1)) arranged in a front-side dielectric layer 506. The front-side metallization is coupled to a third portion 550-3 of a backside metallization 550 through a via 560, in which the backside metallization 550 is arranged in a backside dielectric layer 540. In addition, the gate of the active device 510 includes a gate contact 512, which may be composed of a front-side silicide layer. In addition, a handle substrate 502 is coupled to the front-side dielectric layer 506. The backside dielectric layer 540 is adjacent to and possibly supports the isolation layer 520. In this configuration, a post layer transfer metallization process forms the backside metallization 550.

[0051] In aspects of the present disclosure, a post layer transfer process is used to provide a backside semiconductor layer on a backside of the source/drain regions of the active device 510. In aspects of the present disclosure, the backside semiconductor layer may be deposited as an amorphous semiconductor layer. Alternatively, the backside semiconductor layer may be epitaxially grown as part of a post layer transfer growth process. Once formed, the backside semiconductor layer may be optionally subjected to a post deposition anneal process (e.g., a low temperature or a short local, laser anneal) to form raised source/drain (S/D) regions 530. In this configuration, the backside raised source/drain regions 530 extend from a backside of the source/drain regions of the active device 510 into the isolation layer 520. Once formed, a backside contact 532 (e.g., a backside silicide layer) may be deposited on the backside raised source/drain regions 530 distal from a front-side of the source/drain regions. A post-layer transfer metallization process is then performed to couple a first portion 550-1 and a second portion 550-2 of the backside metallization 550 to the backside contacts 532 of the backside raised source/drain regions 530 of the active device 510. As shown in FIGURE 5A, the front-side metallization 570 is arranged distal from the backside metallization 550.

[0052] FIGURE 5B is a cross-sectional view of an integrated circuit structure 580, in which a post-layer transfer process is also performed on a backside of a source/drain (S/D) region 516 of an active device 510 (e.g., a transistor) according to aspects of the present disclosure. As will be recognized, a configuration of the integrated circuit structure 580 is similar to the configuration of the integrated circuit structure 500 of FIGURE 5A. In the configuration shown in FIGURE 5B, however, the active device 510 includes only one of the backside raised source/drain regions 530. Instead, a backside contact 582 is directly on a backside of the source/drain region 516 of the active device 510. In addition, the second portion 550-2 of the backside metallization 550 is coupled to the backside contact 582 of the source/drain region 516 of the active device 510.

[0053] Referring again to FIGURE 5A, the backside raised source/drain regions 530 are provided in the isolation layer 520 and arranged to enable contact with the backside metallization 550. The extension of the source/drain regions of the active device 510 helps prevent the formation of parasitic capacitance between the body of the active device 510 and conventional front-side raised source/drain regions. In this configuration, the post-layer transfer process may include a post-layer deposition process or a post-layer growth process for forming the backside raised source/drain regions 530. In this configuration, the backside raised source/drain regions 530 may reduce the parasitic capacitance associated with raised source/drain regions fabricated using conventional CMOS processes.

[0054] According to aspects of the present disclosure, the handle substrate 502 may be composed of a semiconductor material, such as silicon. In this configuration, the handle substrate 502 may include at least one other active device. Alternatively, the handle substrate 502 may be a passive substrate to further improve harmonics by reducing parasitic capacitance. In this configuration, the handle substrate 502 may include at least one other passive device. As described herein, the term “passive substrate” may refer to a substrate of a diced wafer or panel, or may refer to the substrate of a wafer/panel that is not diced. In one configuration, the passive substrate is comprised of glass, air, quartz, sapphire, high-resistivity silicon, or other like passive material. The passive substrate may also be a coreless substrate.

[0055] FIGURES 6A to 6E are cross-sectional views illustrating a process for fabrication of an integrated circuit structure, including backside extended source/drain regions, according to aspects of the present disclosure. As shown in FIGURE 6A, an integrated circuit structure 600 is shown in a configuration similar to the configuration of the integrated circuit structure 500 shown in FIGURE 5A. In the configuration shown in FIGURE 6A, however, a layer transfer process is performed to bond the handle substrate 502 to the front-side dielectric layer 506 following formation of the active devices 510 (510-1, and 510-2). As shown in FIGURE 6B, a post-layer transfer process begins with the deposition of a backside dielectric layer 540. Although a single layer is shown, it should be recognized that multiple dielectric layers may be deposited.

[0056] As shown in FIGURE 6C, the post-layer transfer process continues with patterning and etching of the backside dielectric layer 540 and the isolation layer 520 to expose a backside of the source/drain regions of the active devices 510. In FIGURE 6D, a post-layer transfer deposition/growth process is performed to fabricate the backside raised source/drain regions 530. In FIGURE 6E, a post-layer transfer metallization process is performed to couple the backside metallization 550 to the backside raised source/drain regions 530 through the backside contacts 532. In addition, a fifth portion 550-5 of the backside metallization 550 is coupled to the front-side metallization 570 through the via 560. In this configuration, a third portion 550-3 of the backside metallization 550 is coupled to the backside contact 532 of one of the backside raised source/drain regions 530, and a fourth portion 550-4 of the backside metallization 550 is coupled to the backside contact 532 of one of the backside raised source/drain regions 530 of a second active device 510-2.

[0057] Different materials can be used in the growth process to stress the active devices. For example, PFET devices can be stressed with Germanium growth, up to 40% in one configuration. NMOS devices can be stressed using, for example, carbon-doped silicon, with the percentage of carbon being no more than 3% to four percent. This percentage of carbon prevents dislocations in the silicon. It should be recognized that a raised body region can also include stressors.

[0058] FIGURES 7A to 7E are cross-sectional views illustrating a process for fabrication of an integrated circuit structure, including backside extended

source/drain/body regions according to aspects of the present disclosure. As shown in FIGURE 7A, an integrated circuit structure 700 is shown in a configuration similar to the configuration of the integrated circuit structure 500 shown in FIGURE 5A. In the configuration shown in FIGURE 7A, however, a layer transfer process is performed to bond the handle substrate 502 to the front-side dielectric layer 506 following formation of the active devices 510 (510-1, and 510-2). In addition, a first portion 570-1 of the front-side metallization 570 couples a front-side contact 514 of a source/drain region of a first active device 510-1 to a gate contact 512 of a second active device 510-2. Also, a second portion 570-2 of the front-side metallization 570 couples a front-side contact 514 of the source/drain region of the second active device 510-2 to the via 560.

[0059] As shown in FIGURE 7B, the post-layer transfer process also begins with the deposition of the backside dielectric layer 540. As shown in FIGURE 7C, the post-layer transfer process also continues with patterning and etching of the backside dielectric layer 540 and the isolation layer 520 to expose a backside of the source/drain region of the first active device 510-1. In this aspect of the present disclosure, the post layer transfer process exposes a body of the second active device 510-2. In FIGURE 7D, a post-layer transfer deposition/growth process is performed to fabricate a backside raised source/drain region 530 and a backside raised body region 590.

[0060] In FIGURE 7E, a post-layer transfer metallization process is performed to couple the backside metallization 550 to the backside raised source/drain regions 530 through the backside contacts 532. In addition, a fourth portion 550-4 of the backside metallization 550 is coupled to the second portion of front-side metallization 570 through the via 560. In this configuration, a third portion 550-3 of the backside metallization 550 is coupled to a backside contact 592 of the backside raised body region 590. In this aspect of the present disclosure, the backside raised body region 590 is doped with a different dopant than the dopant of the backside raised source/drain regions 530. In addition, the backside raised body region 590 of the first active device 510-1 is doped with a different dopant than the dopant of the backside raised body region 590 of the second active device 510-2.

[0061] FIGURES 8A to 8E are cross-sectional views illustrating a process for self-alignment between the source/drain/body regions of an active device and the backside

extended source/drain/body regions of the active device according to aspects of the present disclosure. As shown in FIGURE 8A, an integrated circuit structure 800 is shown in a configuration similar to the configuration of the integrated circuit structure 700 shown in FIGURE 7A. In the configuration shown in FIGURE 8A, however, the layer transfer process to bond the handle substrate 502 to the front-side dielectric layer 506 following formation of the active devices 510 (510-1, and 510-2) is not shown. In addition, the configuration of the integrated circuit structure shown in FIGURE 8D also includes the first portion 570-1 of the front-side metallization 570 coupling the front-side contact 514 of the source/drain region of the first active device 510-1 to the gate contact 512 of the second active device 510-2. Also, the second portion 570-2 of the front-side metallization 570 couples the front-side contact 514 of the source/drain region of the second active device 510-2 to the via 560.

[0062] As shown in FIGURE 8B, an ion implant process is performed to implant impurities into the backside dielectric layer 540 by implanting ions in the backside dielectric layer 540 and the isolation layer 520. The implanting is performed from a front-side of the integrated circuit structure 800. Specific dopants, e.g., high dose Boron, can be used to damage (create defects in) the buried oxide layer. As shown in FIGURE 8C, the ion implant process is blocked by the gates of the active devices 510. As a result, the implanted defects are generally confined to areas within the backside dielectric layer 540 and the isolation layer that are proximate to the source/drain regions of the active devices 510.

[0063] As shown in FIGURE 8D, a post-layer transfer mask process is performed by depositing a photoresist 594 and exposing the implanted defects within, for example, an under etched semiconductor (e.g., silicon (Si)) layer. As shown in FIGURE 8E, the process continues with etching of the backside dielectric layer 540 and the isolation layer 520 to expose a backside of the source/drain region of the first active device 510-1 and a backside of the source/drain regions of the second active device 510-2. In this aspect of the present disclosure, the implanted defects enable self-alignment between the source/drain/body regions of the active devices 510 and the backside extended source/drain/body regions. That is, the backside etching does not reach the gates. Alternatively, the implanted defects may provide an etch stop layer and reduce an etch rate to support the backside raised source/drain/body regions.

[0064] FIGURE 9 is a process flow diagram illustrating a method 900 of constructing an integrated circuit structure, including an active device having backside extended source/drain/body regions, according to an aspect of the present disclosure. In block 902, a transistor is fabricated using a front-side semiconductor layer supported by an isolation layer. For example, as shown in FIGURE 6A, the active device 310 is fabricated using a front-side semiconductor layer (e.g., a silicon on insulator (SOI) layer) supported by an isolation layer (e.g., a buried oxide (BOX) layer). In the configuration shown in FIGURES 6A to 6E, a front-side metallization is fabricated in a front-side dielectric layer on the active device. For example, as shown in FIGURE 6A, a front-side metallization 570 is coupled to a front-side via 560 that extends through a shallow trench isolation (STI) region and an isolation layer 520. This portion of the process for fabricating the transistor is performed prior to a layer transfer process.

[0065] For example, a layer transfer process is performed, in which a handle substrate 502 is bonded to a front-side dielectric layer 506, as shown in FIGURE 6A. The layer transfer process also includes removal of a sacrificial substrate. As shown in FIGURE 3B, the layer-transfer process includes removal of the sacrificial substrate 301. In this aspect of the present disclosure, fabrication of raised backside source/drain/body regions is performed as part of a post layer-transfer process.

[0066] Referring again to FIGURE 9, in block 904, a backside of a first source/drain/body region of the transistor is exposed. For example, as shown in FIGURE 6B, a post-layer transfer raised source/drain/body formation process may begin with deposition of a backside dielectric layer 540 on the isolation layer 520. As shown in FIGURE 6C, a backside of the source/drain regions of the active devices 510 are exposed. In block 906, a raised source/drain/body region is fabricated. For example, as shown 6D, raised source/drain (S/D) regions are coupled to a backside of the source/drain regions of the active device 510. The raised source/drain regions may extend from the backside of the source/drain regions toward the backside dielectric layer 540 supporting the isolation layer 520. Alternatively, a backside a of second source/drain/body region may be exposed to enable formation of another raised source/drain/body region.

[0067] According to aspects of the present disclosure, the raised source/drain/body regions may be epitaxially grown or fabricated as part of an amorphous deposition process. For example, as shown in FIGURE 6D, an epitaxial growth process may include selectively growing a backside semiconductor layer on an exposed backside of the raised source/drain regions of the active devices 510. This epitaxial growth process also includes subjecting the backside semiconductor layer to an anneal process to form the raised source/drain regions. Once the raised source/drain regions are formed, etching of a surface of the backside dielectric layer 540 and/or the raised source/drain regions of the active devices 510 is performed. By providing backside raised source/drain regions that extend away from a front-side of the integrated circuit structure 500, parasitic capacitance between the transistor gate and conventional raised source/drain regions is avoided.

[0068] According to aspects of the present disclosure, a post-layer transfer growth/deposition process is described for formation of the backside raised source/drain/body regions. The post-layer transfer growth process may involve a pre-clean portion, a growth portion, and a post-deposition anneal. The post-deposition anneal may be a low temperature anneal (e.g., below 350°) or a short-local laser anneal. In addition, the backside raised source/drain/body region may or may not be of a single crystal structure. For example, the backside raised source/drain/body region may be formed by a fully amorphous deposition followed by solid phase epitaxy anneal to form a single crystal structure. Alternatively, in cases when a mono crystalline material is not desired, poly silicon, a silicon alloy, or other like semiconductor compound can be deposited to provide the backside semiconductor layer.

[0069] When an epitaxial growth process is used to form the backside semiconductor layer, a low temperature epitaxial growth may be performed using trisilane. Trisilane may permit the growth of a backside semiconductor layer (e.g., silicon) at lower temperatures below 350° C due to a specific growth mechanism for enhancing H (hydrogen) desorption. By contrast, conventional semiconductor layers grown at temperatures lower than 500° C are defective, irrespective of the carrier gas, pressure and precursor flow used. In addition, a thickness of the epitaxially grown backside semiconductor layer may be higher or lower than the surface of a wafer on which the layer is grown.

[0070] In block 908 of FIGURE 9, a backside metallization is fabricated to couple to the raised source/drain regions. As shown in FIGURE 6E, a backside contact 532 is deposited on the backside raised source/drain regions 530. In addition, a second backside dielectric layer 540-2 is deposited on the backside contact 532 and a first backside dielectric layer 540-1. Once deposited, the second backside dielectric layer 540-2 is patterned according to the backside contact 532. The second backside dielectric layer 540-2 is next etched (e.g., a dry plasma etch and clean process) to expose a portion of the backside contact 532. A backside metallization 550 is then deposited on the exposed portion of the backside contact 532 to contact the source/drain regions of the active devices 510.

[0071] According to a further aspect of the present disclosure, an integrated circuit structure including a transistor on a front-side semiconductor layer supported by an isolation layer is described. The transistor includes a first source/drain/body region. The integrated circuit structure may also include a means for extending a backside of the first source/drain/body region of the transistor from the isolation layer toward a backside dielectric layer supporting the isolation layer. The integrated circuit structure may further include a backside metallization coupled to the backside of first source/drain/body region through the extending means. The extending means may be the raised source/drain region, shown in FIGURES 5A and 5B. The extending means may also be the raised body region, shown in FIGURES 7D and 7E. In another aspect, the aforementioned means may be any module or any apparatus configured to perform the functions recited by the aforementioned means.

[0072] Unfortunately, successful fabrication of transistors using silicon on insulator (SOI) technology may involve the use of raised source/drain regions. Conventionally, a raised source/drain enables contact between the raised source/drain region and subsequent metallization layers. In addition, a raised source/drain region provides a channel for carriers to travel. Unfortunately, conventional transistors with raised source/drain regions generally suffer from the raised source/drain region problem. In addition, conventional CMOS technology is limited to epitaxial growth on the front-side of the active devices. As a result, aspects of the present disclosure include a post-layer transfer process to enable backside semiconductor deposition/growth to eliminate the raised source/drain region problem.

[0073] Aspects of the present disclosure describe integrated circuit structures including transistors having backside raised source/drain/body regions that may be used as antenna switch transistors in integrated radio frequency (RF) circuit structures for high quality (Q)-factor RF applications. In one configuration, a post layer-transfer metallization is used to form the backside raised source/drain/body regions of a transistor. The post-layer transfer process may form a backside semiconductor layer on a backside of the source/drain regions of a transistor. The backside semiconductor layer may extend from a first surface to a second surface of an isolation layer, in which a first surface of the isolation layer supports the transistor.

[0074] In this configuration, the post-layer transfer process may include a post-layer deposition process or a post-layer growth process for forming the backside semiconductor layers on the backside of the source/drain regions of the transistor. A subsequent anneal process is applied to the semiconductor layers to form backside raised source/drain regions of the transistor. In this configuration, the backside raised source/drain regions of the transistor may reduce the parasitic capacitance associated with front-side raised source/drain regions fabricated using conventional CMOS processes. That is, extension of the source/drain regions into a backside of the transistor helps prevent the formation of parasitic capacitance between the body of the transistor and conventional front-side raised source/drain regions.

[0075] FIGURE 10 is a block diagram showing an exemplary wireless communication system 1000 in which an aspect of the disclosure may be advantageously employed. For purposes of illustration, FIGURE 10 shows three remote units 1020, 1030, and 1050 and two base stations 1040. It will be recognized that wireless communication systems may have many more remote units and base stations. Remote units 1020, 1030, and 1050 include IC devices 1025A, 1025C, and 1025B that include the disclosed backside semiconductor growth. It will be recognized that other devices may also include the disclosed backside semiconductor growth, such as the base stations, switching devices, and network equipment. FIGURE 10 shows forward link signals 1080 from the base station 1040 to the remote units 1020, 1030, and 1050 and reverse link signals 1090 from the remote units 1020, 1030, and 1050 to base stations 1040.

[0076] In FIGURE 10, remote unit 1020 is shown as a mobile telephone, remote unit 1030 is shown as a portable computer, and remote unit 1050 is shown as a fixed location remote unit in a wireless local loop system. For example, a remote units may be a mobile phone, a hand-held personal communication systems (PCS) unit, a portable data unit such as a personal digital assistant (PDA), a GPS enabled device, a navigation device, a set top box, a music player, a video player, an entertainment unit, a fixed location data unit such as a meter reading equipment, or other communications device that stores or retrieve data or computer instructions, or combinations thereof. Although FIGURE 10 illustrates remote units according to the aspects of the disclosure, the disclosure is not limited to these exemplary illustrated units. Aspects of the disclosure may be suitably employed in many devices, which include the disclosed RF devices.

[0077] FIGURE 11 is a block diagram illustrating a design workstation used for circuit, layout, and logic design of a semiconductor component, such as the RF devices disclosed above. A design workstation 1100 includes a hard disk 1101 containing operating system software, support files, and design software such as Cadence or OrCAD. The design workstation 1100 also includes a display 1102 to facilitate design of a circuit 1110 or a semiconductor component 1112 such as an RF device. A storage medium 1104 is provided for tangibly storing the circuit design 1110 or the semiconductor component 1112. The circuit design 1110 or the semiconductor component 1112 may be stored on the storage medium 1104 in a file format such as GDSII or GERBER. The storage medium 1104 may be a CD-ROM, DVD, hard disk, flash memory, or other appropriate device. Furthermore, the design workstation 1100 includes a drive apparatus 1103 for accepting input from or writing output to the storage medium 1104.

[0078] Data recorded on the storage medium 1104 may specify logic circuit configurations, pattern data for photolithography masks, or mask pattern data for serial write tools such as electron beam lithography. The data may further include logic verification data such as timing diagrams or net circuits associated with logic simulations. Providing data on the storage medium 1104 facilitates the design of the circuit design 1110 or the semiconductor component 1112 by decreasing the number of processes for designing semiconductor wafers.

[0079] For a firmware and/or software implementation, the methodologies may be implemented with modules (e.g., procedures, functions, and so on) that perform the functions described herein. A machine-readable medium tangibly embodying instructions may be used in implementing the methodologies described herein. For example, software codes may be stored in a memory and executed by a processor unit. Memory may be implemented within the processor unit or external to the processor unit. As used herein, the term "memory" refers to types of long term, short term, volatile, nonvolatile, or other memory and is not to be limited to a particular type of memory or number of memories, or type of media upon which memory is stored.

[0080] If implemented in firmware and/or software, the functions may be stored as one or more instructions or code on a computer-readable medium. Examples include computer-readable media encoded with a data structure and computer-readable media encoded with a computer program. Computer-readable media includes physical computer storage media. A storage medium may be an available medium that can be accessed by a computer. By way of example, and not limitation, such computer-readable media can include RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or other medium that can be used to store desired program code in the form of instructions or data structures and that can be accessed by a computer; disk and disc, as used herein, includes compact disc (CD), laser disc, optical disc, digital versatile disc (DVD), floppy disk and Blu-ray disc where disks usually reproduce data magnetically, while discs reproduce data optically with lasers. Combinations of the above should also be included within the scope of computer-readable media.

[0081] In addition to storage on computer readable medium, instructions and/or data may be provided as signals on transmission media included in a communication apparatus. For example, a communication apparatus may include a transceiver having signals indicative of instructions and data. The instructions and data are configured to cause one or more processors to implement the functions outlined in the claims.

[0082] Although the present disclosure and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the technology of the disclosure as defined by the

appended claims. For example, relational terms, such as “above” and “below” are used with respect to a substrate or electronic device. Of course, if the substrate or electronic device is inverted, above becomes below, and vice versa. Additionally, if oriented sideways, above and below may refer to sides of a substrate or electronic device. Moreover, the scope of the present application is not intended to be limited to the particular configurations of the process, machine, manufacture, and composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed that perform substantially the same function or achieve substantially the same result as the corresponding configurations described herein may be utilized according to the present disclosure. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

CLAIMS

What is claimed is:

1. An integrated circuit structure, comprising:

a transistor on a front-side semiconductor layer supported by an isolation layer, the transistor including a first source/drain/body region;

a raised source/drain/body region coupled to a backside of the first source/drain/body region of the transistor, the raised source/drain/body region extending from the backside of the first source/drain/body region toward a backside dielectric layer supporting the isolation layer; and

a backside metallization coupled to the raised source/drain/body region.

2. The integrated circuit structure of claim 1, in which the raised source/drain/body region is comprised of an epitaxially grown, backside semiconductor material.

3. The integrated circuit structure of claim 1, further comprising a front-side metallization coupled to a second source/drain/body region of the transistor, the front-side metallization being distal from the backside metallization.

4. The integrated circuit structure of claim 3, in which the front-side metallization comprises a back-end-of-line (BEOL) interconnect coupled to a front-side contact on the second source/drain/body region of the transistor, the BEOL interconnect within a front-side dielectric layer.

5. The integrated circuit structure of claim 1, in which the transistor comprises a radio frequency (RF) switch.

6. The integrated circuit structure of claim 1, in which the raised source/drain/body region is doped with a dopant different than the dopant of the first source/drain/body region of the transistor.

7. The integrated circuit structure of claim 1, in which the raised source/drain/body region is self-aligned with the first source/drain/body region of the transistor.

8. The integrated circuit structure of claim 1, in which the raised source/drain/body region extends through the isolation layer to the backside dielectric layer.

9. The integrated circuit structure of claim 1, integrated into a radio frequency (RF) front end module, the RF front end module incorporated into at least one of a music player, a video player, an entertainment unit, a navigation device, a communications device, a personal digital assistant (PDA), a fixed location data unit, a mobile phone, and a portable computer.

10. A method of constructing an integrated circuit structure, comprising:

fabricating a transistor using a front-side semiconductor layer supported by an isolation layer, the transistor including a first source/drain/body region;

exposing a backside of the first source/drain/body region;

fabricating a raised source/drain/body region coupled to the backside of the first source/drain/body region of the transistor, the raised source/drain/body region extending from the backside of the first source/drain/body region toward a first backside dielectric layer supporting the isolation layer; and

fabricating a backside metallization coupled to the raised source/drain/body region.

11. The method of claim 10, in which fabricating the raised source/drain/body region comprises:

implanting ions in at least the first backside dielectric layer supporting the isolation layer, in which the implanting is performed from a front-side of the integrated circuit structure;

patterning the first backside dielectric layer according to implanted defects in the first backside dielectric layer, the implanted defects being proximate the backside of the first source/drain/body region of the transistor; and

exposing the backside of the first source/drain/body region of the transistor through the first backside dielectric layer and the isolation layer.

12. The method of claim 10, in which fabricating the raised source/drain/body region comprises selectively growing a backside semiconductor layer on the backside of the first source/drain/body region of the transistor.

13. The method of claim 12, further comprising annealing the backside semiconductor layer to form the raised source/drain/body region.

14. The method of claim 10, further comprising:

depositing a backside silicide on the raised source/drain/body region; and

depositing a second backside dielectric layer on the backside silicide and the first backside dielectric layer.

15. The method of claim 10, in which fabricating the raised source/drain/body region comprises depositing a backside semiconductor layer on an exposed portion of the backside of the first source/drain/body region.

16. The method of claim 10, further comprising integrating the integrated circuit structure into a radio frequency (RF) front end module, the RF front end module incorporated into at least one of a music player, a video player, an entertainment unit, a navigation device, a communications device, a personal digital assistant (PDA), a fixed location data unit, a mobile phone, and a portable computer.

17. An integrated circuit structure, comprising:

a transistor on a front-side semiconductor layer supported by an isolation layer, the transistor including a first source/drain/body region;

means for extending a backside of the first source/drain/body region of the transistor from the isolation layer toward a backside dielectric layer supporting the isolation layer; and

a backside metallization coupled to the backside of first source/drain/body region through the extending means.

18. The integrated circuit structure of claim 17, further comprising a front-side metallization coupled to a second source/drain/body region of the transistor, the front-side metallization being distal from the backside metallization.

19. The integrated circuit structure of claim 18, in which the front-side metallization comprises a back-end-of-line (BEOL) interconnect coupled to a front-side contact on the second source/drain/body region of the transistor, the BEOL interconnect within a front-side dielectric layer.

20. The integrated circuit structure of claim 17, in which the transistor comprises an RF switch.

21. The integrated circuit structure of claim 17, in which the extending means is self-aligned with the first source/drain/body region of the transistor.

22. The integrated circuit structure of claim 17, integrated into a radio frequency (RF) front end module, the RF front end module incorporated into at least one of a music player, a video player, an entertainment unit, a navigation device, a communications device, a personal digital assistant (PDA), a fixed location data unit, a mobile phone, and a portable computer.

23. A radio frequency (RF) front end module, comprising:

an integrated RF circuit structure, comprising a switch transistor on a front-side semiconductor layer supported by an isolation layer, the switch transistor including a first source/drain/body region, a raised source/drain/body region coupled to a backside of the first source/drain/body region of the switch transistor, in which the raised source/drain/body region extends from the backside of the first source/drain/body region toward a backside dielectric layer supporting the isolation layer, and a backside metallization coupled to the raised source/drain/body region; and

an antenna coupled to an output of the switch transistor.

24. The integrated RF circuit structure of claim 23, in which the raised source/drain/body region is comprised of an epitaxially grown, backside semiconductor material.

25. The integrated RF circuit structure of claim 23, in which the raised source/drain/body region is doped with a dopant different than the dopant of the first source/drain/body region of the switch transistor.

26. The integrated RF circuit structure of claim 23, in which the raised source/drain/body region extends through the isolation layer to the backside dielectric layer.

27. The RF front end module of claim 23, incorporated into at least one of a music player, a video player, an entertainment unit, a navigation device, a communications device, a personal digital assistant (PDA), a fixed location data unit, a mobile phone, and a portable computer.

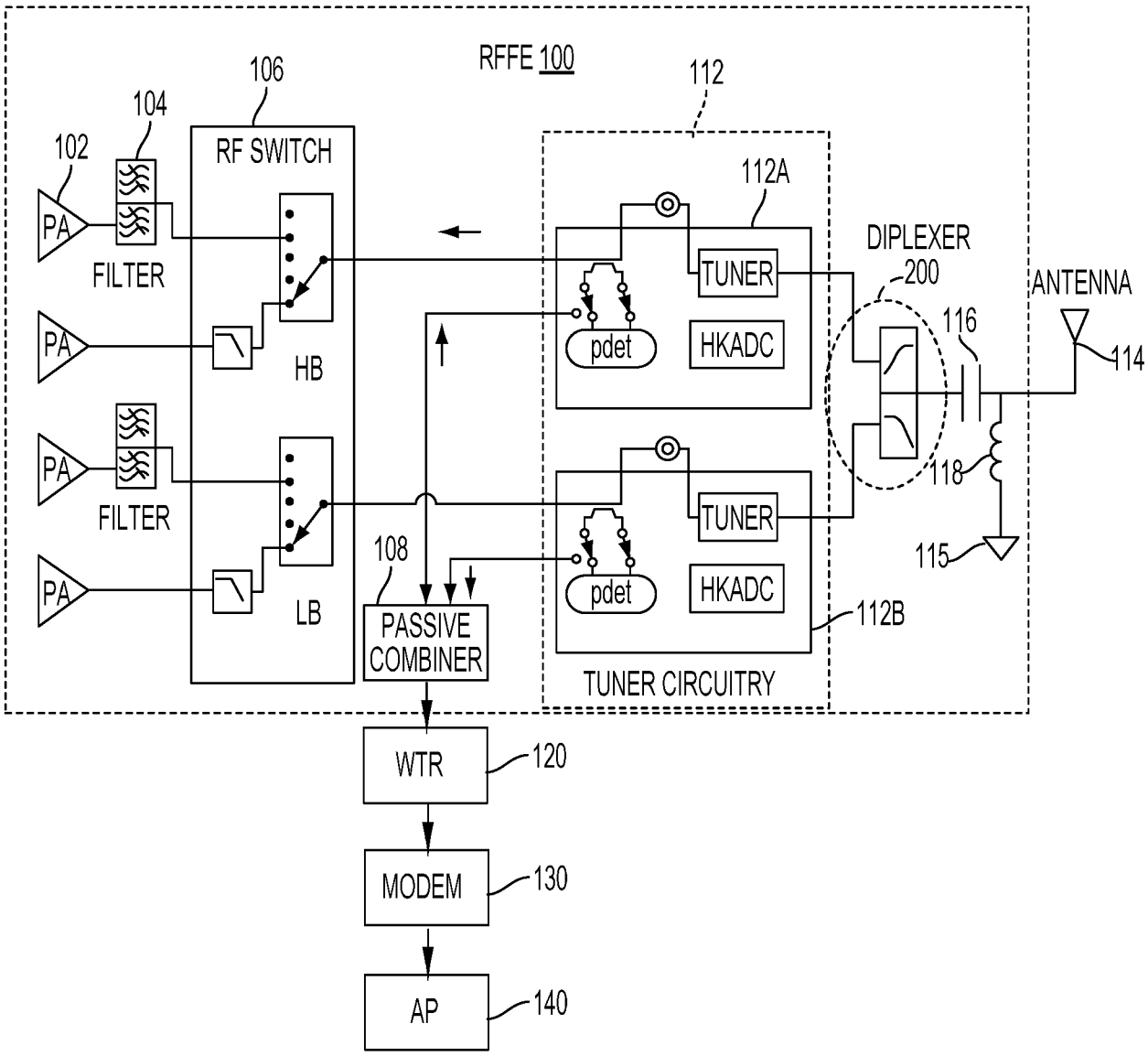
RFFE 100
106
RF SWITCH
104
102
PA
FILTER
PA
HB
PA
FILTER
PA
LB
108
PASSIVE COMBINER
112
112A
TUNER
pdet
HKADC
TUNER
pdet
HKADC
112B
TUNER CIRCUITRY
DIPLEXER
200
116
118
115
ANTENNA
114
WTR
120
MODEM
130
AP
140

FIG. 1A

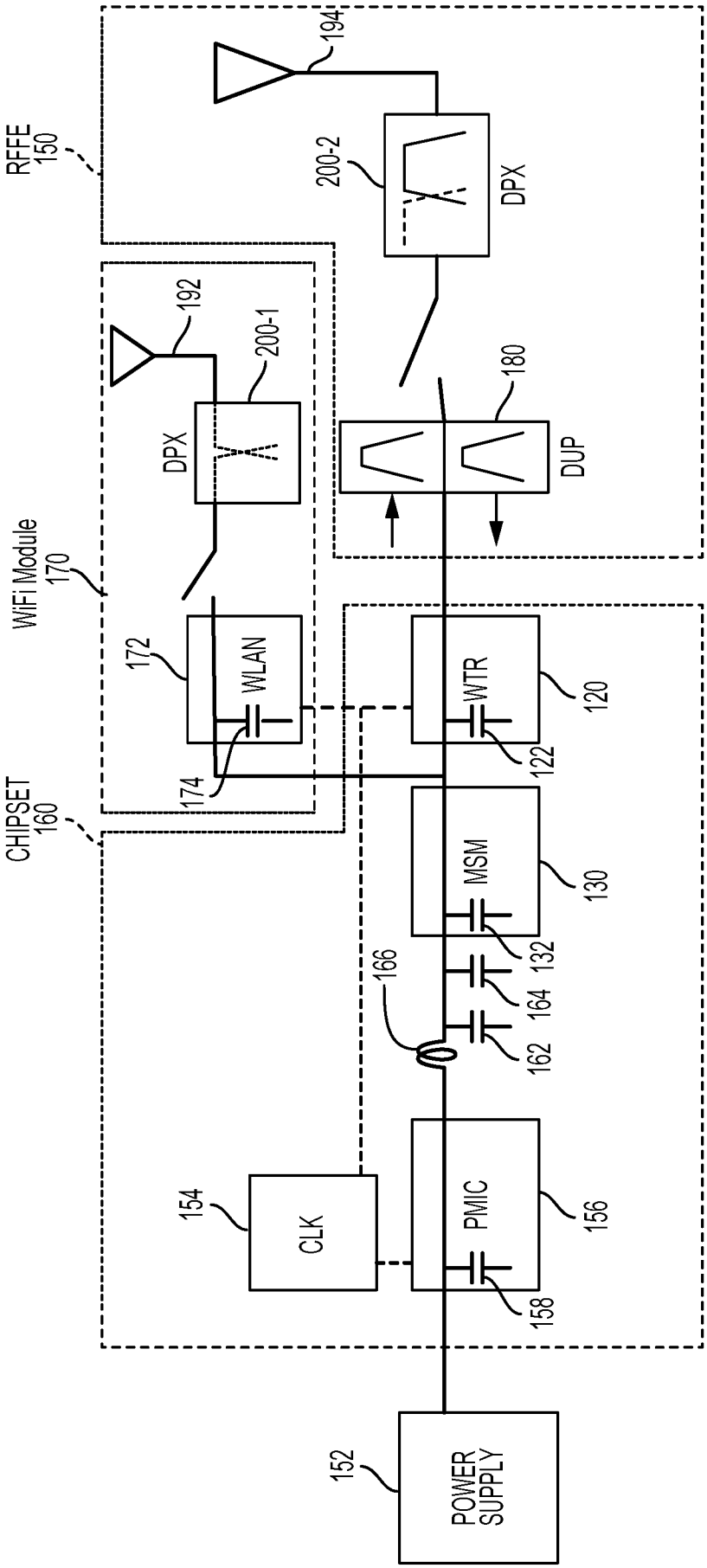
RFFE
150
194
200-2
DPX
180
DUP
192
200-1
DPX
WiFi Module
170
172
WLAN
174
CHIPSET
160
WTR
120
122
MSM
130
132
166
164
162
154
CLK
PMIC
156
158
152
POWER SUPPLY

FIG. 1B

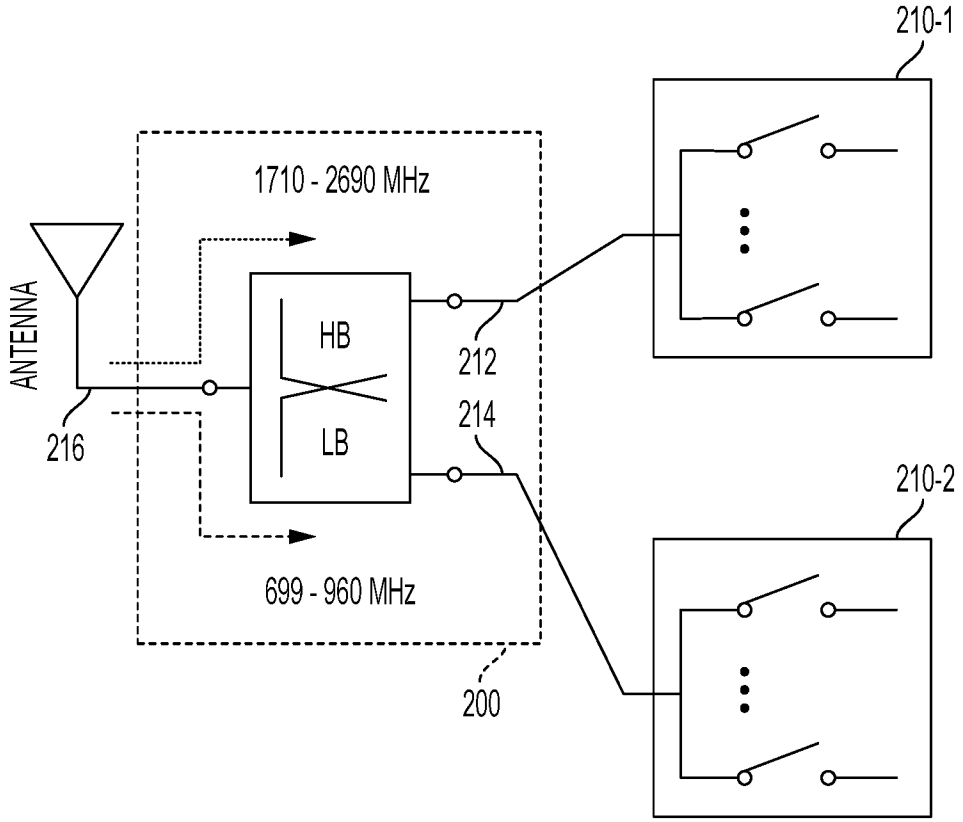
210-1
1710 - 2690 MHz
ANTENNA
HB
LB
212
214
216
210-2
699 - 960 MHz
200

FIG. 2A

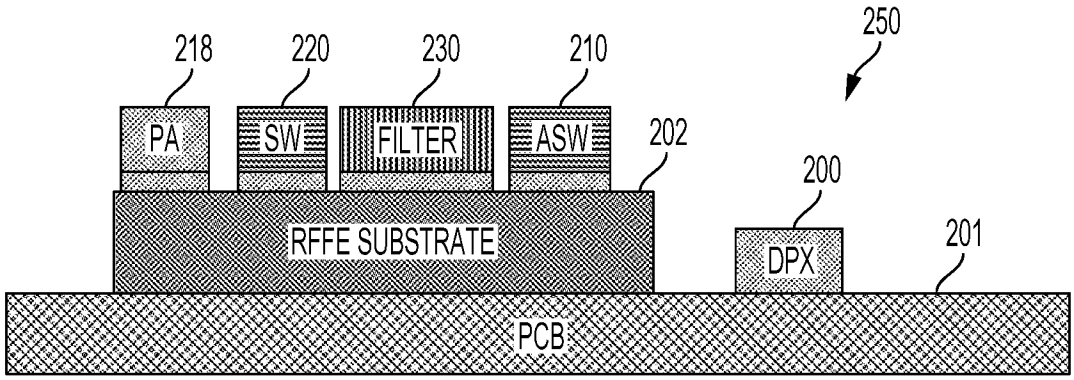
250
218
220
230
210
PA
SW
FILTER
ASW
202
200
RFFE SUBSTRATE
DPX
201
PCB

FIG. 2B

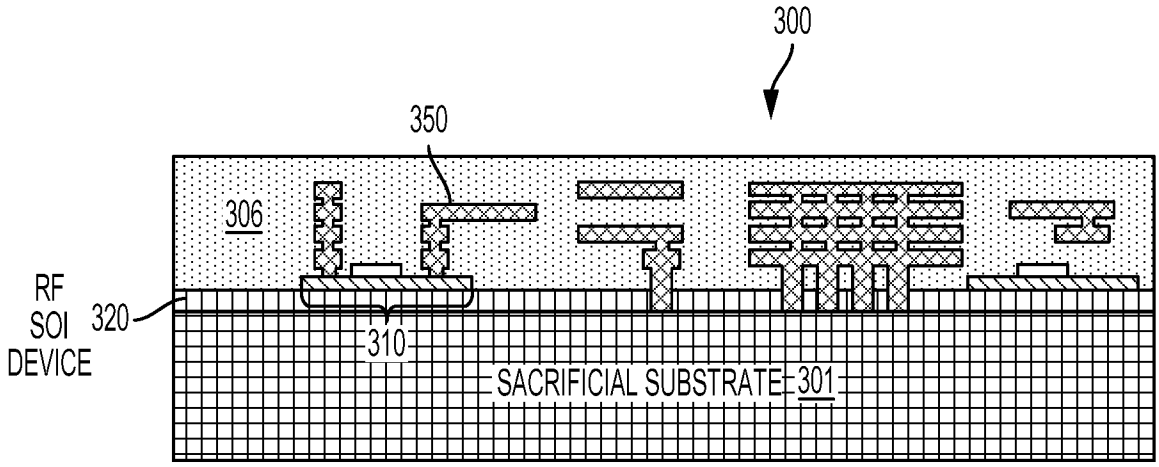

FIG. 3A

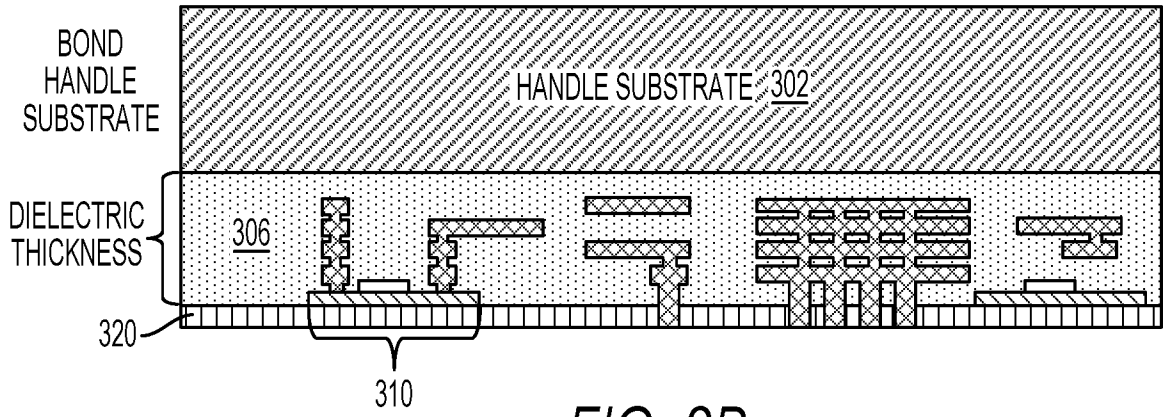

FIG. 3B

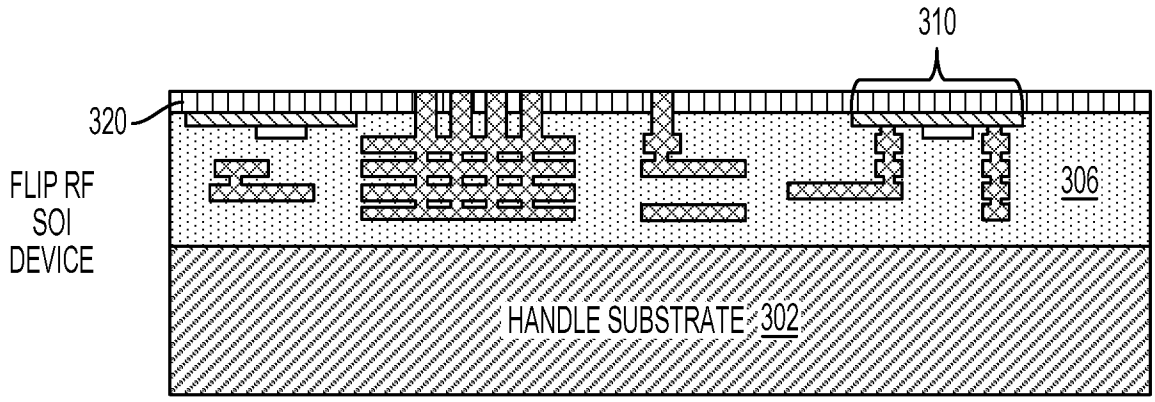

FIG. 3C

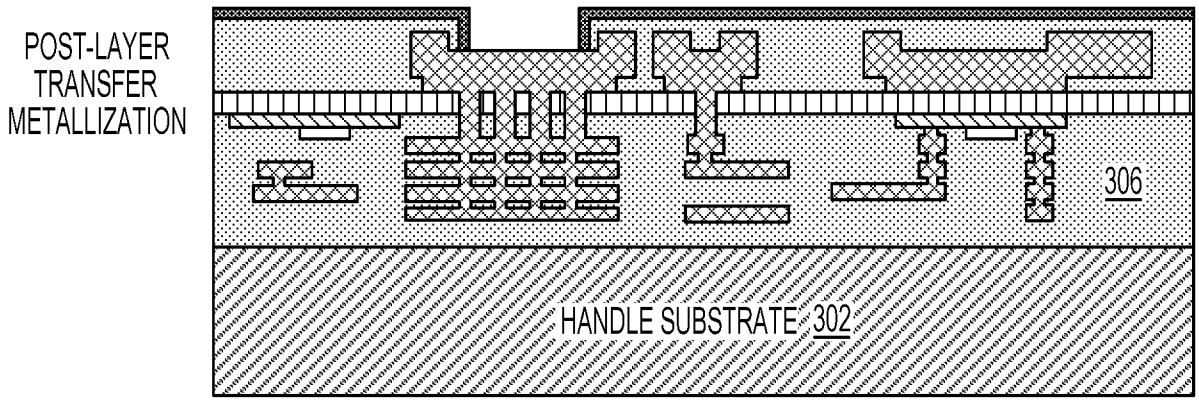
POST-LAYER
TRANSFER
METALLIZATION
306
HANDLE SUBSTRATE 302

FIG. 3D

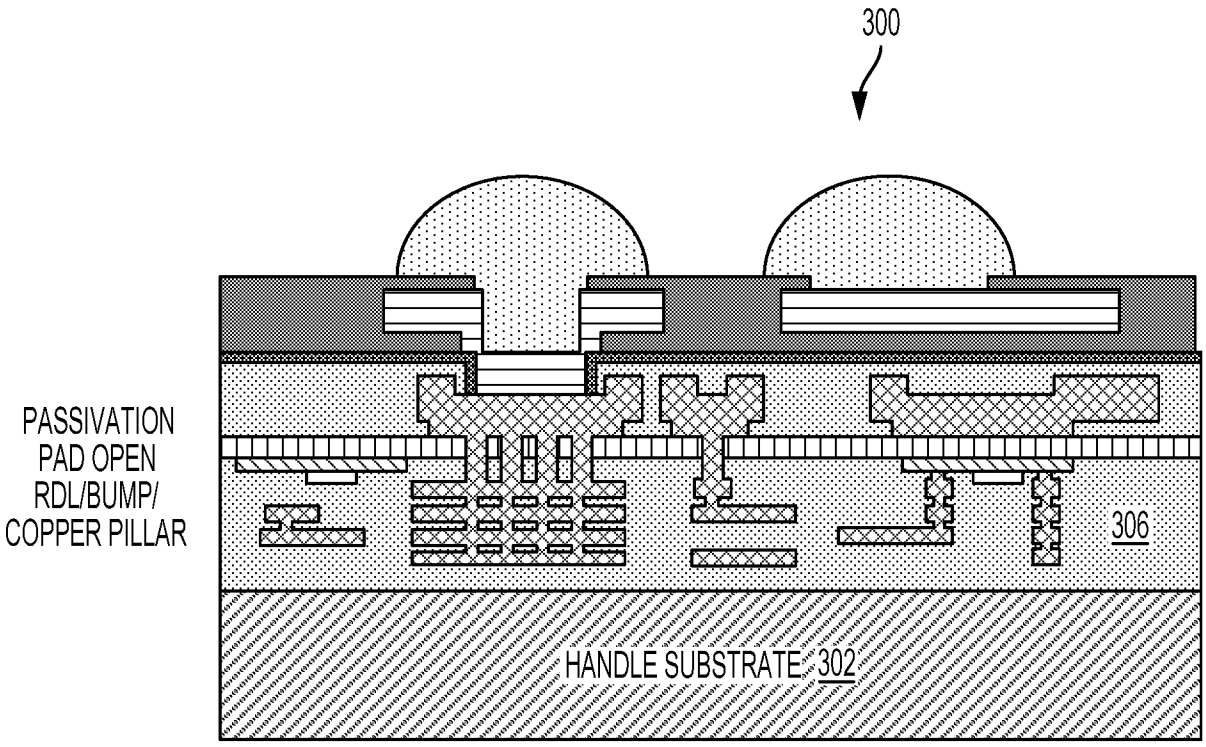
300
PASSIVATION
PAD OPEN
RDL/BUMP/
COPPER PILLAR
306
HANDLE SUBSTRATE 302

FIG. 3E

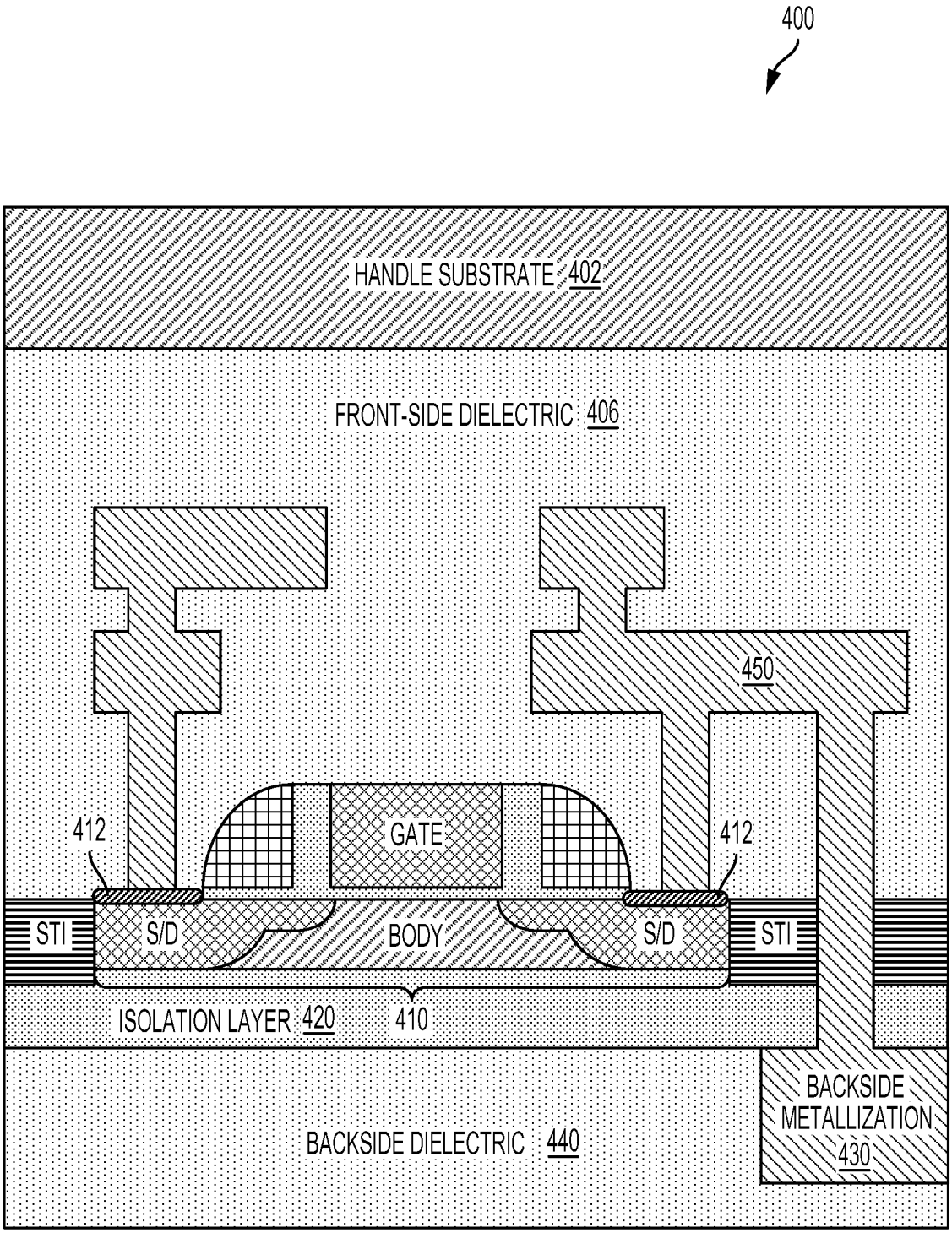
400
HANDLE SUBSTRATE 402
FRONT-SIDE DIELECTRIC 406
450
412
GATE
412
STI
S/D
BODY
S/D
STI
ISOLATION LAYER 420
410
BACKSIDE METALLIZATION 430
BACKSIDE DIELECTRIC 440

FIG. 4

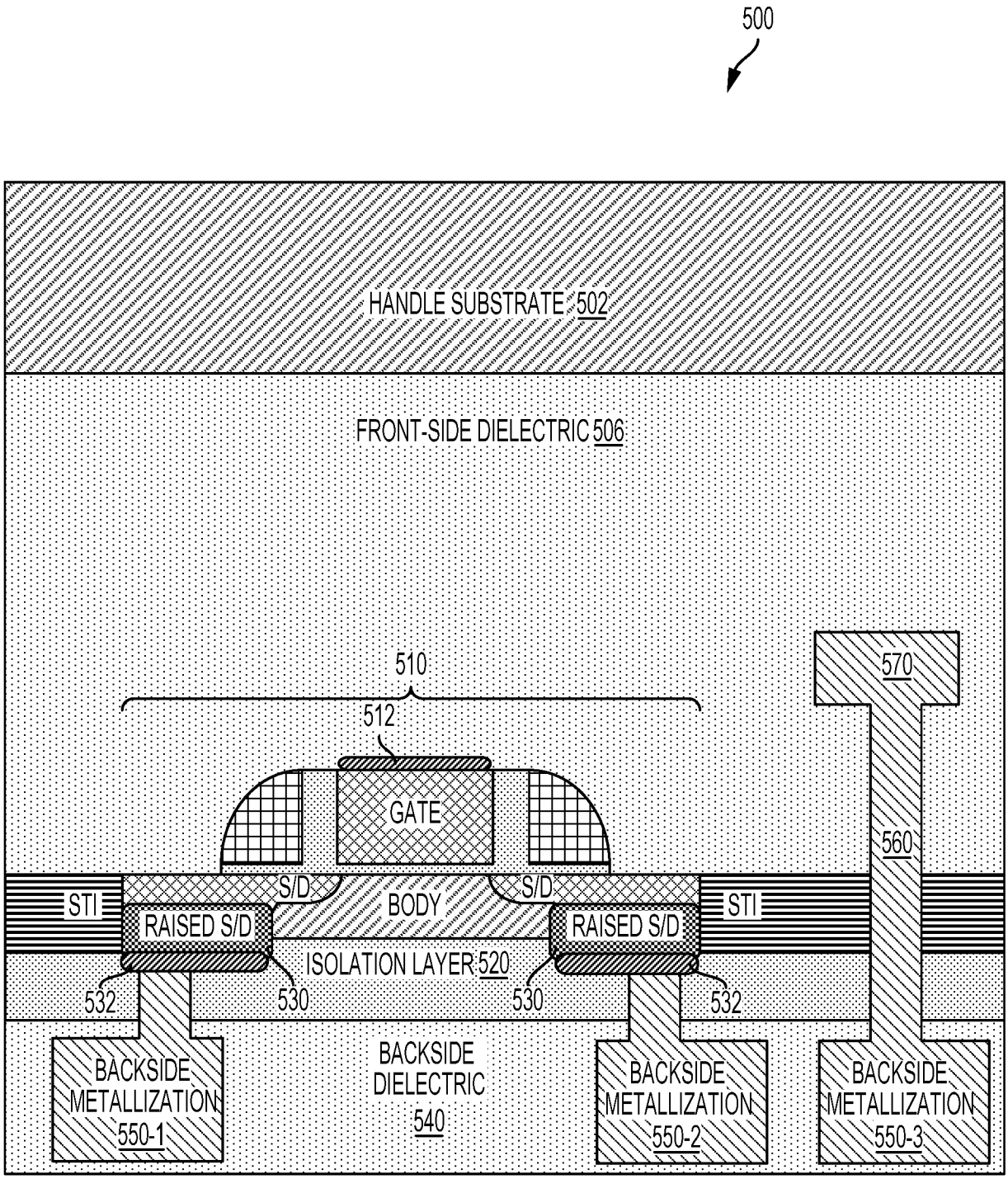
500
HANDLE SUBSTRATE 502
FRONT-SIDE DIELECTRIC 506
510
512
570
GATE
560
S/D
S/D
STI
BODY
STI
RAISED S/D
RAISED S/D
ISOLATION LAYER 520
532
530
530
532
BACKSIDE METALLIZATION 550-1
BACKSIDE DIELECTRIC 540
BACKSIDE METALLIZATION 550-2
BACKSIDE METALLIZATION 550-3

FIG. 5A

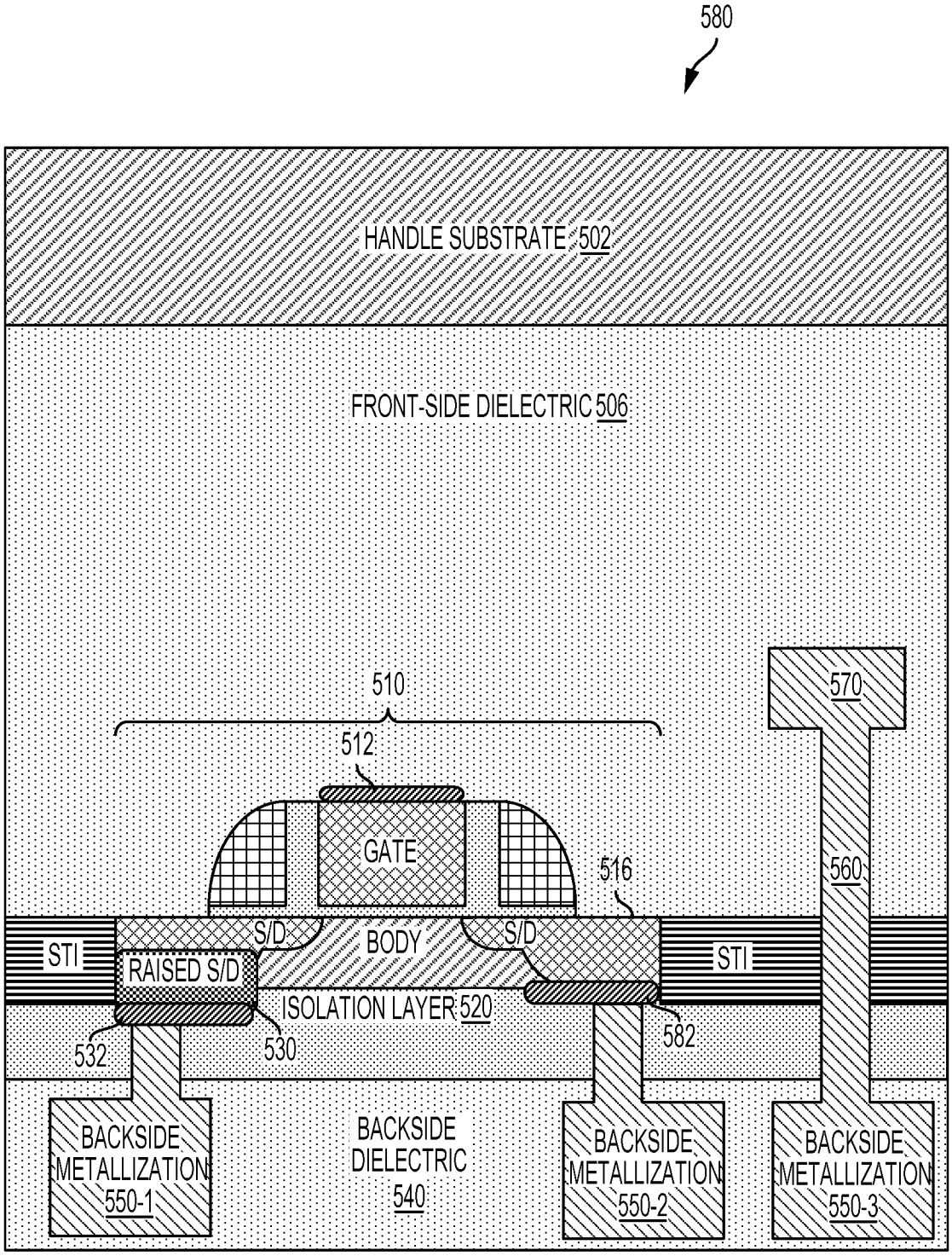
580
HANDLE SUBSTRATE 502
FRONT-SIDE DIELECTRIC 506
510
512
570
GATE
516
560
S/D
BODY
S/D
STI
STI
RAISED S/D
ISOLATION LAYER 520
532
530
582
BACKSIDE METALLIZATION 550-1
BACKSIDE DIELECTRIC 540
BACKSIDE METALLIZATION 550-2
BACKSIDE METALLIZATION 550-3

FIG. 5B

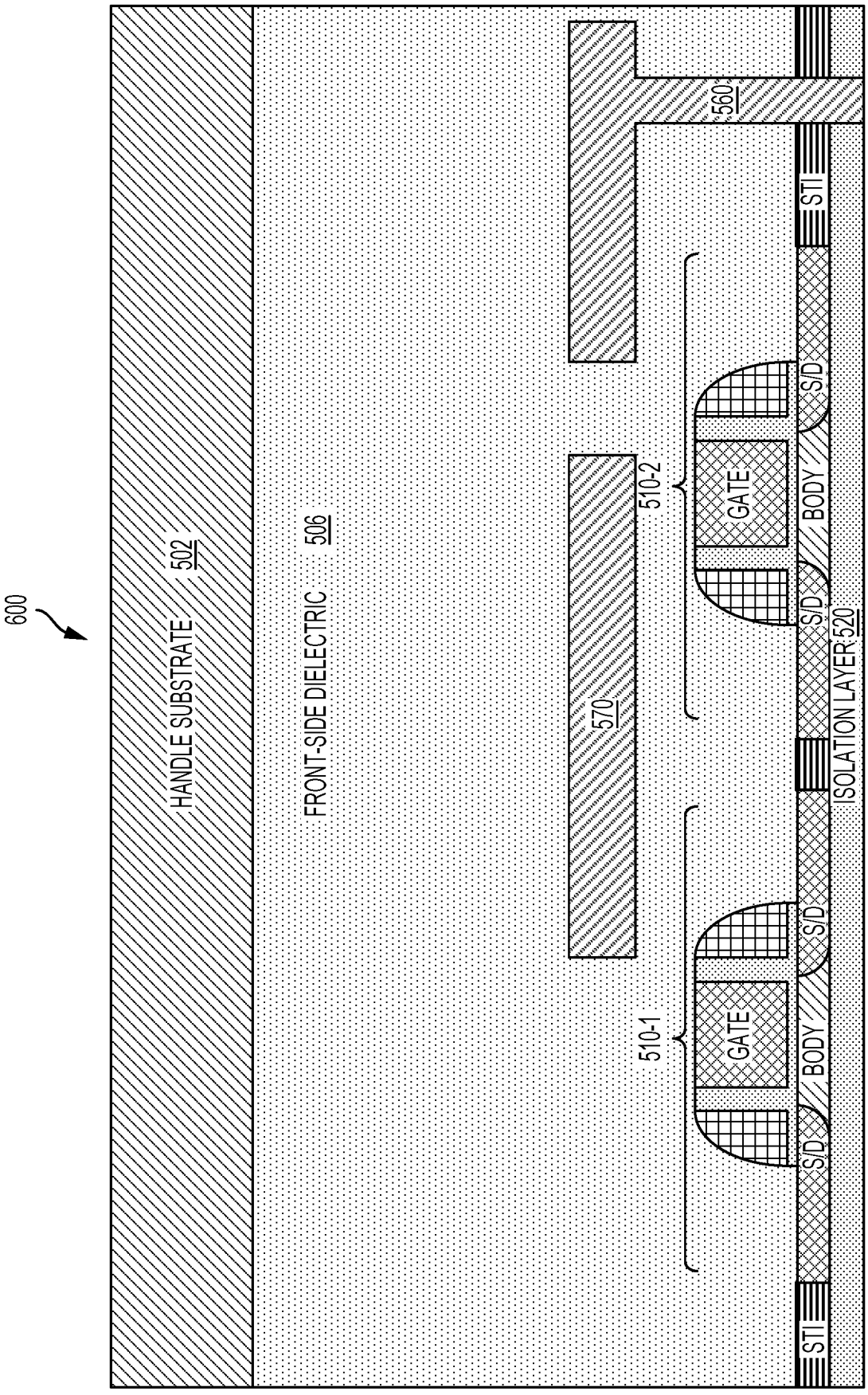
600
HANDLE SUBSTRATE 502
FRONT-SIDE DIELECTRIC 506
560
STI
S/D
BODY
GATE
510-2
570
510-1
ISOLATION LAYER 520

FIG. 6A

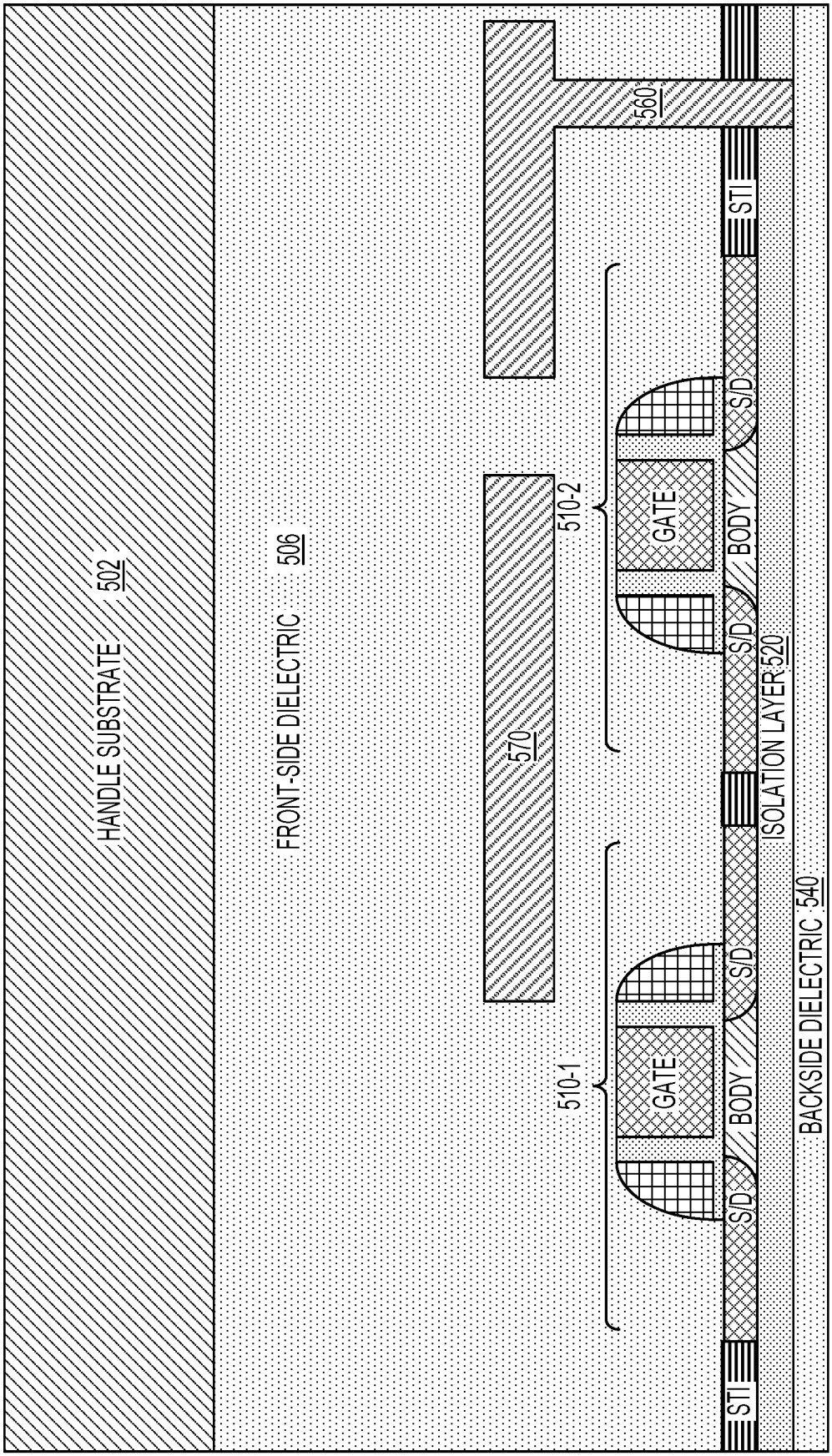
HANDLE SUBSTRATE 502
FRONT-SIDE DIELECTRIC 506
560
570
510-2
510-1
GATE
GATE
S/D
S/D
S/D
S/D
BODY
BODY
STI
STI
ISOLATION LAYER 520
BACKSIDE DIELECTRIC 540

FIG. 6B

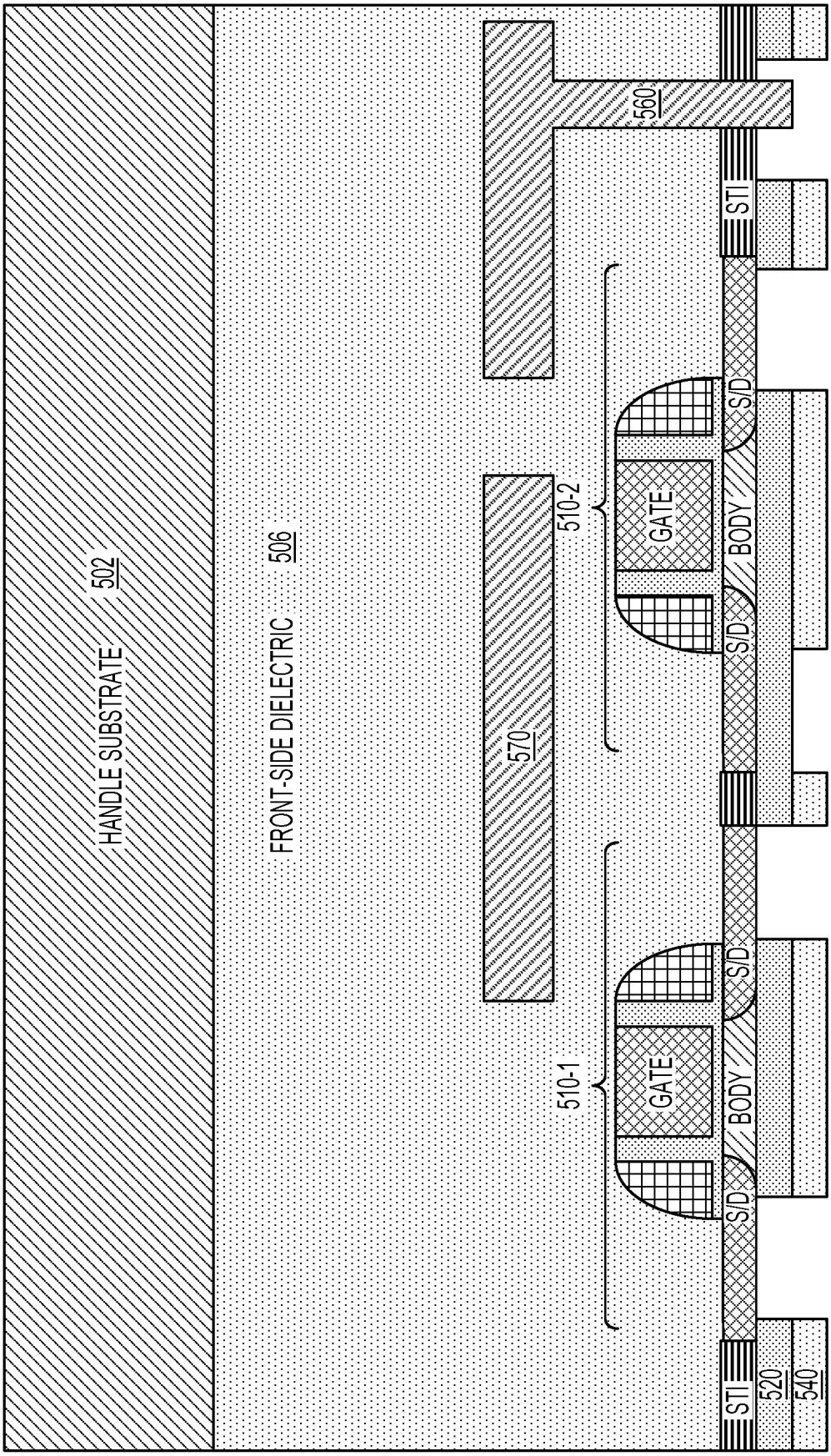
HANDLE SUBSTRATE
502
FRONT-SIDE DIELECTRIC
506
560
570
510-2
510-1
GATE
BODY
S/D
STI
520
540

FIG. 6C

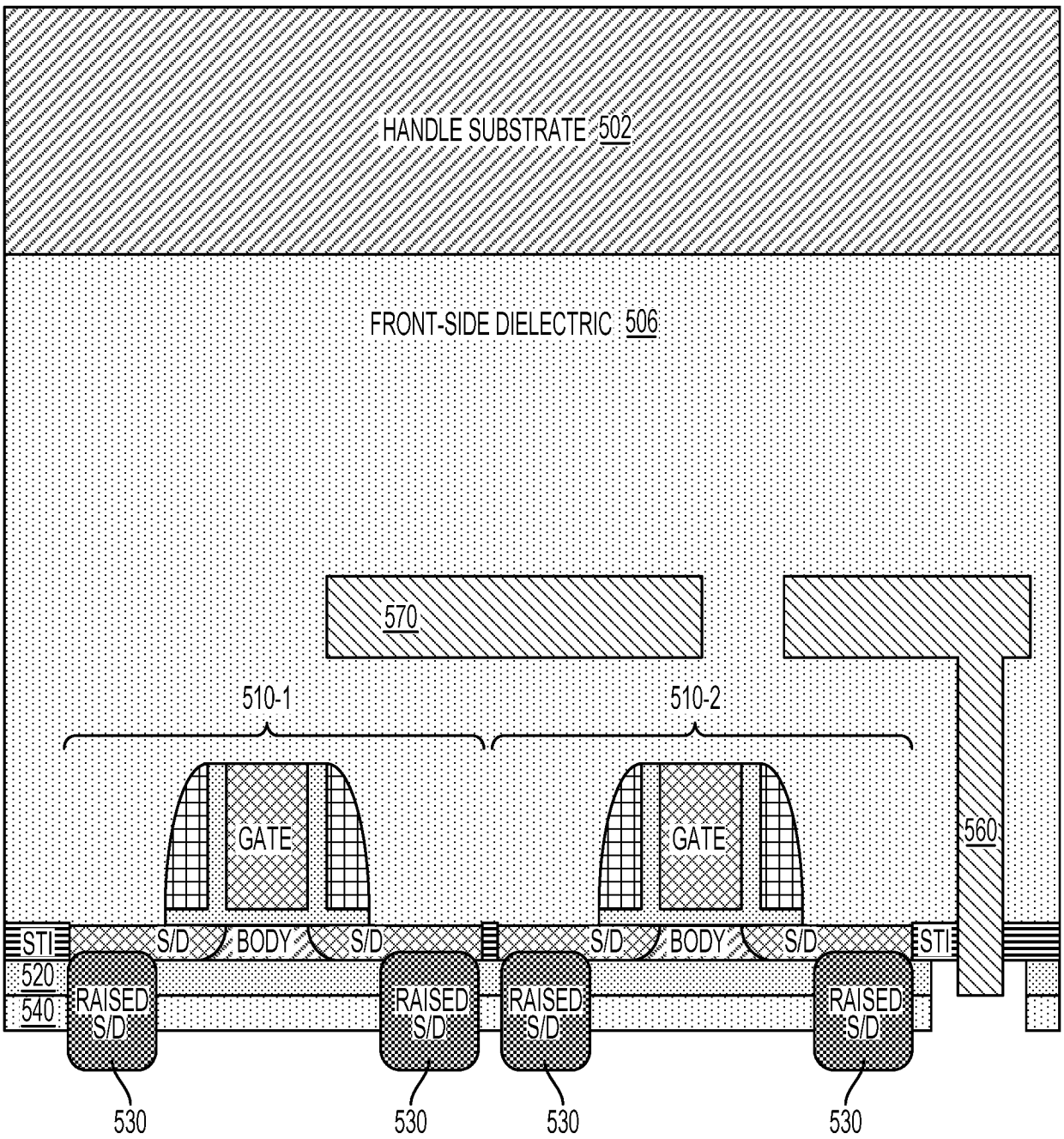
HANDLE SUBSTRATE 502
FRONT-SIDE DIELECTRIC 506
570
510-1
510-2
GATE
GATE
560
STI
S/D
BODY
S/D
S/D
BODY
S/D
STI
520
540
RAISED S/D
RAISED S/D
RAISED S/D
RAISED S/D
530
530
530
530

FIG. 6D

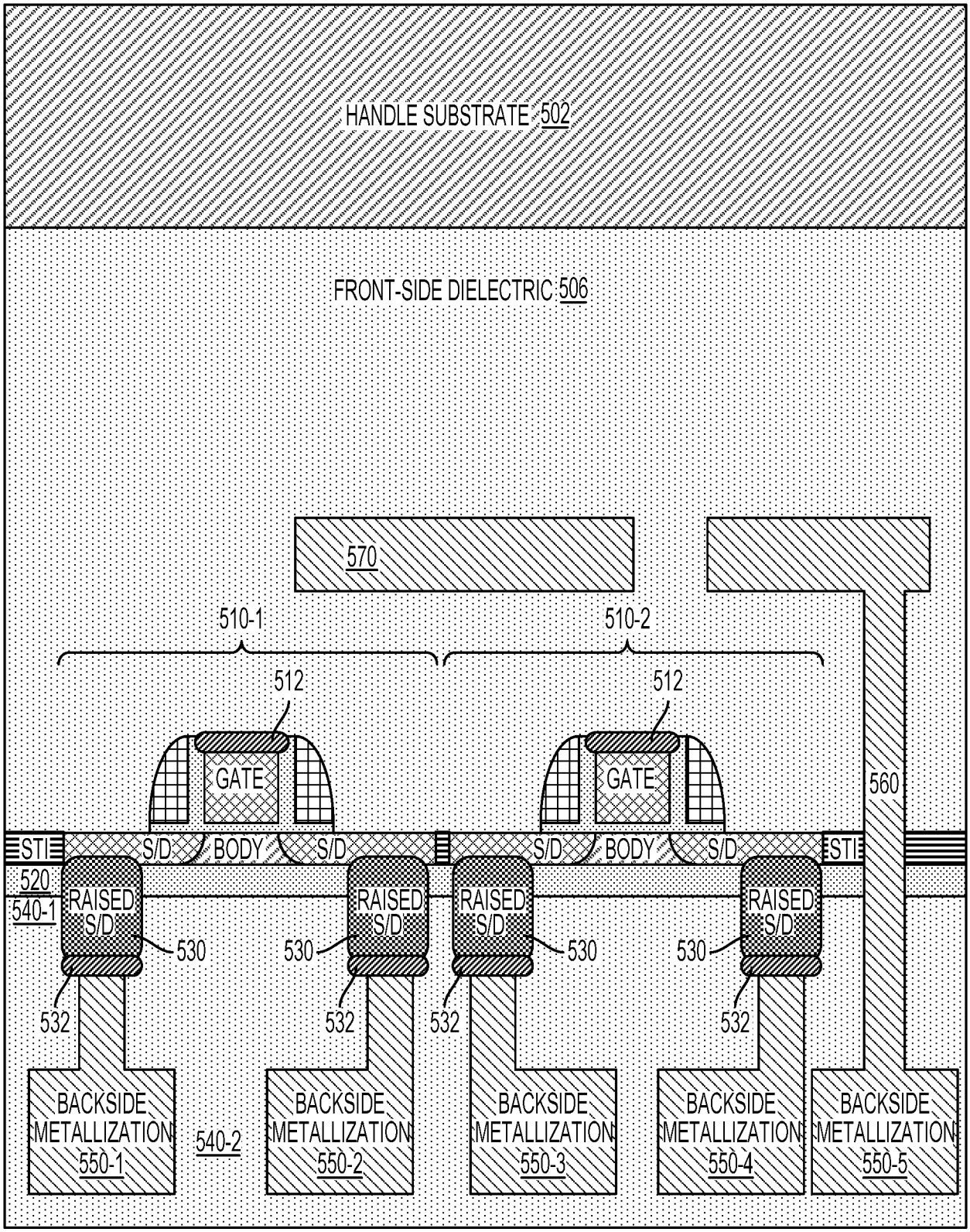
HANDLE SUBSTRATE 502
FRONT-SIDE DIELECTRIC 506
570
510-1
510-2
512
512
GATE
GATE
560
STI
S/D
BODY
S/D
S/D
BODY
S/D
STI
520
540-1
RAISED S/D
RAISED S/D
RAISED S/D
RAISED S/D
530
530
530
530
532
532
532
532
BACKSIDE METALLIZATION 550-1
BACKSIDE METALLIZATION 550-2
BACKSIDE METALLIZATION 550-3
BACKSIDE METALLIZATION 550-4
BACKSIDE METALLIZATION 550-5
540-2

FIG. 6E

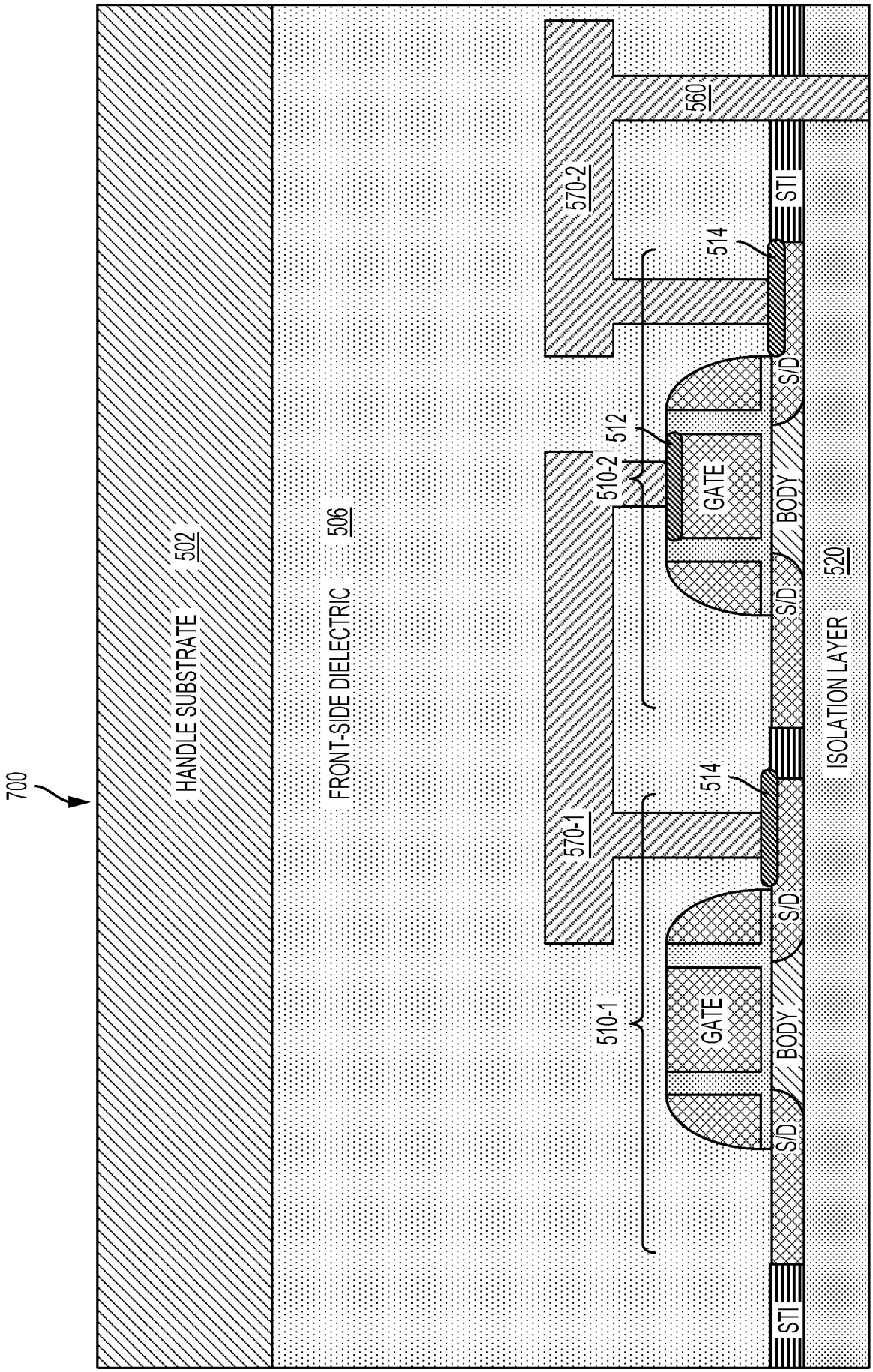
700
HANDLE SUBSTRATE 502
FRONT-SIDE DIELECTRIC 506
560
570-2
514
STI
S/D
512
510-2
GATE
BODY
S/D
S/D
ISOLATION LAYER 520
514
570-1
510-1
GATE
BODY
S/D
S/D
STI

FIG. 7A

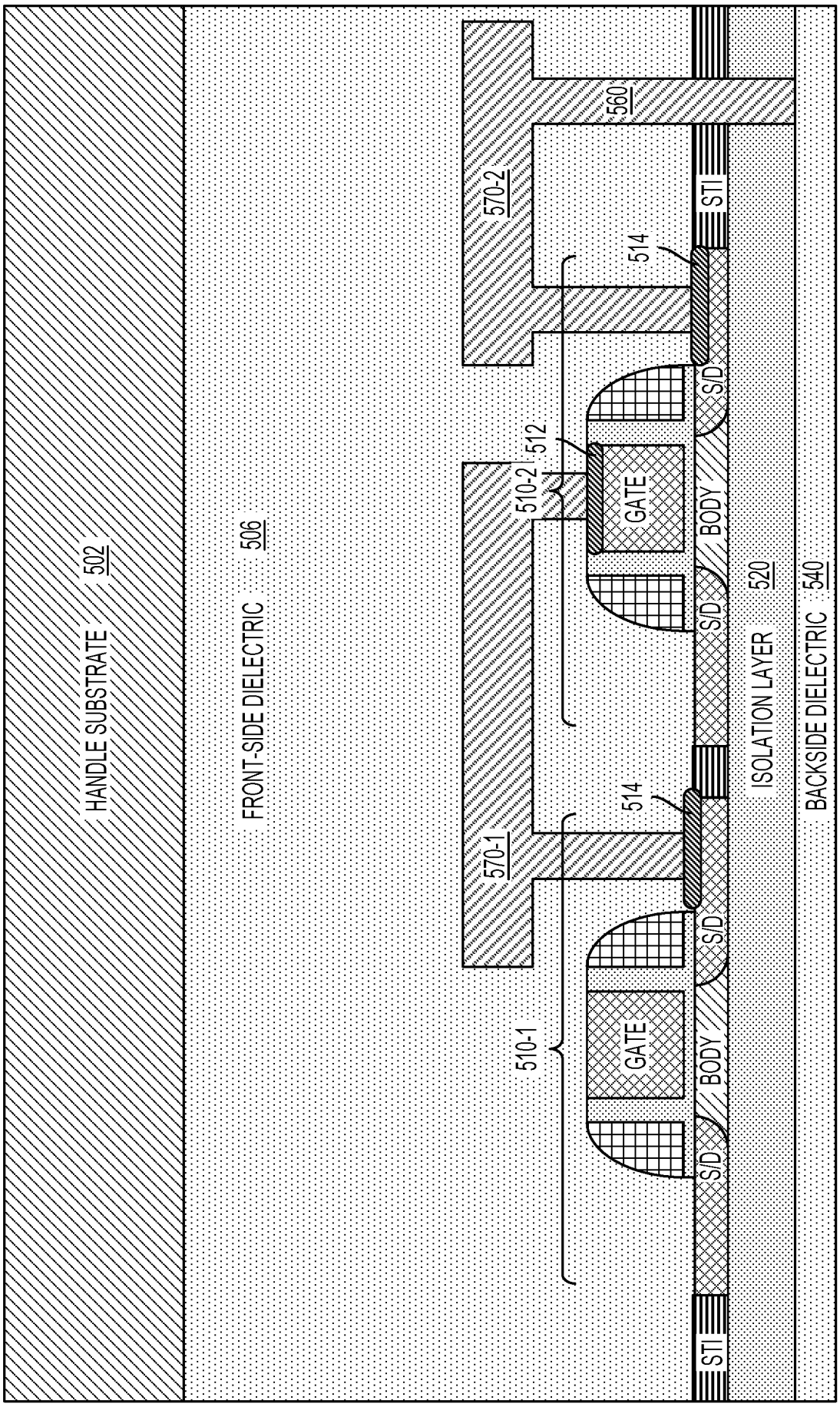
HANDLE SUBSTRATE
502
FRONT-SIDE DIELECTRIC
506
570-2
560
514
STI
S/D
512
510-2
GATE
BODY
S/D
520
ISOLATION LAYER
540
BACKSIDE DIELECTRIC
514
570-1
S/D
510-1
GATE
BODY
S/D
STI

FIG. 7B

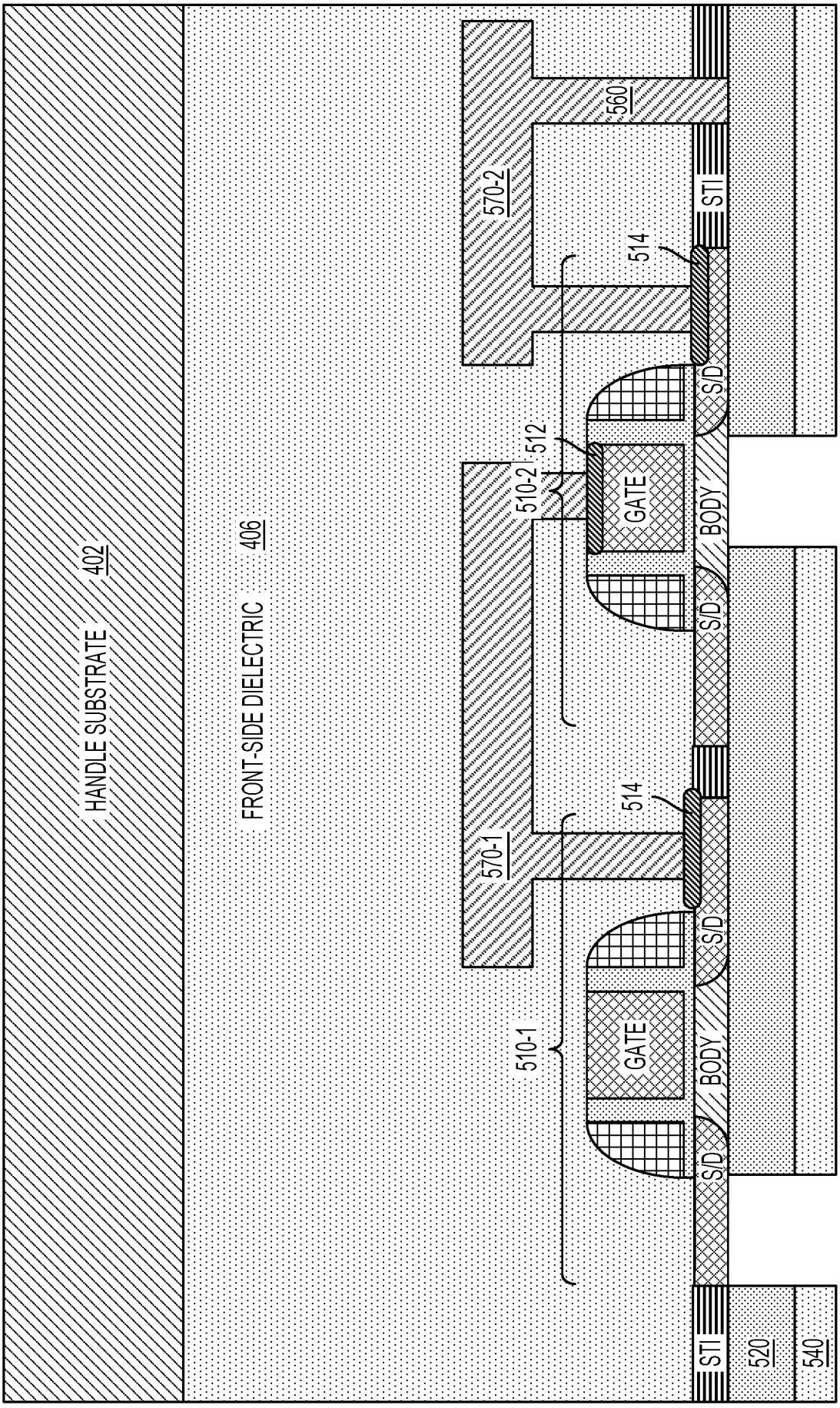
HANDLE SUBSTRATE
402
FRONT-SIDE DIELECTRIC
406
570-2
560
STI
514
S/D
512
510-2
GATE
BODY
S/D
S/D
514
570-1
510-1
GATE
BODY
S/D
STI
520
540

FIG. 7C

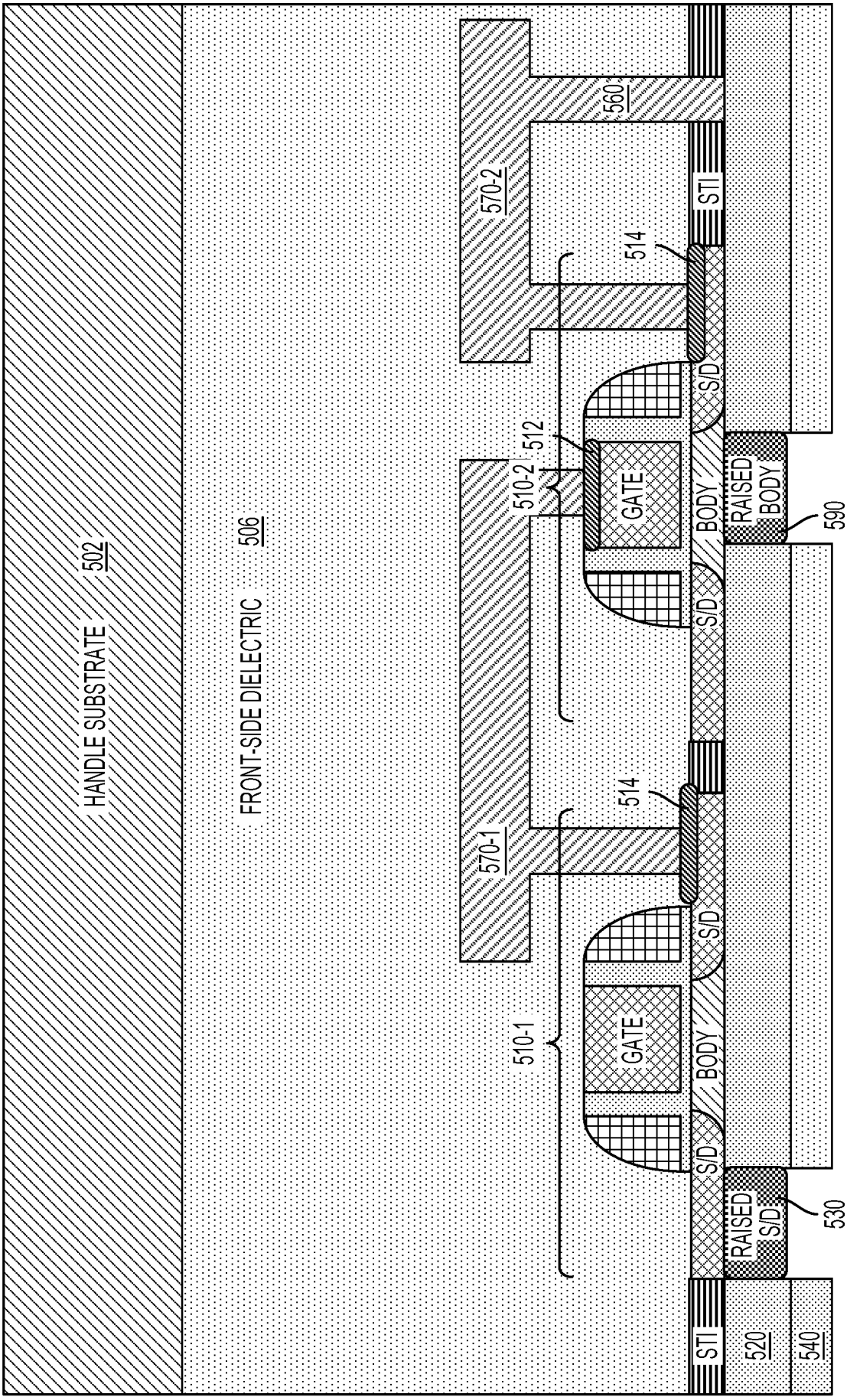
HANDLE SUBSTRATE 502
FRONT-SIDE DIELECTRIC 506
560
570-2
514
STI
S/D
512
510-2
GATE
BODY
RAISED BODY
590
S/D
514
570-1
S/D
510-1
GATE
BODY
S/D
RAISED S/D
530
STI
520
540

FIG. 7D

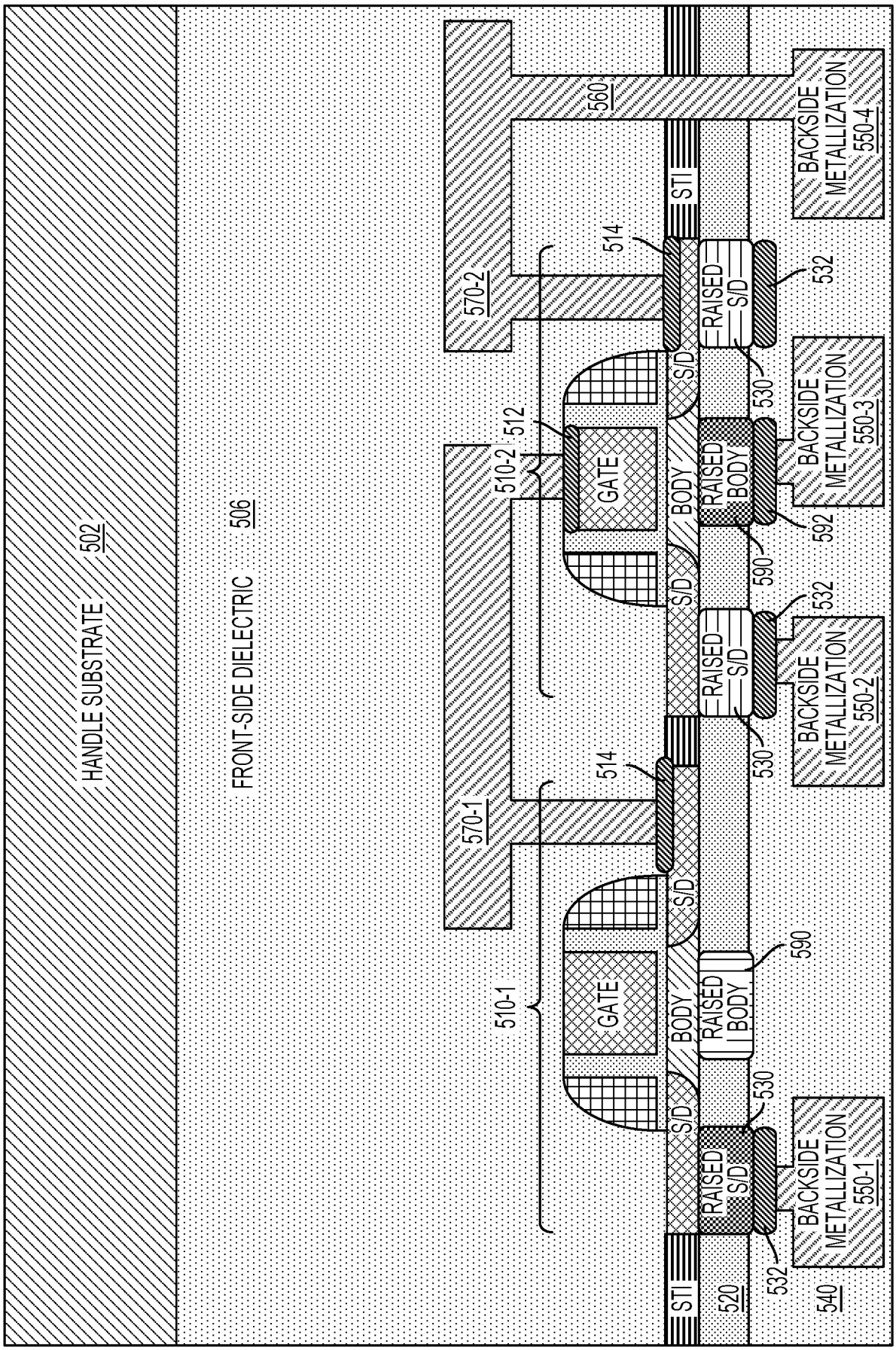
HANDLE SUBSTRATE
502
FRONT-SIDE DIELECTRIC
506
560
570-2
570-1
514
514
STI
STI
510-2
510-1
512
GATE
GATE
S/D
S/D
S/D
S/D
BODY
BODY
RAISED S/D
RAISED S/D
RAISED S/D
RAISED BODY
RAISED BODY
530
530
530
532
532
532
590
590
592
520
540
BACKSIDE METALLIZATION
550-1
BACKSIDE METALLIZATION
550-2
BACKSIDE METALLIZATION
550-3
BACKSIDE METALLIZATION
550-4

FIG. 7E

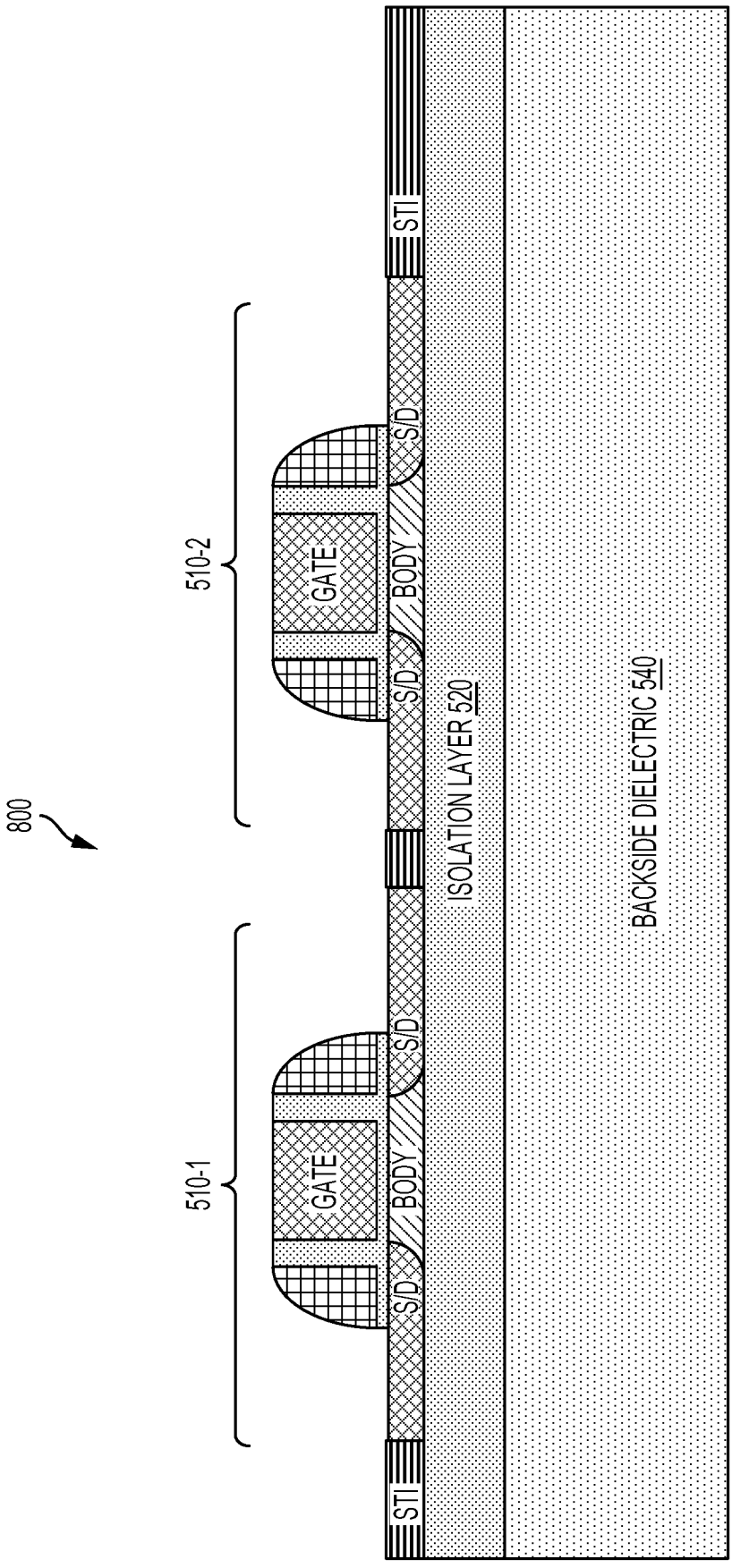
800
510-1
510-2
STI
S/D
GATE
BODY
ISOLATION LAYER 520
BACKSIDE DIELECTRIC 540

FIG. 8A

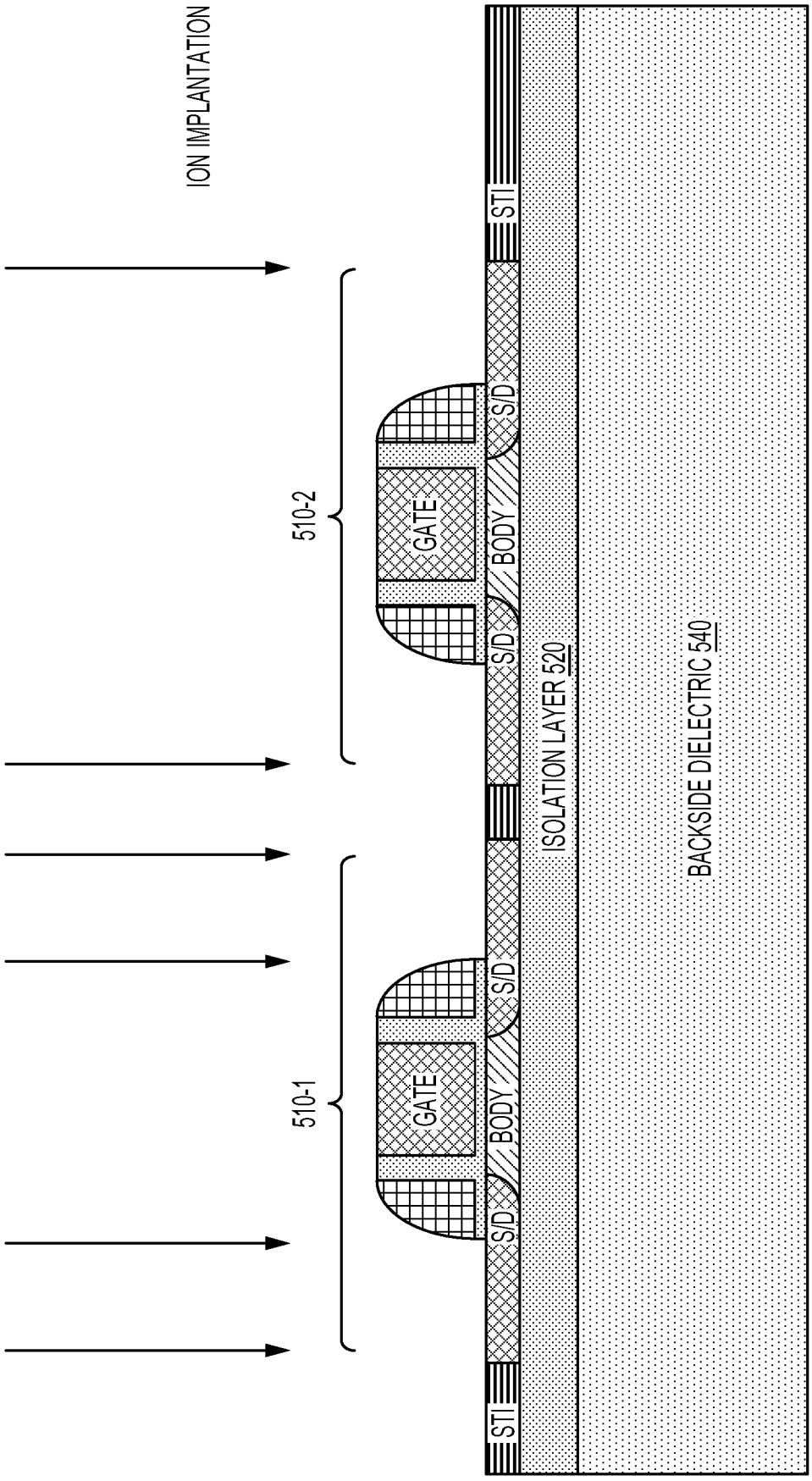
ION IMPLANTATION
510-2
510-1
STI
S/D
GATE
BODY
S/D
S/D
GATE
BODY
S/D
STI
ISOLATION LAYER 520
BACKSIDE DIELECTRIC 540

FIG. 8B

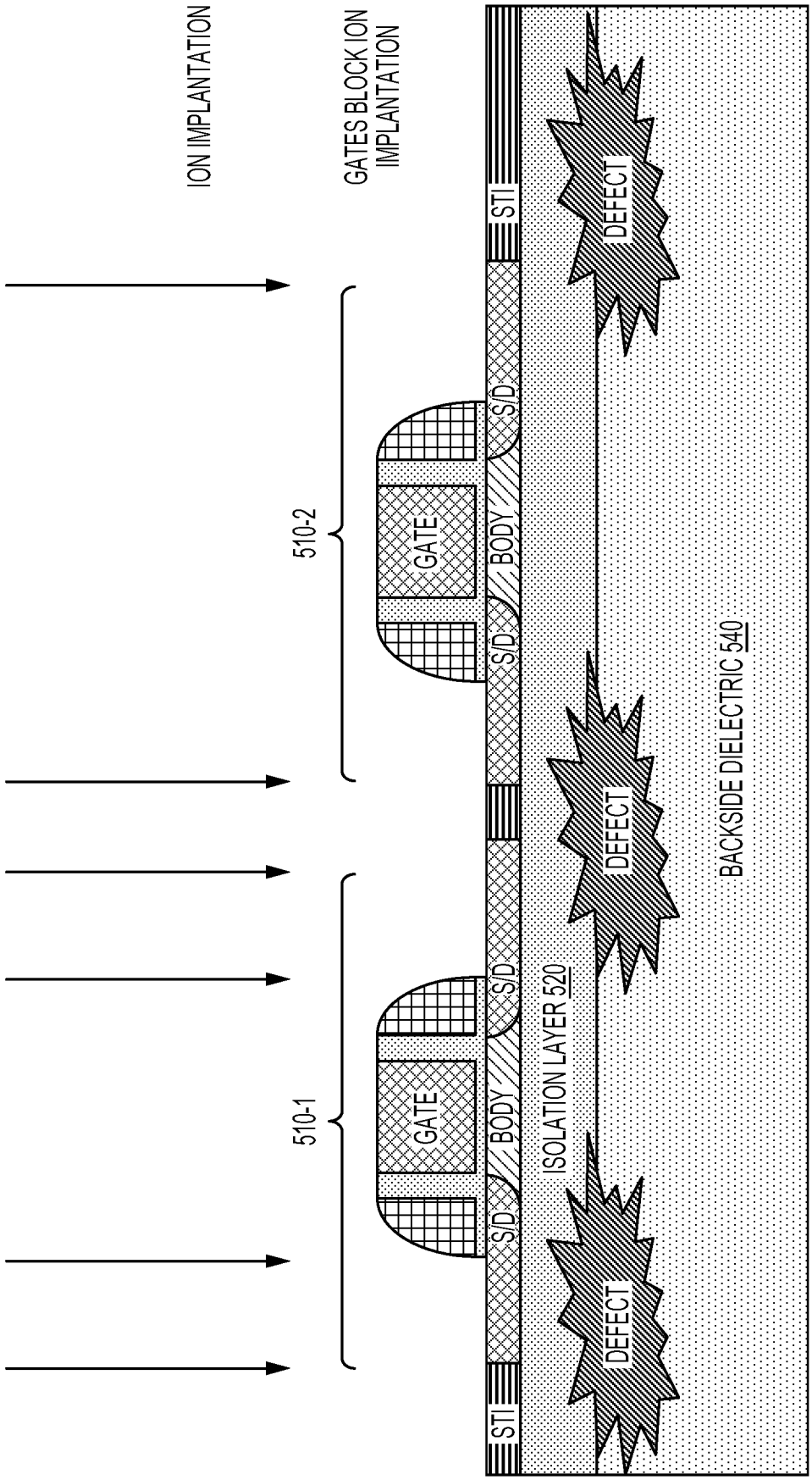
ION IMPLANTATION
GATES BLOCK ION IMPLANTATION
510-2
510-1
GATE
GATE
S/D
S/D
S/D
S/D
BODY
BODY
STI
STI
DEFECT
DEFECT
DEFECT
ISOLATION LAYER 520
BACKSIDE DIELECTRIC 540

FIG. 8C

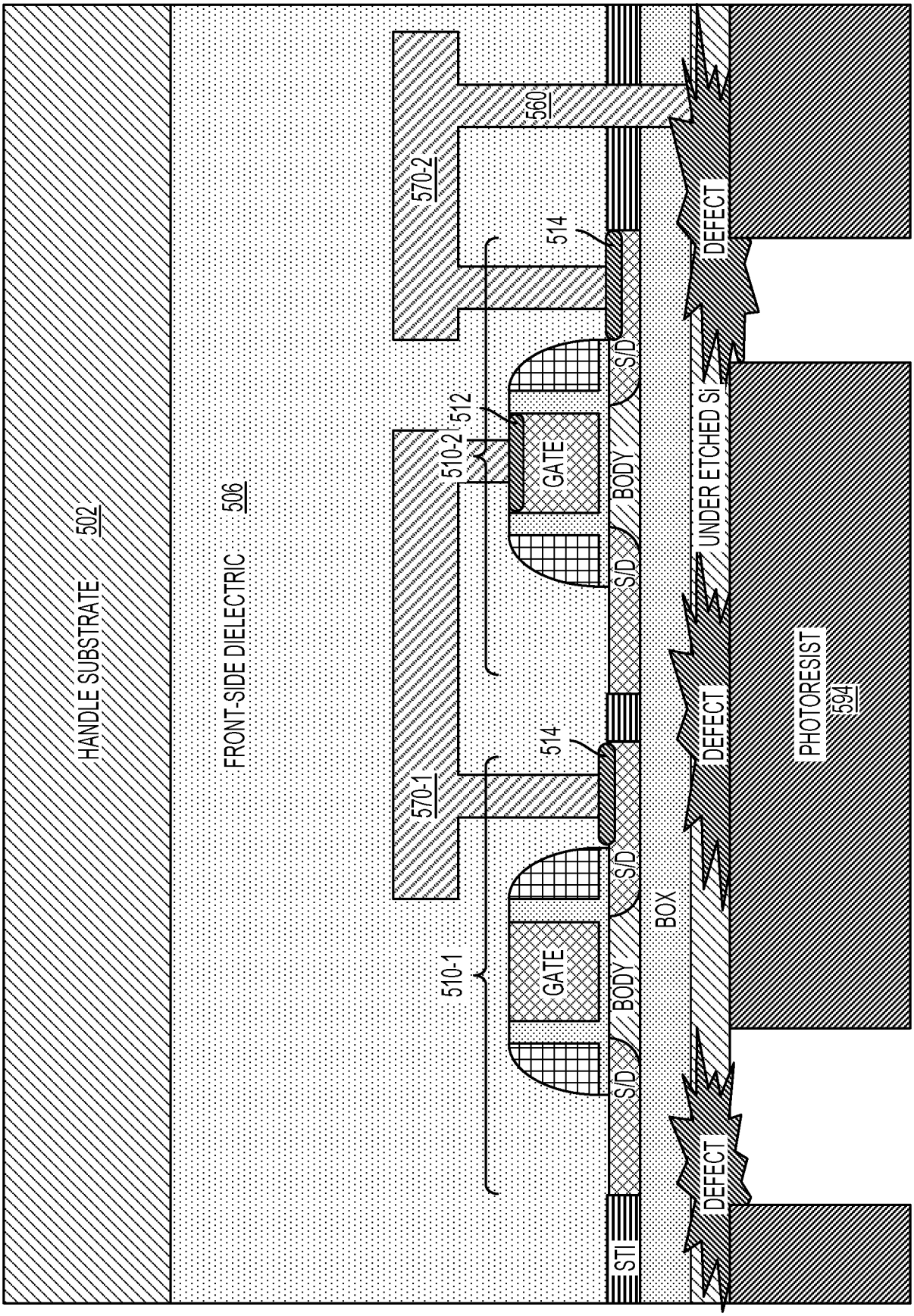
HANDLE SUBSTRATE
502
FRONT-SIDE DIELECTRIC
506
570-2
560
514
DEFECT
S/D
510-2
512
GATE
BODY
S/D
UNDER ETCHED Si
570-1
514
DEFECT
PHOTORESIST
594
S/D
510-1
GATE
BOX
BODY
S/D
STI
DEFECT

FIG. 8D

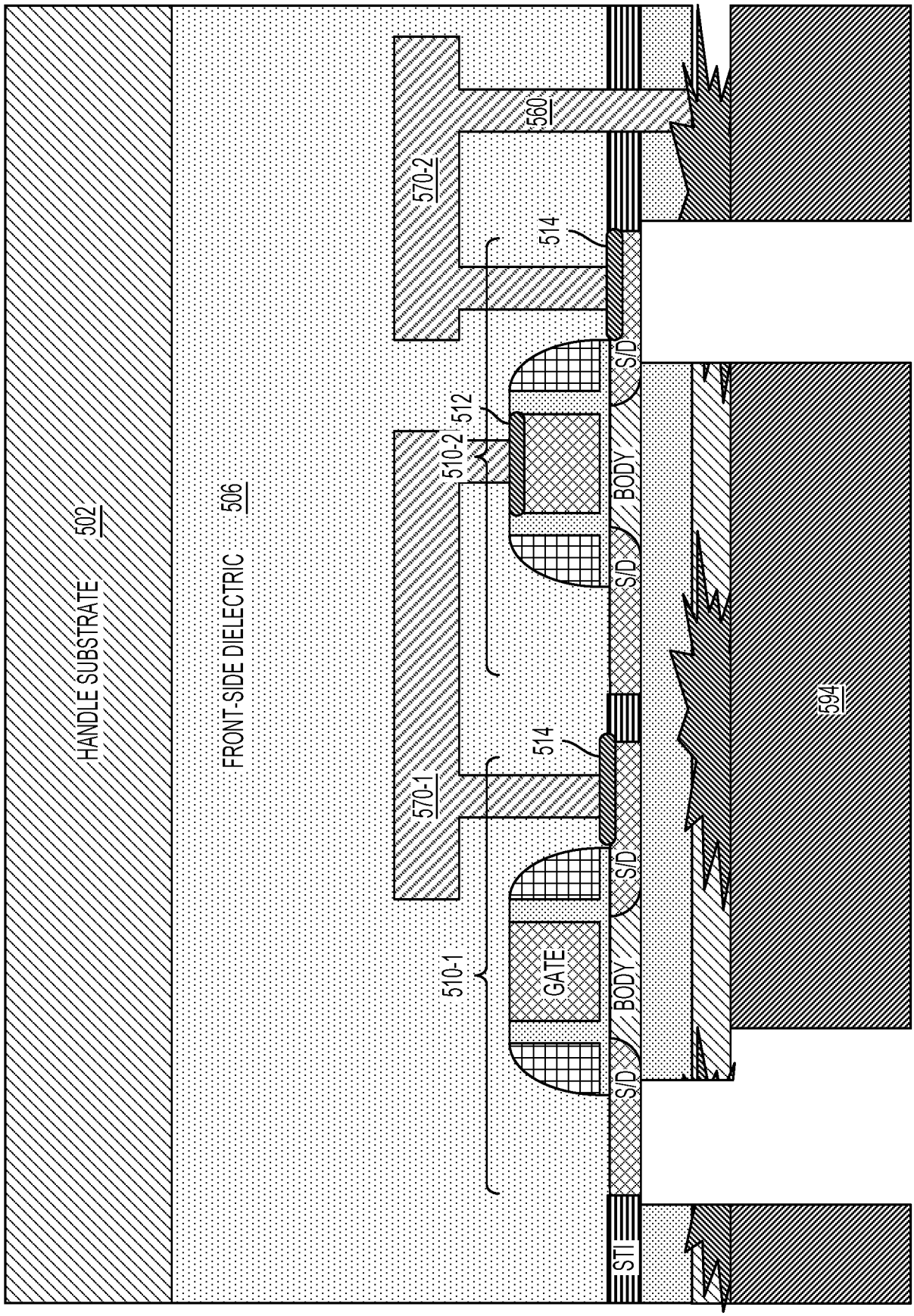
HANDLE SUBSTRATE 502
FRONT-SIDE DIELECTRIC 506
560
570-2
514
S/D
510-2
512
BODY
S/D
514
570-1
S/D
510-1
GATE
BODY
S/D
STI
594

FIG. 8E

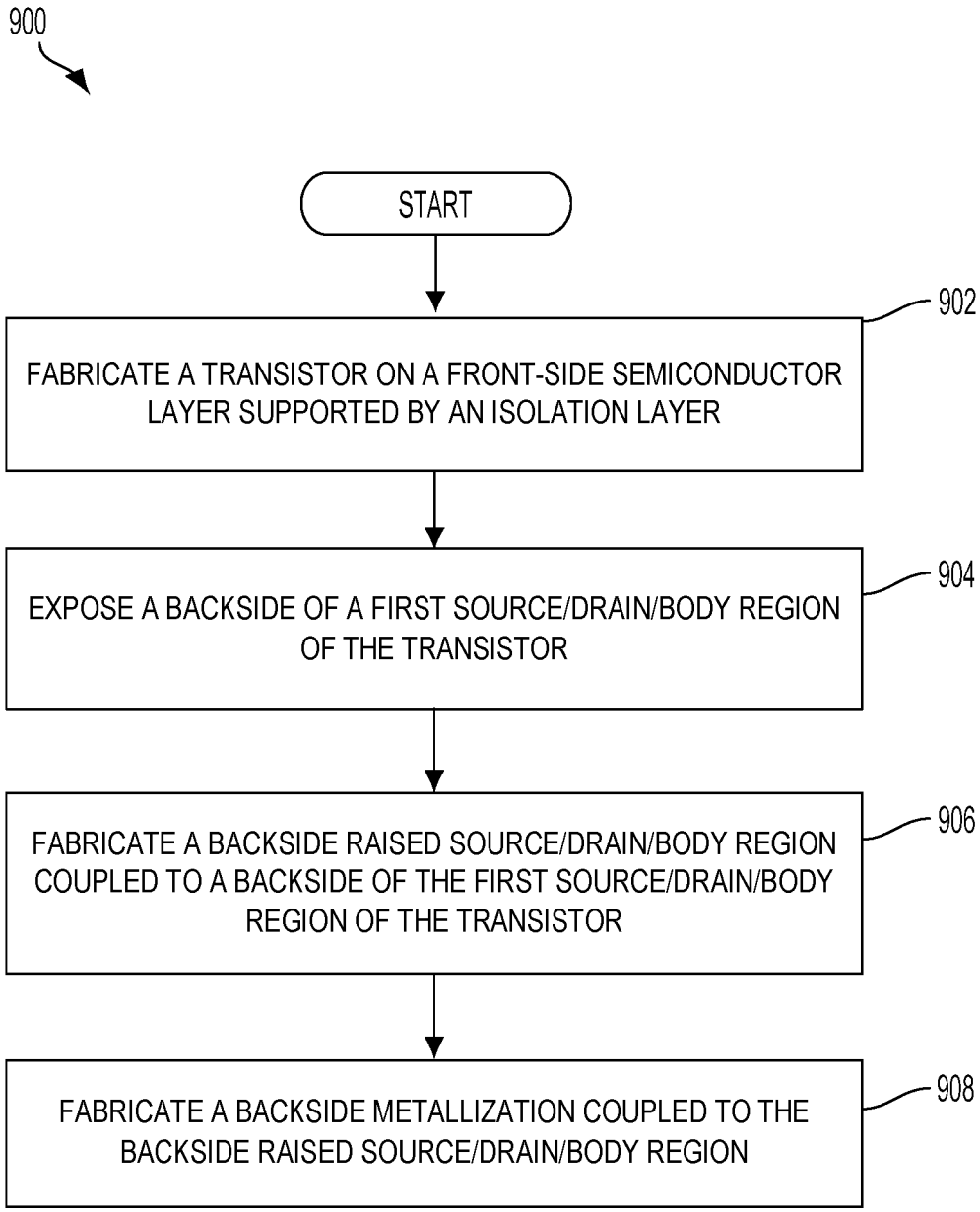
900
START
FABRICATE A TRANSISTOR ON A FRONT-SIDE SEMICONDUCTOR LAYER SUPPORTED BY AN ISOLATION LAYER
902
EXPOSE A BACKSIDE OF A FIRST SOURCE/DRAIN/BODY REGION OF THE TRANSISTOR
904
FABRICATE A BACKSIDE RAISED SOURCE/DRAIN/BODY REGION COUPLED TO A BACKSIDE OF THE FIRST SOURCE/DRAIN/BODY REGION OF THE TRANSISTOR
906
FABRICATE A BACKSIDE METALLIZATION COUPLED TO THE BACKSIDE RAISED SOURCE/DRAIN/BODY REGION
908

FIG. 9

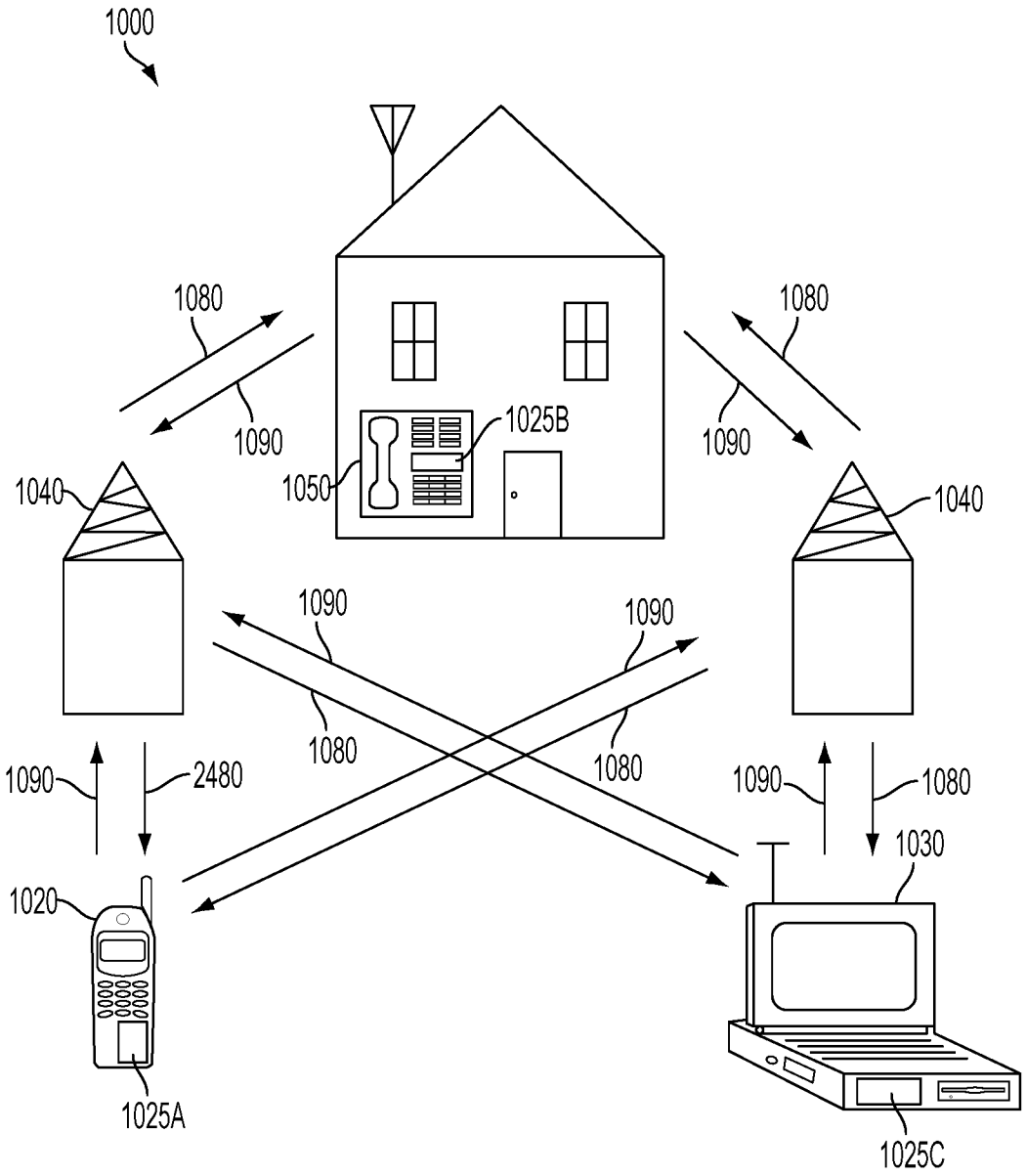
1000
1080
1090
1025B
1050
1080
1090
1040
1040
1090
1090
1080
1080
1090
2480
1090
1080
1030
1020
1025A
1025C

FIG. 10

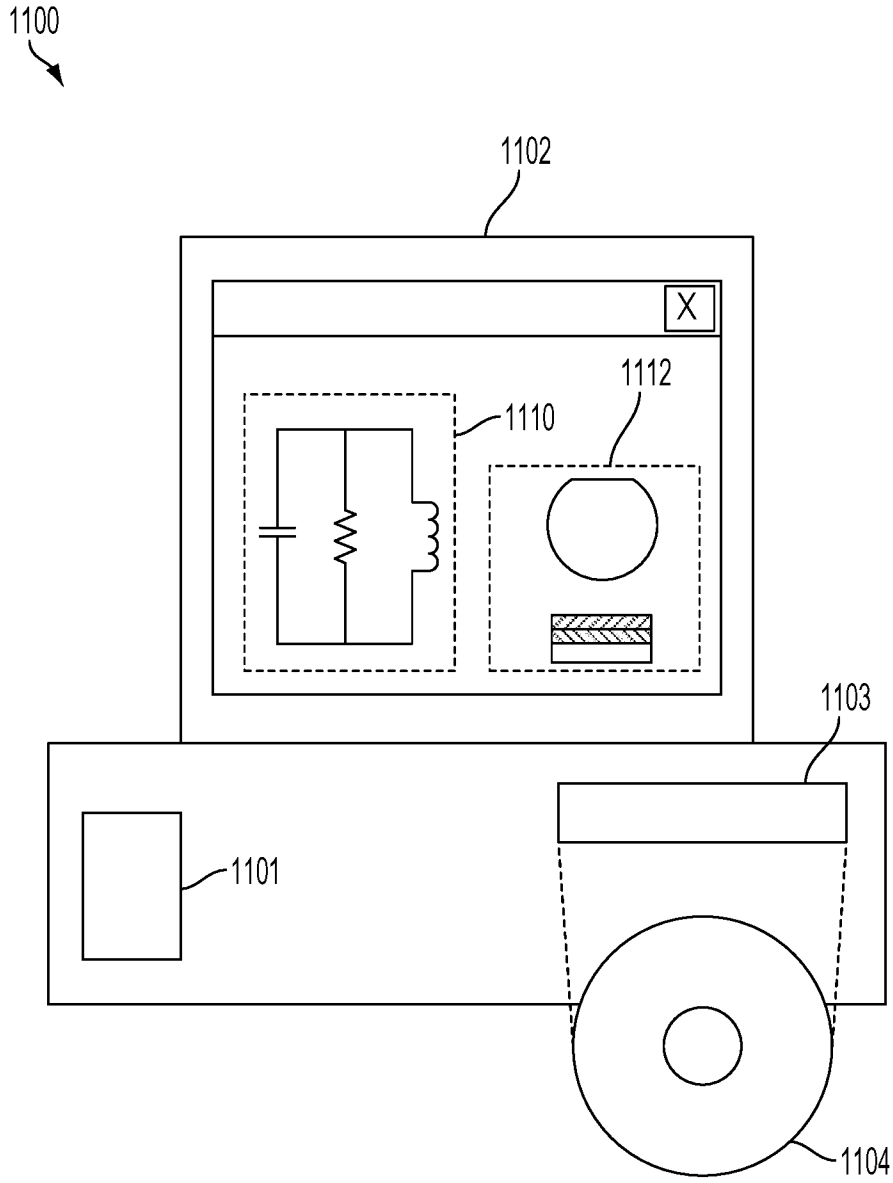

FIG. 11

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2017/041755

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/84 H01L27/12 H01L29/786 H01L21/768 H01L21/3115 H01L21/762
ADD.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2015/091092 A1 (LEE JAM-WEM [TW]) 2 April 2015 (2015-04-02) the whole document -----	1-10, 14-27
X	DE 10 2004 033149 A1 (INFINEON TECHNOLOGIES AG [DE]) 9 February 2006 (2006-02-09) paragraph [0083]; figure 5 paragraph [0108]; figure 10 -----	1-10, 12-27

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 October 2017	02/11/2017

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Hoffmann, Niels

1

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2017/041755

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	ALLAIN F ET AL: "Bonded Planar Double-Metal-Gate NMOS Transistors Down to 10 nm", IEEE ELECTRON DEVICE LETTERS, IEEE SERVICE CENTER, NEW YORK, NY, US, vol. 26, no. 5, 1 May 2005 (2005-05-01), pages 317-319, XP011131287, ISSN: 0741-3106, DOI: 10.1109/LED.2005.846580 page 317, column 1, paragraph 2; figure 1	1-10, 12-27
X	US 2006/043485 A1 (FUKUSHIMA YASUMORI [JP] ET AL) 2 March 2006 (2006-03-02) the whole document	1-10,14, 16-27
X	US 2009/020761 A1 (OKAZAKI YUTAKA [JP]) 22 January 2009 (2009-01-22) figures 7,13	1-7,9, 10, 16-25,27
X	US 2004/222471 A1 (INOH KAZUMI [JP]) 11 November 2004 (2004-11-11) paragraph [0070]; figure 6I	1-5, 7-10, 12-14, 16-27
X,P	WO 2017/052667 A1 (INTEL CORP [US]) 30 March 2017 (2017-03-30) the whole document	1-10, 12-27

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2017/041755

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2015091092 A1	02-04-2015	US 2015091092 A1	02-04-2015
		US 2016013307 A1	14-01-2016
		US 2016372577 A1	22-12-2016
DE 102004033149 A1	09-02-2006	DE 102004033149 A1	09-02-2006
		WO 2006005321 A2	19-01-2006
US 2006043485 A1	02-03-2006	JP 4175650 B2	05-11-2008
		JP 2006066591 A	09-03-2006
		KR 20060050391 A	19-05-2006
		TW I270110 B	01-01-2007
		US 2006043485 A1	02-03-2006
		US 2008318390 A1	25-12-2008
US 2009020761 A1	22-01-2009	JP 5322408 B2	23-10-2013
		JP 2009026800 A	05-02-2009
		US 2009020761 A1	22-01-2009
		US 2011278573 A1	17-11-2011
US 2004222471 A1	11-11-2004	JP 3764401 B2	05-04-2006
		JP 2003309267 A	31-10-2003
		US 2004222471 A1	11-11-2004
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