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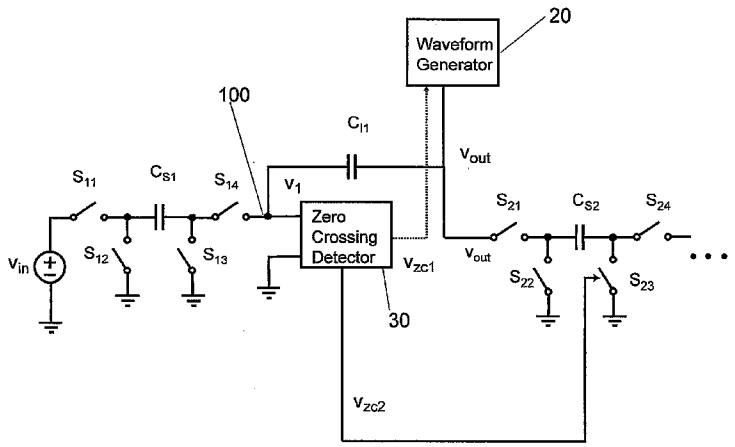
(54) Title: CONSTANT SLOPE RAMP CIRCUITS FOR SAMPLE-DATA CIRCUITS



(57) Abstract: A sample-data analog circuit includes a level-crossing detector. The level- crossing detector controls sampling switches to provide a precise sample of the output voltage when the level-crossing detector senses the predetermined level crossing of the input signal. A multiple segment ramp waveform generator is used in the sample-data analog circuits. The ramp waveform generator includes an amplifier, a variable current source, and a voltage detection circuit coupled to the current source to control the change in the amplitude of the current. The ramp generator produces constant slope within each segment regardless of the load condition. The sample-data analog circuit also utilizes variable bandwidths and thresholds.

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CONSTANT SLOPE RAMP CIRCUITS FOR SAMPLE-DATA CIRCUITS

PRIORITY INFORMATION

[0001] The present application is a continuation-in-part of co-pending US Patent Application Serial Number 11/454,275, filed on June 16, 2006. The present application claims priority, under 35 U.S.C. §120, from co-pending US Patent Application Serial Number 11/454,275, filed on June 16, 2006. Said US Patent Application Serial Number 11/454,275, filed on June 16, 2006 claiming priority, under 35 U.S.C. §119(e), from US Provisional Patent Application, Serial Number 60/595,414, filed on July 1, 2005. Said US Patent Application Serial Number 11/454,275, filed on June 16, 2006 also claiming priority, under 35 U.S.C. §119(e), from US Provisional Patent Application, Serial Number 60/595,493, filed on July 11, 2005. The entire contents of US Patent Application Serial Number 11/454,275, filed on June 16, 2006, US Provisional Patent Application, Serial Number 60/595,414, filed on July 1, 2005, and US Provisional Patent Application, Serial Number 60/595,493, filed on July 11, 2005 are hereby incorporated by reference.

[0002] The present application also claims priority, under 35 U.S.C. §119(e), from US Provisional Patent Application, Serial Number 60/595,605, filed on July 19, 2005. Also, the present application claims priority, under 35 U.S.C. §119(e), from US Provisional Patent Application, Serial Number 60/595,623, filed on July 21, 2005. The entire contents of US Provisional Patent Application, Serial Number 60/595,605, filed on July 19, 2005, and US Provisional Patent Application, Serial Number 60/595,623, filed on July 21, 2005, are hereby incorporated by reference.

FIELD OF THE PRESENT INVENTION

[0003] The present invention relates generally to sample data circuits and, more particularly, to sample data circuits that include constant slope ramp circuits.

BACKGROUND OF THE PRESENT INVENTION

[0004] Most sample-data analog circuits such as switched-capacitor filters, analog-to-digital converters, and delta-sigma modulators require operational amplifiers to process the signal. Consider a switched-capacitor integrator example shown in Figure 2. First, the switches S_{11} and S_{13} are closed so that the input voltage v_{in} is sampled on the sampling capacitor C_{S1}. Next, the switches S_{11} and S_{13} are opened and S_{12} and S_{14} are

closed. This operation transfers the charge in the sampling capacitor C_{S1} to the integrating capacitor C_{I1}. The output voltage, v_{out}, of a first integrator **1100** is typically sampled by another sample-data circuit, for example, another switched-capacitor integrator. In the circuit shown in Figure 2, the circuit consisting of switches S_{21}, S_{22}, S_{23}, S_{24}, and a second sampling capacitor C_{S2} comprise a part of the second switched-capacitor integrator. The output voltage, v_{out}, of the first integrator **10** is sampled on the second sampling capacitor C_{S2} by closing switches S_{21} and S_{23}.

[0005] An example of a timing diagram is shown in Figure 3. The clock signal has two non-overlapping phases Φ_1 and Φ_2. The phase Φ_1 is applied to switches S_{11}, S_{13}, S_{21}, and S_{23}, and phase Φ_2 is applied to switches S_{12}, S_{14}, S_{22}, and S_{24}. With this timing, the circuit performs non-inverting discrete integration with full clock delay. The waveforms at the output of the integrator, v_{out}, and at the virtual ground node **100**, v_1, are also shown in Figure 3. Different clock phasing arrangements yield different responses from the integrator. For example, if Φ_1 is applied to switches S_{11}, S_{13}, S_{22}, and S_{24}, and phase Φ_1 is applied to switches S_{12}, S_{14}, S_{21}, and S_{23}, the circuit performs non-inverting integration with half-clock delay.

[0006] For an accurate integration of the input signal, v_1 must be driven as close to ground as possible. In order to accomplish this, the operational amplifier must provide sufficient open-loop gain and low noise. In addition, for fast operation, the operational amplifier **10** of Figure 2 must settle fast.

[0007] In Figure 3, the voltage v_1 is shown to settle back to ground after a disturbance when the sampling capacitor C_{S1} is switched to Node **100** by closing S_{12} and S_{14}. In addition to high open-loop gain and fast settling time, operational amplifiers must provide large output swing for high dynamic range. As the technology scales, it becomes increasingly difficult to achieve these characteristics from operational amplifiers. The primary factors that make the operational amplifier design difficult are low power supply voltages and low device gain.

[0008] As noted above, accurate output voltage can be obtained if Node **100** in Figure 2 is maintained precisely at ground. However, in sample-data circuits, the only point of time accurate output voltage is required is at the instant the output voltage is sampled by another sampling circuit. Thus, it is not necessary to maintain the voltage at Node **100** at ground all the time.

[0009] It is further noted that delays in the detectors of sample-data circuits may cause errors in the operation thereof. Moreover, it is noted that performance parameters

such as speed, accuracy, and power consumption of sample-data circuits depend upon the design of zero crossing detectors.

[0010] Therefore, it is desirable to provide a sample-data circuit that maintains the proper level at the virtual ground node at the instant the output voltage is sampled by another sampling circuit, substantially eliminates the errors caused by delays, and optimizes the performance parameters such as speed, accuracy, and power consumption of the sample-data circuit.

[0011] Moreover, it is desirable to provide a sample-data circuit that maintains the proper level at the virtual ground node at the instant the output voltage is sampled by another sampling circuit and provides differential signal paths for sample-data circuits, substantially eliminates the errors caused by delays, and optimizes the performance parameters such as speed, accuracy, and power consumption of the sample-data circuit.

[0012] Furthermore, it is desirable to provide a sample-data circuit that reduces the effect of power supply, substrate, and common-mode noise by symmetric differential signal processing, substantially eliminates the errors caused by delays, and optimizes the performance parameters such as speed, accuracy, and power consumption of the sample-data circuit.

[0013] Also, it is desirable to provide a sample-data circuit that increases the signal range by incorporating differential signal paths, substantially eliminates the errors caused by delays, and optimizes the performance parameters such as speed, accuracy, and power consumption of the sample-data circuit.

SUMMARY OF THE PRESENT INVENTION

[0014] One aspect of the present invention is a circuit. The circuit includes a level-crossing detector to generate a level-crossing detection signal when an input signal crosses a predetermined voltage level; a sampling switch, operatively coupled to the level-crossing detector, the sampling switch turning OFF when the level-crossing detection signal indicates a level-crossing; and a waveform generator operatively coupled to the level-crossing detector. The waveform generator includes an amplifier.

[0015] Another aspect of the present invention is a circuit. The circuit includes a level-crossing detector to generate a level-crossing detection signal when an input signal crosses a predetermined voltage level and a waveform generator, operatively coupled to the level-crossing detector, to produce a positive slope waveform and a negative slope waveform. The waveform generator includes a first amplifier, a second amplifier, and a

switching circuit. The switching circuit switching causes the positive slope waveform or the negative slope waveform to be output from the waveform generator.

[0016] Another aspect of the present invention is a method for sampling an analog signal. The method samples an input voltage using the switched capacitance network; generates a ramp waveform by negative feedback; applies negative feedback to linearize the ramp waveform; determines when a node voltage of the switched capacitance network crosses a first predetermined level; and provides a sample of an output voltage of the switched capacitance network.

[0017] Another aspect of the present invention is a method for sampling an analog signal. The method samples an input voltage using the switched capacitance network; determines when a node voltage of the switched capacitance network crosses a predetermined level; generates a voltage ramp signal in response to the determination of when the node voltage of the switched capacitance network crosses the predetermined level; applies negative feedback to linearize the voltage ramp signal; and provides a sample of an output voltage of the switched capacitance network.

[0018] Another aspect of the present invention is a zero-crossing detector circuit. The zero-crossing detector circuit includes an amplifier stage and a bandwidth controller operatively connected to the amplifier stage. The bandwidth controller provides a variable bandwidth for the zero-crossing detector circuit so that the zero-crossing detector circuit provides a first level of zero-crossing detection coarseness during a first period of time and a second level of zero-crossing detection coarseness during a second period of time, the first level of zero-crossing detection coarseness being coarser than the second level of zero-crossing detection coarseness.

[0019] Another aspect of the present invention is a zero-crossing detector circuit. The zero-crossing detector circuit includes an amplifier stage, the amplifier stage including a variable current source, and a bandwidth controller operatively connected to the variable current source of the amplifier stage. The bandwidth controller controls a current level of the variable current source connected thereto so that the zero-crossing detector circuit provides a first level of zero-crossing detection coarseness during a first period of time and a second level of zero-crossing detection coarseness during a second period of time, the first level of zero-crossing detection coarseness being coarser than the second level of zero-crossing detection coarseness.

[0020] Another aspect of the present invention is a switched-capacitor circuit. The switched-capacitor circuit includes a zero-crossing detector to generate a zero-crossing detection signal when an input signal crosses a predetermined voltage level and a

waveform generator operatively coupled to the zero-crossing detector. The waveform generator includes an amplifier and a variable current source. The zero-crossing detector includes an amplifier stage and a bandwidth controller operatively connected to the amplifier stage. The bandwidth controller provides a variable bandwidth for the zero-crossing detector so that the zero-crossing detector provides a first level of zero-crossing detection coarseness during a first period of time and a second level of zero-crossing detection coarseness during a second period of time, the first level of zero-crossing detection coarseness being coarser than the second level of zero-crossing detection coarseness.

[0021] Another aspect of the present invention is a switched-capacitor circuit. The switched-capacitor circuit includes a level-crossing detector to generate a level-crossing detection signal when an input signal crosses a predetermined voltage level and a waveform generator operatively coupled to the level-crossing detector. The waveform generator includes an amplifier and a variable current source. The level-crossing detector includes an amplifier stage and a bandwidth controller operatively connected to the amplifier stage. The bandwidth controller provides a variable bandwidth for the level-crossing detector circuit so that the level-crossing detector circuit provides a first level of level-crossing detection coarseness during a first period of time and a second level of level-crossing detection coarseness during a second period of time, the first level of level-crossing detection coarseness being coarser than the second level of level-crossing detection coarseness.

BRIEF DESCRIPTION OF THE DRAWINGS

[0022] The present invention may take form in various components and arrangements of components, and in various steps and arrangements of steps. The drawings are only for purposes of illustrating a preferred embodiment and are not to be construed as limiting the present invention, wherein:

[0023] Figure 1 illustrates a zero-crossing detector;

[0024] Figure 2 illustrates a switched-capacitor integrator;

[0025] Figure 3 illustrates a timing diagram for the switched-capacitor integrator of Figure 2;

[0026] Figure 4 illustrates a non-inverting integrator according to the concepts of the present invention;

[0027] Figure 5 illustrates a timing diagram for the non-inverting integrator of Figure 4;

[0028] Figure 6 illustrates a non-inverting integrator with a waveform generator being a current source according to the concepts of the present invention;

[0029] Figure 7 illustrates another non-inverting integrator according to the concepts of the present invention;

[0030] Figure 8 illustrates a timing diagram for the non-inverting integrator of Figure 7;

[0031] Figure 9 illustrates another non-inverting integrator according to the concepts of the present invention;

[0032] Figure 10 illustrates another non-inverting integrator according to the concepts of the present invention;

[0033] Figure 11 illustrates a timing diagram for the non-inverting integrator of Figure 10;

[0034] Figure 12 illustrates another non-inverting integrator according to the concepts of the present invention;

[0035] Figure 13 illustrates another non-inverting integrator according to the concepts of the present invention;

[0036] Figure 14 illustrates a timing diagram for the non-inverting integrator of Figure 13;

[0037] Figure 15 illustrates one embodiment of a sample-data circuit according to the concepts of the present invention;

[0038] Figure 16 illustrates another embodiment of a sample-data circuit according to the concepts of the present invention;

[0039] Figure 17 illustrates another embodiment of a sample-data circuit according to the concepts of the present invention;

[0040] Figure 18 illustrates another embodiment of a sample-data circuit according to the concepts of the present invention;

[0041] Figure 19 illustrates another embodiment of a sample-data circuit according to the concepts of the present invention;

[0042] Figure 20 illustrates an embodiment a continuous-time voltage comparator for a sample-data circuit according to the concepts of the present invention;

[0043] Figure 21 illustrates another embodiment a continuous-time voltage comparator for a sample-data circuit according to the concepts of the present invention;

[0044] Figure 22 illustrates another embodiment a continuous-time voltage comparator for a sample-data circuit according to the concepts of the present invention;

[0045] Figure 23 illustrates another embodiment a continuous-time voltage comparator for a sample-data circuit according to the concepts of the present invention;

[0046] Figure 24 illustrates another embodiment a continuous-time voltage comparator for a sample-data circuit according to the concepts of the present invention;

[0047] Figure 25 illustrates another embodiment a continuous-time voltage comparator for a sample-data circuit according to the concepts of the present invention;

[0048] Figure 26 illustrates another embodiment a continuous-time voltage comparator for a sample-data circuit according to the concepts of the present invention;

[0049] Figure 27 illustrates another embodiment a continuous-time voltage comparator for a sample-data circuit according to the concepts of the present invention; and

[0050] Figure 28 illustrates another embodiment a continuous-time voltage comparator for a sample-data circuit according to the concepts of the present invention.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

[0051] The present invention will be described in connection with preferred embodiments; however, it will be understood that there is no intent to limit the present invention to the embodiments described herein. On the contrary, the intent is to cover all alternatives, modifications, and equivalents as may be included within the spirit and scope of the present invention, as defined by the appended claims.

[0052] For a general understanding of the present invention, reference is made to the drawings. In the drawings, like reference have been used throughout to designate identical or equivalent elements. It is also noted that the various drawings illustrating the present invention may not have been drawn to scale and that certain regions may have been purposely drawn disproportionately so that the features and concepts of the present invention could be properly illustrated.

[0053] It is noted that, in the various Figures, the earth symbol indicates the system's common-mode voltage. For example, in a system with 2.5 V and –2.5 V power supplies, the system's common-mode voltage may be at ground. In a system with a single 2.5 power supply, the system's common-mode voltage may be at 1.25 V.

[0054] As noted above, accurate output voltage can be obtained if Node **100** in Figure 2 is maintained precisely at ground. However, in sample-data circuits, the only point of time accurate output voltage is required is at the instant the output voltage is sampled by another sampling circuit. Thus, it is not necessary to maintain the voltage at Node **100** at ground all the time.

[0055] Figure 4 illustrates a non-inverting integrator according to the concepts of the present invention. More specifically, as an example, a non-inverting integrator with half-clock delay is illustrated in Figure 4.

[0056] As illustrated in Figure 4, a clock phase Φ_1 is applied to switches S_{11}, S_{13}, S_{22}, and S_{24}, and another phase Φ_2 is applied to switches S_{12}, S_{14}, and S_{21}. A zero crossing detector **30** is used to detect the point of time at which Node **100** crosses ground. The switch S_{23} is controlled by the output of the zero crossing detector **30**. The output of the zero crossing detector **30** is used to determine the time point to take the sample of the output voltage v_{out}. A waveform generator **20** generates a voltage waveform as the output voltage v_{out} in such way the voltage at Node **100** crosses zero if the charge in capacitors C_{S1} and C_{I1} is within a normal operating range.

[0057] In the timing diagram shown in Figure 5, the waveform generated by the waveform generator **20** is shown as a ramp. When v_1, the voltage at Node **100**, crosses zero at time t_1, the output v_{zc} of the zero crossing detector **30** goes low, turning the switch S_{23} OFF. At that instant, the output voltage v_{out} is sampled on C_{S2}.

[0058] Since v_1 is very close to zero when the sample of v_2 is taken, an accurate output voltage is sampled on C_{S2}. A similar operation repeats during the next clock cycle, and the sample of the output voltage is taken at time t_2.

[0059] It is noted that the zero crossing detector **30** may optionally have an overflow detection feature that determines when the charge in capacitors C_{S1} and C_{I1} is outside the normal range of operation. It can be implemented by a logic circuit that makes the output v_{zc} of the zero-crossing detector **30** to go low when Φ_2 goes low. In the event v_1 fails to cross zero, the sample is taken on the falling edge of Φ_2. At the same time, the logic circuit produces a flag indicating overflow.

[0060] In the embodiment described above and in the various embodiments described below, a zero crossing detector is utilized in lieu of a comparator. Typically, a comparator is designed to compare two arbitrary input voltages. A comparator may be implemented as cascaded amplifiers, a regenerative latch, or a combination of both. A comparator may be used to detect a zero voltage level or a predetermined voltage level crossing.

[0061] It is noted that the input waveform of the various described embodiments is not arbitrary, but deterministic and repetitive. Thus, the various described embodiments determine the instant the zero voltage level or the predetermined voltage level is crossed than relative amplitudes of the input signals. For such a deterministic input, a zero crossing detector is more efficient.

[0062] An example of a zero-crossing detector for the detection of a positive-going input signal is shown in Figure 1. Initially, node **1** and node **2** are precharged to V_{DD} and ground, respectively. The ramp input voltage V_{IN} is applied according to the zero crossing circuit. At the time the input node crosses the threshold, node **1** is discharged rapidly, and node **2** is pulled up to V_{DD}. Since the zero crossing detector in Figure 1 is a dynamic circuit, there is no DC power consumption, allowing extremely low power and fast operation. For the detection of zero-crossing of a negative-going signal, a complementary circuit with a PMOS input transistor can be utilized.

[0063] As illustrated in Figure 6, the non-inverting integrator includes a waveform generator which is a current source **200**. As illustrated in Figure 6, a clock phase Φ_1 is applied to switches S_{11}, S_{13}, S_{22}, and S_{24}, and another phase Φ_2 is applied to switches S_{12}, S_{14}, and S_{21}. A zero crossing detector **30** is used to detect the point of time at which Node **100** crosses ground. The switch S_{23} is controlled by the output of the zero crossing detector **30**. The output of the zero crossing detector **30** is used to determine the time point to take the sample of the output voltage v_{out}.

[0064] The current source **200** charges the capacitors C_{S2} and the series connected C_{S1} and C_{I1}, generating a ramp. At the start of Φ_2, the output is briefly shorted to a known voltage V_{NEG}, the value of which is chosen to ensure the voltage v_1 at Node **100** crosses zero with signals in the normal operating range.

[0065] As illustrated in Figure 7, the non-inverting integrator includes a waveform generator **20** that produces, preferably, a plurality of segments in the waveform with varying rate of change of the output voltage. The first segment may be controlled so as to have the highest rate of change, with subsequent segments having progressively lower rate of change. The detection of zero crossing by the zero crossing detector **30** causes the waveform to advance to the next segment. An output signal v_{zc2} of the zero crossing detector **30** remains high until the zero crossing is detected in the last segment of the waveform.

[0066] One clock cycle of the timing diagram is shown in Figure 8. At the start of Φ_2, the waveform generator **20** produces an up ramp. The voltage v_1 is shown to cross zero at time t_1. One output, v_{zc1}, of the zero crossing detector **30** changes its state after a finite delay t_{d1}.

[0067] The delay t_{d1} represents finite delay of a typical zero crossing detector **30**. This change of state advances the waveform to the next segment.

[0068] Due to the delay t_{d1} of the zero crossing detector **30**, the voltage v_1 overshoots by a small amount above ground. The second segment of the waveform generator is a

down ramp to permit another zero crossing at time t_2. After a second delay t_{d2}, the output v_{zc2} of the zero crossing detector **30** goes low, causing the switch S_{23} to turn OFF, locking the sample of the output voltage v_{out}.

[0069] The delay t_{d2} of the second zero crossing is not necessarily the same as the delay associated with the first zero crossing t_{d1}. The delay t_{d2} contributes a small overshoot to the sampled output voltage. The effect of the overshoot can be shown to be constant offset in the sampled charge. In most sample-data circuits, such constant offset is of little issue.

[0070] The zero crossing detector **30** preferably becomes more accurate in detecting the zero crossing as the segments of the waveform advances. The first detection being a coarse detection, it doesn't have to be very accurate. Therefore, the detection can be made faster with less accuracy. The last zero crossing detection in a given cycle determines the accuracy of the output voltage. For this reason, the last zero crossing detection must be the most accurate.

[0071] The accuracy, speed, and the power consumption can be appropriately traded among progressive zero crossing detections for the optimum overall performance. For example, the first detection is made less accurately and noisier but is made faster (shorter delay) and lower power. The last detection is made more accurately and quieter while consuming more power or being slower (longer delay).

[0072] An example of a two-segment waveform generator constructed of two current sources (**210** and **220**) is shown in Figure 9. As illustrated in Figure 9, a clock phase Φ_1 is applied to switches S_{11}, S_{13}, S_{22}, and S_{24}, and another phase Φ_2 is applied to switches S_{12}, S_{14}, and S_{21}. A zero crossing detector **30** is used to detect the point of time at which Node **100** crosses ground. The switch S_{23} is controlled by the output of the zero crossing detector **30**. The output of the zero crossing detector **30** is used to determine the time point to take the sample of the output voltage v_{out}.

[0073] Current sources **210** and **220** charge the capacitors C_{S2} and the series connected C_{S1} and C_{I1} generating two segments of a ramp waveform. At the start of Φ_2, the output is briefly shorted to a known voltage V_{NEG}, the value of which is chosen to ensure the voltage v_1 crosses zero with signals in the normal operating range. During the first segment, the current source **210** is directed to the output, while during the second segment, the current source **220** is directed to the output, generating two different slopes of ramp.

[0074] As illustrated in Figure 10, the non-inverting integrator includes a level crossing detector **300** having plurality of thresholds. As illustrated in Figure 10, a clock

phase Φ_1 is applied to switches S_{11}, S_{13}, S_{22}, and S_{24}, and another phase Φ_2 is applied to switches S_{12}, S_{14}, and S_{21}. A level crossing detector **300** is used to detect the point of time at which Node **100** crosses one of plurality of predetermined levels as discussed below. The switch S_{23} is controlled by the output of the level crossing detector **300**. The output of the level crossing detector **300** is used to determine the time point to take the sample of the output voltage v_{out}.

[0075] The thresholds are predetermined voltage levels. The thresholds of the level crossing detector **300** can be adjusted to minimize overshoot.

[0076] For example, the threshold for the first detection may be made negative by a slightly smaller amount than the expected overshoot in the first segment. This minimizes the ramp-down time in the second segment. Also, the threshold for the second segment may be made more positive by the amount of the overshoot in the second segment in order to cancel the effect of the overshoot. Alternatively, the threshold for the first segment may be made more negative than the expected overshoot during the first segment. This permits the second segment to be a positive ramp rather than a negative ramp as shown in Figure 11.

[0077] It is advantageous to make the detection during the last segment to be the most accurate detection. The accuracy of the detection during the last segment is made higher than during other segments. This can be achieved by making the delay longer or making the power consumption higher during the last segment.

[0078] As illustrated in Figure 12, the non-inverting integrator includes a level crossing detector having two zero-crossing detectors, Zero Crossing Detector 1 (**310**) and Zero Crossing Detector 2 (**320**). As illustrated in Figure 12, a clock phase Φ_1 is applied to switches S_{11}, S_{13}, S_{22}, and S_{24}, and another phase Φ_2 is applied to switches S_{12}, S_{14}, and S_{21}. Zero Crossing Detector 1 (**310**) and Zero Crossing Detector 2 (**320**) are used to detect the point of time at which Node **100** crosses one of plurality of predetermined levels as discussed below. The switch S_{23} is controlled by the output of the Zero Crossing Detector 2 (**320**). The output of the Zero Crossing Detector 2 (**320**) is used to determine the time point to take the sample of the output voltage v_{out}.

[0079] The thresholds of the Zero Crossing Detector 1 (**310**) and Zero Crossing Detector 2 (**320**) are selected to minimize overshoot. For example, the threshold for Zero Crossing Detector 1 (**310**) may be made negative by a slightly smaller amount than the expected overshoot in the first segment. This minimizes the ramp-down time in the second segment. Also, the threshold for Zero Crossing Detector 2 (**320**) may be made more positive by the amount of the overshoot in the second segment in order to cancel

the effect of the overshoot. Alternatively, the threshold for Zero Crossing Detector 1 (**310**) may be made more negative than the expected overshoot during the first segment. This permits Zero Crossing Detector 2 (**320**) to be a positive ramp rather than a negative ramp.

[0080] In other words, Zero Crossing Detector 1 (**310**) makes a coarse detection, whereas Zero Crossing Detector 2 (**320**) makes a fine detection. Thus, it is advantageous to make Zero Crossing Detector 2 (**320**) to have a higher accuracy.

[0081] As illustrated in Figure 13, the non-inverting integrator includes a level crossing detector having two zero-crossing detectors, Zero Crossing Detector 1 (**310**) and Zero Crossing Detector 2 (**320**). As illustrated in Figure 13, a clock phase Φ_1 is applied to switches S_{11}, S_{13}, S_{22}, and S_{24}, and another phase Φ_2 is applied to switches S_{12}, S_{14}, and S_{21}. Zero Crossing Detector 1 (**310**) and Zero Crossing Detector 2 (**320**) are used to detect the point of time at which Node **100** crosses one of plurality of predetermined levels as discussed below. The switch S_{23} is controlled by the output of the Zero Crossing Detector 2 (**320**). The output of the Zero Crossing Detector 2 (**320**) is used to determine the time point to take the sample of the output voltage v_{out}.

[0082] Both detectors, Zero Crossing Detector 1 (**310**) and Zero Crossing Detector 2 (**320**), have nominally zero thresholds. The detection thresholds are determined by voltages V_{tr1} and V_{tr2} applied to the inputs of Zero Crossing Detector 1 (**310**) and Zero Crossing Detector 2 (**320**), respectively. Zero Crossing Detector 1 (**310**) makes a coarse detection, whereas Zero Crossing Detector 2 (**320**) makes a fine detection. Thus, it is advantageous to make Zero Crossing Detector 2 (**320**) to have a higher accuracy.

[0083] It is noted that the above-described embodiment may operate as a self-timed system. In this configuration, Rather than supplying constant frequency clock phases Φ_1 and Φ_2, the clock phases are derived from the outputs of Zero Crossing Detector 1 (**310**) and Zero Crossing Detector 2 (**320**). Figure 14 illustrates a self-timed operation.

[0084] As illustrated in Figure 14, the end of the phase Φ_2 is defined by the output of the detection during the last segment. The beginning of the clock phase Φ_1 is defined by a short delay, such as logic delays, after the end of Φ_2. The short delay is generally necessary to ensure non-overlapping clock phases. The end of the clock phase Φ_1 is determined by the zero crossing detection of the previous stage or the following stage in the similar manner.

[0085] It is noted that the various embodiments described above can be utilized in a pipeline analog-to-digital converter, an algorithmic analog-to-digital converter, a

switched-capacitor amplifier, a delta-sigma modulator, or a self-timed algorithmic analog-to-digital converter.

[0086] It is further noted that the various embodiments described above have signal paths that are single-ended, thus, it is desirable to provide differential signal paths. The various embodiments described below provide differential signal paths.

[0087] As noted above, it is desirable to substantially eliminate the errors associated with time delays. One solution to substantially eliminate the errors associated with time delays is to have the error in a form that can be easily managed.

[0088] For example, if a waveform generator produces a ramp whose slope is constant in each segment of the ramp, the error associated with the delays becomes a constant DC offset. A constant DC offset can be easily compensated or tolerated in most systems. However, simple waveform generators, for example, the one shown in Fig. 6, produce non-linear ramp signals. The nonlinearity in the ramp slope of the conventional sample-data circuits causes nonlinearity in the resulting sample-data circuit error. The non-linear error is difficult to compensate.

[0089] To address this problem, the present invention provides a circuit that generates ramp waveforms with plurality of linear segments of varying slopes whereby the slope is independent of the output voltage and load conditions in each segment of the ramp. By generating ramp waveforms with plurality of linear segments of varying slopes, the error is a plurality of constant DC offsets that can easily compensated for or tolerated.

[0090] Furthermore, to address this problem, the present invention provides a circuit that generates ramp waveforms with plurality of linear segments of varying slopes whereby the advancement to the next segment is controlled by an output of a zero crossing detector.

[0091] One embodiment of the present invention that provides a circuit that generates ramp waveforms with plurality of linear segments of varying slopes is illustrated in Figure 15. As illustrated in Figure 15, a sample-data circuit includes an amplifier **500** that preferably provides large open loop gain. A zero crossing detector **400** detects the condition when an input voltage v_1 crosses another input voltage v_2, at which time the output signal v_{zcd} changes, signaling the detection of zero-crossing.

[0092] It is noted that a continuous-time voltage comparator can be used as a zero crossing detector. It is further noted that the zero crossing detector **400** may have a non-zero threshold voltage, if desired. Thus, a voltage level detector can be employed instead.

[0093] As illustrated in Figure 15, before the start of the first segment of a ramp waveform generation, a capacitor **C** is precharged to a start voltage V_{start} by turning a switch S_1 ON and connecting a switch S_2 to the upper position, the upper position being connected to start voltage V_{start}. Next, the switch S_1 is turned OFF, and the switch S_2 is connected to the lower position. The capacitor **C** now provides negative feedback. In a single-slope operation as shown in Figure 5, current source **I** provides constant current. For a multi-slope operation as shown in Figures 8 and 11, the current source **I** is a variable current source, and set to one of a plurality of current levels I_1. The output voltage v_{out} is approximately a linear ramp given by $v_{out}=V_{start} + I_1t/C$. In one embodiment, the current source **I** is implemented by a resistor connected to a constant voltage. In another embodiment, the current source I is implemented by a MOS transistor.

[0094] If I_1 is positive, the resulting v_{out} is a positive-going ramp. In a multi-slope operation, when the output signal v_{zcd} of the zero crossing detector **400** changes at time $t=t_1$, the value of the current source **I** is changed to the next value I_2 in order to produce the next segment of the ramp. The output voltage v_{out} in the second segment is $v_{out}=V_{start} + I_1t_1/C + I_2t/C$.

[0095] A negative-going second segment of the ramp can be generated by making I_2 negative. More segments can be produced by changing the value of the current **I**. In this embodiment, a ramp waveform generator produces substantially constant slope within each segment regardless of the load condition.

[0096] Figure 16 shows another embodiment of the present invention created with CMOS technology. The structure and the operation are similar to the embodiment illustrated and described with respect to Figure 15.

[0097] As illustrated in Figure 16, an amplifier includes MOS transistors M_1 and M_2. A zero crossing detector **400** detects the condition when an input voltage v_1 crosses another input voltage v_2, at which time the output signal v_{zcd} changes, signaling the detection of a zero-crossing.

[0098] It is noted that a continuous-time voltage comparator can be used as a zero crossing detector. It is further noted that the zero crossing detector 400 may have a non-zero threshold voltage, if desired. Thus, a voltage level detector can be employed instead.

[0099] As illustrated in Figure 16, before the start of the first segment of a ramp waveform generation, a capacitor **C** is precharged by turning a switch S_1 ON and connecting a switch S_2 to the upper position, the upper position being connected to start

voltage V_{start}. This precharges the capacitor **C** to $V_{start} - V_{bias1}$. The voltage V_{bias1} may be approximately the same as the gate voltage of M_1. Next, the switch S_1 is turned OFF, and the switch S_2 is connected to the lower position. The capacitor **C** now provides negative feedback. In a single-slope operation as shown in Figure 5, current source **I** provides constant current. For a multi-slope operation as shown in Figures 8 and 11, the current source **I** is a variable current source, and set to one of the plurality of current levels I_1. The output voltage v_{out} is approximately a linear ramp given by $v_{out}=V_{start} + I_1t/C$. In one embodiment, the current source **I** is implemented by a resistor connected to a constant voltage. In another embodiment, the current source I is implemented by a MOS transistor.

[0100] If I_1 is positive, the resulting v_{out} is a positive-going ramp. In a multi-slope operation, when the output signal v_{zcd} of the zero crossing detector **400** changes at time $t=t_1$, the value of the current source **I** is changed to the next value I_2 in order to produce the next segment of the ramp. The output voltage v_{out} is $v_{out}=V_{start}+ I_1t_1/C + I_2t/C$.

[0101] A negative-going second segment of the ramp can be generated by making I_2 negative. More segments can be produced by changing the value of the current **I**. In this embodiment, a ramp waveform generator produces substantially constant slope within each segment regardless of the load condition.

[0102] Figure 17 shows another embodiment of the present invention. As illustrated in Figure 17, a sample-data circuit includes a differential amplifier **500** that provides, preferably, a large open-loop gain. Before the start of the ramp generation, the switch S_1 is closed, and a first value R_1 of the resistor **R** is selected.

[0103] By the negative feedback through the transistor M_1 and the resistor **R**, the voltage across the resistor **R** is maintained at $V_{bias}-V_{SS}$. Thus, the current through the resistor is $I_1= (V_{bias}-V_{SS}) /R_1$, and the initial output voltage is V_{bias}.

[0104] Next, the switch S_1 is opened. By the negative feedback through the transistor M_1, the capacitor **C**, and the resistor **R**, the voltage across **R** is still maintained at $V_{bias} -V_{SS}$ and the current through the resistor **R** at $I_1=(V_{bias}-V_{SS})/R_1$. The capacitor **C** is charged by the current I_1, giving the output voltage $v_{out}=V_{bias}+I_1t/C=V_{bias}+(V_{bias} - V_{SS})t/R_1C$.

[0105] In a multi-slope operation, when the output signal v_{zcd} of the zero crossing detector changes at time $t=t_1$, the value of the resistor **R** is changed to the next value R_2 in order to produce the next segment of the ramp. The output voltage v_{out} in the second segment is $v_{out}= V_{bias}+(V_{bias} -V_{SS})t_1/R_1C+(V_{bias} -V_{SS})t_2/R_2C$. More segments can be produced by further changing the value of the resistor **R**. In this embodiment, a ramp

waveform generator produces substantially constant slope within each segment regardless of the load condition.

[0106] The embodiment of Figure 17 can generate multiple segments of a positive-going ramp waveform. The ramp can be stopped by turning the switch S_2 ON, which cuts off the transistor M_1.

[0107] Figure 18 shows a complimentary embodiment of Figure 17. As illustrated in Figure 18, a sample-data circuit includes a differential amplifier **500** that provides, preferably, a large open-loop gain. Before the start of the ramp generation, the switch S_1 is closed, and a first value R_1 of the resistor **R** is selected.

[0108] By the negative feedback through the transistor M_1 and the resistor **R**, the voltage across the resistor **R** is maintained at V_{bias}-V_{DD}. Thus, the current through the resistor is $I_1 = (V_{bias}-V_{DD})/R_1$, and the initial output voltage is V_{bias}.

[0109] Next, the switch S_1 is opened. By the negative feedback through the transistor M_1, the capacitor **C**, and the resistor **R**, the voltage across **R** is still maintained at $V_{bias}-V_{DD}$ and the current through the resistor **R** at $I_1=(V_{bias}-V_{DD})/R_1$. The capacitor **C** is charged by the current I_1, giving the output voltage $v_{out}=V_{bias}+I_1t/C=V_{bias}+(V_{bias}-V_{DD})t/R_1C$.

[0110] In multi-slope operation, when the output signal v_{zcd} of the zero crossing detector changes at time $t=t_1$, the value of the resistor **R** is changed to the next value R_2 in order to produce the next segment of the ramp. The output voltage v_{out} in the second segment is $v_{out}= V_{bias}+(V_{bias}-V_{DD})t_1/R_1C+(V_{bias}-V_{DD})t_2/R_2C$. Multiple segments of a negative-going ramp waveform can be produced by further changing the value of the resistor **R**. In this embodiment, a ramp waveform generator produces substantially constant slope within each segment regardless of the load condition.

[0111] Both positive-going and negative-going segments can be generated by another embodiment, as illustrated by Figure 19. As illustrated by Figure 19, before the start of the first segment, switches S_1, S_2, S_3, and S_5 are closed, and S_4 is opened. This configuration precharges a capacitor C_1 at $V_{start} - V_{bias1}$ and another capacitor C_2 at $V_{start} - V_{bias2}$, setting the initial condition of the output voltage at V_{start}.

[0112] A first value $R_2(1)$ of the resistor R_2 is selected. By the negative feedback through the transistor M_2 and the resistor R_2, the voltage across R_2 is maintained at V_{bias2}-V_{SS}. Thus, the current through the resistor is given by $I_1= (V_{bias2}-V_{SS}) / R_2(1)$.

[0113] The first segment starts by opening switches S_3 and S_5. The capacitor C_2 is charged by the current I_1, giving a positive-going ramp output voltage. Negative-going segments can be produced by turning switches S_3 and S_4 ON, and turning S_1 and S_2 OFF.

In this embodiment, a ramp waveform generator produces substantially constant slope within each segment regardless of the load condition.

[0114] It is noted that since a zero crossing detector must detect the zero crossing preferably continuously, a continuous-time voltage comparator can be used as a zero-crossing detector.

[0115] Figure 20 illustrates an embodiment of a continuous-time voltage comparator to be used in the present invention. As illustrated in Figure 20, the continuous-time comparator includes a first amplifier stage **505** that amplifies the difference between the two input voltages v_1 and v_2.

[0116] The first amplifier stage **505** includes a clamping circuit **5050**, as illustrated in Figure 21, wherein the clamping circuit **5050** includes transistors M_8 and M_9. The clamping circuit **5050** limits the output voltage swing to shorten the delay. It is noted that a similar clamping circuit can be employed in other amplifier stages if desired.

[0117] As illustrated in Figure 20, the output of the amplifier **505** is connected to a bandwidth select circuit **600**. The output of the first amplifier stage is further amplified by a second amplifier stage **510**. A latch circuit **700** generates logic level output. It is noted that a Schmitt trigger-type circuit can be used as a continuous-time latch.

[0118] The bandwidth select circuit **600** provides different bandwidths depending on different segments of the ramp waveform. The zero crossing detection during the first segment can be a coarse detection, as the zero crossing detection during the first segment does not have to be very accurate. However, since the detection is made while the input to the detector is changing rapidly, the detection needs to be fast.

[0119] On the other hand, the zero crossing detection during the last segment in a given cycle determines the accuracy of the output voltage. Therefore, the bandwidth during the first segment can be designed to be high and progressively lower for detection in successive segments to reduce noise for accurate zero crossing detection.

[0120] Since the mean-square value of noise is approximately proportional to bandwidth, the bandwidth is made lower during the later segments by the bandwidth select circuit. The bandwidth selection is made at the output of the first amplifier stage **505** by the input signal **BW**, as illustrated by Figure 21. Alternatively, the bandwidth selection can be made at the output of the second amplifier stage **510** as illustrated by Figure 22. Also, it is noted that the number of amplifier stages is increased in a high resolution operation.

[0121] An alternative method of bandwidth change is to control the bias currents I_{bias1} and/or I_{bias2} by the zero crossing detector instead of switching in or out the band-

limiting capacitors C_1 and C_2. The higher the bias currents of a stage, the higher the bandwidth of that stage becomes.

[0122] As noted above, Figure 21 illustrates another embodiment of a continuous-time voltage comparator to be used in the present invention. As illustrated in Figure 21, a first amplifier stage **505** includes transistors M_1 and M_2 and resistors R_1 and R_2. A second amplifier stage **510** includes transistors M_5 and M_6 and resistors R_3 and R_4.

[0123] It is noted that a clamping circuit that limits the output voltage swing can be employed to shorten the delay in the amplifier stages.

[0124] Since the effect of the noise from the second amplifier stage **510** is reduced by the voltage gain of the first stage **505**, a second stage bias current I_{bias2} can be made lower than a first stage bias current I_{bias1} in order to reduce power consumption.

[0125] As illustrated in Figure 21, a latch includes transistors M_7 and M_8 and inverters Inv_1 and Inv_2. A bandwidth select circuit **600** includes switches M_3 and M_4 and capacitors C_1 and C_2

[0126] For the zero crossing detection during the first segment where high speed is desired, the switches M_3 and M_4 are kept OFF. The bandwidth of the first amplifier stage **505** is determined by the resistors R_1 and R_2 and parasitic capacitance at the output of the first stage **505**.

[0127] For the zero crossing detection during the segments where low noise is necessary, the switches M_3 are M_4 are turned ON. The added capacitance from C_1 and C_2 at the outputs of the first stage **505** reduces the bandwidth, lowering the noise.

[0128] With nominally matched transistors and resistors, the detection threshold is zero. However, by varying either R_1 or R_2, the detection threshold can be varied to cancel the effect of overshoot in each segment of the ramp.

[0129] Figure 22 illustrates another embodiment of a continuous-time voltage comparator to be used in the present invention. As illustrated in Figure 22, a first amplifier stage **505** includes transistors M_1 and M_2 and resistors R_1 and R_2. A second amplifier stage **510** includes transistors M_5 and M_6 and resistors R_3 and R_4.

[0130] It is noted that a clamping circuit that limits the output voltage swing can be employed to shorten the delay in the amplifier stages.

[0131] Since the effect of the noise from the second amplifier stage **510** is reduced by the voltage gain of the first stage **505**, a second stage bias current I_{bias2} can be made lower than a first stage bias current I_{bias1} in order to reduce power consumption.

[0132] As illustrated in Figure 22, a latch includes transistors M_7 and M_8 and inverters Inv_1 and Inv_2. A bandwidth select circuit includes switches M_3 and M_4 and capacitors C_1 and C_2.

[0133] For the zero crossing detection during the first segment where high speed is desired, the switches M_3 and M_4 are kept OFF. The bandwidth of the first amplifier stage **505** is determined by the resistors R_1 and R_2 and parasitic capacitance at the output of the first stage **505**.

[0134] For the zero crossing detection during the segments where low noise is necessary, the switches M_3 are M_4 are turned ON. The added capacitance from C_1 and C_2 at the outputs of the second stage **510** reduces the bandwidth, lowering the noise.

[0135] With nominally matched transistors and resistors, the detection threshold is zero. However, by varying either R_1 or R_2, the detection threshold can be varied. This is a useful feature to cancel the effect of overshoot in each segment of the ramp.

[0136] Figure 23 illustrates another embodiment of a continuous-time voltage comparator to be used in the present invention. As illustrated in Figure 23, a first amplifier stage **505** includes M_1, M_2, M_3, and M_4. A second amplifier stage **510** includes transistors M_7, M_8, M_9, and M_{10}. Bias voltages V_{bias1} and V_{bias2} are chosen to provide appropriate gain in the first and the second amplifier stages.

[0137] For small gain, the load transistors M_3, M_4, M_9, and M_{10} are biased in the triode region. If a large voltage gain is desired from the first stage amplifier **505**, the load transistors M_3 and M_4 can be biased in the saturation region. In such cases, the voltage V_{bias1} is controlled by a common-mode feedback circuit.

[0138] It is noted that a clamping circuit, which limits the output voltage swing, can be utilized to shorten the delay in the amplifier stages.

[0139] Since the effect of the noise from the second amplifier stage **510** is reduced by the voltage gain of the first stage **505**, the second stage bias current I_{bias2} can be made lower than the first stage bias current I_{bias1} in order to reduce power consumption.

[0140] As illustrated in Figure 23, a latch includes transistors M_{11} and M_{12} and inverters Inv_1 and Inv_2. A bandwidth select circuit includes switches M_5 and M_6 and capacitors C_1 and C_2.

[0141] For the zero crossing detection during the first segment where high speed is desired, the switches M_5 are M_6 are kept OFF. The bandwidth of the first amplifier stage **505** is determined by bias voltages V_{bias1} and parasitic capacitance at the output of the first stage.

[0142] For the zero crossing detection during the segments where low noise is necessary, the switches M_5 are M_6 are turned ON. The added capacitance from C_1 and C_2 at the outputs of the first stage reduces the bandwidth, lowering the noise. With nominally matched transistors and resistors, the detection threshold is zero. However, by varying the gate voltages on M_3 or M_4 individually, the detection threshold can be varied to cancel the effect of overshoot in each segment of the ramp.

[0143] Figure 24 illustrates another embodiment of a continuous-time voltage comparator to be used in the present invention. As illustrated in Figure 24, a first amplifier stage **505** includes transistors M_1, M_2, M_3, and M_4. A second amplifier stage **510** includes transistors M_7, M_8, M_9, and M_{10}.

[0144] It is noted that a clamping circuit, which limits the output voltage swing, can be utilized to shorten the delay in the amplifier stages.

[0145] Bias voltages V_{bias1} and V_{bias2} are controlled together with transistor sizes and bias currents for appropriate gain and bandwidth in the first and the second amplifier stages. For small gain and large bandwidth, the load transistors M_3, M_4, M_9, and M_{10} are biased in the triode region.

[0146] Bandwidth can be reduced and gain made larger by raising one or both of the bias voltages. Alternatively, bandwidth can be reduced and gain made larger by making bias current I_{bias1} lower. If larger voltage gain and correspondingly low bandwidth is desired, the load transistors M_3 and M_4 can be biased in the saturation region. In such cases, the voltage V_{bias1} is controlled by a common-mode feedback circuit.

[0147] With nominally matched transistors and resistors, the detection threshold is zero. However, by varying the gate voltages on M_3 or M_4 individually, the detection threshold can be varied to cancel the effect of overshoot in each segment of the ramp.

[0148] Figure 25 illustrates another embodiment of a continuous-time voltage comparator with offset cancellation to be used in the present invention. As illustrated in Figure 25, a first amplifier stage **505** includes transistors M_1 and M_2 and resistors R_1 and R_2. A second amplifier stage **510** includes transistors M_5 and M_6 and resistors R_3 and R_4.

[0149] It is noted that a clamping circuit, which limits the output voltage swing, can be utilized to shorten the delay in the amplifier stages.

[0150] Since the effect of the noise from the second amplifier stage **510** is reduced by the voltage gain of the first stage **505**, a second stage bias current I_{bias2} can be made lower than a first stage bias current I_{bias1} in order to reduce power consumption.

[0151] As illustrated in Figure 25, a latch includes transistors M_7 and M_8 and inverters Inv_1 and Inv_2. A bandwidth select circuits include switches M_3 and M_4 and capacitors C_1 and C_2.

[0152] During the offset cancellation phase, switches M_3 and M_4 are closed so that the system common-mode voltage V_{CM} can be applied to inputs, v_1 and v_2, and the desired threshold V_{th} is added to the upper input v_1. The offset of the first stage amplifier **505** plus the desired threshold V_{th} is amplified and output from the first stage **505**. This voltage is differentially sampled on capacitors C_1 and C_2.

[0153] Next, switches M_3 and M_4 are opened, and the comparator operates normally. The voltage sampled on C_1 and C_2 counteracts with the offset in the first amplified stage canceling the effect and provides accurate detection threshold of V_{th}.

[0154] Figure 26 illustrates another embodiment of a continuous-time voltage comparator with offset cancellation to be used in the present invention. As illustrated in Figure 26, an offset cancellation is included to cancel the offset voltage due to device mismatches in the first stage amplifier.

[0155] It is noted that similar offset cancellation method can be applied to other amplifier stages if greater precision is desired.

[0156] Figure 26 illustrates an open loop offset cancellation method; however, it is noted that other methods of offset cancellation can be utilized

[0157] During the offset cancellation phase, switches S_1 and S_2 are closed so that the inputs to the amplifiers **505** and **510** are pulled to ground. The offset of the first stage amplifier **505** is amplified and shows up at the output of the first stage. This voltage is sampled on a capacitor **C**. Next, switches S_1 and S_2 are opened, and the comparator operates normally. The voltage sampled on **C** counteracts with the offset in the first amplified stage canceling the effect of the offset.

[0158] Figure 27 illustrates another embodiment of a zero crossing detector. As illustrated in Figure 27, a zero crossing detector includes plurality of threshold voltages. The circuit in Figure 27 provides two different detection thresholds although more thresholds can be introduced as desired.

[0159] A first voltage V_{th1} is first applied to the input of the first stage amplifier **505** by throwing the switch S_1 to a first position. Switches S_2 and S_4 are closed to sample the output voltage of the first stage amplifier **505**. The switch S_4 is first opened, and then S_2 is opened.

[0160] Next, a second voltage V_{th2} is first applied to the input of the first stage amplifier **505** by throwing the switch S_1 to a second position. Switches S_3 and S_4 are

closed to sample the output voltage of the first stage amplifier **505**. The switch S_4 is first opened, and then S_3 is opened.

[0161] The zero crossing detector is then operated normally by throwing the switch S_1 to the third (open) position. With S_2 closed, the first detection threshold V_{th1} is selected, and with S_3 closed, the second detection threshold V_{th2} is selected. Each detection threshold can be adjusted to cancel the effect of overshoot during each segment.

[0162] Figure 28 illustrates another embodiment of a zero crossing detector. As illustrated in Figure 28, a zero crossing detector includes a plurality of zero-crossing detectors. A first zero-crossing detector is preferably fast, but the first zero-crossing detector is not necessarily very accurate. On the other hand, a second zero crossing detector is preferably low noise and high accuracy, but the second zero crossing detector is not necessarily fast.

[0163] The first detector is activated during the first segment, whereas the second detector is activated in the second segment. The detection threshold of each detector can be adjusted to cancel the effect of overshoot during each segment.

[0164] As illustrated in Figure 28, the first zero crossing detector includes a first stage amplifier **505**, a second stage amplifier **510**, and a first latch **700**. The second zero crossing detector includes a third amplifier **515** and a second latch **710**.

[0165] For fast speed, the third amplifier **515** is a Schmitt trigger type with positive feedback. The detection thresholds for each zero crossing detector are optimized separately to cancel the effect of the overshoot. The bandwidth of the first detector is made lower than that of the second detector for lower noise.

[0166] While various examples and embodiments of the present invention have been shown and described, it will be appreciated by those skilled in the art that the spirit and scope of the present invention are not limited to the specific description and drawings herein, but extend to various modifications and changes.

What is claimed is:

1. A circuit, comprising:

a level-crossing detector to generate a level-crossing detection signal when an input signal crosses a predetermined voltage level;

a sampling switch, operatively coupled to said level-crossing detector, said sampling switch turning OFF when said level-crossing detection signal indicates a level-crossing; and

a waveform generator operatively coupled to said level-crossing detector;

said waveform generator including an amplifier.

2. The circuit as claimed in claim 1, wherein said waveform generator further includes a current source.

3. The circuit as claimed in claim 2, wherein said current source is a current source is a variable current source;

said variable current source being operatively coupled to said level-crossing detector;

said variable current source changing a current level therefrom in response to said level-crossing detection signal.

4. The circuit as claimed in claim 1, wherein said waveform generator produces a predetermined waveform.

5. The circuit as claimed in claim 1, wherein said waveform generator produces a plurality of segments, each segment having a distinct substantially constant slope, said plurality of segments forming a predetermined waveform.

6. The circuit as claimed in claim 5, wherein said waveform generator provides a predetermined waveform to compensate for a voltage error generated by a finite delay associated with said level-crossing detector.

7. The circuit as claimed in claim 1, wherein said waveform generator includes a capacitor, said capacitor being operatively connectable to said amplifier so as to enable a negative feedback loop.

8. The circuit as claimed in claim 7, wherein said waveform generator further includes a switch to enable said capacitor to be operatively connected to said amplifier as an element of a negative feedback loop.

9. The circuit as claimed in claim 1, wherein said level-crossing detector is a zero-crossing detector.

10. The circuit as claimed in claim 1, wherein said waveform generator produces a predetermined positive slope waveform.

11. The circuit as claimed in claim 1, wherein said waveform generator produces a predetermined negative slope waveform.

12. The circuit as claimed in claim 2, wherein said current source comprises a constant voltage source and a resistor.

13. The circuit as claimed in claim 3, wherein said variable current source comprises a constant voltage source and a variable resistor.

14. The circuit as claimed in claim 3, wherein said variable current source comprises plurality of selectable current sources.

15. A circuit, comprising:

a level-crossing detector to generate a level-crossing detection signal when an input signal crosses a predetermined voltage level; and

a waveform generator, operatively coupled to said level-crossing detector, to produce a positive slope waveform and a negative slope waveform;

said waveform generator including,

a first amplifier,

a second amplifier, and

a switching circuit;

said switching circuit switching causing said positive slope waveform or said negative slope waveform to be output from said waveform generator.

16. The circuit as claimed in claim 15, wherein said waveform generator produces at least one positive slope segment and at least one negative slope segment, each positive slope segment having a distinct substantially constant slope, each negative slope segment having a distinct substantially constant slope.

17. The circuit as claimed in claim 15, wherein said waveform generator provides a predetermined waveform to compensate for a voltage error generated by a finite delay associated with said level-crossing detector.

18. The circuit as claimed in claim 15, wherein said waveform generator includes a first capacitor and a second capacitor, said first capacitor being operatively connectable to said first amplifier so as to enable a negative feedback loop, said second capacitor being operatively connectable to said second amplifier so as to enable a negative feedback loop.

19. The circuit as claimed in claim 15, wherein said level-crossing detector is a zero-crossing detector.

20. The circuit as claimed in claim 15, wherein said variable current source is a constant voltage source and a variable resistor.

21. A method for sampling an analog signal, the method comprising:
(a) sampling an input voltage using the switched capacitance network;
(b) generating a ramp waveform by negative feedback;
(c) applying negative feedback to linearize the ramp waveform;
(d) determining when a node voltage of the switched capacitance network crosses a first predetermined level; and
(e) providing a sample of an output voltage of the switched capacitance network.

22. The method as claimed in claim 21, wherein the first predetermined level is a zero voltage level.

23. The method as claimed in claim 21, wherein the ramp waveform has at least one positive slope.

24. The method as claimed in claim 21, wherein the ramp waveform has at least one negative slope.

25. A method for sampling an analog signal, the method comprising:
(a) sampling an input voltage using the switched capacitance network;
(b) determining when a node voltage of the switched capacitance network crosses a predetermined level;
(c) generating a voltage ramp signal in response to the determination of when the node voltage of the switched capacitance network crosses the predetermined level;
(d) applying negative feedback to linearize the voltage ramp signal; and
(e) providing a sample of an output voltage of the switched capacitance network.

26. The method as claimed in claim 25, wherein the first predetermined level is a zero voltage level.

27. The method as claimed in claim 25, wherein the ramp waveform has a positive slope.

28. The method as claimed in claim 25, wherein the ramp waveform has a negative slope.

29. The method as claimed in claim 25, wherein each voltage ramp signal has a positive slope.

30. The method as claimed in claim 25, wherein each voltage ramp signal has a negative slope.

31. The method as claimed in claim 25, wherein the voltage ramp signal have negative and positive slopes.

32. The method as claimed in claim 25, wherein the voltage ramp signal has alternating negative and positive slopes.

33. A zero-crossing detector circuit, comprising:

an amplifier stage; and

a bandwidth controller operatively connected to said amplifier stage;

said bandwidth controller providing a variable bandwidth for the zero-crossing detector circuit so that the zero-crossing detector circuit provides a first level of zero-crossing detection coarseness during a first period of time and a second level of zero-crossing detection coarseness during a second period of time, said first level of zero-crossing detection coarseness being coarser than said second level of zero-crossing detection coarseness.

34. The zero-crossing detector circuit as claimed in claim 33, wherein said amplifier stage includes a clamping circuit to shorten a delay in the amplifier stage.

35. The zero-crossing detector circuit as claimed in claim 33, wherein said bandwidth controller comprises a capacitor and a switch.

36. The zero-crossing detector circuit as claimed in claim 33, further comprising a waveform generator to produce a predetermined waveform.

37. The zero-crossing detector circuit as claimed in claim 36, wherein said bandwidth controller provides said variable bandwidth in response to said predetermined waveform.

38. The zero-crossing detector circuit as claimed in claim 33, further comprising a plurality of bandwidth controllers, each bandwidth controller being operatively connected to said amplifier stage.

39. A zero-crossing detector circuit, comprising:

an amplifier stage, said amplifier stage including a variable current source; and

a bandwidth controller operatively connected to the variable current source of said amplifier stage;

said bandwidth controller controlling a current level of the variable current source connected thereto so that the zero-crossing detector circuit provides a first level of zero-crossing detection coarseness during a first period of time and a second level of zero-

crossing detection coarseness during a second period of time, said first level of zero-crossing detection coarseness being coarser than said second level of zero-crossing detection coarseness.

40. The zero-crossing detector as claimed in claim 39, wherein said amplifier stage includes a clamping circuit to shorten a delay in the amplifier stage.

41. The zero-crossing detector circuit as claimed in claim 39, further comprising a waveform generator to produce a predetermined waveform.

42. The zero-crossing detector circuit as claimed in claim 41, wherein said bandwidth controller controls the current level of the variable current source operatively connected thereto in response to said predetermined waveform.

43. A switched-capacitor circuit, comprising:

a zero-crossing detector to generate a zero-crossing detection signal when an input signal crosses a predetermined voltage level; and

a waveform generator operatively coupled to said zero-crossing detector;

said waveform generator including,

an amplifier, and

a variable current source;

said zero-crossing detector including,

an amplifier stage, and

a bandwidth controller operatively connected to said amplifier stage;

said bandwidth controller providing a variable bandwidth for the zero-crossing detector so that the zero-crossing detector provides a first level of zero-crossing detection coarseness during a first period of time and a second level of zero-crossing detection coarseness during a second period of time, said first level of zero-crossing detection coarseness being coarser than said second level of zero-crossing detection coarseness.

44. The switched-capacitor circuit as claimed in claim 43, wherein said amplifier stage includes a clamping circuit to shorten a delay in the amplifier stage.

45. The switched-capacitor circuit as claimed in claim 43, wherein said bandwidth controller comprises a capacitor and a switch.

46. The switched-capacitor circuit as claimed in claim 43, further comprising a waveform generator to produce a predetermined waveform.

47. The switched-capacitor circuit as claimed in claim 46, wherein said bandwidth controller provides said variable bandwidth in response to said predetermined waveform.

48. The switched-capacitor circuit as claimed in claim 43, further comprising a plurality of bandwidth controllers, each bandwidth controller being operatively connected to said amplifier stage.

49. A switched-capacitor circuit, comprising:

a level-crossing detector to generate a level-crossing detection signal when an input signal crosses a predetermined voltage level; and

a waveform generator operatively coupled to said level-crossing detector;

said waveform generator including,

an amplifier, and

a variable current source;

said level-crossing detector including,

an amplifier stage, and

a bandwidth controller operatively connected to said amplifier stage;

said bandwidth controller providing a variable bandwidth for the level-crossing detector circuit so that the level-crossing detector circuit provides a first level of level-crossing detection coarseness during a first period of time and a second level of level-crossing detection coarseness during a second period of time, said first level of level-crossing detection coarseness being coarser than said second level of level-crossing detection coarseness.

50. The switched-capacitor circuit as claimed in claim 49, wherein said amplifier stage includes a clamping circuit to shorten a delay in the amplifier stage.

51. The switched-capacitor circuit as claimed in claim 49, wherein said bandwidth controller comprises a capacitor and a switch.

52. The switched-capacitor circuit as claimed in claim 49, further comprising a waveform generator to produce a predetermined waveform.

53. The switched-capacitor circuit as claimed in claim 52, wherein said bandwidth controller provides said variable bandwidth in response to said predetermined waveform.

54. The switched-capacitor circuit as claimed in claim 49, further comprising a plurality of bandwidth controllers, each bandwidth controller being operatively connected to said amplifier stage.

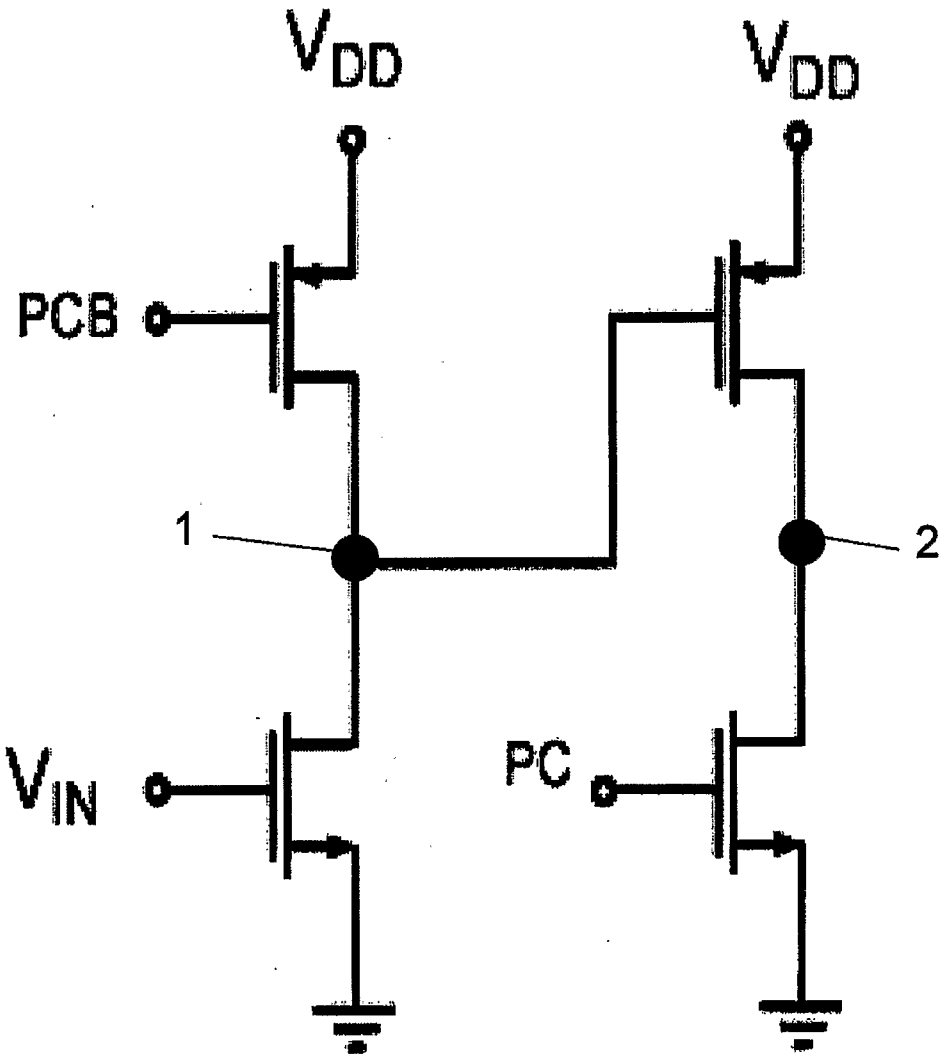


FIGURE 1

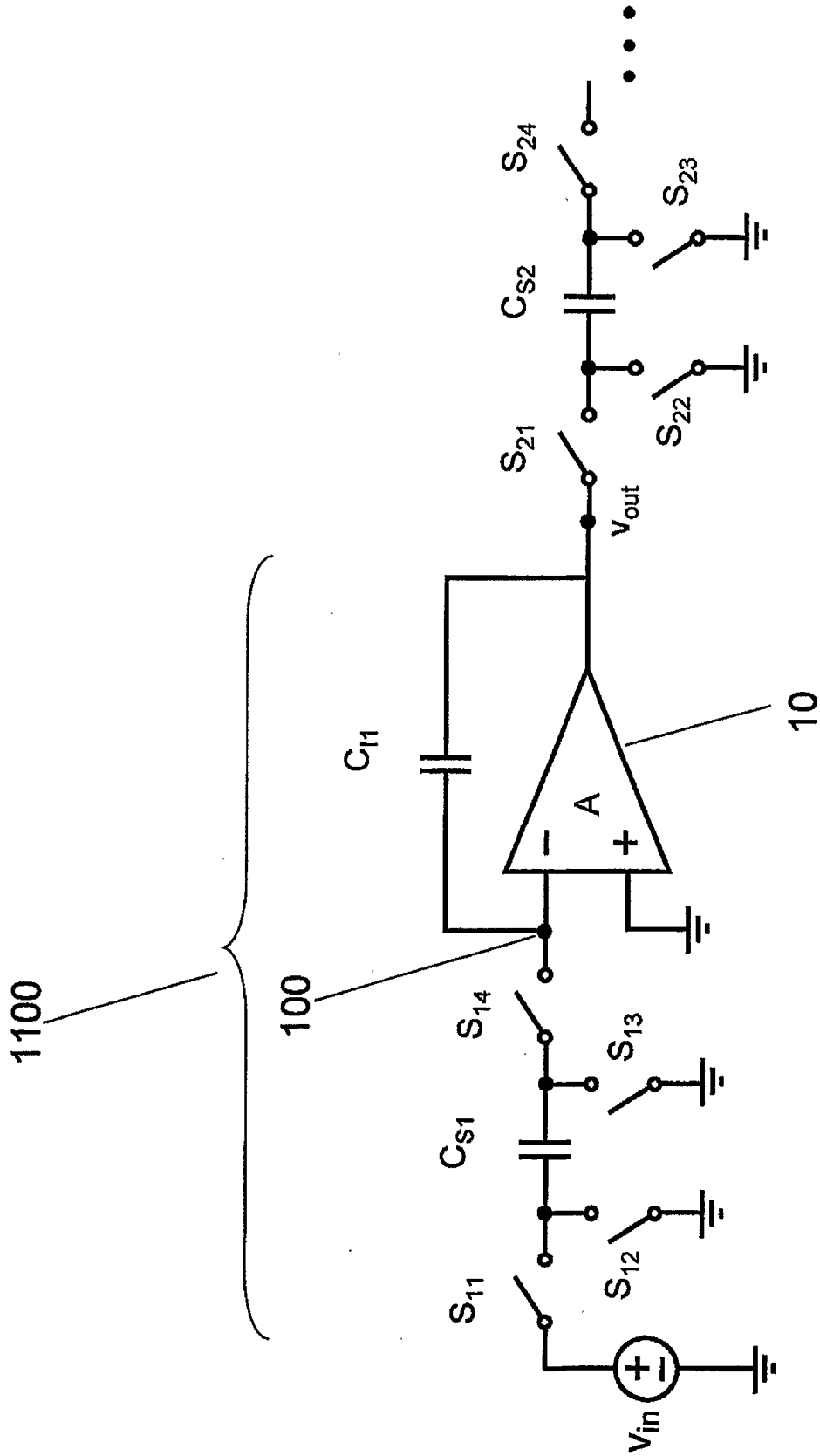
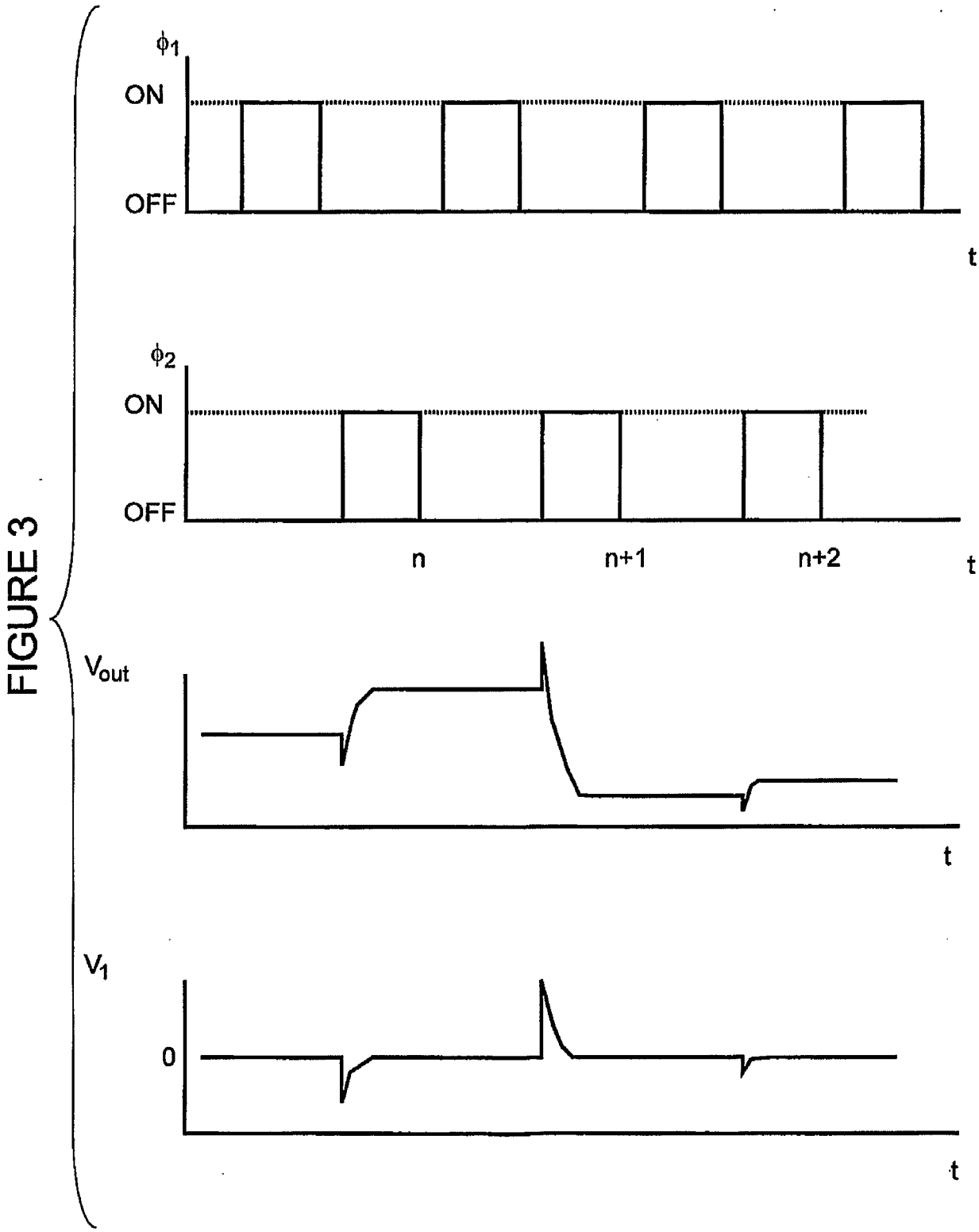

1100
100
10
A
C_{I1}
C_{S1}
C_{S2}
S_{11}
S_{12}
S_{13}
S_{14}
S_{21}
S_{22}
S_{23}
S_{24}
V_{out}
V_{in}

FIGURE 2

FIGURE 3



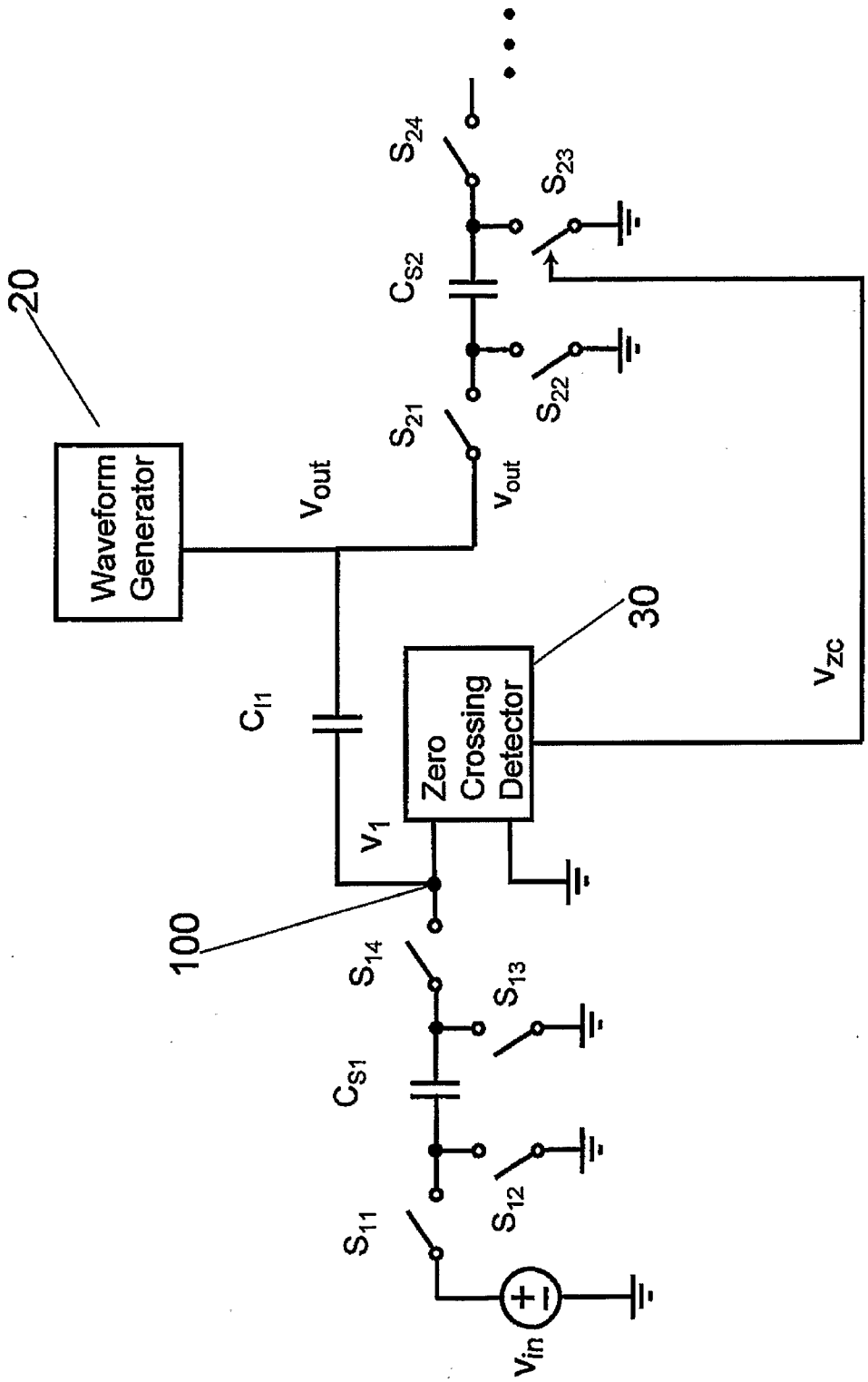
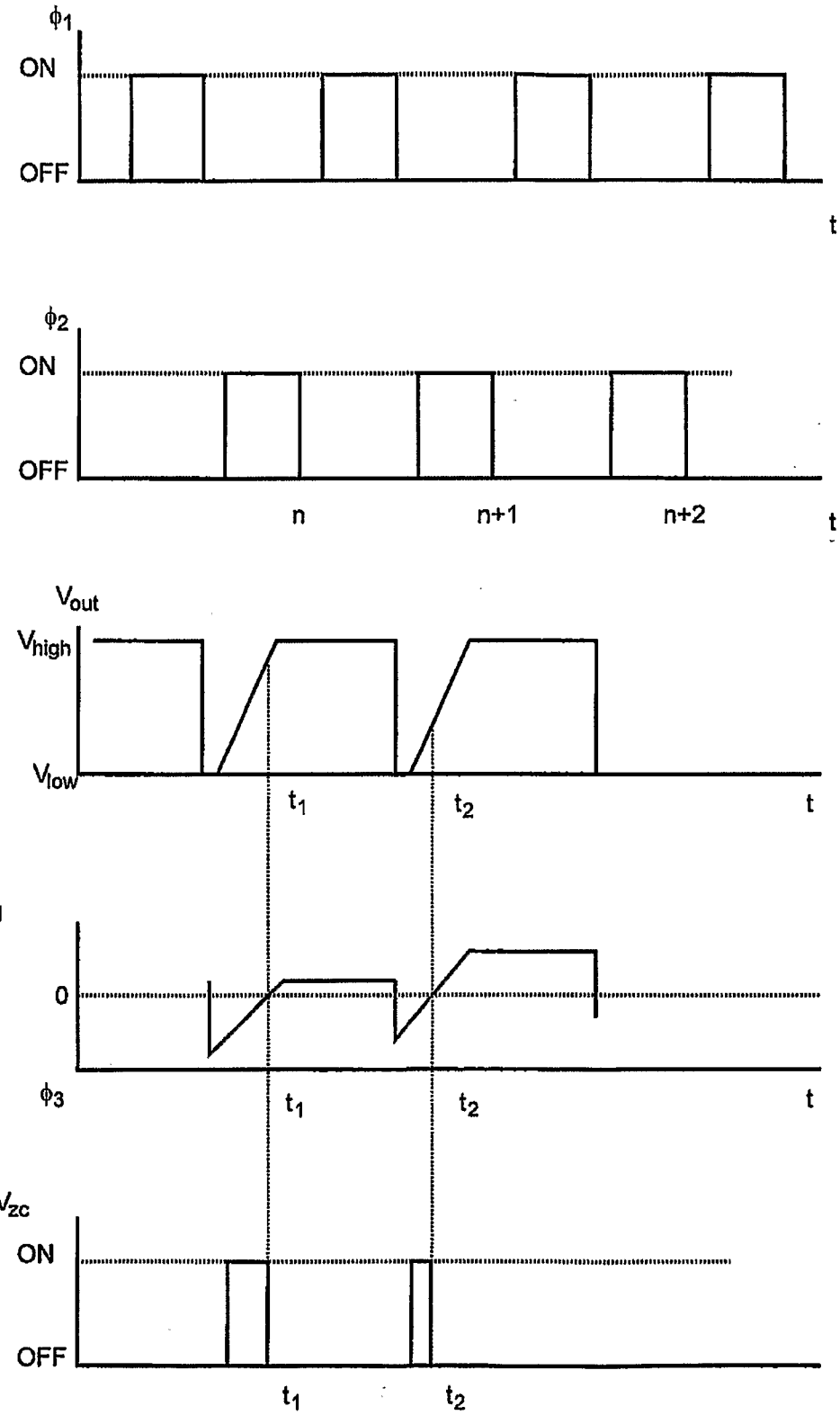

20
Waveform Generator
V_{out}
V_{out}
S_{21}
S_{22}
S_{23}
S_{24}
C_{S2}
30
Zero Crossing Detector
V_{ZC}
C_{I1}
V_1
100
S_{11}
S_{12}
S_{13}
S_{14}
C_{S1}
V_{in}

FIGURE 4

FIGURE 5


ϕ1
ON
OFF
t
ϕ2
ON
OFF
n
n+1
n+2
t
Vout
Vhigh
Vlow
t1
t2
t
V1
0
ϕ3
t1
t2
t
Vzc
ON
OFF
t1
t2

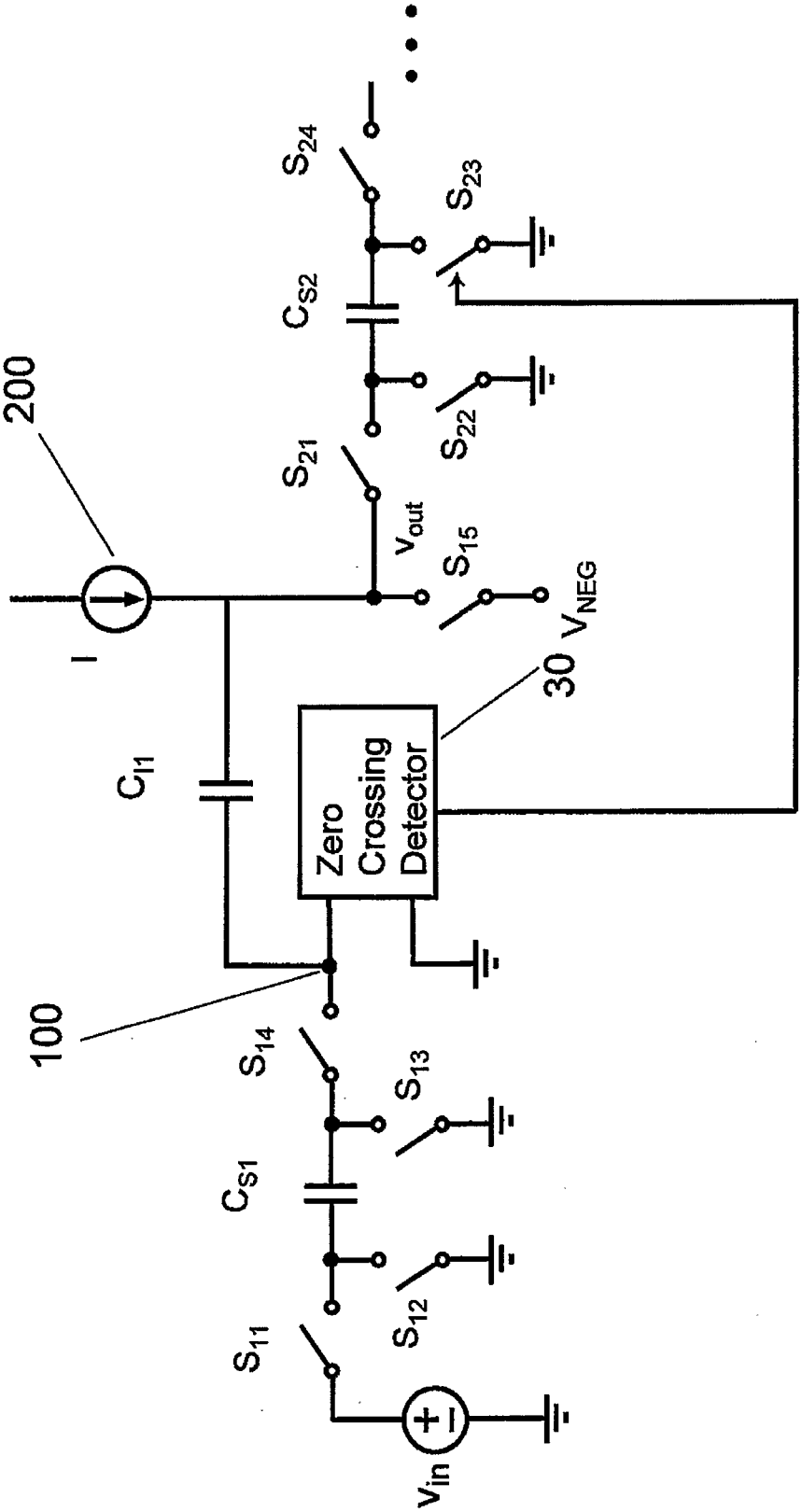

200
I
C_{I1}
100
Zero Crossing Detector
30
V_{NEG}
S_{15}
V_{out}
S_{21}
S_{22}
C_{S2}
S_{23}
S_{24}
S_{11}
S_{12}
C_{S1}
S_{13}
S_{14}
V_{in}

FIGURE 6

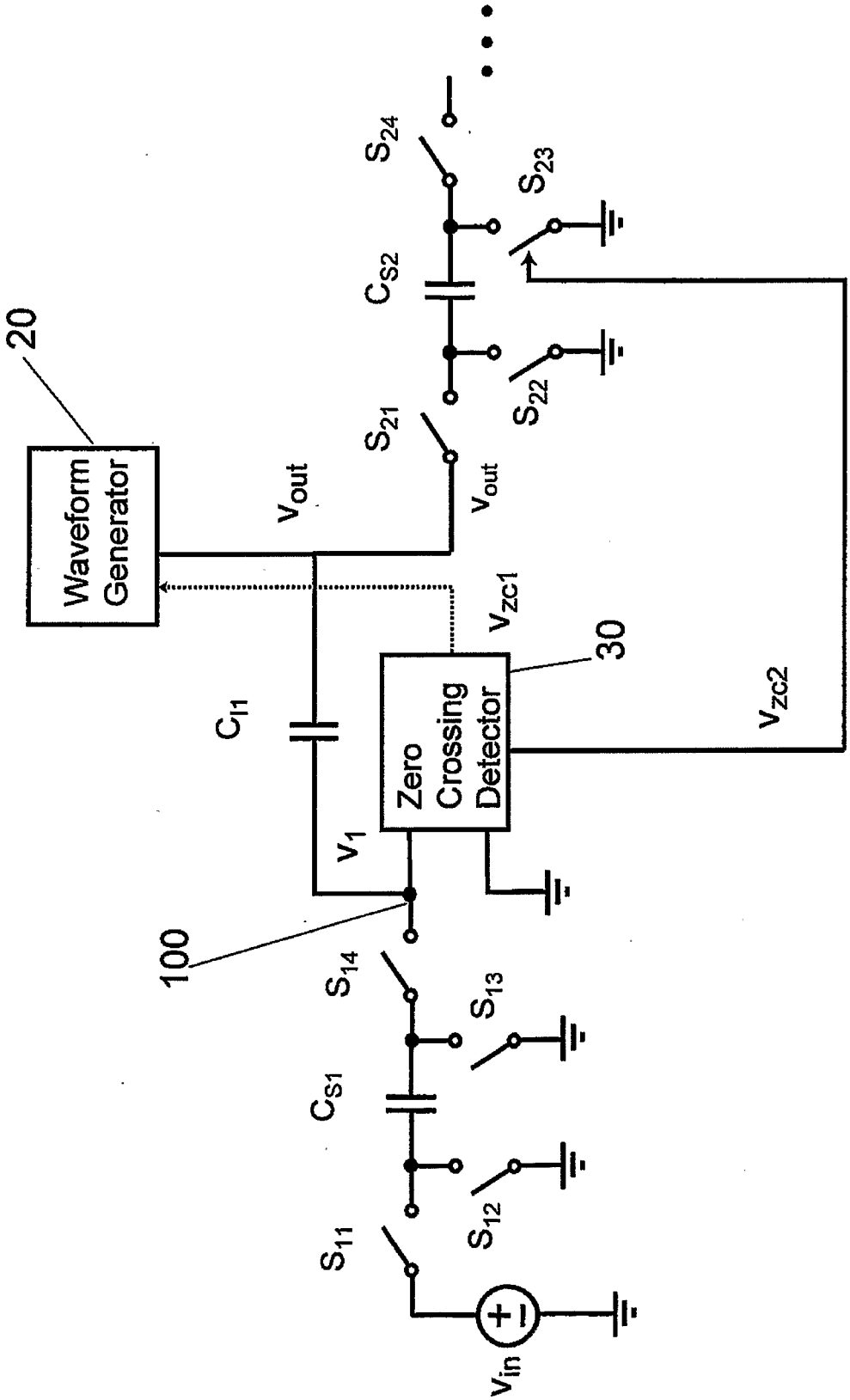
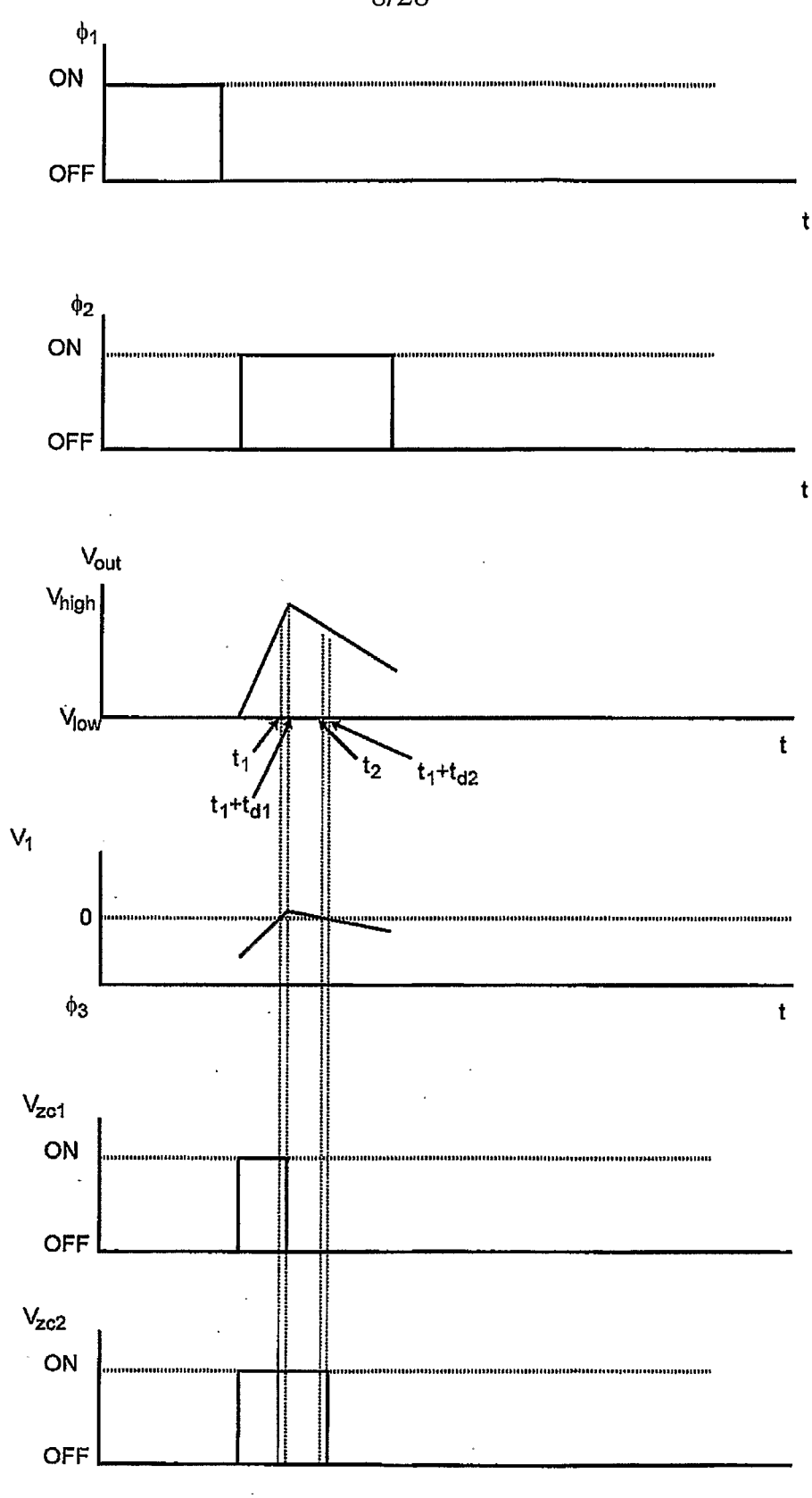

20
Waveform Generator
V_{out}
V_{out}
S_{21}
S_{22}
S_{23}
S_{24}
C_{S2}
V_{zc1}
30
Zero Crossing Detector
V_{zc2}
C_{I1}
V_1
100
S_{11}
S_{12}
S_{13}
S_{14}
C_{S1}
V_{in}

FIGURE 7

FIGURE 8


ϕ_1
ON
OFF
t
ϕ_2
ON
OFF
t
V_{out}
V_{high}
V_{low}
t
t_1
t_1+t_{d1}
t_2
t_1+t_{d2}
V_1
0
ϕ_3
t
V_{zc1}
ON
OFF
V_{zc2}
ON
OFF

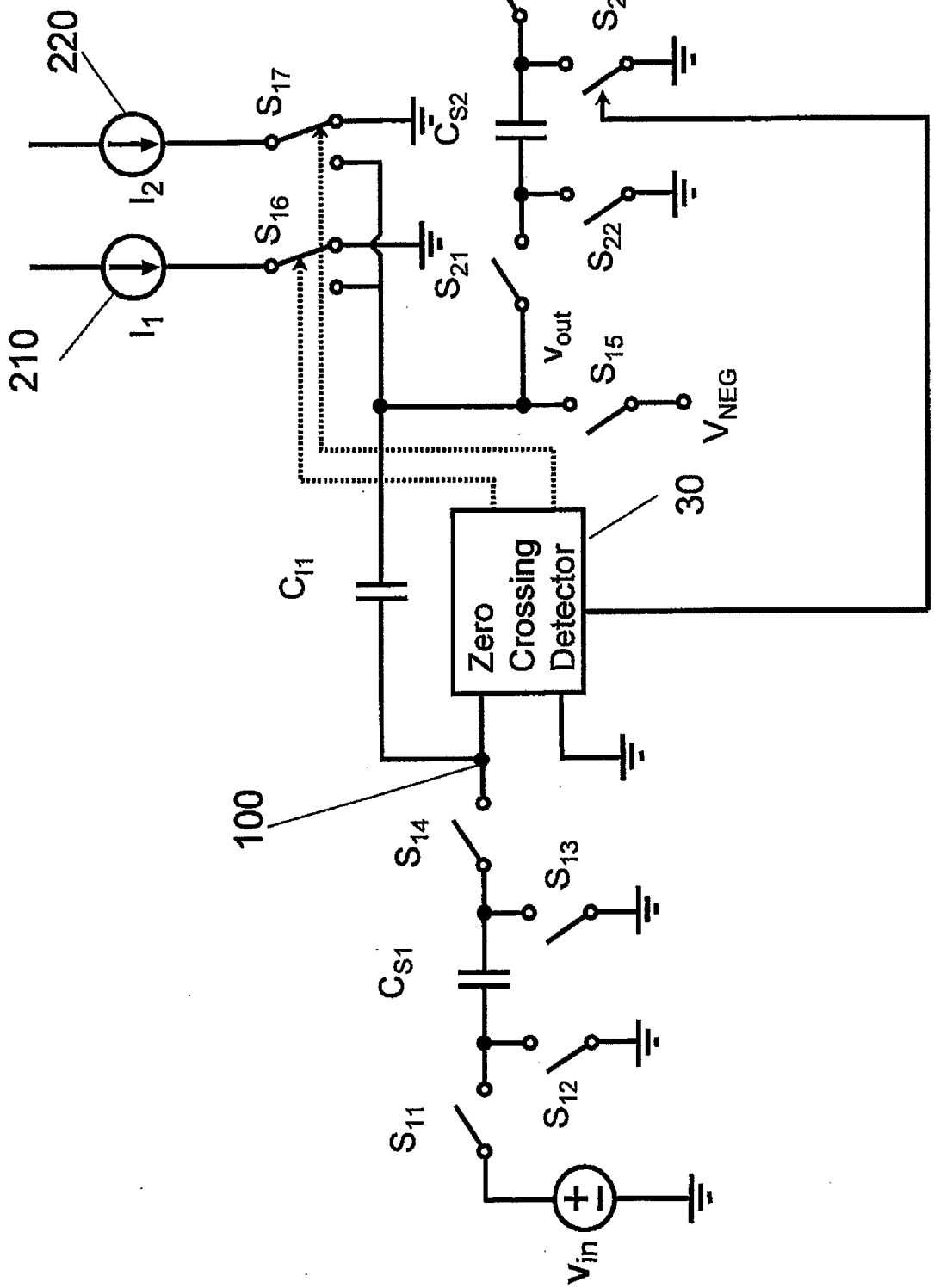

220
210
I_2
I_1
S_{17}
S_{16}
C_{S2}
S_{24}
S_{23}
S_{22}
S_{21}
V_{out}
S_{15}
V_{NEG}
30
Zero Crossing Detector
C_{I1}
100
S_{14}
S_{13}
C_{S1}
S_{12}
S_{11}
V_{in}

FIGURE 9

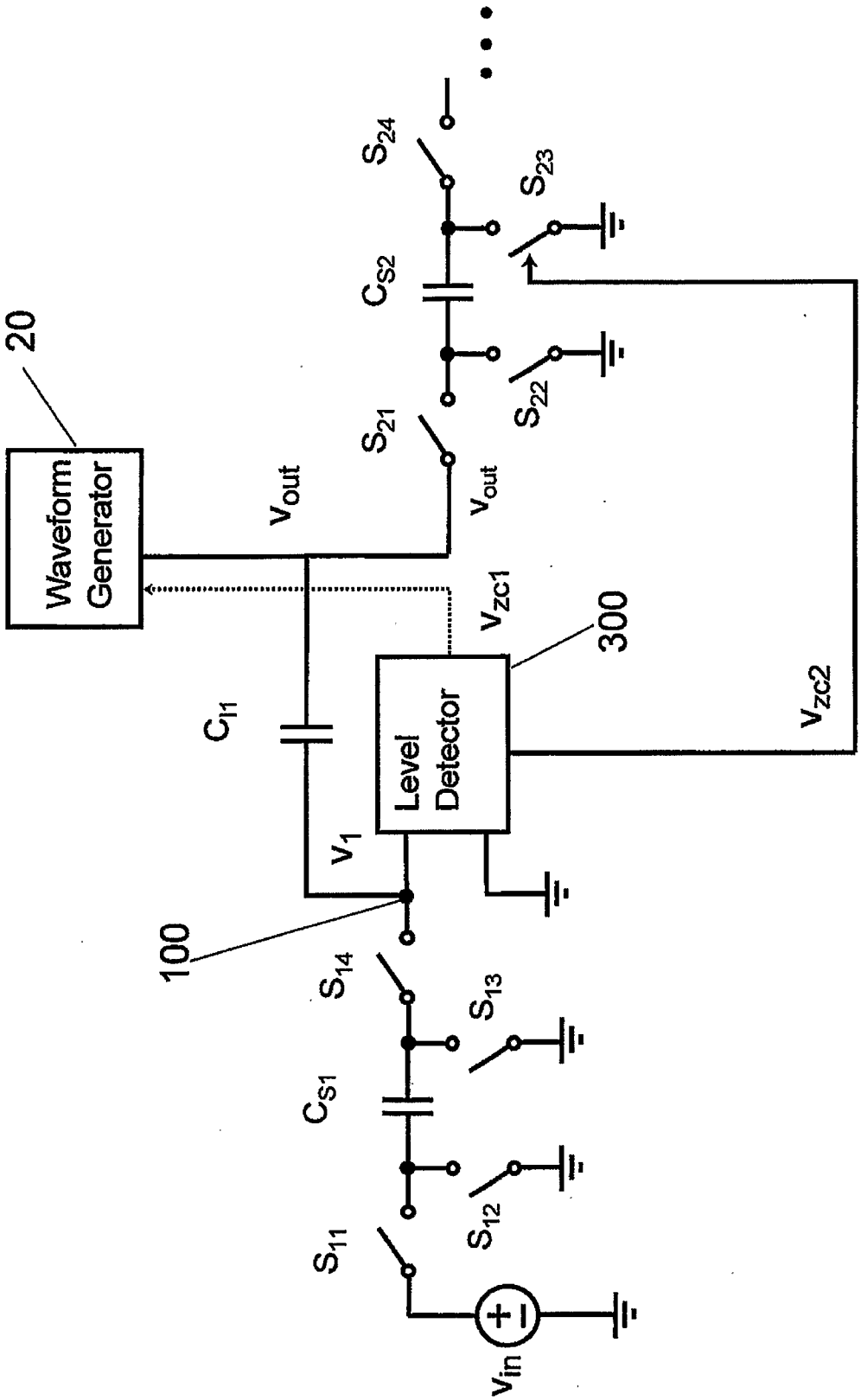
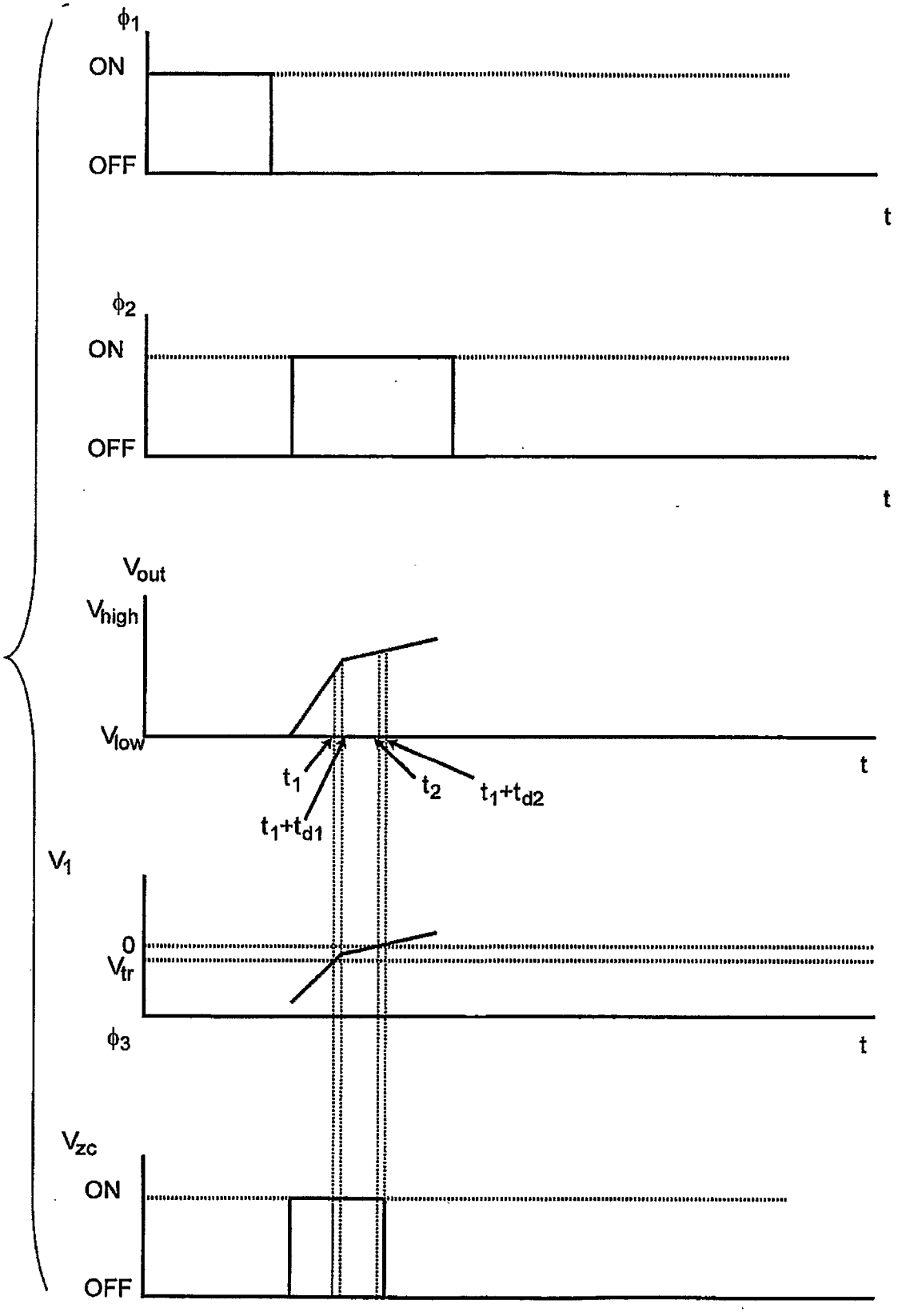

20
Waveform Generator
V_{out}
V_{out}
S_{21}
S_{24}
S_{23}
S_{22}
C_{S2}
V_{zc1}
300
V_{zc2}
C_{I1}
Level Detector
V_1
100
S_{14}
S_{13}
C_{S1}
S_{12}
S_{11}
V_{in}

FIGURE 10

FIGURE 11


ϕ_1
ON
OFF
t
ϕ_2
ON
OFF
t
V_{out}
V_{high}
V_{low}
t
t_1
t_1+t_{d1}
t_2
t_1+t_{d2}
V_1
0
V_{tr}
ϕ_3
t
V_{zc}
ON
OFF

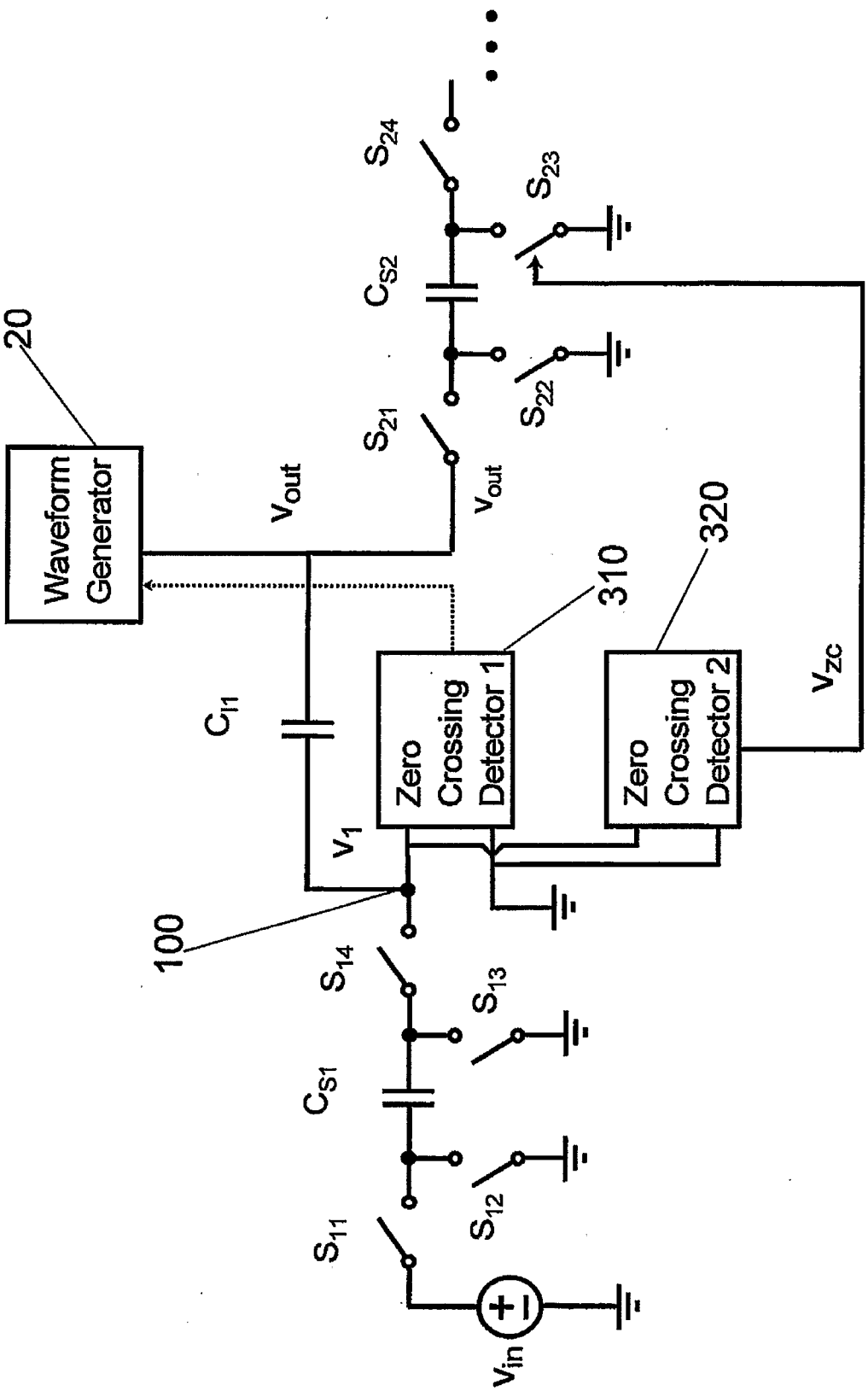

20
Waveform Generator
V_{out}
V_{out}
S_{24}
S_{23}
S_{22}
S_{21}
C_{S2}
310
320
Zero Crossing Detector 1
Zero Crossing Detector 2
V_{zc}
C_{I1}
V_1
100
S_{14}
S_{13}
S_{12}
S_{11}
C_{S1}
V_{in}

FIGURE 12

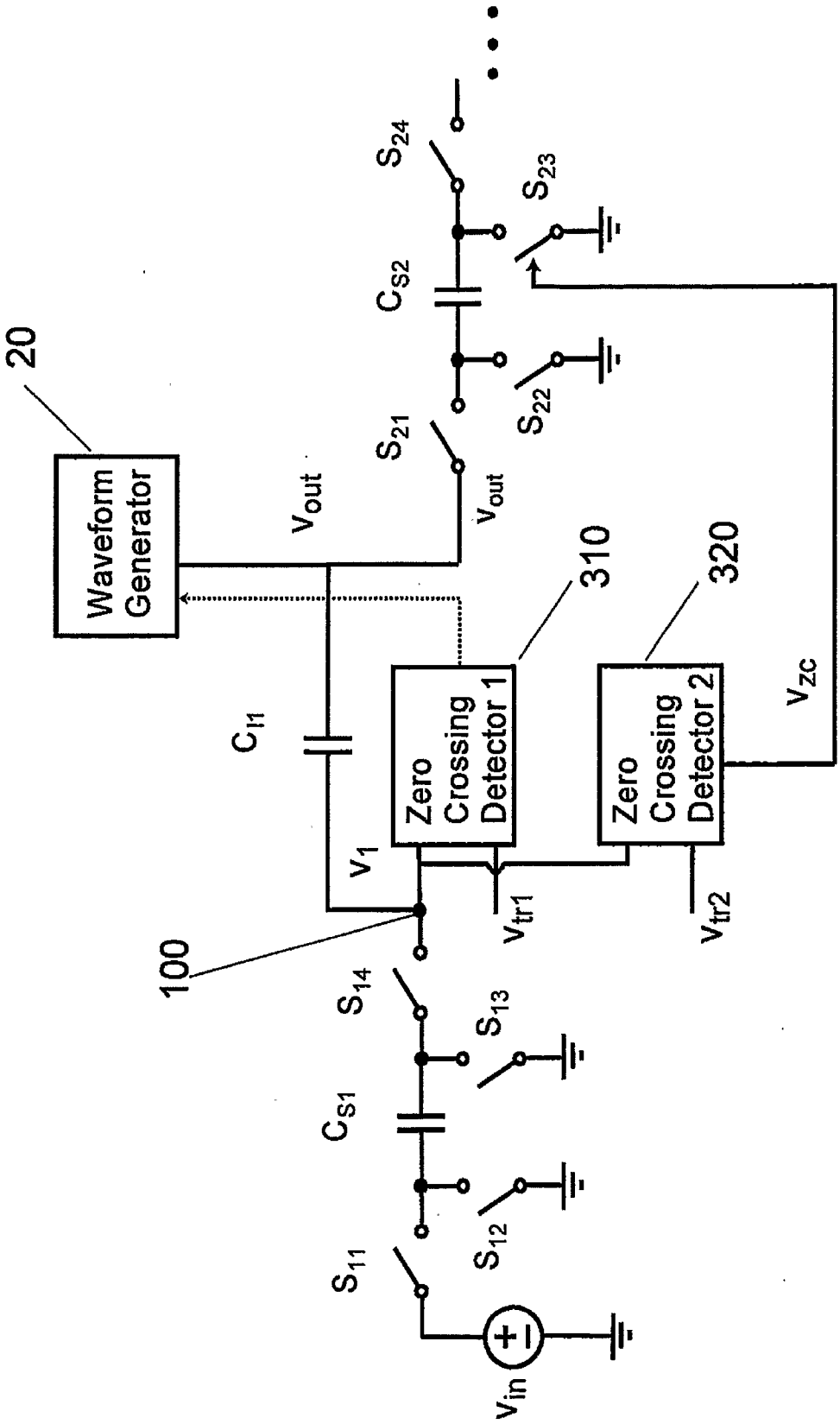
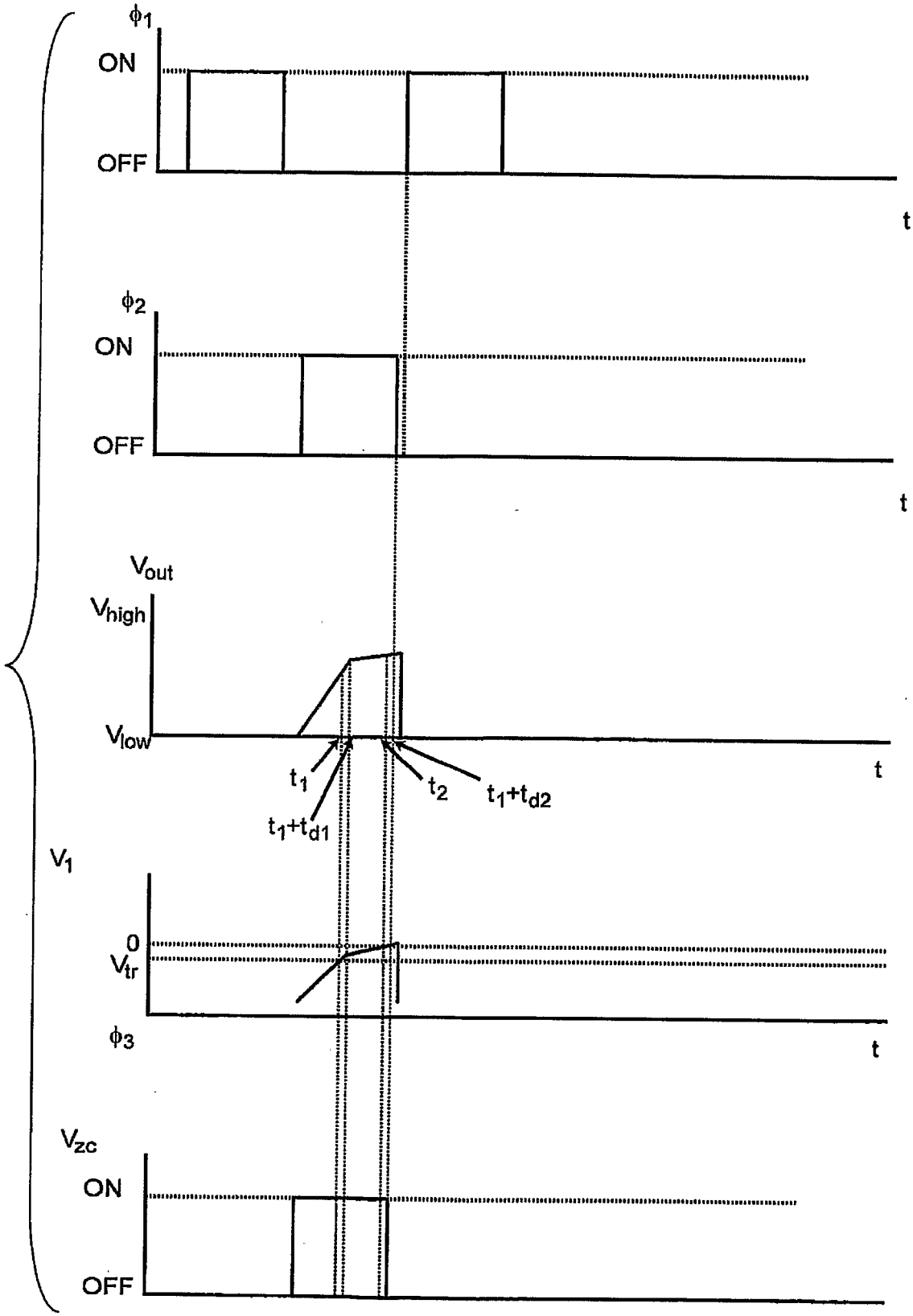

20
Waveform Generator
V_{out}
V_{out}
S_{21}
S_{22}
S_{23}
S_{24}
C_{S2}
310
320
Zero Crossing Detector 1
Zero Crossing Detector 2
V_{zc}
C_{I1}
V_1
V_{tr1}
V_{tr2}
100
S_{11}
S_{12}
S_{13}
S_{14}
C_{S1}
V_{in}

FIGURE 13

FIGURE 14


ϕ_1
ON
OFF
t
ϕ_2
ON
OFF
t
V_{out}
V_{high}
V_{low}
t
t_1
t_1+t_{d1}
t_2
t_1+t_{d2}
V_1
0
V_{tr}
ϕ_3
t
V_{zc}
ON
OFF

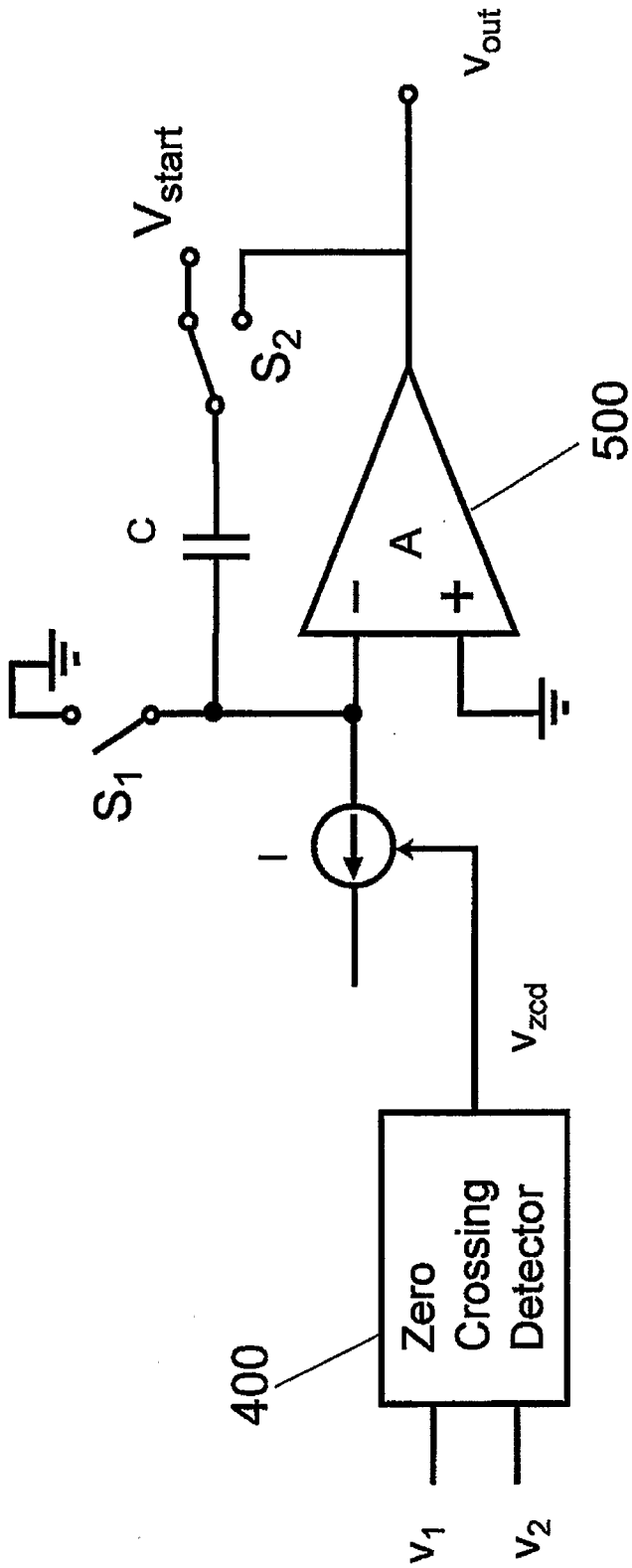

V_{out}
V_{start}
S_2
500
C
A
−
+
S_1
I
V_{zcd}
Zero Crossing Detector
400
V_1
V_2

FIGURE 15

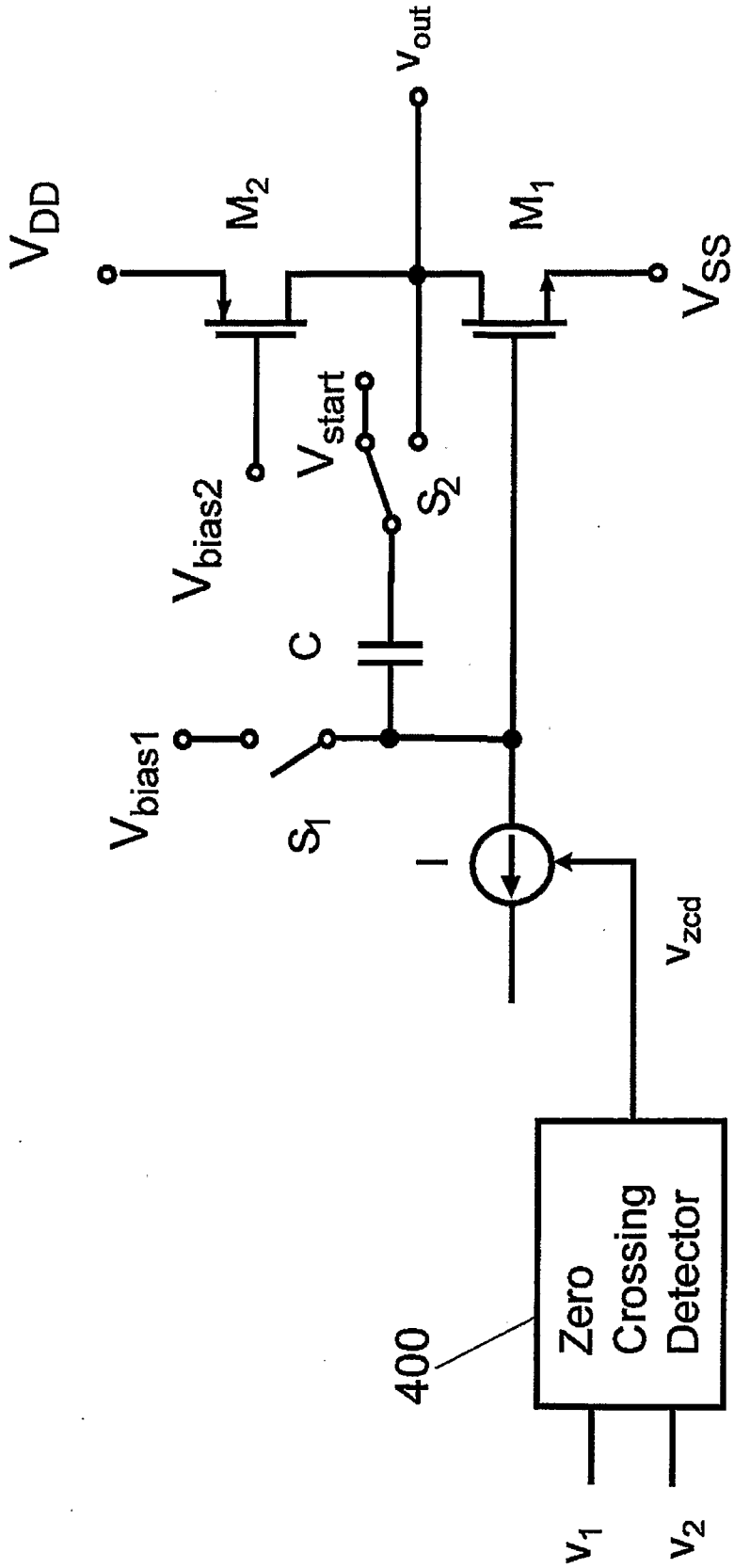

V_{out}
V_{DD}
M_2
M_1
V_{SS}
V_{start}
S_2
V_{bias2}
C
V_{bias1}
S_1
I
V_{zcd}
400
Zero Crossing Detector
V_1
V_2

FIGURE 16

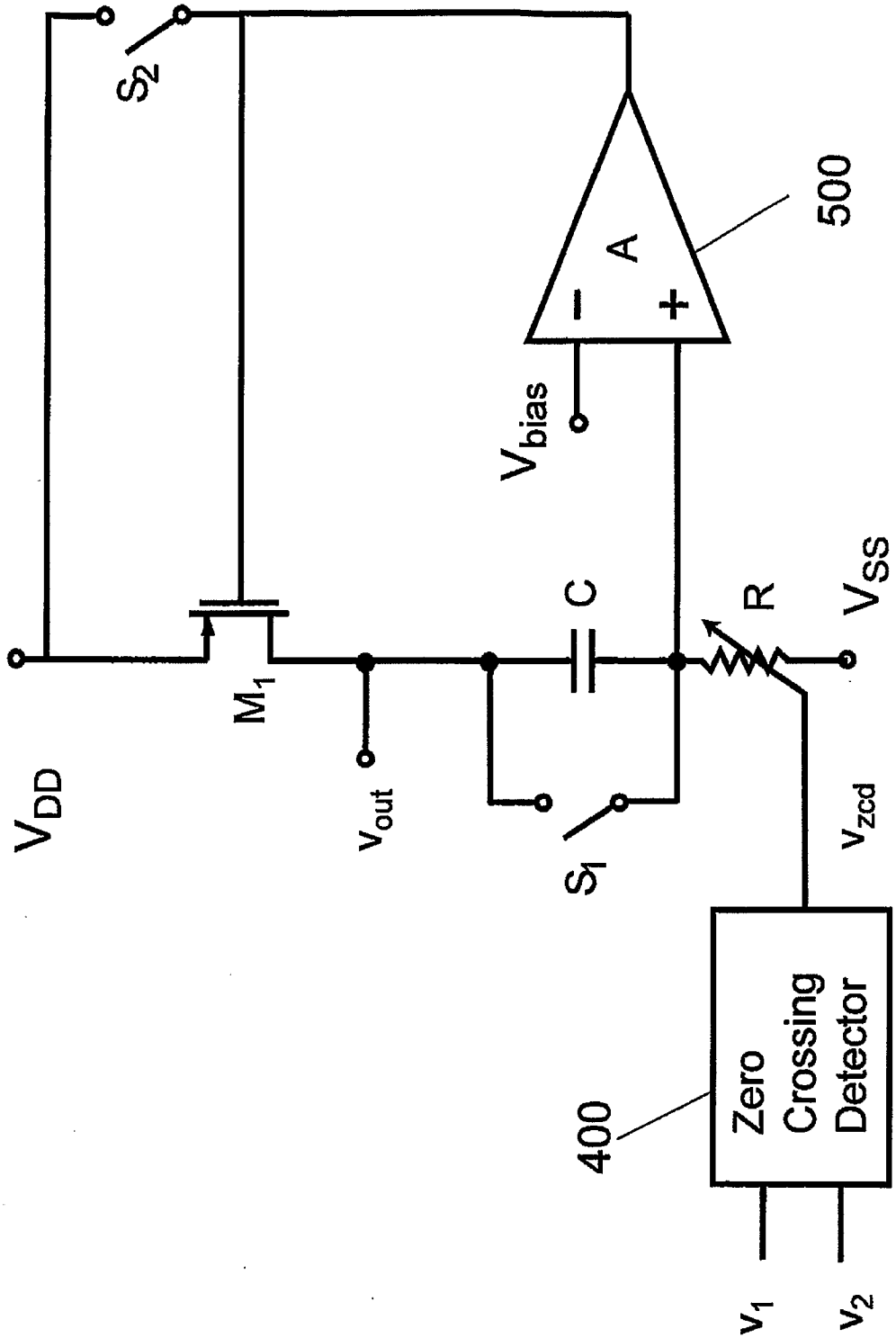

S2
A
500
Vbias
C
R
VSS
M1
VDD
Vout
S1
Vzcd
Zero
Crossing
Detector
400
V1
V2

FIGURE 17

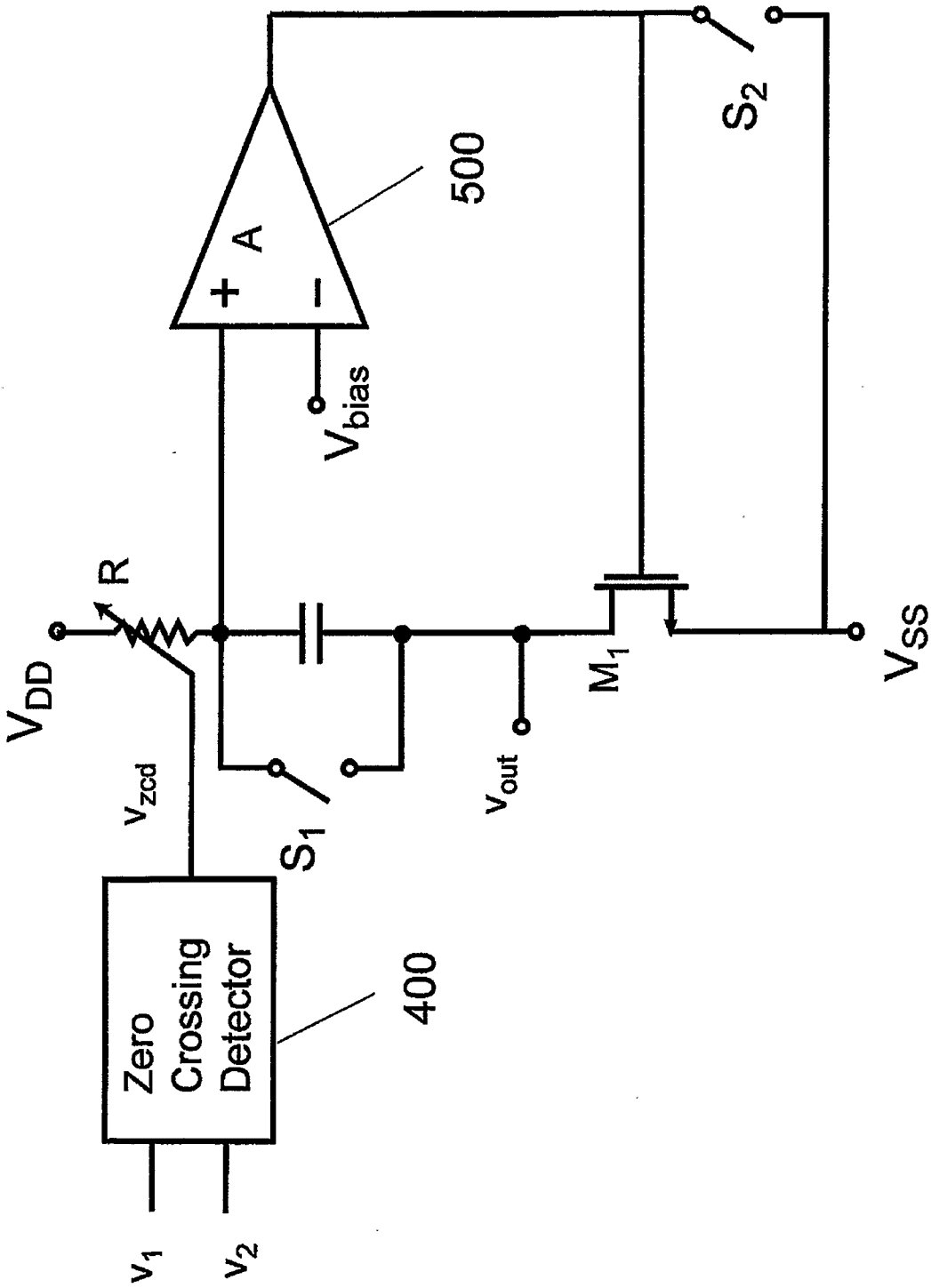

500
A
+
−
V_{bias}
S_2
R
V_{DD}
V_{zcd}
S_1
V_{out}
M_1
V_{SS}
Zero Crossing Detector
400
V_1
V_2

FIGURE 18

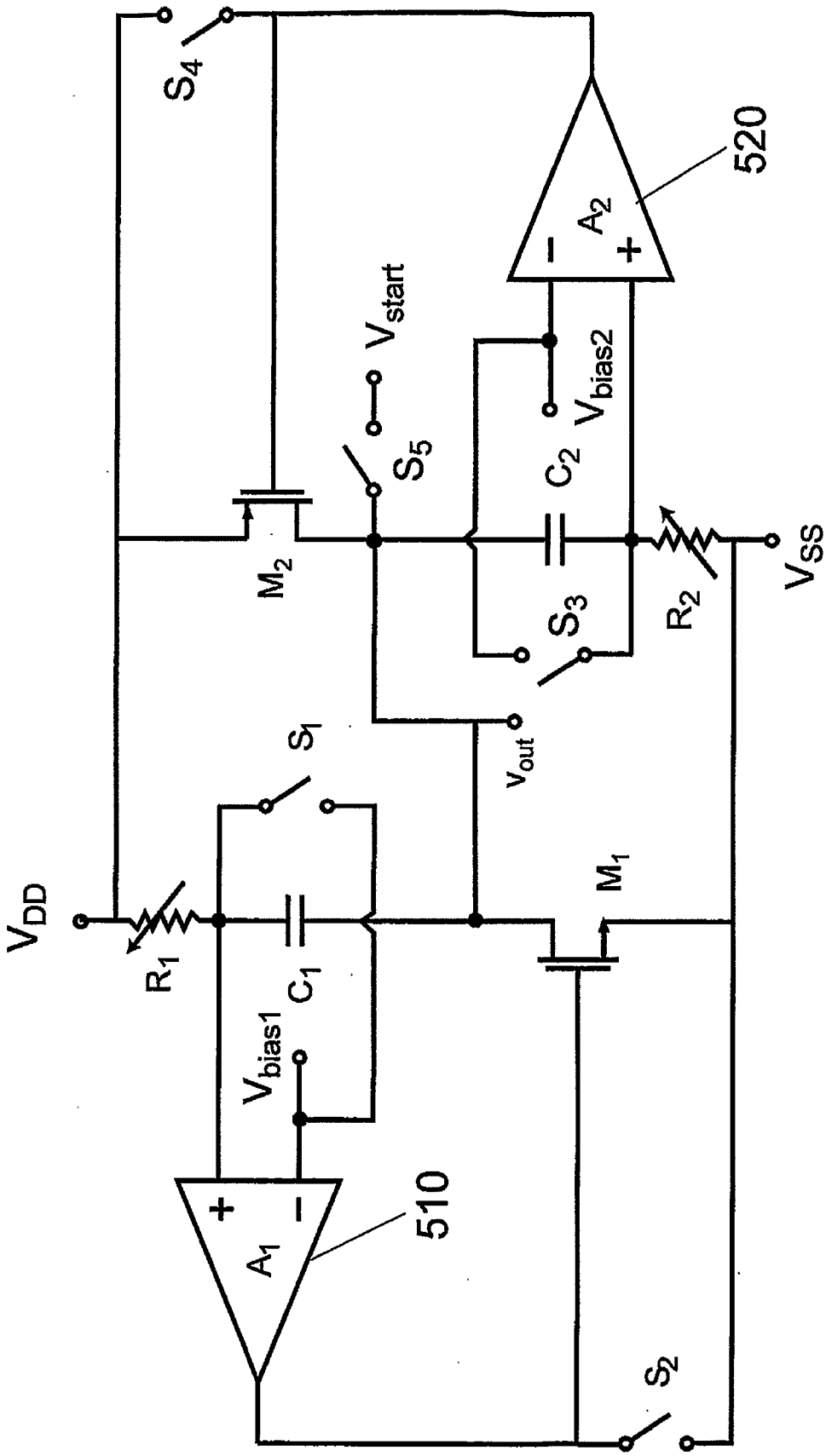

S4
520
A2
Vstart
S5
Vbias2
C2
M2
S3
R2
VSS
S1
Vout
VDD
R1
C1
M1
Vbias1
510
A1
S2

FIGURE 19

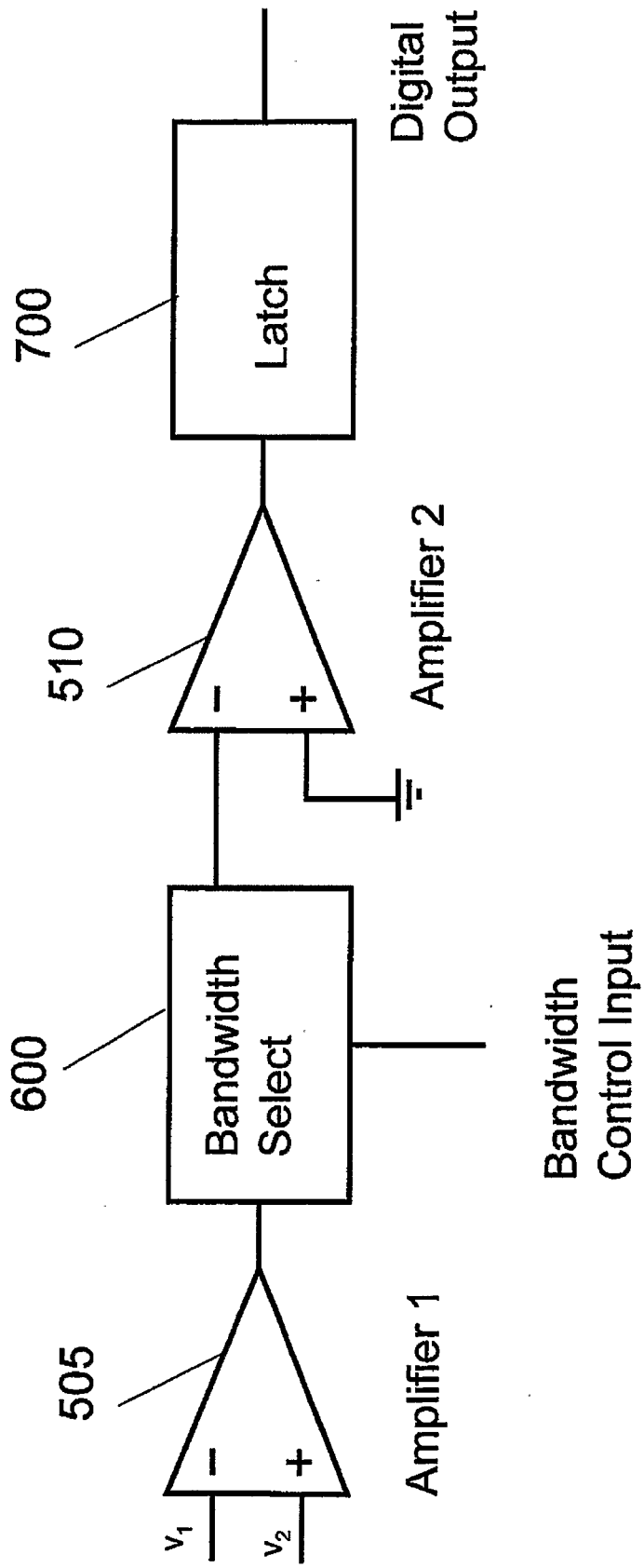

Digital Output
700
Latch
510
Amplifier 2
600
Bandwidth Select
Bandwidth Control Input
505
Amplifier 1
V_1
V_2

FIGURE 20

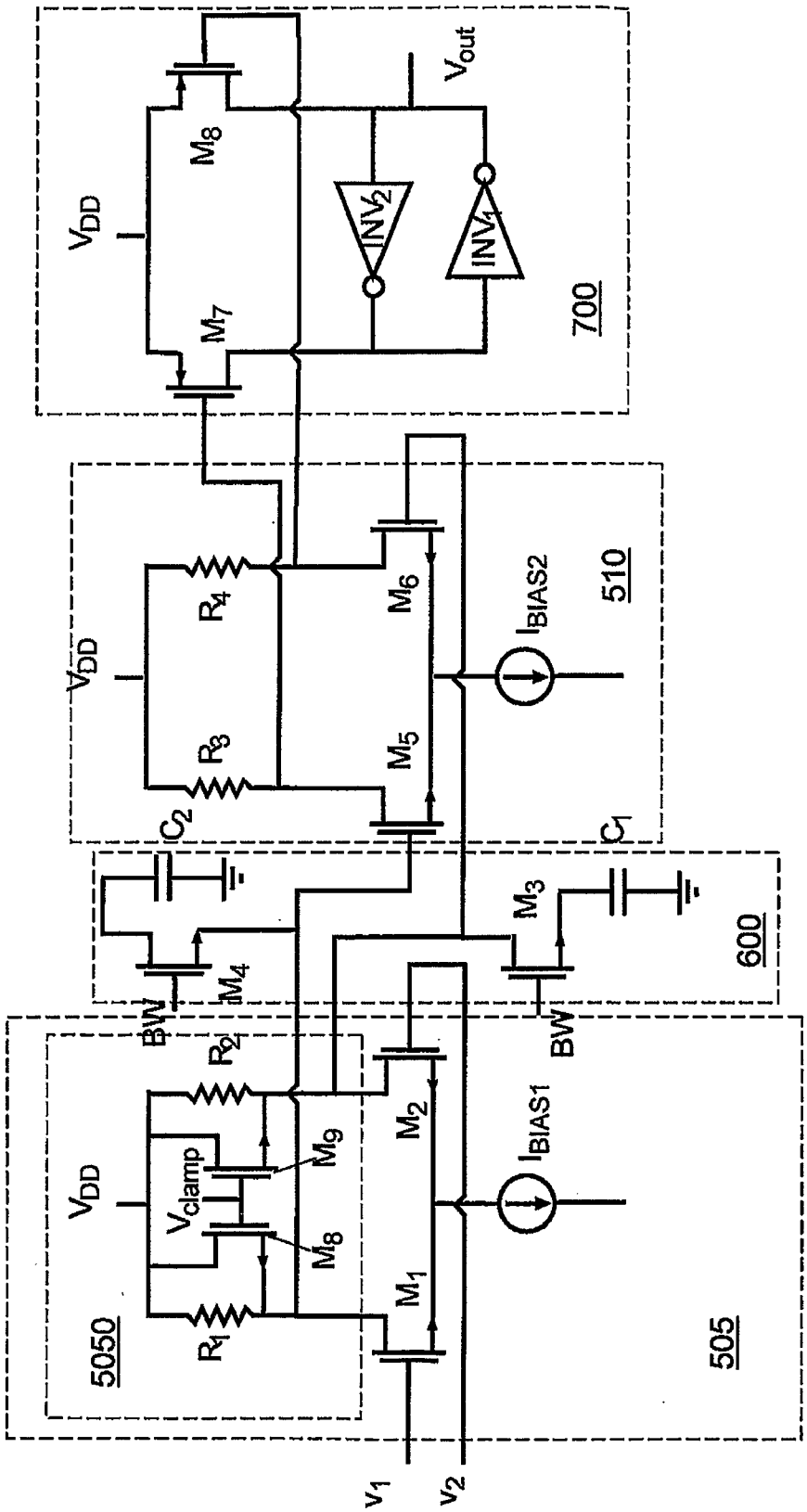

700
V_{out}
V_{DD}
M_8
M_7
INV_2
INV_1
510
R_4
R_3
M_6
M_5
I_{BIAS2}
C_2
C_1
600
M_4
M_3
BW
BW
505
5050
R_2
R_1
M_9
M_8
M_2
M_1
V_{clamp}
I_{BIAS1}
V_1
V_2

FIGURE 21

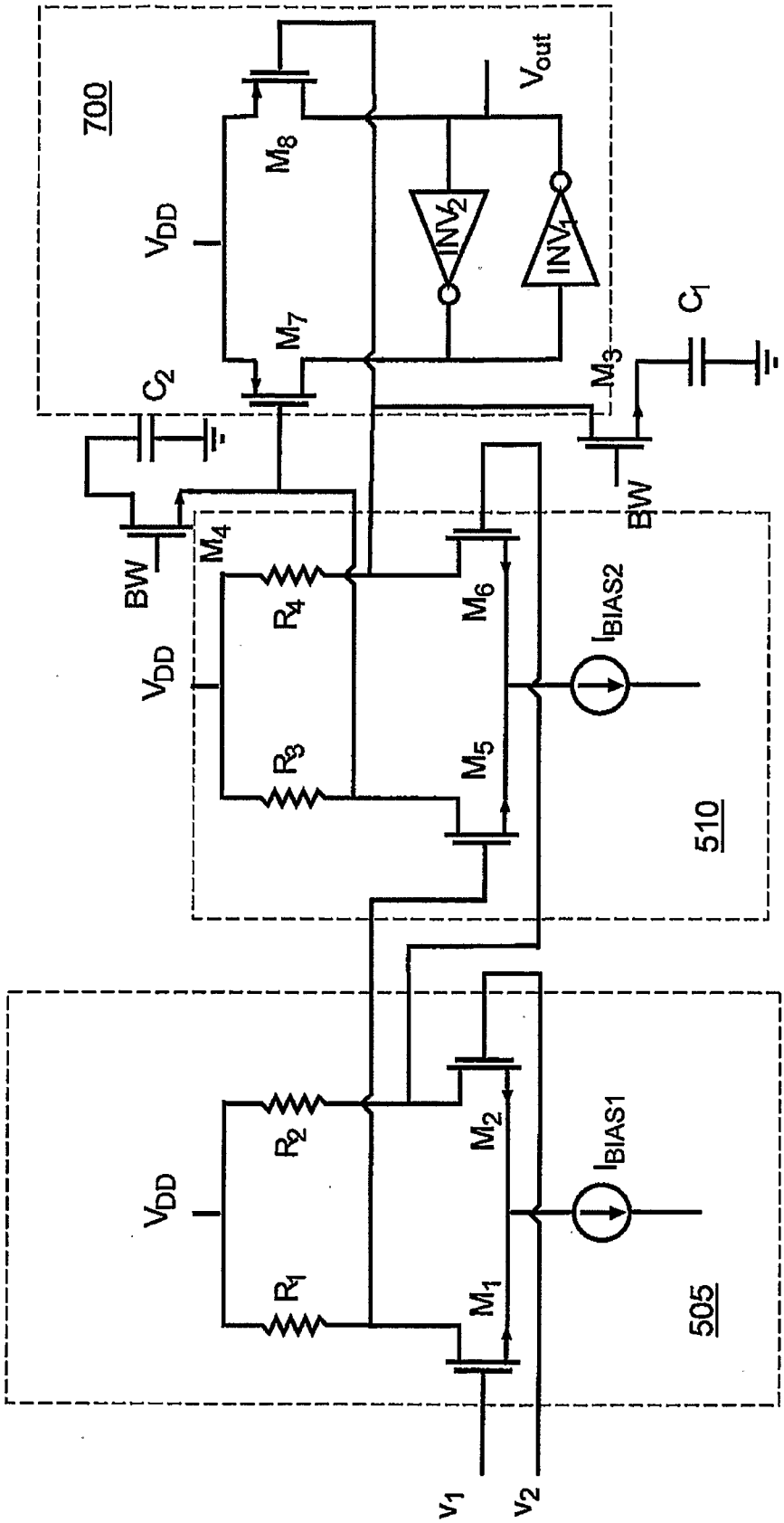

700
V_{out}
M_8
V_{DD}
INV_2
INV_1
M_7
C_1
C_2
M_3
BW
BW
M_4
R_4
M_6
I_{BIAS2}
V_{DD}
R_3
M_5
510
R_2
M_2
I_{BIAS1}
V_{DD}
R_1
M_1
505
V_1
V_2

FIGURE 22

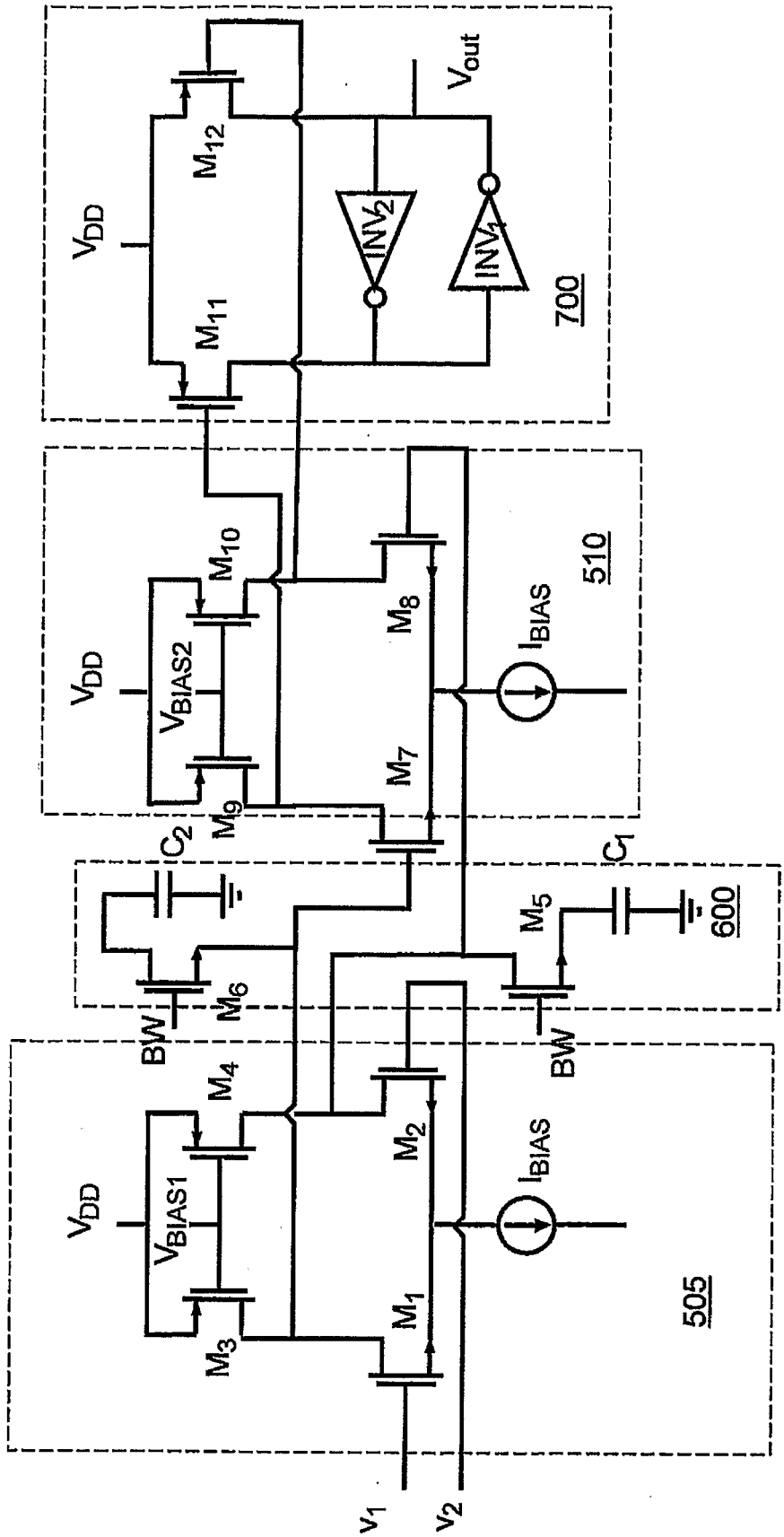

V_{out}
M_{12}
V_{DD}
INV_2
INV_1
700
M_{11}
M_{10}
M_8
510
I_{BIAS}
V_{DD}
V_{BIAS2}
M_7
M_9
C_2
C_1
M_5
600
M_6
BW
BW
M_4
M_2
V_{DD}
V_{BIAS1}
I_{BIAS}
505
M_1
M_3
V_1
V_2

FIGURE 23

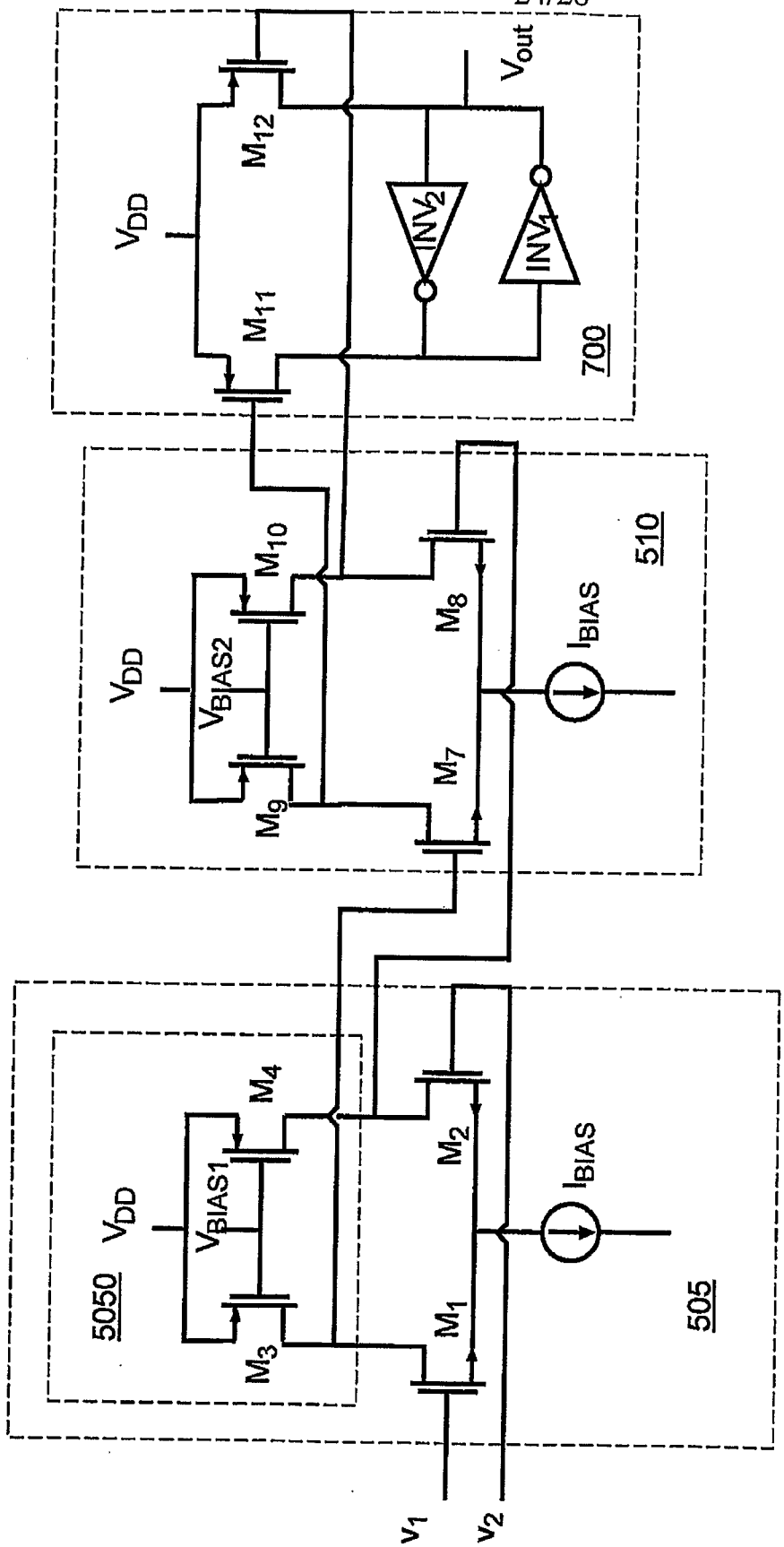

V_{out}
M_{12}
V_{DD}
INV_2
INV_1
M_{11}
700
M_{10}
M_8
510
V_{DD}
V_{BIAS2}
I_{BIAS}
M_9
M_7
M_4
M_2
V_{BIAS1}
V_{DD}
I_{BIAS}
5050
505
M_3
M_1
V_1
V_2

FIGURE 24

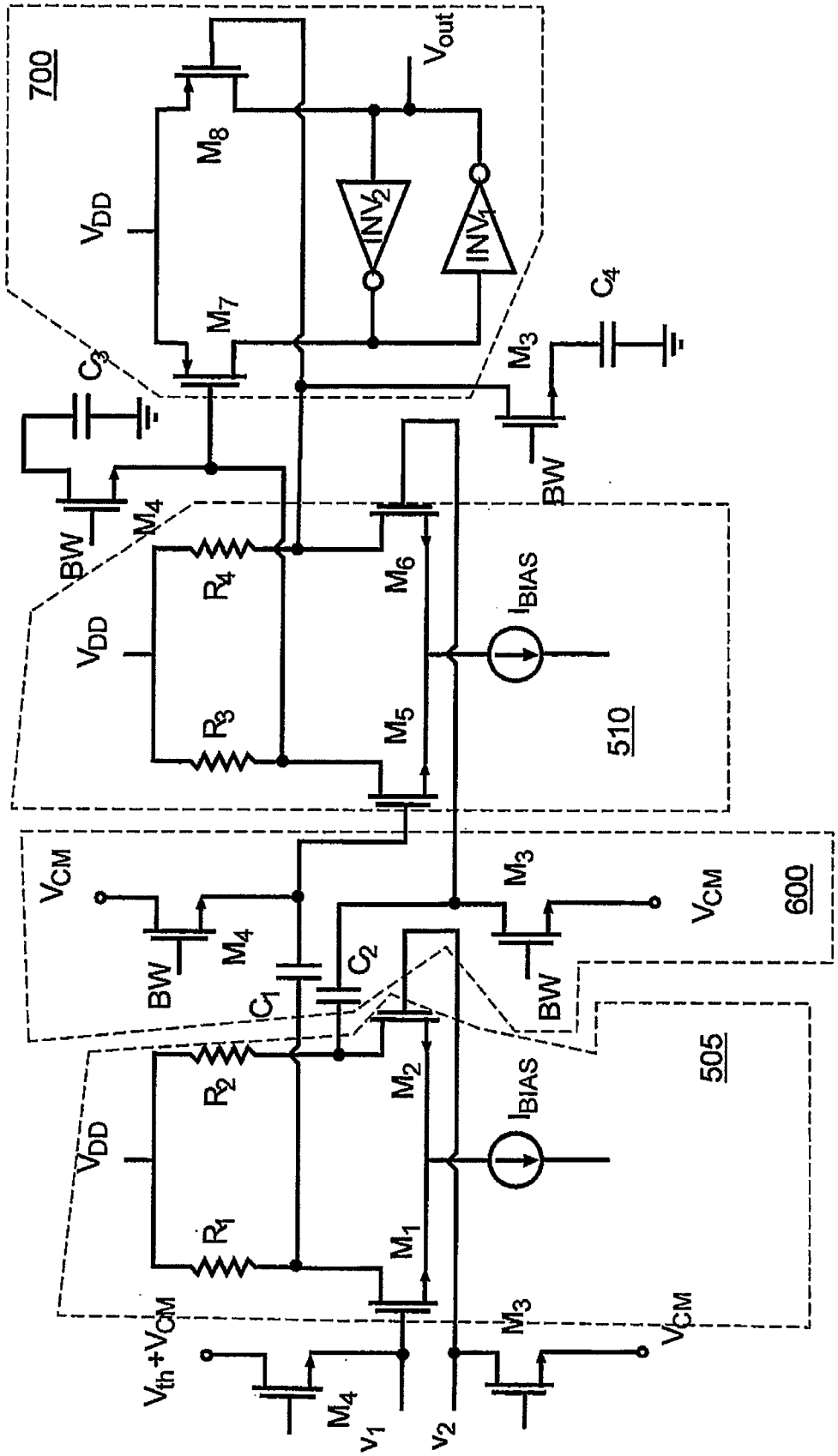

700
V_{out}
M_8
V_{DD}
INV_2
INV_1
M_7
C_3
C_4
M_3
BW
M_4
R_4
M_6
I_{BIAS}
R_3
M_5
510
V_{CM}
600
C_2
C_1
R_2
M_2
505
R_1
M_1
$V_{th}+V_{CM}$
v_1
v_2

FIGURE 25

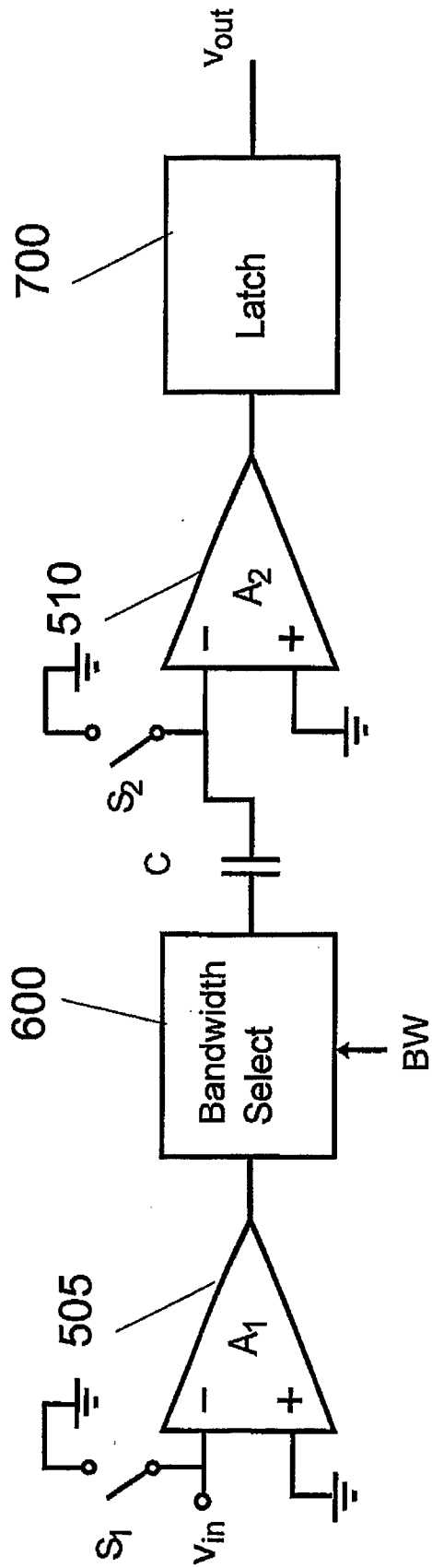

V_{out}
700
Latch
510
A_2
S_2
C
600
Bandwidth Select
BW
505
A_1
S_1
V_{in}

FIGURE 26

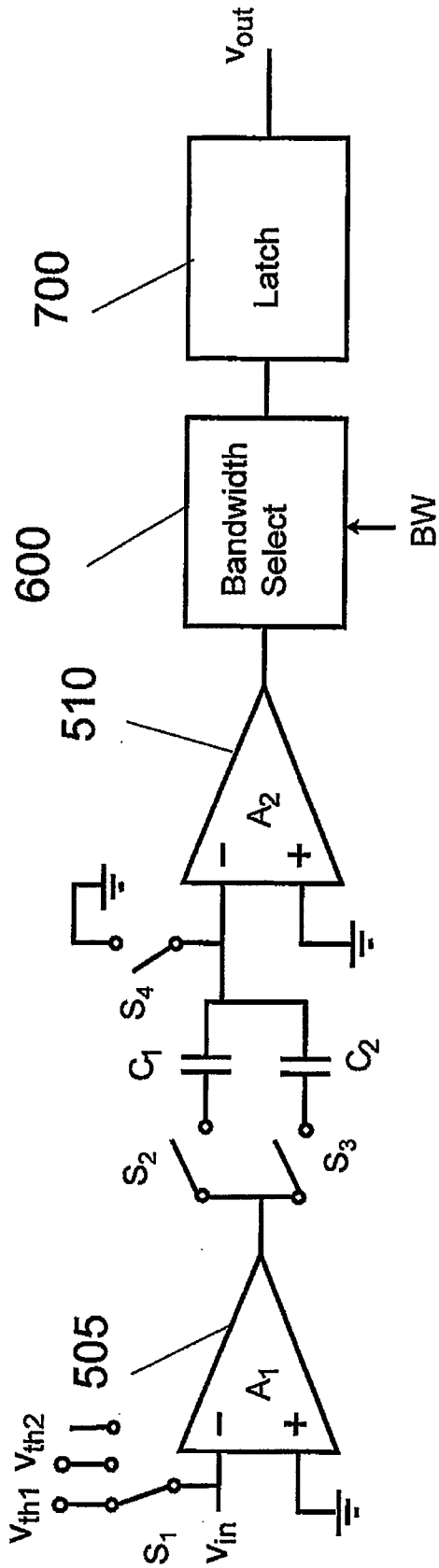

V_{out}
700
Latch
600
Bandwidth Select
BW
510
A_2
S_4
C_1
C_2
S_2
S_3
505
A_1
V_{th1}
V_{th2}
S_1
V_{in}

FIGURE 27

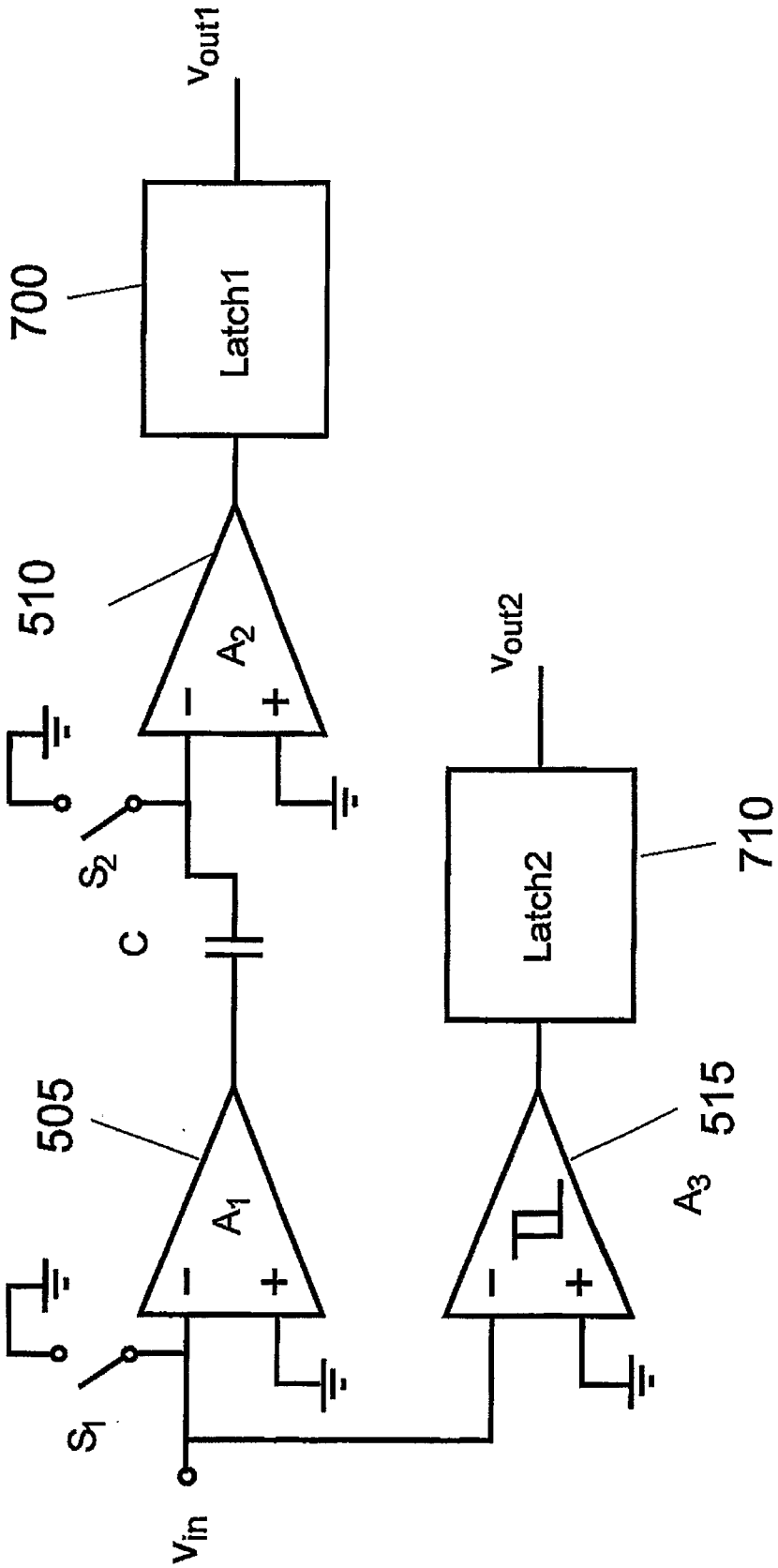

V_{out1}
700
Latch1
510
A_2
S_2
C
V_{out2}
710
Latch2
505
A_1
515
A_3
S_1
V_{in}

FIGURE 28

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2006/028047

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03M1/00 G11C27/02

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03M G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 103 230 A (KALTHOFF TIMOTHY V [US] ET AL) 7 April 1992 (1992-04-07) column 3, line 6 - column 9, line 50; figures 2,3	1-54

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

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Date of the actual completion of the international search	Date of mailing of the international search report
17 November 2006	27/11/2006

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Lindquist, Jim

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2006/028047

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5103230 A	07-04-1992	NONE	