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(54) Method for making a bipolar transistor

Verfahren zur Herstellung eines bipolaren Transistors

Méthode de fabrication d'un transistor bipolaire

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- **IBM TECHNICAL DISCLOSURE BULLETIN, vol. 35, no. 6, 1 November 1992 pages 453-454, XP 000314217 'DISPOSABLE OXIDE SIDEWALL FOR LATERAL SELF-ALIGNMENT IN EPITAXIAL BASE, SINGLE POLY, BIPOLAR TRANSISTORS'**
- **PATENT ABSTRACTS OF JAPAN vol. 009 no. 185 (E-332) ,31 July 1985 & JP-A-60 054452 (OKI DENKI KOGYO KK) 28 March 1985,**
- **PATENT ABSTRACTS OF JAPAN vol. 007 no. 111 (E-175) ,14 May 1983 & JP-A-58 031515 (NIPPON DENKI KK) 24 February 1983,**

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Description

Background of the Invention

[0001] The present invention relates to semiconductor structures, and more particularly to altering the orientation of grain boundaries of certain semiconductor layers.

[0002] One particularly useful device in the semiconductor industry, and particularly in the analog radio frequency (RF) device industry, is the epitaxial-base bipolar transistor. In certain configurations, the epitaxial-base bipolar transistor comprises a base portion which includes an epitaxial portion adjacent a polycrystalline portion. A crystal "grain boundary" exists at the interface between the polycrystalline portion and the epitaxial portion of the base. The grain boundary has a particular orientation. The nature of this orientation significantly affects the base resistance (R_b) of the device. It is well understood by those skilled in the art that the base resistance effects important performance parameters such as power gain and noise figure, in the case of RF devices. It is desirable to minimize R_b.

[0003] Consequently, what is needed is a method for affecting/altering the orientation of a grain boundary in a semiconductor layer, and in particular the orientation of a grain boundary in the base of an epitaxial-base bipolar transistor, in order to favorably affect R_b.

Brief Description of the Drawings

[0004]

FIG. 1 is a cross-sectional view representing a portion of an epitaxial-base bipolar transistor;

FIGs. 2-5 are cross-sectional views representing a portion of an epitaxial-base bipolar transistor at respective stages during fabrication;

FIGs. 6-8 are cross-sectional views representing a portion of an epitaxial-base bipolar transistor at respective stages of fabrication according to an alternate fabrication method; and

FIGs. 9-11 are cross-sectional views representing a portion of an epitaxial-base bipolar transistor at respective stages of processing according to yet another method of manufacture.

Detailed Description of the Drawings

[0005] FIG. 1 is a cross-sectional view representing a portion of an epitaxial-base bipolar transistor. FIG. 1 illustrates the structure to which a preferred method in accordance with the present invention is applied, and particularly illustrates the R_b issues outlined in the Background section of the present specification. FIG. 1 illustrates a portion of epitaxial-base bipolar transistor 10. Transistor 10 includes epitaxial-collector portion 11. An active area, generally toward the center of the device as indicated by arrow 12, is defined by forming LOCOS (local oxidation of silicon) oxide isolation regions 13, 14. Isolation regions 13, 14 along with epitaxial-collector portion 11 together comprise underlying structure 16. In order to provide the base of the device, undoped (also called intrinsic) semiconductor layer 17 is deposited over underlying structure 16. Typically, the deposition is performed with well understood low temperature epitaxy (LTE) techniques. In the present application, undoped silicon is deposited using a mixture of silane and hydrogen gases at 800°C by reduced pressure chemical vapor deposition technique (RPCVD). When undoped semiconductor layer 17 is deposited, an epitaxial portion 18 will tend to form over the epitaxial-collector portion 11, while polycrystalline portions 19, 20 will tend to form over LOCOS isolation portions 13, 14, respectively.

[0006] Subsequently, according to typical methods, an in-situ doped base layer 21 is deposited with LTE techniques. The layer can be silicon or silicon-germanium alloy doped with boron as a <P>-type impurity. Germanium and boron are incorporated in the film during RPCVD growth by adding germane and diborane gases to silane and hydrogen. Typical boron concentration is in the 10^{18} - 10^{19} atoms/cm^3 range, and germanium content is in the 10 - 20% atoms/cc range. Base layer 21 will tend to follow the formation of undoped-layer 17 with respect to polycrystalline portions and epitaxial portions, as illustrated by the figure. Later, the dopants in layer 21 may be diffused into undoped layer 17, both layers together serving as the base.

[0007] Subsequently, an "emitter stack", indicated generally by arrow 24, is formed. Emitter stack 24 includes oxide isolation portions 25, 26 which define an emitter contact region 27. A polycrystalline emitter 28 is formed, contacting active region 12 at emitter contact region 27. Portions of a polycrystalline emitter 28 are separated from active region 12 with nitride portions 29, 30. Additionally, sidewall spacers 32, 33 are provided along the sides of emitter stack 24, comprising TEOS isolation portions 34, 35 and nitride sidewalls 36, 37, respectively. Spacers 32,33 serve to isolate base contact areas 22,23, respectively, from active area 12, and provide masking for doping and alignment as necessary.

[0008] Prior to the formation of emitter stack 24, in a typical device, a thin layer of emitter dopant such as arsenic, may be implanted toward the center of active region 12, into base layer 21.

[0009] The structure of FIG. 1 has particular features that are relevant to a method in accordance with the present invention. As previously discussed, one performance parameter which significantly affects the performance of the device is R_b. With reference to FIG. 1, the major contributions to R_b are R_{bx1} and R_{bx2}. R_{bx1} is the resistance in the epitaxial portion of layers 21 and 17 lying between the tip of the polycrystalline region 19 and the emitter contact region 27, as indicated in FIG. 1. R_{bx2} is the resistance in the polycrystalline portions of layers 21 and 17 beneath the emitter stack, as indi-

cated in FIG. 1.

[0010] Although it is desirable to minimize R_b, and therefore R_{bx1} and R_{bx2}, several factors limit minimizing these parameters. For example, R_b could be decreased if the dopants implanted in regions 22,23 (which provides conductive contact to the base) could reach at least the R_{bx2} region. However, the polycrystalline nature of regions 19,20 prevent lateral diffusion of the dopants toward active area 12. Furthermore, the fact the R_{bx2} comprises polycrystalline material rather than epitaxial material increases base resistance. Additionally, the length of R_{bx1} combined with R_{bx2}, which bears directly on R_b, must be sufficient to provide at least 0.3 microns between the tip of grain boundary 38 and emitter region 27, i.e., the distance between the dotted lines indicating R_{bx1}. It is understood by those skilled in the art that this minimum distance is required to avoid undesired emitter/base leakage current.

[0011] For the purposes of clarity and simplicity, the following discussions of preferred methods focus on only one half (the left half) of the device. It will be understood that the concepts apply symmetrically to both sides. According to a preferred method consistent with the present invention, one solution for reducing R_b is to anneal undoped-layer 17 once it has been deposited, in order to alter the orientation of the grain boundary 38 of polycrystalline portion 19. As discussed previously, when undoped-layer 17 is initially deposited, a grain boundary originates at the interface between LOCOS isolation region 13 and collector epitaxial portion 11. It is well understood by those skilled in the art that LOCOS isolation region 13 tends to form a pointed "bird's beak" 50 at its edge near active region 12. When undoped-layer 17 is deposited, grain boundary 38 forms, originating at edge 50. Due to the downward sloping direction of LOCOS region 13 near edge 50, grain boundary 38 will tend to extend inward, toward the center of active region 12.

[0012] Referring to FIG. 2, according to a preferred method, after collector epitaxial region 11 is formed and LOCOS isolation structure 13 is formed, undoped-layer 17 is deposited using LTE techniques to a thickness of approximately 1,000-2,000 angstroms. Silane gas may be used in order to form a seed layer over LOCOS regions 13, to provide for the formation polycrystalline portion 19.

[0013] After layer 17 is deposited, an anneal is performed at a relatively high temperature, on the order of greater than 1,000°C, in order to recrystallize the polycrystalline silicon regions of layer 17 (portions 19, 20), thereby altering the orientation of grain boundary 38. This leads to the structure shown in FIG. 3.

[0014] Grain boundary 38 has been altered by annealing, and new grain boundary 55 has been formed. Grain boundary 55 now points away from active region 12, rather than toward active region 12, as was the case with grain boundary 38. Note, that according to the presently described method, the origin of grain boundary 55 remains substantially at edge 50 of LOCOS region 13.

[0015] Turning to FIG. 4, base layer 21 is grown with LTE techniques. Typically, base layer 21 is in-situ doped Si or SiGe alloy. Note that the polycrystalline faceting of layer 21 tends to follow that of layer 17, as indicated by the extension of grain boundary 55. Turning to FIG. 5, emitter stack 24 is subsequently formed according to well known methods.

[0016] An important advantage of the method just described, is that the length of R_{bx2} has been significantly reduced. The length of R_{bx1} must remain approximately 0.3 microns in order to prevent emitter/base leakage, as discussed above. However, since grain boundary 55 now points away from active region 12, rather than toward active region 12, the length of R_{bx2} has been significantly reduced. In some devices, this reduction may be as much as 50% of the original length of R_{bx2}. Consequently, the overall length of R_b has been reduced, resulting in a significant reduction in the magnitude of R_b.

[0017] An alternate method in accordance with the present invention is illustrated by FIGs. 6-8. This alternate method is similar to the previously discussed method. However, undoped-layer 17 is recrystallized with a more extreme anneal in order to relocate the polycrystalline grain boundary a substantial distance from active area 12. This method provides the added benefits of a further reduced extrinsic base resistance R_b because the grain boundary 60 is no longer between a surface contact to the base (area 22 in the completed device) and the active area 12. Additionally, because grain boundary 60 is moved a substantial distance away from active region 12, dopant which is implanted in order to enhance contact to the base may laterally diffuse closer to active region 12.

[0018] More specifically, this process is carried out as follows. Referring to FIG. 6, undoped-layer 17 is deposited according to the methods previously discussed. Subsequently, undoped-layer 17 is annealed as in the previous method, but at a much high temperature and for a longer period of time, typically 1150°C and 3 minutes, in order recrystallize most of undoped-layer 17. The result is that single crystalline portion 18 is substantially extended in a direction away from active region 12, and therefore grain boundary 60 is pushed away from active region 12.

[0019] Referring to FIG. 7, similar to the method previously discussed, an in-situ doped Si or SiGe base layer is deposited using the previously discussed methods. As illustrated by FIG. 7, a grain boundary 61 of base layer 21 naturally follows grain boundary 60 of undoped-layer 17. Consequently, the entire portion to the right of grain boundaries 60,61 is substantially single crystalline.

[0020] Following the deposition of layer 21, mask portion 62 is provided using well known photolithographic methods. Subsequently, an extrinsic dopant such as boron is implanted in the region indicated by arrows 63, in

order to provide an effective contact to the base of the device.

[0021] Moving to FIG. 8, mask 62 has been removed according to well known processes, and emitter stack 24 has been formed. One notable feature illustrated by FIG. 8 is region 65, across which the implant indicated by 63 in FIG. 7 has been able to laterally diffuse during the processing associated with emitter stack 24. This lateral diffusion provides the benefits discussed earlier, of a lower R_b, compared to a structure where a grain boundary lies under the emitter stack, thus preventing such lateral diffusion of dopants.

[0022] A third method in accordance with the present invention is illustrated in FIGs. 9-11. This method takes into account the concern of dislocations propagating toward active area 12 due to dopant implants (such as that indicated by 63 in FIG. 7). According to this alternative method, undoped-layer 17 is deposited as in the previously discussed methods. Subsequently, undoped-layer 17 is annealed, as in the previously discussed method immediately above, in order to substantially relocate grain boundary 60 away from active region 12.

[0023] According to the presently discussed method, following the anneal of layer 17, an implant step is performed. As illustrated in FIG. 9, mask 68 is formed according to well known photolithographic methods. Subsequently, a dopant is implanted, as indicated by arrows 69. The dopant provides an effective base contact for the device, and may be boron, as is well understood by those skilled in the art.

[0024] Moving to FIG. 10, following the doping step, the structure is annealed in order to activate the dopant, laterally diffuse the dopant toward active region 12, and importantly, anneal away crystalline defects. Turning to FIG. 11, base layer 21 is formed. Subsequently, emitter stack 24 is fabricated, resulting in a structure very similar to that illustrated in FIG. 8. The significant difference between this method and the most previously discussed method is that the extrinsic dopant implantation, which provides effective base contact for the device, occurs before the deposition of base layer 21, rather than after. Additionally, an anneal which activates and laterally diffuses the dopant, and removes defects, is performed. The removal of defects is particularly important when the base comprises epitaxial SiGe. SiGe is a pseudomorphic epitaxial strained layer and consequently mechanically fragile. Defects from the underlying layer can generate dislocations in the SiGe layer which will propagate in the active area during subsequent processing steps. Such defects tend to cause undesirable emitter/base electrical leakage.

[0025] As will be appreciated by now, new methods in accordance with the present invention are provided to reduce the base resistance, R_b, in devices such as epitaxial-base bipolar transistor structures. Among other advantages, grain boundaries are altered or moved in order to substantially the reduce base resistance.

[0026] While specific illustrative methods have been shown, obvious modification and improvements will naturally occur to those skilled in the art. Consequently, it should be understood that this invention is not limited to the particular methods shown and discussed.

Claims

1. A method for making a semiconductor structure (10) comprising the steps of:

providing a collector epitaxial layer (11) having an active region (12);
forming an oxide region (13) in the collector epitaxial layer (11), the oxide region (13) having an edge (50);
depositing an undoped layer (17) over the collector epitaxial layer (11) and the oxide region (13) such that an epitaxial portion (18) forms over the collector epitaxial layer (11) and a polycrystalline portion (19) forms over the oxide region (13), the polycrystalline portion (19) having a grain boundary (38) which has its origin approximately at the edge (50) of the oxide layer, the grain boundary forming an acute angle with the interface between the epitaxial portion (18) of the layer (17) and the underlying collector epitaxial layer (11); and
annealing the layer (17) to recrystalize the polycrystalline portion and thereby alter the grain boundary (38, 55, 60) to form an obtuse angle with the interface between the epitaxial portion (18) of the layer (17) and the underlying collector epitaxial layer (11) or the underlying oxide region (13).

2. The method of claim 1 wherein the step of annealing the layer (17) includes relocating the origin of the grain boundary (38, 60) away from the edge (50).

3. The method of claim 1 wherein the step of annealing the layer (17) includes keeping the origin of the grain boundary (38, 55) approximately at the edge (50).

4. The method of claims 1, 2, or 3 further comprising the steps of:

depositing a base layer (21) over the layer (17); and
forming an emitter layer (28) over the base layer (21).

5. The method of claim 4 wherein the step of depositing the base layer (21) includes forming an in-situ doped base layer (21).

6. The method of claim 4 further comprising the steps of:

forming a mask (62) over the active region (12); and
implanting impurities (63) into the base layer (21).

7. The method of claim 1 or 2 further comprising implanting impurities (69) into the layer (17).

8. The method of any of the preceding claims wherein the step of annealing the layer (17) includes reducing a base resistance of the semiconductor structure (10).

Patentansprüche

1. Ein Verfahren zur Herstellung einer Halbleiterstruktur (10) mit den Schritten:

Bereitstellung einer epitaxialen Kollektor-Schicht (11) mit einem aktiven Bereich (12) ;

Bildung eines Oxidbereichs (13) in der epitaxialen Kollektor-Schicht (11), und der Oxidbereich (13) eine Kante (50) hat;

Abscheidung einer undotierten Schicht (17) über der epitaxialen Kollektor-Schicht (11) und dem Oxidbereich (13) derart, dass sich ein epitaxialer Teil (18) über der epitaxialen Kollektor-Schicht (17) und ein polykristalliner Teil (19) über dem Oxidbereich (13) bildet, wobei der polykristalline Teil (19) eine grobkörnige Grenzlinie (38) hat, die ihren Ursprung in etwa an der Kante (50) der Oxidschicht hat, und die grobkörnige Grenzlinie einen spitzen Winkel mit der Schnittstelle zwischen dem epitaxialen Teil (18) der Schicht (17) und der darunter liegenden epitaxialen Kollektor-Schicht (11) bildet; und

Ausheilung der Schicht (17), um den polykristallinen Teil zu rekristallisieren und wodurch die grobkörnige Grenzlinie (38, 55, 60) verändert wird, um einen stumpfen Winkel mit der Schnittstelle zwischen dem epitaxialen Teil (18) der Schicht (17) und der darunter liegenden epitaxialen Kollektor-Schicht (11) oder dem darunter liegenden Oxidbereich (13) zu bilden.

2. Das Verfahren nach Anspruch 1, worin der Schritt der Ausheilung von Schicht (17) die Verschiebung des Ursprungs der grobkörnigen Grenzlinie (38, 60) fort von der Kante (50) enthält.

3. Das Verfahren nach Anspruch 1, worin der Schritt der Ausheilung von Schicht (17) das Beibehalten des Ursprungs der grobkörnigen Grenzlinie (38, 55) in etwa an der Kante (50) enthält.

4. Die Verfahren nach den Ansprüchen 1, 2 oder 3 mit den weiteren Schritten:

Abscheidung einer Basis-Schicht (21) über der Schicht (17); und

Bildung einer Emitter-Schicht (28) über der Basis-Schicht (21).

5. Das Verfahren nach Anspruch 4, worin der Schritt der Abscheidung der Basis-Schicht (21) die Bildung einer in-situ dotierten Basis-Schicht (21) enthält.

6. Das Verfahren nach Anspruch 4 mit den weiteren Schritten;

Bildung einer Maske (62) über dem aktiven Bereich (12); und

Implantierung von Verunreinigungen (63) in die Basis-Schicht (21).

7. Das Verfahren nach den Ansprüchen 1 oder 2, weiter aufweisend die Implantierung von Verunreinigungen (69) in die Schicht (17).

8. Das Verfahren nach jedem der voranstehenden Ansprüche, worin der Schritt der Ausheilung der Schicht (17) die Verminderung eines Basis-Widerstands der Halbleiterstruktur (10) enthält.

Revendications

1. Procédé permettant de fabriquer une structure semiconductrice (10), comprenant les opérations suivantes :

produire une couche épitaxiale de collecteur (11) possédant une région active (12) ;
former une région d'oxyde (13) dans la couche épitaxiale de collecteur (11), la région d'oxyde (13) possédant un bord (50) ;
déposer une couche non dopée (17) sur la couche épitaxiale de collecteur (11) et la région d'oxyde (13) de façon qu'une partie épitaxiale (18) se forme sur la couche épitaxiale de collecteur (11) et qu'une partie polycristalline (19) se forme sur la région d'oxyde (13), la partie polycristalline (19) ayant une frontière de grain (38) dont l'origine est approximativement située au niveau du bord (50) de la couche d'oxyde, la frontière de grain formant un angle aigu avec l'interface entre la partie épitaxiale (18) de

la couche (17) et la couche épitaxiale de collecteur sous-jacente (11) ; et
recuire la couche (17) afin de recristalliser la partie polycristalline et, ainsi, modifier la frontière de grain (38, 55, 60) afin qu'elle forme un angle obtus avec l'interface entre la partie épitaxiale (18) de la couche (17) et la couche épitaxiale de collecteur sous-jacente (11) ou la région d'oxyde sous-jacente (13).

2. Procédé selon la revendication 1, où l'opération de recuit de la couche (17) comporte un repositionnement de l'origine de la frontière de grain (38, 60) dans un sens d'écartement par rapport au bord (50).

3. Procédé selon la revendication 1, où l'opération de recuit de la couche (17) maintient l'origine de la frontière de grain (38, 55) approximativement au niveau du bord (50).

4. Procédé selon la revendication 1, 2 ou 3, comprenant en outre les opérations suivantes :

déposer une couche de base (21) sur la couche (17) ; et
former une couche d'émetteur (28) sur la couche de base (21).

5. Procédé selon la revendication 4, où l'opération de dépôt de la couche de base (21) comporte la formation d'une couche de base dopée in situ (21).

6. Procédé selon la revendication 4, comprenant en outre les opérations suivantes :

former un masque (62) sur la région active (12) ; et
implanter des impuretés (63) dans la couche de base (21).

7. Procédé selon la revendication 1 ou 2, comprenant en outre l'implantation d'impuretés (69) dans la couche (17).

8. Procédé selon l'une quelconque des revendications précédentes, où l'opération de recuit de la couche (17) comporte la réduction de la résistance de base de la structure semiconductrice (10).

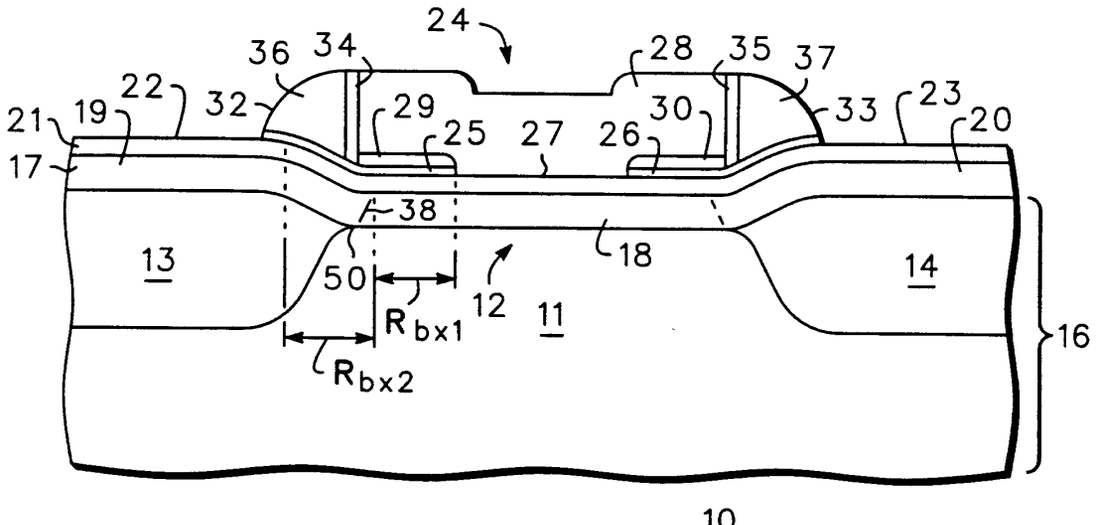

FIG. 1

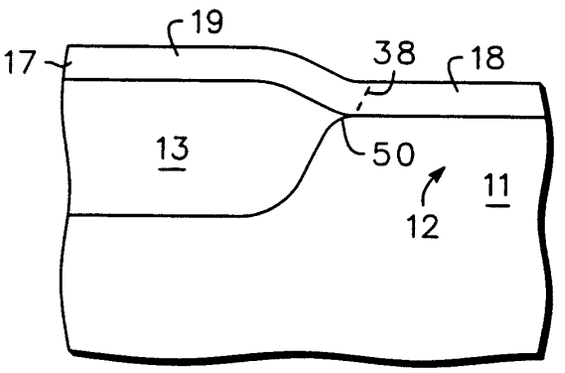

FIG. 2

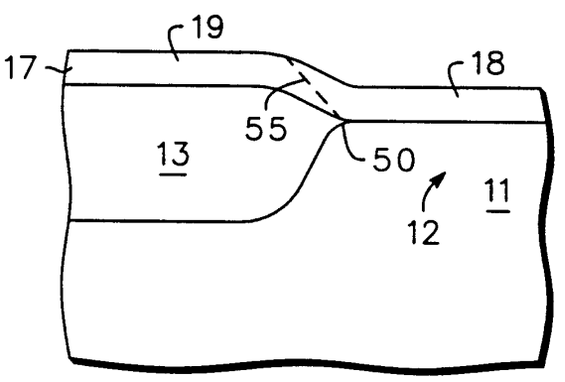

FIG. 3

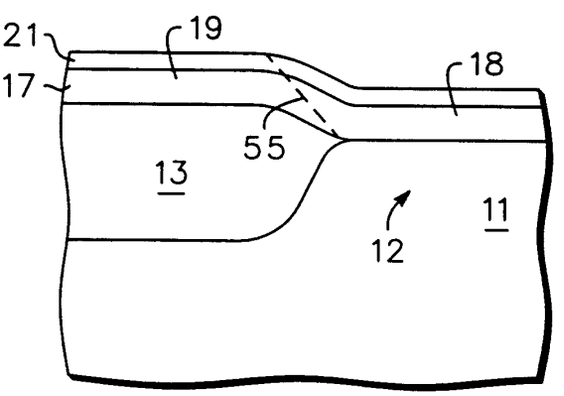

FIG. 4

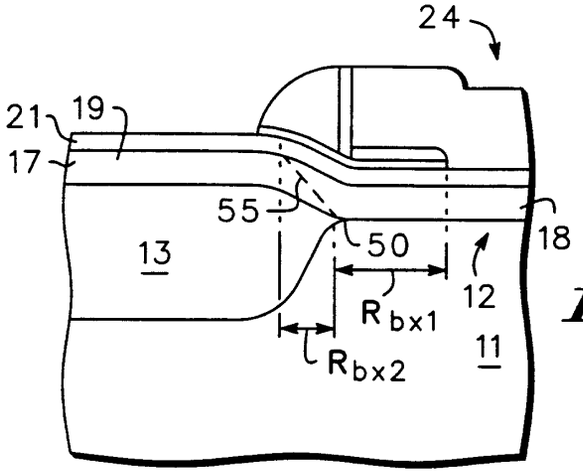

FIG. 5

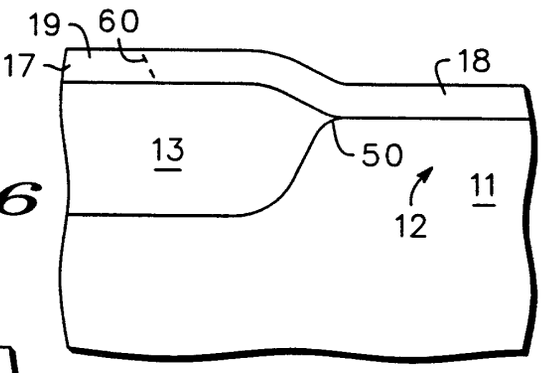

FIG. 6

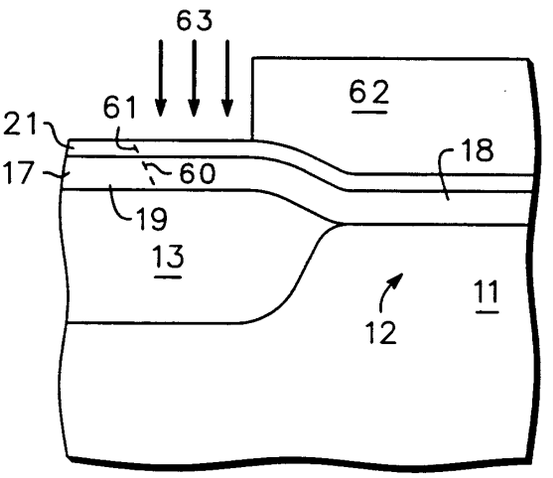

FIG. 7

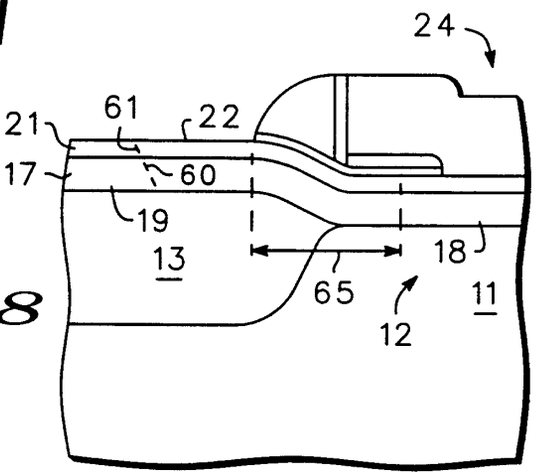

FIG. 8

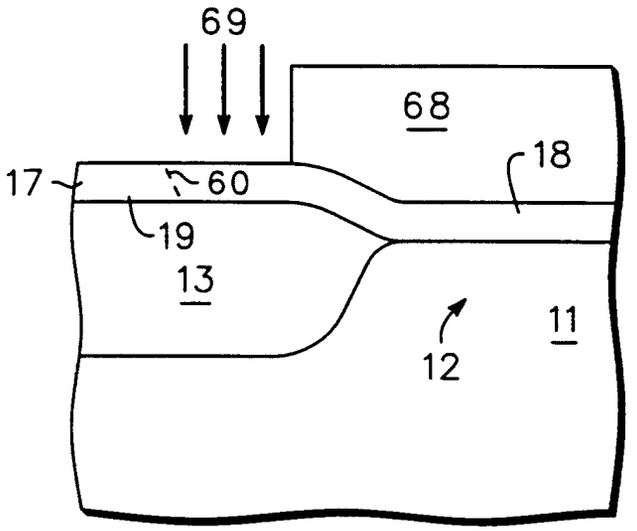

FIG. 9

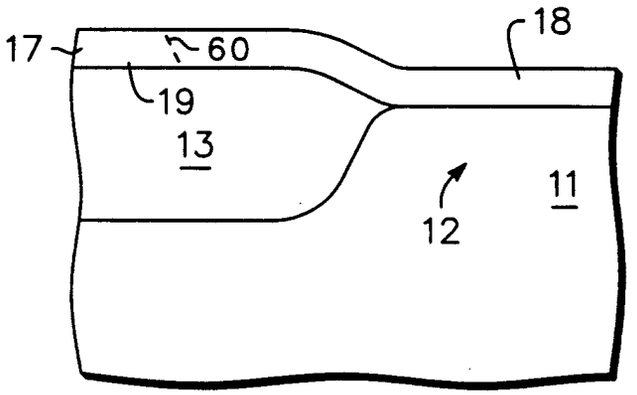

FIG. 10

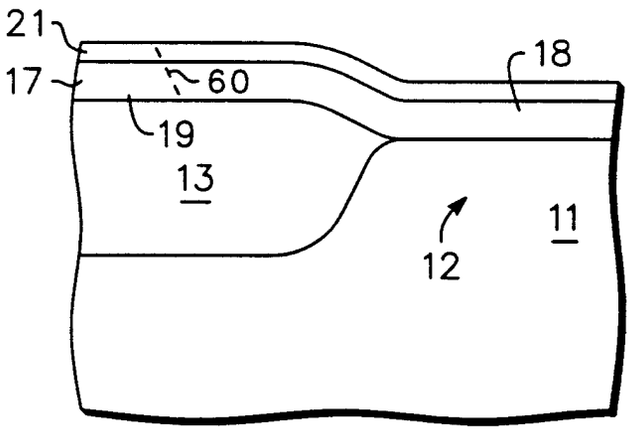

FIG. 11