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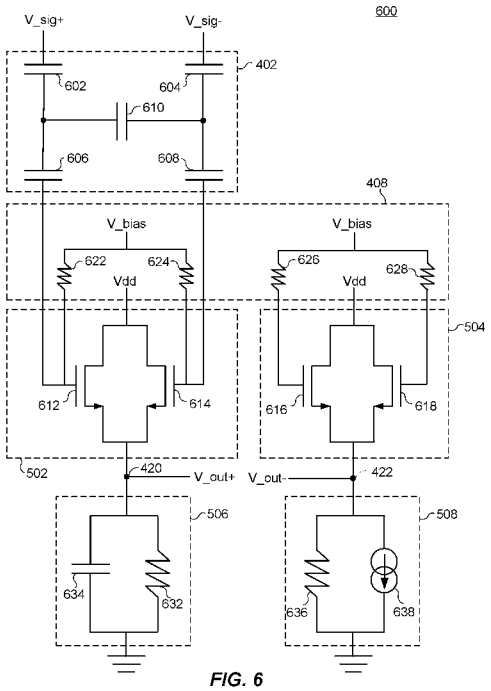

FIG. 6

(57) Abstract: The disclosure relates to technology for signal strength detection. An apparatus for detecting signal strength is disclosed. The apparatus comprises a differential sensor stage having an input and an output, a differential reference stage having an input and an output, a capacitor stage configured to couple an input signal to the input of the differential sensor stage, a biasing circuit configured to bias the differential sensor stage and the differential reference stage. The apparatus has a differential output between the output of the differential sensor stage and the output of the differential reference stage. The differential output is configured to provide a signal indicative of strength of the input signal.

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SIGNAL STRENGTH DETECTOR

FIELD

[0001] The disclosure generally relates to detecting a strength of a signal, such as a Radio Frequency (RF) signal.

BACKGROUND

[0002] Signal power detectors are widely used to detect the power level of signal. For example, signal power detectors may be used in communication systems, radar systems, and measurement instruments. A signal power detector may produce a voltage signal indicative of a power of an input signal. For example, an RF power detector may produce a voltage signal indicative of a power of an RF signal. RF power detectors may be used in wireless RF communication systems to monitor the power of an RF signal transmitted by an RF transmitter and/or the power of an RF signal received by an RF receiver.

[0003] The accuracy of a signal power detectors may be impacted by factors such as process variations and operating temperature. A process variation refers to the process used to fabricate the signal power detector. For example, there could be mismatches be transistors, capacitors, resistors or other electrical components that may result in inaccurate determination of the signal power level.

[0004] Changes in operating temperature may also impact the accuracy of the signal power detector. For example, the output voltage for a given signal power level may be temperature dependent for some conventional signal power detectors. Thus, some conventional signal power detectors may not produce an accurate result across a range of operating temperatures. In many cases, a signal power detector is used in an environment in which there could be a wide range in operating temperature. For

example, the signal power detector could be located near electrical components that generate substantial heat.

BRIEF SUMMARY

[0005] According to one aspect of the present disclosure, there is provided an apparatus for detecting signal strength. The apparatus comprises a differential sensor stage having an input and an output, a differential reference stage having an input and an output, a capacitor stage configured to couple an input signal to the input of the differential sensor stage, a biasing circuit configured to bias the differential sensor stage and the differential reference stage, a differential output between the output of the differential sensor stage and the output of the differential reference stage. The differential output is configured to provide a signal indicative of strength of the input signal.

[0006] Optionally, in any of the preceding aspects, the biasing circuit is configured to bias the differential sensor stage and the differential reference stage in a weak inversion region.

[0007] Optionally, in any of the preceding aspects, the biasing circuit is configured to apply substantially the same bias conditions to the differential sensor stage and to the differential reference stage.

[0008] Optionally, in any of the preceding aspects, the capacitor stage is configured to keep the differential sensor stage operating in the weak inversion region.

[0009] Optionally, in any of the preceding aspects, the capacitor stage is configured to keep the input signal at the input of the differential sensor stage within a target range to keep the differential sensor stage operating in the weak inversion region.

[0010] Optionally, in any of the preceding aspects, the capacitor stage comprises an H-type capacitor bridge.

[0011] Optionally, in any of the preceding aspects, the H-type capacitor bridge comprises: a first capacitor having a first terminal and a second terminal; a second

capacitor having a first terminal and a second terminal, the first terminals of the first capacitor and the second capacitor configured to receive the input signal; a third capacitor having a first terminal connected to the second terminal of the first capacitor, the third capacitor having a second terminal connected to a first terminal of the input of the differential sensor stage; a fourth capacitor having a first terminal connected to the second terminal of the second capacitor, the fourth capacitor having a second terminal connected to a second terminal of the input of the differential sensor stage; and a fifth capacitor having a first terminal connected to the second terminal of the first capacitor and to the first terminal of the third capacitor, the fifth capacitor having a second terminal connected to the second terminal of the second capacitor and to the first terminal of the fourth capacitor.

[0012] Optionally, in any of the preceding aspects, the first capacitor and the second capacitor have substantially the same capacitance.

[0013] Optionally, in any of the preceding aspects, the third capacitor and the fourth capacitor have substantially the same capacitance.

[0014] Optionally, in any of the preceding aspects, the differential sensor stage comprises a first transistor and a second transistor having a source follower configuration. The differential reference stage comprises a third transistor and a fourth transistor having a source follower configuration.

[0015] Optionally, in any of the preceding aspects, the differential sensor stage comprises a first MOSFET transistor and a second MOSFET transistor having a source follower configuration. The differential reference stage comprises a third MOSFET transistor and a fourth MOSFET transistor having a source follower configuration.

[0016] Optionally, in any of the preceding aspects, the differential sensor stage comprises a first loading block coupled to the output of the differential sensor stage. The differential reference stage comprises a second loading block coupled to the output of the differential reference stage.

[0017] Optionally, in any of the preceding aspects, the first loading block comprises a first resistor. The second loading block comprises a second resistor. The first resistor and the second resistor have substantially the same resistance.

[0018] Optionally, in any of the preceding aspects, the second loading block is configured to provide temperature compensation for the circuit.

[0019] Optionally, in any of the preceding aspects, the second loading block is configured to keep the signal at the differential output within a target range independent of temperature.

[0020] Optionally, in any of the preceding aspects, the second loading block further comprises a proportional to absolute temperature (PTAT) current source in parallel with the second resistor.

[0021] Optionally, in any of the preceding aspects, the first loading block further comprises a capacitor in parallel with the first resistor.

[0022] Optionally, in any of the preceding aspects, the first loading block comprises a passive loading block. The second loading block comprises an active loading block.

[0023] Optionally, in any of the preceding aspects, the first loading block is configured to provide temperature compensation.

[0024] Optionally, in any of the preceding aspects, the first loading block is configured to keep the signal at the differential output within a target range independent of temperature.

[0025] Optionally, in any of the preceding aspects, the first loading block further comprises a complimentary to absolute temperature (CTAT) current source in parallel with the first resistor.

[0026] Optionally, in any of the preceding aspects, the first loading block comprises an active loading block. The second loading block comprises a passive loading block.

[0027] Optionally, in any of the preceding aspects, the input signal is based on a radio frequency (RF) signal.

[0028] Optionally, in any of the preceding aspects, the apparatus further comprises an RF transmitter configured to generate the RF signal. The apparatus still further comprises an antenna coupled to the RF transmitter and configured to transmit the RF signal. The strength of the input signal is proportional to power of the transmitted RF signal.

[0029] Optionally, in any of the preceding aspects, the apparatus further comprises an RF receiver configured to generate the RF signal. The apparatus still further comprises an antenna coupled to the RF receiver and configured to receive the RF signal. The strength of the input signal is proportional to power of the received RF signal.

[0030] Optionally, in any of the preceding aspects, the strength comprises a peak voltage of the input signal.

[0031] Optionally, in any of the preceding aspects, the strength corresponds to a peak power of the input signal.

[0032] A further aspect comprises a method for detecting signal strength. The method comprises biasing a differential sensor stage having an input and an output. The method comprises biasing a differential reference stage having an input and an output. The method comprises coupling an input signal to the input of the differential sensor stage using a capacitor stage. The method comprises providing a signal indicative of strength of the input signal at a differential output between the output of the differential sensor stage and the output of the differential reference stage.

[0033] A further aspect comprises a wireless communication device. The wireless communication device comprises a transceiver configured to receive and to transmit radio frequency (RF) signals, a differential sensor stage having an input and an output, a differential reference stage having an input and an output, a capacitor stage coupled to the transceiver and configured to couple a voltage signal based on an RF signal to

the input of the differential sensor stage, a biasing circuit configured to bias the differential sensor stage and the differential reference stage, and a differential output between the output of the differential sensor stage and the output of the differential reference stage. The differential output is configured to provide a signal indicative of power of the RF signal.

[0034] This Summary is provided to introduce a selection of concepts in a simplified form that are further described below in the Detailed Description. This Summary is not intended to identify key features or essential features of the claimed subject matter, nor is it intended to be used as an aid in determining the scope of the claimed subject matter. The claimed subject matter is not limited to implementations that solve any or all disadvantages noted in the Background.

BRIEF DESCRIPTION OF THE DRAWINGS

[0035] Aspects of the present disclosure are illustrated by way of example and are not limited by the accompanying figures for which like references indicate elements.

[0036] FIG. 1 illustrates a wireless network for communicating data.

[0037] FIG. 2 illustrates example details of user equipment (UE) that may implement the methods and teachings according to this disclosure.

[0038] FIG. 3 illustrates an example base station (BS) that may implement the methods and teachings according to this disclosure.

[0039] FIG. 4 depicts an apparatus that is configured to detect the strength of an input signal.

[0040] FIG. 5 depicts one embodiment of an apparatus that is configured to detect a strength of an input signal.

[0041] FIG. 6 is a circuit schematic of one embodiment of a signal power detector.

[0042] FIG. 7 is a circuit schematic of one embodiment of a signal power detector.

[0043] FIG. 8 depicts a flowchart of one embodiment of a process of detecting a power of an input signal.

[0044] FIG. 9 depicts a flowchart of one embodiment of a process of operating differential stages of a signal power detector in a weak inversion region.

[0045] FIG. 10 depicts a flowchart of one embodiment of a process of providing temperature compensation in a signal power detector.

[0046] FIG. 11 depicts relationships between signal power and voltages of a MOSFETs in an embodiment of a signal power detector.

[0047] FIG. 12 depicts a flowchart of one embodiment of a process of adjusting the sensitivity of an RF receiver based on a detected power level of an RF signal received by the RF receiver.

[0048] FIG. 13 depicts a flowchart of one embodiment of a process of adjusting the gain of an RF transmitter based on a detected power level of an RF signal transmitted by the RF transmitter.

DETAILED DESCRIPTION

[0049] The present disclosure will now be described with reference to the figures, which in general relate to an apparatus and method for detecting a strength of a signal. The signal strength could be a power level, a voltage level, but is not limited thereto. The apparatus is able to detect the signal strength with high accuracy. In some embodiments, the apparatus compensates for process variations. For example, there may be some structural differences between transistors. In some embodiments, the apparatus compensates for operating temperature variations.

[0050] It is understood that the present embodiments of the disclosure may be implemented in many different forms and that claims scopes should not be construed as being limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete and will fully convey the inventive embodiment concepts to those skilled in the art. Indeed, the disclosure is

intended to cover alternatives, modifications and equivalents of these embodiments, which are included within the scope and spirit of the disclosure as defined by the appended claims. Furthermore, in the following detailed description of the present embodiments of the disclosure, numerous specific details are set forth in order to provide a thorough understanding. However, it will be clear to those of ordinary skill in the art that the present embodiments of the disclosure may be practiced without such specific details.

[0051] Signal power detectors may be used within wireless networks for communicating data, but are not limited to wireless networks. FIG. 1 illustrates a wireless network for communicating data. The communication system 100 includes, for example, user equipment 110A, 110B, and 110C, radio access networks (RANs) 120A and 120B, a core network 130, a public switched telephone network (PSTN) 140, the Internet 150, and other networks 160. Additional or alternative networks include private and public data-packet networks including corporate intranets. While certain numbers of these components or elements are shown in the figure, any number of these components or elements may be included in the system 100. Some embodiments of signal power detectors are implemented in UE 110. Some embodiments of signal power detectors are implemented in RAN 120. Signal power detectors may be used elsewhere in the communication system 100.

[0052] In one embodiment, the wireless network may be a fifth generation (5G) network including at least one 5G base station which employs orthogonal frequency-division multiplexing (OFDM) and/or non-OFDM and a transmission time interval (TTI) shorter than 1 ms (e.g., 100 or 200 microseconds), to communicate with the communication devices. In general, a base station may also be used to refer any of the eNB and the 5G BS (gNB). In addition, the network may further include a network server for processing information received from the communication devices via the at least one eNB or gNB.

[0053] System 100 enables multiple wireless users to transmit and receive data and other content. The system 100 may implement one or more channel access methods, such as but not limited to code division multiple access (CDMA), time

division multiple access (TDMA), frequency division multiple access (FDMA), orthogonal FDMA (OFDMA), or single-carrier FDMA (SC-FDMA).

[0054] The user equipment (UE) 110A, 110B, and 110C, which can be referred to individually as a UE 110, or collectively as the UEs 110, are configured to operate and/or communicate in the system 100. For example, a UE 110 can be configured to transmit and/or receive wireless signals or wired signals. Each UE 110 represents any suitable end user device and may include such devices (or may be referred to) as a user equipment/device, wireless transmit/receive unit (UE), mobile station, fixed or mobile subscriber unit, pager, cellular telephone, personal digital assistant (PDA), smartphone, laptop, computer, touchpad, wireless sensor, wearable devices or consumer electronics device.

[0055] In the depicted embodiment, the RANs 120A, 120B include one or more base stations (BSs) 170A, 170B, respectively. The RANs 120A and 120B can be referred to individually as a RAN 120, or collectively as the RANs 120. Similarly, the base stations (BSs) 170A and 170B can be referred individually as a base station (BS) 170, or collectively as the base stations (BSs) 170. Each of the BSs 170 is configured to wirelessly interface with one or more of the UEs 110 to enable access to the core network 130, the PSTN 140, the Internet 150, and/or the other networks 160. For example, the base stations (BSs) 170 may include one or more of several well-known devices, such as a base transceiver station (BTS), a Node-B (NodeB), an evolved NodeB (eNB), a next (fifth) generation (5G) NodeB (gNB), a Home NodeB, a Home eNodeB, a site controller, an access point (AP), or a wireless router, or a server, router, switch, or other processing entity with a wired or wireless network.

[0056] In one embodiment, the BS 170A forms part of the RAN 120A, which may include one or more other BSs 170, elements, and/or devices. Similarly, the BS 170B forms part of the RAN 120B, which may include one or more other BSs 170, elements, and/or devices. Each of the BSs 170 operates to transmit and/or receive wireless signals within a particular geographic region or area, sometimes referred to as a “cell.” In some embodiments, multiple-input multiple-output (MIMO) technology may be employed having multiple transceivers for each cell.

[0057] The BSs 170 communicate with one or more of the UEs 110 over one or more air interfaces (not shown) using wireless communication links. The air interfaces may utilize any suitable radio access technology.

[0058] It is contemplated that the system 100 may use multiple channel access functionality, including for example schemes in which the BSs 170 and UEs 110 are configured to implement the Long Term Evolution wireless communication standard (LTE), LTE Advanced (LTE-A), and/or LTE Multimedia Broadcast Multicast Service (MBMS). In other embodiments, the base stations 170 and user equipment 110A-110C are configured to implement UMTS, HSPA, or HSPA+ standards and protocols. Of course, other multiple access schemes and wireless protocols may be utilized.

[0059] The RANs 120 are in communication with the core network 130 to provide the UEs 110 with voice, data, application, Voice over Internet Protocol (VoIP), or other services. As appreciated, the RANs 120 and/or the core network 130 may be in direct or indirect communication with one or more other RANs (not shown). The core network 130 may also serve as a gateway access for other networks (such as PSTN 140, Internet 150, and other networks 160). In addition, some or all of the UEs 110 may include functionality for communicating with different wireless networks over different wireless links using different wireless technologies and/or protocols.

[0060] The RANs 120 may also include millimeter and/or microwave access points (APs). The APs may be part of the BSs 170 or may be located remote from the BSs 170. The APs may include, but are not limited to, a connection point (an mmW CP) or a BS 170 capable of mmW communication (e.g., a mmW base station). The mmW APs may transmit and receive signals in a frequency range, for example, from 24 GHz to 100 GHz, but are not required to operate throughout this range. As used herein, the term base station is used to refer to a base station and/or a wireless access point.

[0061] Although FIG. 1 illustrates one example of a communication system, various changes may be made to FIG. 1. For example, the communication system 100 could include any number of user equipment, base stations, networks, or other components in any suitable configuration. It is also appreciated that the term user equipment may refer to any type of wireless device communicating with a radio network node in a

cellular or mobile communication system. Non-limiting examples of user equipment are a target device, device-to-device (D2D) user equipment, machine type user equipment or user equipment capable of machine-to-machine (M2M) communication, laptops, PDA, iPad, Tablet, mobile terminals, smart phones, laptop embedded equipped (LEE), laptop mounted equipment (LME) and USB dongles.

[0062] FIG. 2 illustrates example details of a UE 110 that may implement the methods and teachings according to this disclosure. The UE 110 may for example be a mobile telephone, but may be other devices in further examples such as a desktop computer, laptop computer, tablet, hand-held computing device, automobile computing device and/or other computing devices. As shown in the figure, the exemplary UE 110 is shown as including at least one transmitter 202, at least one receiver 204, memory 206, at least one processor 208, and at least one input/output device 212. The processor 208 can implement various processing operations of the UE 110. For example, the processor 208 can perform signal coding, data processing, power control, input/output processing, or any other functionality enabling the UE 110 to operate in the system 100 (FIG. 1). The processor 208 may include any suitable processing or computing device configured to perform one or more operations. For example, the processor 208 may include a microprocessor, microcontroller, digital signal processor, field programmable gate array, or application specific integrated circuit. The memory 206 is non-transitory memory storage, in one embodiment.

[0063] The transmitter 202 can be configured to modulate data or other content for transmission by at least one antenna 210. The transmitter 202 can also be configured to amplify, filter and a frequency convert RF signals before such signals are provided to the antenna 210 for transmission. The transmitter 202 can include any suitable structure for generating signals for wireless transmission. In some embodiments, a signal power detector is used to detect a power level of a signal generated by transmitter 202. In some embodiments, the signal power detector output includes a DC voltage that is indicative of the power of the signal (e.g., RF signal). The DC voltage could be indicative of the power of the signal at the output of the transmitter 202, or the power of a wireless RF signal transmitted by the antenna 210.

[0064] The receiver 204 can be configured to demodulate data or other content received by the at least one antenna 210. The receiver 204 can also be configured to amplify, filter and frequency convert RF signals received via the antenna 210. The receiver 204 is an RF signal receiver, in some embodiments. The receiver 204 can include any suitable structure for processing signals received wirelessly. The antenna 210 can include any suitable structure for transmitting and/or receiving wireless signals. The same antenna 210 can be used for both transmitting and receiving RF signals, or alternatively, different antennas 210 can be used for transmitting signals and receiving signals. In some embodiments, a signal power detector is used to detect a power level of a signal received by antenna. In some embodiments, the signal power detector output includes a DC voltage that is indicative of the power of the signal (e.g., RF signal) received by antenna.

[0065] It is appreciated that one or multiple transmitters 202 could be used in the UE 110, one or multiple receivers 204 could be used in the UE 110, and one or multiple antennas 210 could be used in the UE 110. Although shown as separate blocks or components, at least one transmitter 202 and at least one receiver 204 could be combined into a transceiver. Accordingly, rather than showing a separate block for the transmitter 202 and a separate block for the receiver 204 in FIG. 2, a single block for a transceiver could have been shown.

[0066] The UE 110 further includes one or more input/output devices 212. The input/output devices 212 facilitate interaction with a user. Each input/output device 212 includes any suitable structure for providing information to or receiving information from a user, such as a speaker, microphone, keypad, keyboard, display, or touch screen.

[0067] In addition, the UE 110 includes at least one memory 206. The memory 206 stores instructions and data used, generated, or collected by the UE 110. For example, the memory 206 could store software or firmware instructions executed by the processor(s) 208 and data used to reduce or eliminate interference in incoming signals. Each memory 206 includes any suitable volatile and/or non-volatile storage and retrieval device(s). Any suitable type of memory may be used, such as random

access memory (RAM), read only memory (ROM), hard disk, optical disc, subscriber identity module (SIM) card, memory stick, secure digital (SD) memory card, and the like.

[0068] FIG. 3 illustrates an example BS 170 that may implement the methods and teachings according to this disclosure. As shown in the figure, the BS 170 includes at least one processor 308, at least one transmitter 302, at least one receiver 304, one or more antennas 310, and at least one memory 306. The processor 308 implements various processing operations of the BS 170, such as signal coding, data processing, power control, input/output processing, or any other functionality. Each processor 308 includes any suitable processing or computing device configured to perform one or more operations. Each processor 308 could, for example, include a microprocessor, microcontroller, digital signal processor, field programmable gate array, or application specific integrated circuit. The memory 306 is non-transitory memory storage, in one embodiment.

[0069] Each transmitter 302 includes any suitable structure for generating signals for wireless transmission to one or more UEs 110 or other devices. Each receiver 304 includes any suitable structure for processing signals received wirelessly from one or more UEs 110 or other devices. Although shown as separate blocks or components, at least one transmitter 302 and at least one receiver 304 could be combined into a transceiver. Each antenna 310 includes any suitable structure for transmitting and/or receiving wireless signals. While a common antenna 310 is shown here as being coupled to both the transmitter 302 and the receiver 304, one or more antennas 310 could be coupled to the transmitter(s) 302, and one or more separate antennas 310 could be coupled to the receiver(s) 304. Each memory 306 includes any suitable volatile and/or non-volatile storage and retrieval device(s).

[0070] In some embodiments, the base station 170 includes a signal power detector that is configured to detect a power level of a signal transmitted by transmitter 302. In some embodiments, the base station 170 includes a signal power detector that is configured to detect a power level of a signal received by receiver 304. In some embodiments, the signal power detector outputs a DC voltage that is indicative of the

power level of an RF signal (which may be received or transmitted by base station 170).

[0071] FIG. 4 depicts an apparatus 400 that is configured to detect the strength of an input signal. For example, the apparatus 400 could detect a power level or a voltage level of the input signal to the capacitor stage 402. In some cases, it is desirable to determine a power level of a RF signal, such as a wireless RF signal. In such cases, the input signal in FIG. 4 is not necessarily the wireless RF signal. Rather, the input signal may be a voltage signal that has a magnitude that is proportional to the power of the wireless RF signal. For purposes of comparing the magnitude of the voltage signal to the power of the RF signal, the voltage signal may associated with a resistance. In one embodiment, the relationship between the input signal and the power of an RF signal is given by:

$$P = A * V^2 / R \qquad \text{Eq. 1}$$

[0072] In equation 1, P is the power of the RF signal, V is the voltage of the input signal, R is a resistance associated with the input signal, and A is a proportionality factor, which may be determined empirically. Thus, based on the strength of the input signal, the power of the wireless RF signal may be determined.

[0073] In one embodiment, the input signal in FIG. 4 is an RF signal (but not required to be a wireless RF signal). The apparatus 400 may be used in system 100, but is not limited to a communication system. In one embodiment, the apparatus 400 is used in UE 110 (such as a wireless communication device). The apparatus 400 may be used in other devices such as RANs 120. In one embodiment, the apparatus 400 is used to detect a power level of a RF signal that is received by a wireless communication device. In one embodiment, the apparatus 400 is used to detect a power level of a RF signal that is transmitted by a wireless communication device. The term “input signal” is used because the signal is input into the apparatus 400. However, this does not mean that the signal is necessarily input to, for example, a wireless communication device. For example, the input signal could come from a transmitter in a wireless communication device.

[0074] The apparatus includes a capacitor stage 402, a differential sensor stage 404, a differential reference stage 406, and a biasing circuit 408. In some embodiments, the differential sensor stage 404 and the differential reference stage 406 are operated in a weak inversion region. A weak inversion system is one in which transistors are operated in the weak inversion region (e.g., gate-to-source voltages are below required threshold voltages). Operating the transistors in the weak inversion region may make the apparatus 400 less sensitive to structural differences between the transistors. Such structural differences may occur due to limitations in the process of fabricating the transistors. Hence, operating the transistors in the weak inversion region may reduce inaccuracies due to such structural differences. One possible equation to describe the weak inversion region is given by Equation 2.

$$I_{ds} = I_s \, e^{\frac{V_{gs}-V_{th}}{nV_t}} \quad \text{Eq. 2}$$

[0075] In Equation 2, I_{ds} is the drain to source current, I_s is a characteristic current that defines the current that leaks through the transistor, Vgs is the gate to source voltage, V_{th} is the threshold voltage of the transistor, n is the subthreshold slope factor, and Vt is the thermal voltage (kT/q). Equation 1 applies for when Vgs is less than or equal to Vth. Note that while Equation 1 represents one possible way to describe the weak inversion region, other equations may be used. For example, other equations could add additional factors.

[0076] The biasing circuit 408 is configured to bias the differential sensor stage 404 and the differential reference stage 406. In one embodiment, the biasing circuit 408 is configured to bias the differential sensor stage 404 and the differential reference stage 406 in the weak inversion region. The biasing circuit 408 provides voltages to bias input 416 of the differential sensor stage 404 and a bias input 418 of the differential reference stage 406.

[0077] The capacitor stage 402 is configured to couple the input signal to the differential sensor stage 404. The capacitor stage 402 has an input 410 that is configured to receive the input signal. Note that the input signal could be provided by, for example, transmitter 202 or receiver 204 (see FIG. 2). Such signals are not

necessarily wireless signals (such as the RF signal received by or transmitted from antenna 210). In some embodiments, the apparatus 400 detects the power level of the input signal, which may be correlated to the power level of, for example, an RF signal received by or transmitted from antenna 210.

[0078] The capacitor stage 402 has an output 412 that is connected to a signal input 414 of the differential sensor stage 404. Note that the signal input 414 may overlap in whole or in part with the bias input 416. For example, both the signal input 414 and the bias input 416 may include gate terminals of MOS transistors.

[0079] In one embodiment, the capacitor stage 402 is configured to keep the strength of the input signal at the input of the differential sensor stage 404 within a target range, which in turn keeps the transistors (in the differential sensor stage 404) in the weak inversion region. In one embodiment, the target range is a target voltage range. Therefore, in some embodiments, the capacitor stage 402 helps to overcome structural differences in the transistors due to, for example, process variations. Therefore, the capacitor stage 402 may improve accuracy of the apparatus 400 in signal strength detection.

[0080] The differential sensor stage 404 has an output 420. The differential reference stage 406 has an output 422. A voltage between these two outputs 420, 422 serves as a differential output for the apparatus 400. In some embodiments, the DC voltage between these two outputs 420, 422 serves as the differential output for the apparatus 400. In one embodiment, the voltage (e.g., DC voltage) between outputs 420, 422 is indicative of the strength of the input signal. In some cases, the strength of the input signal may be proportional to the power another signal, such as a wireless RF signal, as described in Equation 1. In one embodiment, the apparatus 400 is configured as a peak power detector. For example, the apparatus 400 could detect the peak power of an RF signal.

[0081] FIG. 5 depicts one embodiment of an apparatus 500 that is configured to detect a strength (e.g., voltage level, power level) of an input signal. The input signal may be based on an RF signal. The apparatus 500 may be used to, for example, detect a power of a wireless RF signal without directly measuring the power of the RF

signal. As discussed above in connection with Equation 1, the strength of the input signal may be proportional to the power in a wireless RF signal. However, the apparatus 500 has other uses than detecting the power of a wireless RF signal. The apparatus 500 may be used in system 100, but is not limited to a communication system. In one embodiment, the apparatus 400 is used in UE 110 (such as a wireless communication device). The apparatus 500 may be used on other devices such as RANs 120.

[0082] The apparatus 500 depicts further details of one embodiment of apparatus 400. In particular, further details of one embodiment of the differential sensor stage 404 and the differential reference stage 406 are depicted. The differential sensor stage 404 includes sensor transistors 502 and a sensor loading block 506. The differential reference stage 406 includes reference transistors 504 and a reference loading block 508.

[0083] In one embodiment, the sensor transistors 502 and the reference transistors 504 include MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor) transistors. The sensor transistors 502 and the reference transistors 504 may be of the same type. In one embodiment, the sensor transistors 502 and the reference transistors 504 include MOSFET transistors. The sensor transistors 502 and the reference transistors 504 may have the same configuration. In one embodiment, the sensor transistors 502 and the reference transistors 504 include MOSFET transistors having a source follower configuration.

[0084] The various transistors could have some structural differences due to variations in the fabrication process. There could be structural differences between the sensor transistors 502 and the reference transistors 504. There could be structural differences between transistors in the sensor transistors 502. There could be structural differences between transistors in the reference transistors 504. Such structural difference could result in different properties, such as different capacitance. In some cases, there could be up to a 20 percent difference in the capacitance of two transistors. In some cases, there could be greater than a 20 percent difference in the capacitance of two transistors. In some embodiments, the apparatus 500 operates

the transistors in the weak inversion region. Operating the transistors in the weak inversion region may make the transistors less sensitive to such structural and property variations, such that accuracy of the apparatus 500 is improved.

[0085] In one embodiment, the sensor loading block 506 and the reference loading block 508 each include a resistor. These resistors may be substantially matched in resistance. However, the resistors are not required to have exactly the same resistance. For example, due to limitations of the fabrication process, the resistances could differ somewhat from each other. In one embodiment, the resistance values are within two percent of each other. In one embodiment, the resistance values are within five percent of each other. In one embodiment, the resistance values are within 10 percent of each other.

[0086] In one embodiment, the signal at the differential sensor stage output 420 has both a DC component and an AC component. The DC component may arise at least in part from the biasing circuit 408. The AC component may arise due to the input signal. The sensor loading block 506 has a capacitor in parallel with the aforementioned resistor. The capacitor and resistor may form a filter. In one embodiment, the filter smooths the AC component, which may serve to stabilize the voltage at the differential sensor stage output 420.

[0087] In some embodiments, the apparatus 500 provides temperature compensation. In one embodiment, the temperature compensation is provided in the reference loading block 508. In one embodiment, the temperature compensation is provided by a proportional to absolute temperature (PTAT) current source in the reference loading block 508. In one embodiment, the temperature compensation is provided in the sensor loading block 506. In one embodiment, the temperature compensation is provided by a complimentary to absolute temperature (CTAT) current source in the sensor loading block 506.

[0088] The PTAT or CTAT current source may help to keep the output signal at the differential output (between the outputs 420, 422) within a target range. For example, the current source can be tuned in the factory to target an output signal range of between 10 dB to 20 dB. As another example, the current source can be tuned in the

factory to target an output signal range of between 0 dB to 10 dB. In one embodiment, the PTAT current source in the reference loading block 508 helps to keep the output signal in the target range independent of operating temperature. In one embodiment, the CTAT current source in the sensor loading block 506 helps to keep the output signal in the target range independent of operating temperature. In some embodiment, each output 420, 422 is at the source terminal of a MOSFET transistor. By regulating the source terminal voltage, the gate to source voltage of the MOSFETs may be regulated. Thus, either technique helps to keep the transistors operating in the weak inversion region where they are less sensitive to process variation. Therefore, the accuracy of the apparatus 500 is improved.

[0089] FIG. 6 is a circuit schematic of one embodiment of a signal power detector. The signal power detector 600 may be used to detect the power of an RF signal, but is not limited to RF signals. The signal power detector 600 may be used in system 100, but is not limited to a communication system. In one embodiment, the signal power detector 600 is used in UE 110 (such as a wireless communication device). The signal power detector 600 may be used on other devices such as RANs 120.

[0090] The signal power detector 600 includes a capacitor stage 402, a biasing circuit 408, sensor transistors 502, reference transistors 504, sensor loading block 506, and reference loading block 508. Together the sensor transistors 502 and the sensor loading block 506 are one embodiment of a differential sensor stage 404. Together the reference transistors 504 and the reference loading block 508 are one embodiment of a differential reference stage 406.

[0091] The capacitor stage 402 includes an H-type capacitor bridge. The capacitor stage 402 receives an input signal (V_sig+, V_sig-). The input signal (V_sig+, V_sig-) may be based on or otherwise derived from an RF signal. In some embodiments, an RF signal is converted to the input signal. The input signal may be referred to herein as a voltage signal. In one embodiment, the input signal is derived from an RF signal generated by transmitter 202. In one embodiment, the input signal is derived from an RF signal received from antenna 210. In some embodiments, the signal power

detector 600 detects a peak power level of an RF wireless signal based on detecting a peak voltage of V_sig+, V_sig-.

[0092] The H-type capacitor bridge includes five capacitors in the described embodiment. Herein, an "H-type capacitor bridge" is defined to include at least five capacitors in the configuration depicted in the capacitor stage 402 in FIG. 6. The capacitors in an H-type capacitor bridge may be referred to as first input capacitor 602, second input capacitor 604, first output capacitor 606, second output capacitor 608, and H-capacitor 610. The first input capacitor 602 has a first terminal configured to receive V_sig+. The first input capacitor 602 has a second terminal connected to a first terminal of the first output capacitor 606 and to a first terminal of the H-capacitor 610. The second input capacitor 604 has a first terminal configured to receive V_sig-. The second input capacitor 604 has a second terminal connected to a first terminal of the second output capacitor 608 and to a second terminal of the H-capacitor 610. The first output capacitor 606 has its first terminal connected to the first terminal of the H-capacitor 610. The first output capacitor 606 has its second terminal connected to a gate terminal of transistor 612. The second output capacitor 608 has its first terminal connected to the second terminal of the H-capacitor 610. The second output capacitor 608 has its second terminal connected to a gate terminal of transistor 614. Therefore, the H-type capacitor bridge is configured to couple the input signal to the gates of transistors 612, 614. Note that the gates of transistors 612, 614 may serve as a signal input of the differential sensor stage 404. Thus, the H-type capacitor bridge is configured to couple the input signal to the signal input of the differential sensor stage 404.

[0093] In one embodiment, the first input capacitor 602 and the second input capacitor 604 have substantially the same capacitance. In one embodiment, the first output capacitor 606 and the second output capacitor 608 have substantially the same capacitance. In one embodiment, two capacitors have substantially the same capacitance of their capacitances are withing two percent of each other. In one embodiment, two capacitors have substantially the same capacitance of their capacitances are withing five percent of each other. In one embodiment, two

capacitors have substantially the same capacitance of their capacitances are withing ten percent of each other.

[0094] In one embodiment, the ratio of the capacitance of the input capacitors 602, 604 to the capacitance of the output capacitors 606, 608 is selected in order to control how much of the input signal is coupled to the gates of the sensor transistors 502. In one embodiment, the capacitance of the H-capacitor 610 may range from about ten percent the capacitance as the input capacitors 602, 604 to being about the capacitance as the input capacitors 602, 604. In one embodiment, the capacitance of the H-capacitor 610 may range from about ten percent the capacitance as the output capacitors 606, 608 to being about the capacitance as the output capacitors 606, 608. The H-capacitor 610 could have a larger or smaller amounts of capacitance than these examples.

[0095] The sensor transistors 502 include first sensor NMOS transistor 612 and second sensor NMOS transistor 614. The sensor transistors 502 have a source follower configuration. The reference transistors 504 include first reference NMOS transistor 616 and second reference NMOS transistor 618. The reference transistors 504 have a source follower configuration. Note that the gates of the first sensor NMOS transistor 612 and the second sensor NMOS transistor 612 are one embodiment of the bias input 416 of the differential sensor stage 404. Similarly, the gates of the first reference NMOS transistor 616 and the second reference NMOS transistor 618 are one embodiment of the bias input 418 of the differential reference stage 406.

[0096] The bias circuit 408 has four bias resistors 622, 624, 626, 628. Bias resistor 622 is connected to the gate of first sensor NMOS transistor 612 in order to provide a bias voltage (V_bias). Bias resistor 624 is connected to the gate of second sensor NMOS transistor 614 in order to provide the bias voltage (V_ bias). Bias resistor 626 is connected to the gate of first reference NMOS transistor 616 in order to provide the bias voltage (V_bias). Bias resistor 628 is connected to the gate of second reference NMOS transistor 618 in order to provide the bias voltage (V_ bias). In one embodiment, the bias circuit 408 is configured to bias each of the transistors 612, 614, 616, and 618 in the weak inversion region.

[0097] The sensor loading block 506 includes a sensor load resistor 632 and a load capacitor 634. In one embodiment, the sensor load resistor 632 and the load capacitor 634 serve as a filter. The filter may be used to smooth an AC signal component at output 420. In some embodiments, output 422 of does not have an AC signal component. In some embodiments, the voltage between output 420 and output 422 is indicative of the peak power of the input signal. In FIG. 6, the sensor loading block 506 may be referred to as a passive loading block.

[0098] The reference loading block 508 includes a reference load resistor 636 and a PTAT current source 638. In one embodiment, the sensor load resistor 632 and the reference load resistor 636 are matched in resistance. There may be some difference in the resistances due to limitations of the process of fabricating the resistors.

[0099] The reference loading block 508 is configured to provide temperature compensation for the signal power detector 600. The PTAT current source 638 may be configured to provide the temperature compensation. In one embodiment, the PTAT current source 638 is tuned such that the output signal at the differential output (between output 420 and output 422) is within a target range. The PTAT current source helps to keep the output signal in the target range independent of operating temperature. Because the outputs are at the source terminals of the MOSFET transistors, the PTAT current source helps to keep the source voltage within a target range, even if the temperature varies. Therefore, the gate to source voltage of the MOSFET transistors may be regulated. Hence, the PTAT current source may help to keep the MOS transistors operating in weak inversion where they are less sensitive to process variation. Therefore, the accuracy of the detector 600 is improved. In FIG. 6, the reference loading block 508 may be referred to as an active loading block.

[00100] FIG. 7 is a circuit schematic of one embodiment of a signal power detector. The signal power detector 700 may be used to detect the power of an RF signal, but is not limited to RF signals. The signal power detector 700 may be used in system 100, but is not limited to a communication system. In one embodiment, the signal power detector 600 is used in UE 110 (such as a wireless communication device). The signal power detector 600 may be used on other devices such as RANs 120.

[00101] The signal power detector 700 in FIG. 7 is similar to the signal power detector 700, but the sensor loading block 506 and reference loading block 508 are configured differently. Whereas temperature compensation is provided by the reference loading block 508 in the circuit of FIG. 6, temperature compensation is provided by the sensor loading block 506 in the circuit of FIG. 7. The capacitor stage 402, biasing circuit 408, sensor transistors 502, and reference transistors 504 in signal power detector 700 are similar to those in signal power detector 600, as thus will not be described in detail.

[00102] The sensor loading block 506 includes a sensor load resistor 732, load capacitor 734, and CTAT current source 736. In one embodiment, the sensor load resistor 732 and the load capacitor 734 serve as a filter. The filter may be used to smooth an AC signal component at output 420. In some embodiments, output 422 of does not have an AC signal component. In some embodiments, the voltage between output 420 and output 422 is indicative of the peak power of the input signal.

[00103] The sensor loading block 506 is configured to provide temperature compensation for the signal power detector 700. The CTAT current source 736 may be configured to provide the temperature compensation. In one embodiment, the CTAT current source 736 is tuned such that the output signal at the differential output (between output 420 and output 422) is within a target range. The CTAT current source helps to keep the output signal in the target range independent of operating temperature. Because the outputs are at the source terminals of the MOSFET transistors, the CTAT current source helps to keep the source voltage within a target range, even if the temperature varies. Therefore, the gate to source voltage of the MOSFET transistors may be regulated. Hence, the CTAT current source may help to keep the MOSFET transistors operating in weak inversion where they are less sensitive to process variation. Therefore, the accuracy of the signal power detector 700 is improved. In FIG. 6, the passive loading block 508 may be referred to as an active loading block.

[00104] The reference loading block 508 includes a reference load resistor 738. In one embodiment, the sensor load resistor 732 and the reference load resistor 738 are

matched in resistance. There may be some difference in the resistances due to limitations of the process of fabricating the resistors. In FIG. 7, the reference loading block 508 may be referred to as a passive loading block.

[00105] FIG. 8 depicts a flowchart of one embodiment of a process 800 of detecting a strength of an input signal. In one embodiment, the input signal is an RF signal, or is a least based on an RF signal. The process 800 may be practiced in apparatus 400, apparatus 500, signal power detector 600, signal power detector 700, but is not limited thereto. The steps are described in a certain order as a matter of convenience of explanation. Some, or all, steps may occur at the same time.

[00106] Step 802 includes biasing a differential sensor stage 404. Step 802 may include the biasing circuit 408 applying V_bias to the gates of MOSFET transistor 612 and MOSFET transistor 614. Step 802 may also include applying Vdd to the drain terminals of MOSFET transistor 612 and MOSFET transistor 614. Step 802 may also include grounding the sensor loading block 506.

[00107] Step 804 includes biasing a differential reference stage 406. In some embodiments, substantially the same bias conditions are applied to the differential sensor stage 404 and to the differential reference stage 406. In one embodiment, step 804 includes the biasing circuit 408 applying V_bias to the gates of MOSFET transistor 616 and MOSFET transistor 618. Step 804 may also include applying Vdd to the drain terminals of MOSFET transistor 616 and MOSFET transistor 618. Step 804 may also include grounding the reference loading block 508.

[00108] Substantially the same bias conditions may be achieved by applying the same bias voltage to the gate terminals, and by applying substantially the supply voltage (e.g., Vdd) to the drain terminals. In some cases, there may some small differences in the exact bias voltage that is applied to the gates due to, for example, small differences in the resistances of the various bias resistors 622, 624, 626, 628. Also, there may some small differences in the exact bias voltage that is applied to the gates due to, for example, small differences in the bias voltage (e.g., V_bias) that is applied to the bias resistors 622, 624, 626, 628.

[00109] Step 806 includes coupling an input signal to the differential sensor using a capacitor stage 402. In one embodiment, the capacitor stage 402 includes an H-type capacitor bridge. The input signal could be generated by converting an RF signal to a voltage signal, where the voltage signal is proportional to the power of the RF signal as indicated in Equation 1.

[00110] Step 808 includes accessing, at a differential output, a signal that is indicative of the strength of the input signal. In some embodiments, the differential output is formed by the output 420 of the differential sensor stage 404 and the output 422 of the differential reference stage 406. In one embodiment, the signal is indicative of the peak voltage level of the input signal. In one embodiment, the signal is indicative of the peak power level of the input signal. Note that given Equation 1, the strength of the input signal may be correlated to another signal, such as the power of a wireless RF signal.

[00111] FIG. 9 depicts a flowchart of one embodiment of a process 900 of operating differential stages of a signal power detector in a weak inversion region. Process 900 describes one embodiment for operating differential sensor stage 404 and differential reference stage 406 in a weak inversion region. Process 900 describes further details for one embodiment of steps 802, 804, and 806 in process 800. In one embodiment, the input signal is an RF signal. The process 900 may be practiced in apparatus 400, apparatus 500, signal power detector 600, signal power detector 700, but is not limited thereto. The steps are described in a certain order as a matter of convenience of explanation. Some, or all, steps may occur at the same time.

[00112] Step 902 includes biasing a source follower configuration in a differential sensor stage 404 in a weak inversion region. Step 904 includes biasing a source follower configuration in a differential reference stage 406 in a weak inversion region. Steps 902 and 904 include applying a suitable bias voltage (V_bias) to the gates of the MOSFETs 612, 614, 616, and 618. The magnitude of the bias voltage will depend on the threshold voltage of the MOSFETs. The magnitude of the bias voltage may also depend on other factors such as the resistance of bias resistors 622, 624, 626, and 628, as well as load resistors 632, 636, 732, and/or 738.

[00113] Step 906 incudes coupling a voltage signal (e.g., V_sig+, V_sig-) to an input of a differential sensor stage 404 while keeping the differential sensor stage 404 in the weak inversion region. In one embodiment, the capacitor stage 402 is configured to keep the magnitude of the input signal that is coupled to the gates of the MOSFETs in the differential sensor stage 404 within a target range such that the MOSFETs in the differential sensor stage 404 are kept in the weak inversion region with the combination of the bias voltage and the coupled input voltage.

[00114] FIG. 10 depicts a flowchart of one embodiment of a process 1000 of providing temperature compensation in a signal power detector. Process 1000 describes further details of one embodiment of process 800. In one embodiment, the input signal is an RF signal. The process 1000 may be practiced in apparatus 400, apparatus 500, signal power detector 600, signal power detector 700, but is not limited thereto. The steps are described in a certain order as a matter of convenience of explanation. Some, or all, steps may occur at the same time.

[00115] Step 1002 includes biasing a differential sensor stage 404 having sensor transistors 612, 614 and a sensor loading block 506.

[00116] Step 1004 includes biasing a differential reference stage 406 having reference transistors 616, 618 and a reference loading block 508.

[00117] Step 1006 includes coupling an input signal to the differential sensor using a capacitor stage 402. In one embodiment, the capacitor stage 402 includes an H-type capacitor bridge.

[00118] Step 1008 includes providing temperature compensation using one of the loading blocks. In one embodiment, reference loading block 508 is used to provide the temperature compensation. In one embodiment, providing temperature compensation includes using a proportional to absolute temperature (PTAT) current source in the reference loading block 508. Providing temperature compensation using the reference loading block 508 may result in keeping the output signal at the differential output within a target range independent of temperature. This may help to

keep the MOSFETs operating in the weak inversion region, which can improve accuracy of the signal detector.

[00119] In one embodiment, sensor loading block 506 is used to provide the temperature compensation. In one embodiment, providing temperature compensation includes using a complimentary to absolute temperature (CTAT) current source in the sensor loading block 506. Providing temperature compensation using the sensor loading block 506 may result in keeping the output signal at the differential output within a target range independent of temperature. This may help to keep the MOSFETs operating in the weak inversion region, which can improve accuracy of the signal detector.

[00120] Step 1010 includes accessing, at a differential output, a signal that is indicative of the strength of the input signal.

[00121] FIG. 11 depicts relationships between signal power and voltages of a MOSFETs in an embodiment of a signal power detector. FIG. 11 pertains to one embodiment of the sensor MOSETs 612, 614. Line 1102 represents the DC gate voltage (Vg) of the MOSFET. This is the voltage that may arise due to biasing the MOSFET. Line 1106 represents the threshold voltage (Vth) of the MOSFET. Neither the DC gate voltage 1102 nor the threshold voltage 1106 depend on the signal power. Curve 1104 represents the source terminal voltage (Vs) of the MOSFET. Note that Vs increases as the signal power increases. Curve 1108 represents Vgs, which is given by the difference between line 1102 and curve 1104. Thus, as Vs increases, Vgs decreases. Note that for any power, Vgs is below Vth, which indicates that the MOSFET is in the weak inversion region. Also note that as the power increases, Vgs decreases, which provides some room for an AC signal at the gate of the MOSFET due to the input signal being coupled to the gate. However, even with the input signal being coupled to the gate of the MOSFET, the MOSFET can still be operated in the weak inversion region.

[00122] There are numerous possible applications for embodiments of a signal strength detector. One embodiment includes an apparatus that adjusts the sensitivity of an RF receiver based on a detected power level of an RF signal received by the

apparatus. The apparatus could be a wireless communication device, such as a cellular telephone, but is not limited thereto. FIG. 12 depicts a flowchart of one embodiment of a process 1200 of adjusting the sensitivity of an RF receiver based on a detected power level of an RF signal received by the RF receiver. The process 1200 may be implemented in a UE 110, but is not limited thereto.

[00123] Step 1202 includes receiving an RF signal at a wireless communication device (e.g., UE 110). The received RF signal may be a wireless RF signal. With reference to FIG. 2, antenna 210 may be used to access a wireless RF signal, which is processed by receiver 204.

[00124] Step 1204 includes sampling the RF signal and converting the RF signal to a voltage signal. The strength of the voltage signal has a magnitude that is proportional to the power of the wireless RF signal. For purposes of comparing the strength of the voltage signal to the power of the RF signal, the voltage signal may be associated with a resistance. Therefore, there will be a power associated with the voltage signal ($P = V^2 / R$). In one embodiment, a directional coupler is used to sample the RF signal. The directional coupler may also convert the RF signal to a voltage signal. Thus, process 1200 describes a technique in which the power of the wireless RF signal is not measured directly. Instead, the strength of the voltage signal is measured, wherein the power of the wireless RF signal may be determined from the strength of the voltage signal.

[00125] Step 1206 includes providing the voltage signal to an input of an RF power detector. For example, the voltage signal may be the input signal to apparatus 400 or apparatus 500. For example, the voltage signal (V_sig+, V_sig-) may be input to signal power detector 600 or signal strength detector 700.

[00126] Step 1208 includes detecting the strength of the voltage signal. Because the voltage signal is proportional to the power of the wireless RF signal, step 1208 indirectly determines the power of the wireless RF signal. As has been discussed above, the voltage at the differential output (420, 422) may be indicative of the strength of the input signal. Step 1208 may be based on the voltage at the differential output (420, 422). This voltage (e.g., DC voltage) may be used to determine a strength (e.g.,

voltage or power) of the input signal (e.g., V_sig+, V_sig-). In some embodiments, the strength of V_sig+, V_sig- is used to determine a power level of a wireless RF signal received by the wireless communication device.

[00127] Step 1210 includes determining whether to adjust a sensitivity of the RF receiver 204. This is based on the detected strength of the voltage signal. Step 1210 may include a determination of whether the strength is outside of a window. The window may correspond to a range of power levels for the wireless RF signal that are acceptable. If the sensitivity is to adjusted, then control passes to step 1212. Step 1212 includes a adjusting a sensitivity of an RF receiver 204. After adjusting the sensitivity, the process 1200 may repeat such that adjustments may be made on an on-going basis. In the event that it is determined in step 1210 to not make any adjustments, the process 1200 may repeat such that adjustments may be made in the event that the RF signal strength changes.

[00128] One embodiment includes an apparatus that adjusts the gain of an RF transmitter based on a detected power level of an RF signal transmitted by the apparatus. The apparatus could be a wireless communication device, such as a cellular telephone, but is not limited thereto. FIG. 13 depicts a flowchart of one embodiment of a process 1300 of adjusting the gain of an RF transmitter based on a detected power level of an RF signal transmitted by the RF transmitter. The process 1300 may be implemented in a UE 110, but is not limited thereto.

[00129] Step 1302 includes accessing an RF signal that is transmitted by a wireless communication device (e.g., UE 110). With reference to FIG. 2, transmitter 202 may be used to generate an RF signal, which is then transmitted by the antenna 210. The RF signal may be accessed prior to wireless transmission. For example, a directional coupler may be used to sample the RF signal prior to wireless transmission by antenna 210.

[00130] Step 1304 includes converting the accessed RF signal to a voltage signal. The voltage signal has a magnitude that is proportional to the power of the transmitted wireless RF signal. Thus, process 1300 describes a technique in which the power of

the wireless RF signal is not measured directly. Instead, the strength of the voltage signal is measured.

[00131] Step 1306 includes providing the voltage signal to an input of an RF power detector. The voltage signal may be input signal to apparatus 400, apparatus 500, signal power detector 600, or signal strength detector 700.

[00132] Step 1308 includes detecting the strength of the voltage signal. Step 1308 may indirectly determine the power of the transmitted wireless RF signal. As has been discussed above, the voltage at the differential output (420, 422) may be indicative of the strength of the input signal.

[00133] Step 1310 includes determining whether to adjust a gain of the RF transmitter 202. This is based on the detected strength of the voltage signal. Step 1308 may include a determination of whether the detected strength of the voltage signal is outside of a window that corresponds to an acceptable range of power for the transmitted RF signal. The window refers to a range of power levels for the transmitted RF signal that are acceptable. For example, there may be regulations that limit the power level of a transmitted RF signal. On the other hand, the transmitted RF signal should be strong enough to be adequately received by the target of the RF transmission. In effect, the gain of the RF transmitter may thus be adjusted based on the power of the transmitted RF signal.

[00134] If the gain is to adjusted, then control passes to step 1312. Step 1312includes adjusting a gain of an RF transmitter 202. After adjusting the gain, the process 1300 may repeat, such that adjustments may be made on an on-going basis. In the event that it is determined in step 1310 to not make any adjustments, the process 1300 may repeat such that adjustments may be made in the event that the transmitted RF signal strength changes. For example, operating conditions such as temperature may impact the gain of the RF transmitter. Also, in some cases the window in step 1310 could change. For example, it may be desirable to increase the gain to transmit a stronger RF signal in the event that the target is having trouble receiving the RF signal.

[00135] The technology described herein can be implemented using hardware, software, or a combination of both hardware and software. The software used is stored on one or more of the processor readable storage devices described above to program one or more of the processors to perform the functions described herein. The processor readable storage devices can include computer readable media such as volatile and non-volatile media, removable and non-removable media. By way of example, and not limitation, computer readable media may comprise computer readable storage media and communication media. Computer readable storage media may be implemented in any method or technology for storage of information such as computer readable instructions, data structures, program modules or other data. Examples of computer readable storage media include RAM, ROM, EEPROM, flash memory or other memory technology, CD-ROM, digital versatile disks (DVD) or other optical disk storage, magnetic cassettes, magnetic tape, magnetic disk storage or other magnetic storage devices, or any other medium which can be used to store the desired information and which can be accessed by a computer. A computer readable medium or media does (do) not include propagated, modulated or transitory signals.

[00136] Communication media typically embodies computer readable instructions, data structures, program modules or other data in a propagated, modulated or transitory data signal such as a carrier wave or other transport mechanism and includes any information delivery media. The term “modulated data signal” means a signal that has one or more of its characteristics set or changed in such a manner as to encode information in the signal. By way of example, and not limitation, communication media includes wired media such as a wired network or direct-wired connection, and wireless media such as RF and other wireless media. Combinations of any of the above are also included within the scope of computer readable media.

[00137] In alternative embodiments, some or all of the software can be replaced by dedicated hardware logic components. For example, and without limitation, illustrative types of hardware logic components that can be used include Field-programmable Gate Arrays (FPGAs), Application-specific Integrated Circuits (ASICs), Application-specific Standard Products (ASSPs), System-on-a-chip systems (SOCs), Complex

Programmable Logic Devices (CPLDs), special purpose computers, etc. In one embodiment, software (stored on a storage device) implementing one or more embodiments is used to program one or more processors. The one or more processors can be in communication with one or more computer readable media/ storage devices, peripherals and/or communication interfaces.

[00138] It is understood that the present subject matter may be embodied in many different forms and should not be construed as being limited to the embodiments set forth herein. Rather, these embodiments are provided so that this subject matter will be thorough and complete and will fully convey the disclosure to those skilled in the art. Indeed, the subject matter is intended to cover alternatives, modifications and equivalents of these embodiments, which are included within the scope and spirit of the subject matter as defined by the appended claims. Furthermore, in the following detailed description of the present subject matter, numerous specific details are set forth in order to provide a thorough understanding of the present subject matter. However, it will be clear to those of ordinary skill in the art that the present subject matter may be practiced without such specific details.

[00139] Aspects of the present disclosure are described herein with reference to flowchart illustrations and/or block diagrams of methods, apparatuses (systems) and computer program products according to embodiments of the disclosure. It will be understood that each block of the flowchart illustrations and/or block diagrams, and combinations of blocks in the flowchart illustrations and/or block diagrams, can be implemented by computer program instructions. These computer program instructions may be provided to a processor of a general-purpose computer, special-purpose computer, or other programmable data processing apparatus to produce a machine, such that the instructions, which execute via the processor of the computer or other programmable instruction execution apparatus, create a mechanism for implementing the functions/acts specified in the flowchart and/or block diagram block or blocks.

[00140] The description of the present disclosure has been presented for purposes of illustration and description, but is not intended to be exhaustive or limited to the disclosure in the form disclosed. Many modifications and variations will be apparent

to those of ordinary skill in the art without departing from the scope and spirit of the disclosure. The aspects of the disclosure herein were chosen and described in order to best explain the principles of the disclosure and the practical application, and to enable others of ordinary skill in the art to understand the disclosure with various modifications as are suited to the particular use contemplated.

[00141] For purposes of this document, each process associated with the disclosed technology may be performed continuously and by one or more computing devices. Each step in a process may be performed by the same or different computing devices as those used in other steps, and each step need not necessarily be performed by a single computing device.

[00142] Although the subject matter has been described in language specific to structural features and/or methodological acts, it is to be understood that the subject matter defined in the appended claims is not necessarily limited to the specific features or acts described above. Rather, the specific features and acts described above are disclosed as example forms of implementing the claims.

CLAIMS

What is claimed is:

1. An apparatus for detecting signal strength, the apparatus comprising:

a differential sensor stage having an input and an output;

a differential reference stage having an input and an output;

a capacitor stage configured to couple an input signal to the input of the differential sensor stage;

a biasing circuit configured to bias the differential sensor stage and the differential reference stage; and

a differential output between the output of the differential sensor stage and the output of the differential reference stage, the differential output configured to provide a signal indicative of strength of the input signal.

2. The apparatus of claim 1, wherein:

the biasing circuit is configured to bias the differential sensor stage and the differential reference stage in a weak inversion region.

3. The apparatus of claim 1 or 2, wherein:

the biasing circuit is configured to apply substantially the same bias conditions to the differential sensor stage and to the differential reference stage.

4. The apparatus of claim 2 or 3, wherein the capacitor stage is configured to keep the differential sensor stage operating in the weak inversion region.

5. The apparatus of claim 4, wherein the capacitor stage is configured to keep the input signal at the input of the differential sensor stage within a target range to keep the differential sensor stage operating in the weak inversion region.

6. The apparatus of any of claims 1 to 5, wherein:

the capacitor stage comprises an H-type capacitor bridge.

7. The apparatus of claim 6, wherein the H-type capacitor bridge comprises:

a first capacitor having a first terminal and a second terminal;

a second capacitor having a first terminal and a second terminal, the first terminals of the first capacitor and the second capacitor configured to receive the input signal;

a third capacitor having a first terminal connected to the second terminal of the first capacitor, the third capacitor having a second terminal connected to a first terminal of the input of the differential sensor stage;

a fourth capacitor having a first terminal connected to the second terminal of the second capacitor, the fourth capacitor having a second terminal connected to a second terminal of the input of the differential sensor stage; and

a fifth capacitor having a first terminal connected to the second terminal of the first capacitor and to the first terminal of the third capacitor, the fifth capacitor having a second terminal connected to the second terminal of the second capacitor and to the first terminal of the fourth capacitor.

8. The apparatus of claim 7, wherein the first capacitor and the second capacitor have substantially the same capacitance.

9. The apparatus of claim 7 or 8, wherein the third capacitor and the fourth capacitor have substantially the same capacitance.

10. The apparatus of any of claims 1 to 9, wherein:

the differential sensor stage comprises a first transistor and a second transistor having a source follower configuration; and

the differential reference stage comprises a third transistor and a fourth transistor having a source follower configuration.

11. The apparatus of any of claims 1 to 10, wherein:

the differential sensor stage comprises a first MOSFET transistor and a second MOSFET transistor having a source follower configuration; and

the differential reference stage comprises a third MOSFET transistor and a fourth MOSFET transistor having a source follower configuration.

12. The apparatus of any of claims 1 to 11, wherein:

the differential sensor stage comprises a first loading block coupled to the output of the differential sensor stage; and

the differential reference stage comprises a second loading block coupled to the output of the differential reference stage.

13. The apparatus of claim 12, wherein:

the first loading block comprises a first resistor; and

the second loading block comprises a second resistor, wherein the first resistor and the second resistor have substantially the same resistance.

14. The apparatus of claim 12 or 13, wherein the second loading block is configured to provide temperature compensation for the circuit.

15. The apparatus of any of claims 12 to 14, wherein the second loading block is configured to keep the signal at the differential output within a target range independent of temperature.

16. The apparatus of any of claims 12 to 15, wherein the second loading block further comprises a proportional to absolute temperature (PTAT) current source in parallel with the second resistor.

17. The apparatus of any of claims 12 to 16, wherein the first loading block further comprises a capacitor in parallel with the first resistor.

18. The apparatus of any of claims 11 to 17, wherein:

the first loading block comprises a passive loading block; and

the second loading block comprises an active loading block.

19. The apparatus of claim 12 or 13, wherein the first loading block is configured to provide temperature compensation.

20. The apparatus of claim 12, 13 or 19, wherein the first loading block is configured to keep the signal at the differential output within a target range independent of temperature.

21. The apparatus of claim 12, 13, 19, or 20, wherein the first loading block further comprises a complimentary to absolute temperature (CTAT) current source in parallel with the first resistor.

22. The apparatus of any of claims 12, 13, or 19 to 21, wherein:
the first loading block comprises an active loading block; and
the second loading block comprises a passive loading block.

23. The apparatus of any of claims 1 to 22, wherein the input signal is based on a radio frequency (RF) signal.

24. The apparatus of claim 23, further comprising:
an RF transmitter configured to generate the RF signal; and
an antenna coupled to the RF transmitter and configured to transmit the RF signal, wherein the strength of the input signal is proportional to power of the transmitted RF signal.

25. The apparatus of claim 23, further comprising:
an RF receiver configured to generate the RF signal; and
an antenna coupled to the RF receiver and configured to receive the RF signal, wherein the strength of the input signal is proportional to power of the received RF signal.

26. The apparatus of any of claims 1 to 25, wherein the strength comprises a peak voltage of the input signal.

27. The apparatus of any of claims 1 to 26, wherein the strength corresponds to a peak power of the input signal.

28. A method for detecting a signal strength, the method comprising:

biasing a differential sensor stage having an input and an output;

biasing a differential reference stage having an input and an output;

coupling an input signal to the input of the differential sensor stage using a capacitor stage; and

providing a signal indicative of strength of the input signal at a differential output between the output of the differential sensor stage and the output of the differential reference stage.

29. The method of claim 28, wherein biasing the differential sensor stage and biasing the differential reference stage comprises:

biasing the differential sensor stage in a weak inversion region; and

biasing the differential reference stage in a weak inversion region.

30. The method of claim 28 or 29, wherein biasing the differential sensor stage and biasing the differential reference stage comprises:

applying substantially the same bias conditions to the differential sensor stage and to the differential reference stage.

31. The method of any of claims 28 to 30, wherein:

biasing the differential sensor stage comprises biasing a first MOSFET transistor and a second MOSFET transistor having a source follower configuration; and

biasing the differential reference stage comprises biasing a third MOSFET transistor and a fourth MOSFET transistor having a source follower configuration.

32. The method of any of claims 29 to 31, further comprising:

keeping the differential sensor stage in the weak inversion region by using the capacitor stage to couple the input signal to the input of the differential sensor stage.

33. The method of any of claims 29 to 32, further comprising:

keeping the input signal at the input of the differential sensor stage within a target range to keep the differential sensor stage operating in the weak inversion region.

34. The method of any of claims 28 to 33, wherein coupling the input signal to the input of the differential sensor stage using the capacitor stage comprises:

coupling the input signal to the input of the differential sensor stage using an H-type capacitor bridge in the capacitor stage.

35. The method of any of claims 28 to 34, wherein:

biasing the differential sensor stage further comprises grounding a first loading block coupled to the output of the differential sensor stage; and

biasing the differential reference stage further comprises grounding a second loading block coupled to the output of the differential reference stage.

36. The method of claim 35, further comprising:

providing temperature compensation using the first loading block.

37. The method of claim 35 or 36, further comprising:

providing temperature compensation using a proportional to absolute temperature (PTAT) current source in the first loading block.

38. The method of any of claims 36 or 37, wherein providing temperature compensation using the first loading block comprises:

keeping the signal at the differential output within a target range independent of temperature.

39. The method of claim 35, further comprising:

providing temperature compensation using the second loading block.

40. The method of claim 35, further comprising:

providing temperature compensation using a complimentary to absolute temperature (CTAT) current source in the second loading block.

41. The method of any of claims 39 or 40, wherein providing temperature compensation using the second loading block comprises:

keeping the signal at the differential output within a target range independent of temperature.

42. The method of any of claims 28 to 41, wherein the input signal is based on a radio frequency (RF) signal.

43. The method of claim 42, further comprising:

adjusting a radio transceiver responsive to the signal indicative of the strength of the input signal being outside of a threshold.

44. A wireless communication device, comprising:

a transceiver configured to receive and to transmit radio frequency (RF) signals;

a differential sensor stage having an input and an output;

a differential reference stage having an input and an output;

a capacitor stage coupled to the transceiver and configured to couple a voltage signal based on an RF signal to the input of the differential sensor stage;

a biasing circuit configured to bias the differential sensor stage and the differential reference stage; and

a differential output between the output of the differential sensor stage and the output of the differential reference stage, the differential output configured to provide a signal indicative of power of the RF signal.

45. The wireless communication device of claim 44, wherein:

the biasing circuit is configured to bias the differential sensor stage and the differential reference stage in a weak inversion region.

46. The wireless communication device of claim 44 or 45, wherein:

the biasing circuit is configured to apply substantially the same bias conditions to the differential sensor stage and to the differential reference stage.

47. The wireless communication device of claim 45 or 46, wherein the capacitor stage is configured to keep the differential sensor stage operating in the weak inversion region.

48. The wireless communication device of claim 47, wherein the capacitor stage is configured to keep the voltage signal at the input of the differential sensor stage within a target range to keep the differential sensor stage operating in the weak inversion region.

49. The wireless communication device of any of claims 44 to 48, wherein:

the capacitor stage comprises an H-type capacitor bridge.

50. The wireless communication device of claim 49, wherein the H-type capacitor bridge comprises:

a first capacitor having a first terminal and a second terminal;

a second capacitor having a first terminal and a second terminal, the first terminals of the first capacitor and the second capacitor configured to receive the voltage signal;

a third capacitor having a first terminal connected to the second terminal of the first capacitor, the third capacitor having a second terminal connected to a first terminal of the input of the differential sensor stage;

a fourth capacitor having a first terminal connected to the second terminal of the second capacitor, the fourth capacitor having a second terminal connected to a

second terminal of the input of the differential sensor stage; and

a fifth capacitor having a first terminal connected to the second terminal of the first capacitor and to the first terminal of the third capacitor, the fifth capacitor having a second terminal connected to the second terminal of the second capacitor and to the first terminal of the fourth capacitor.

51. The wireless communication device of claim 50, wherein the first capacitor and the second capacitor have substantially the same capacitance.

52. The wireless communication device of claim 50 or 51, wherein the third capacitor and the fourth capacitor have substantially the same capacitance.

53. The wireless communication device of any of claims 44 to 52, wherein:

the differential sensor stage comprises a first transistor and a second transistor having a source follower configuration; and

the differential reference stage comprises a third transistor and a fourth transistor having a source follower configuration.

54. The wireless communication device of any of claims 44 to 53, wherein:

the differential sensor stage comprises a first MOSFET transistor and a second MOSFET transistor having a source follower configuration; and

the differential reference stage comprises a third MOSFET transistor and a fourth MOSFET transistor having a source follower configuration.

55. The wireless communication device of any of claims 44 to 54, wherein:

the differential sensor stage comprises a first loading block coupled to the output of the differential sensor stage; and

the differential reference stage comprises a second loading block coupled to the output of the differential reference stage.

56. The wireless communication device of claim 55, wherein:

the first loading block comprises a first resistor; and

the second loading block comprises a second resistor, wherein the first resistor and the second resistor have substantially the same resistance.

57. The wireless communication device of claim 55 or 56, wherein the second loading block is configured to provide temperature compensation for the circuit.

58. The wireless communication device of any of claims 55 to 57, wherein the second loading block is configured to keep the signal at the differential output within a target range independent of temperature.

59. The wireless communication device of any of claims 55 to 58, wherein the second loading block further comprises a proportional to absolute temperature (PTAT) current source in parallel with the second resistor.

60. The wireless communication device of any of claims 55 to 59, wherein the first loading block further comprises a capacitor in parallel with the first resistor.

61. The wireless communication device of any of claims 55 to 60, wherein:
the first loading block comprises a passive loading block; and
the second loading block comprises an active loading block.

62. The wireless communication device of claim 55 or 56, wherein the first loading block is configured to provide temperature compensation.

63. The wireless communication device of any of claims 55, 56, or 62, wherein the first loading block is configured to keep the voltage signal at the differential output within a target range independent of temperature.

64. The wireless communication device of claim 55, 56, 63, or 63, wherein the first loading block further comprises a complimentary to absolute temperature (CTAT) current source in parallel with the first resistor.

65. The wireless communication device of any of claims 55, 56, or 62 to 64, wherein:

the first loading block comprises an active loading block; and

the second loading block comprises a passive loading block.

66. The wireless communication device of any of claims 44 to 65, wherein the RF signal is transmitted by a transmitter in the transceiver, and further comprising:

adjust a gain of the transmitter responsive to the power of the RF signal being outside of a window.

67. The wireless communication device of any of claims 44 to 65, wherein the RF signal is received by a receiver in the transceiver, and further comprising:

adjust a sensitivity of the receiver responsive to the power of the RF signal being outside of a window.

68. The wireless communication device of any of claims 44 to 67, wherein the power comprises a peak power level of the RF signal.

69. The wireless communication device of any of claims 44 to 68, wherein the signal indicative of the power of the RF signal comprises a DC voltage at the differential output.

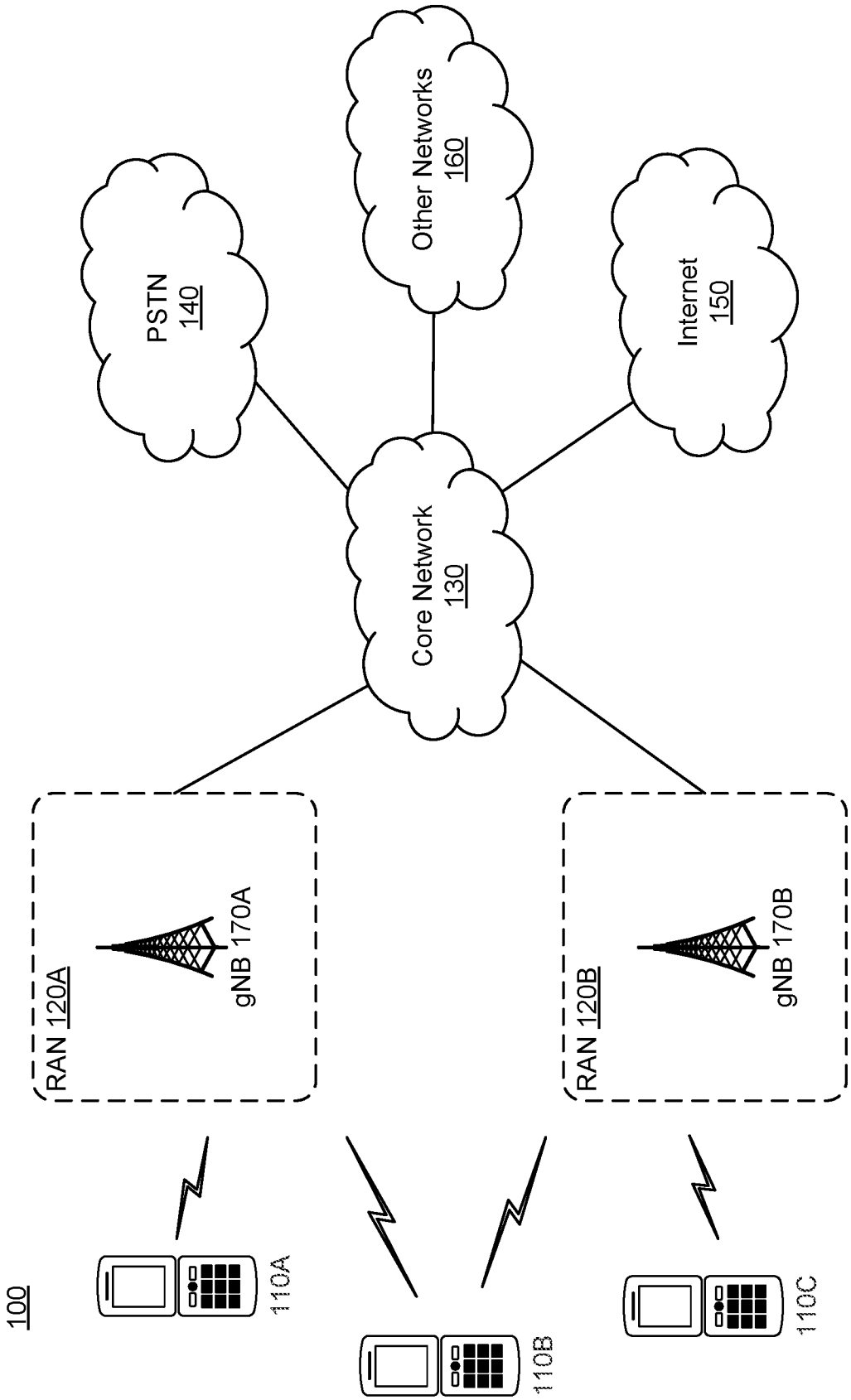
100
110A
110B
110C
RAN 120A
gNB 170A
RAN 120B
gNB 170B
Core Network 130
PSTN 140
Other Networks 160
Internet 150

FIG. 1

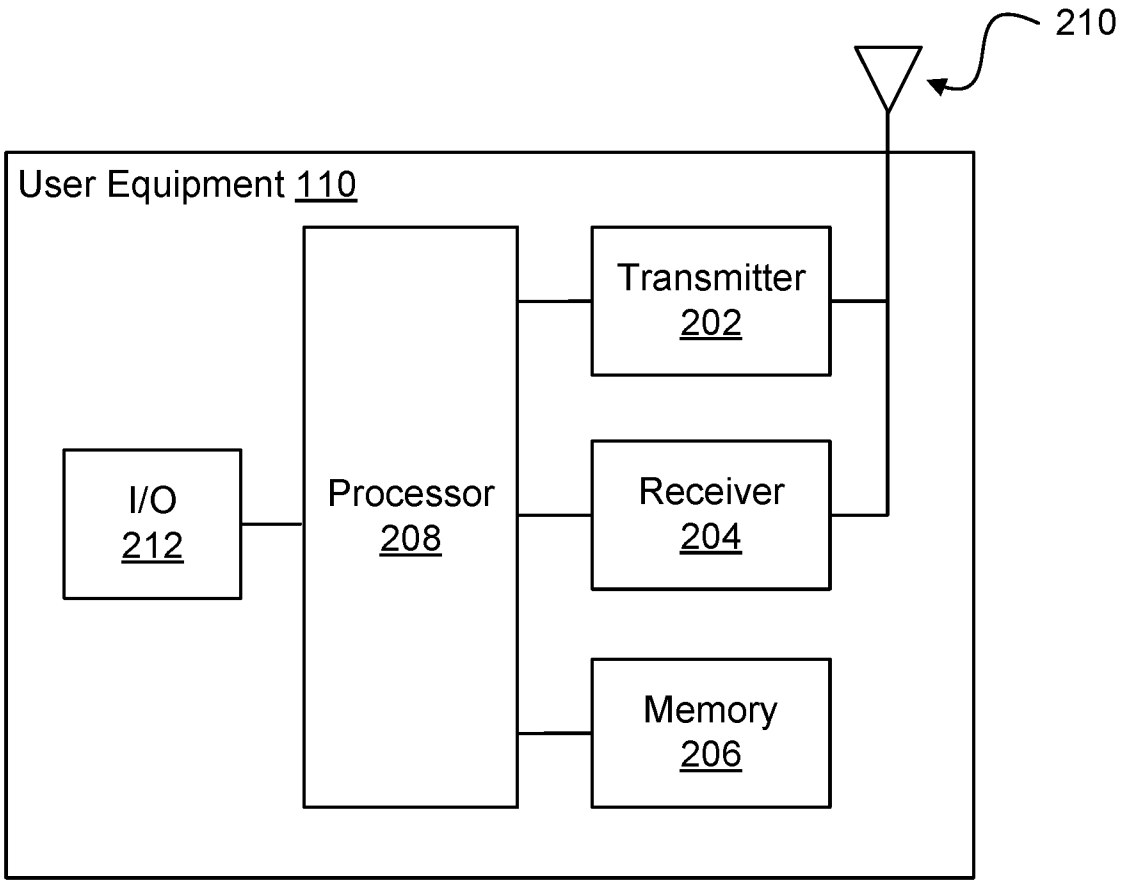
210
User Equipment 110
Transmitter 202
Processor 208
I/O 212
Receiver 204
Memory 206

FIG. 2

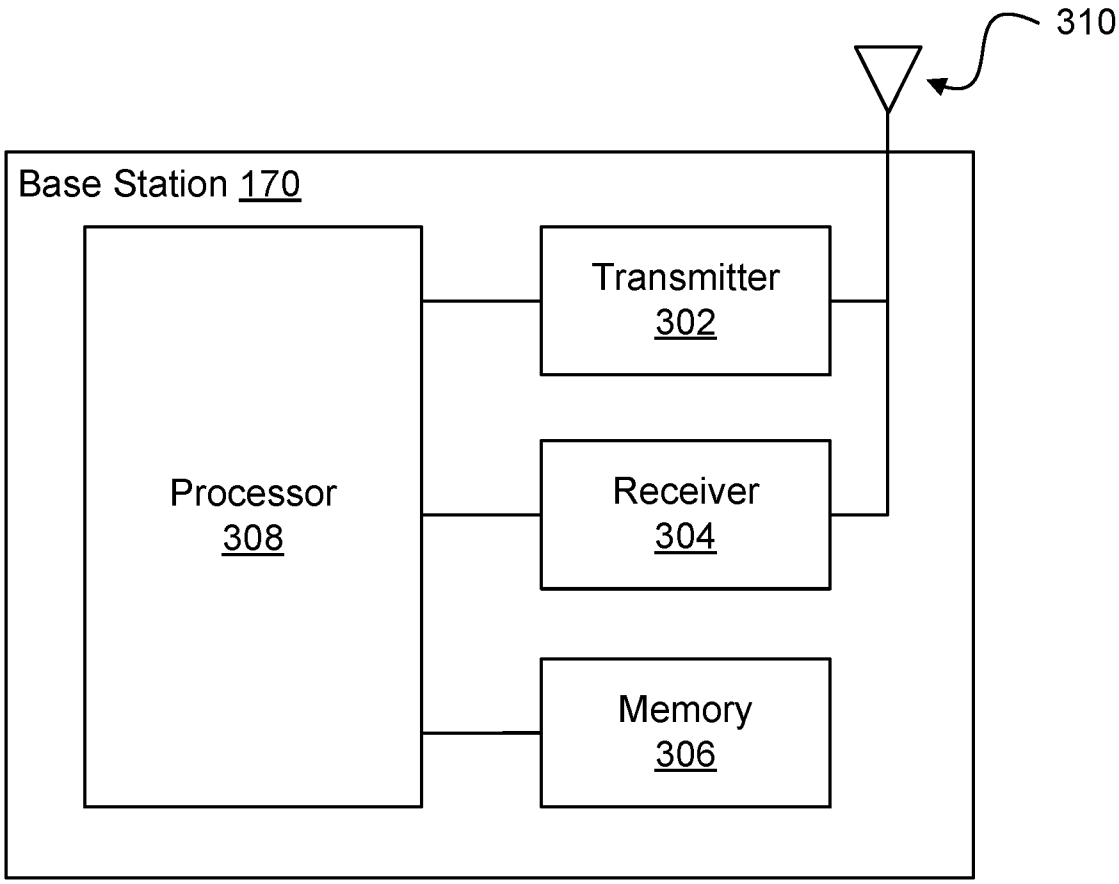
310
Base Station 170
Processor
308
Transmitter
302
Receiver
304
Memory
306

FIG. 3

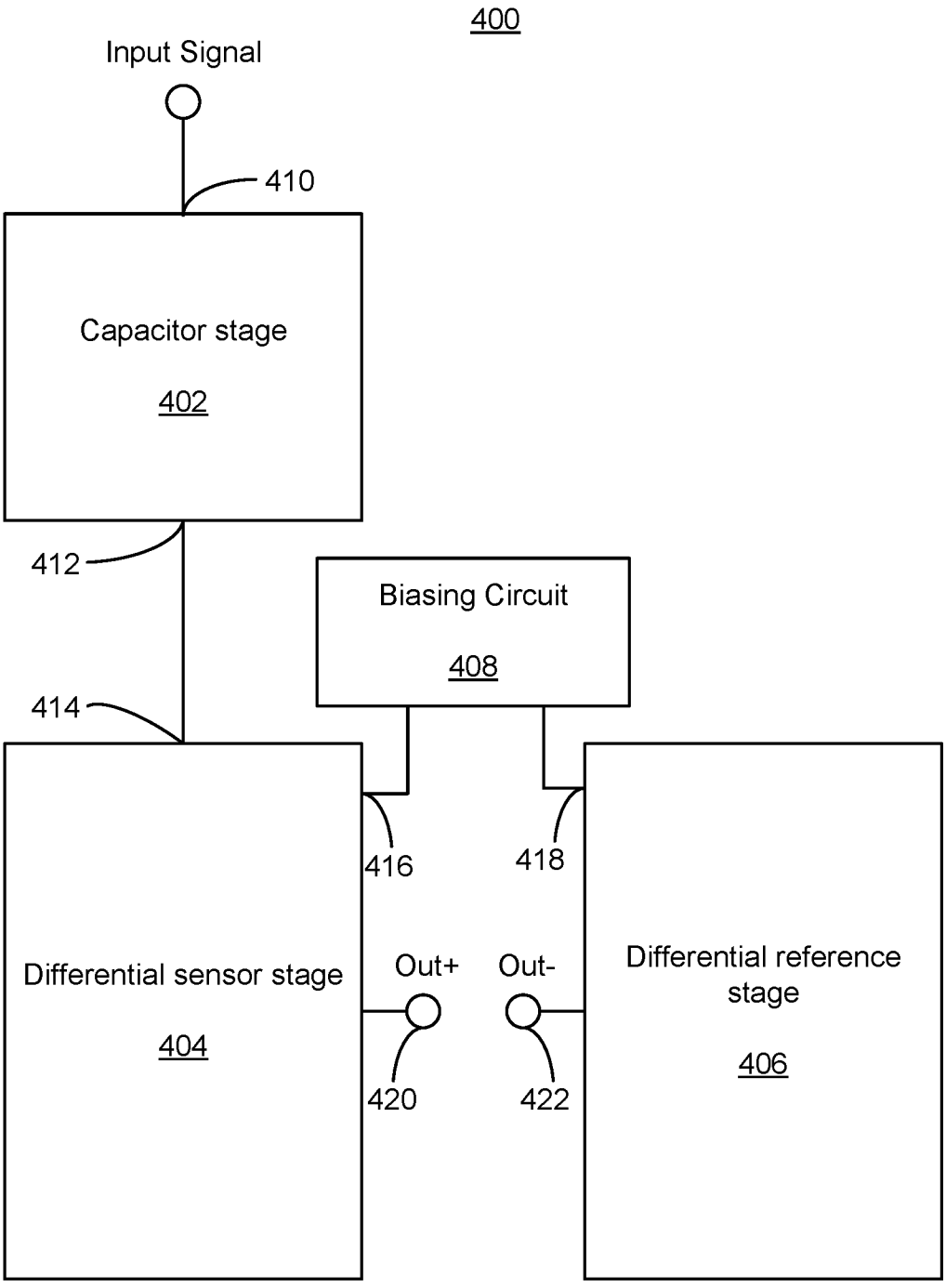
400
Input Signal
410
Capacitor stage
402
412
Biasing Circuit
408
414
416
418
Differential sensor stage
404
Out+
Out-
Differential reference stage
406
420
422

FIG. 4

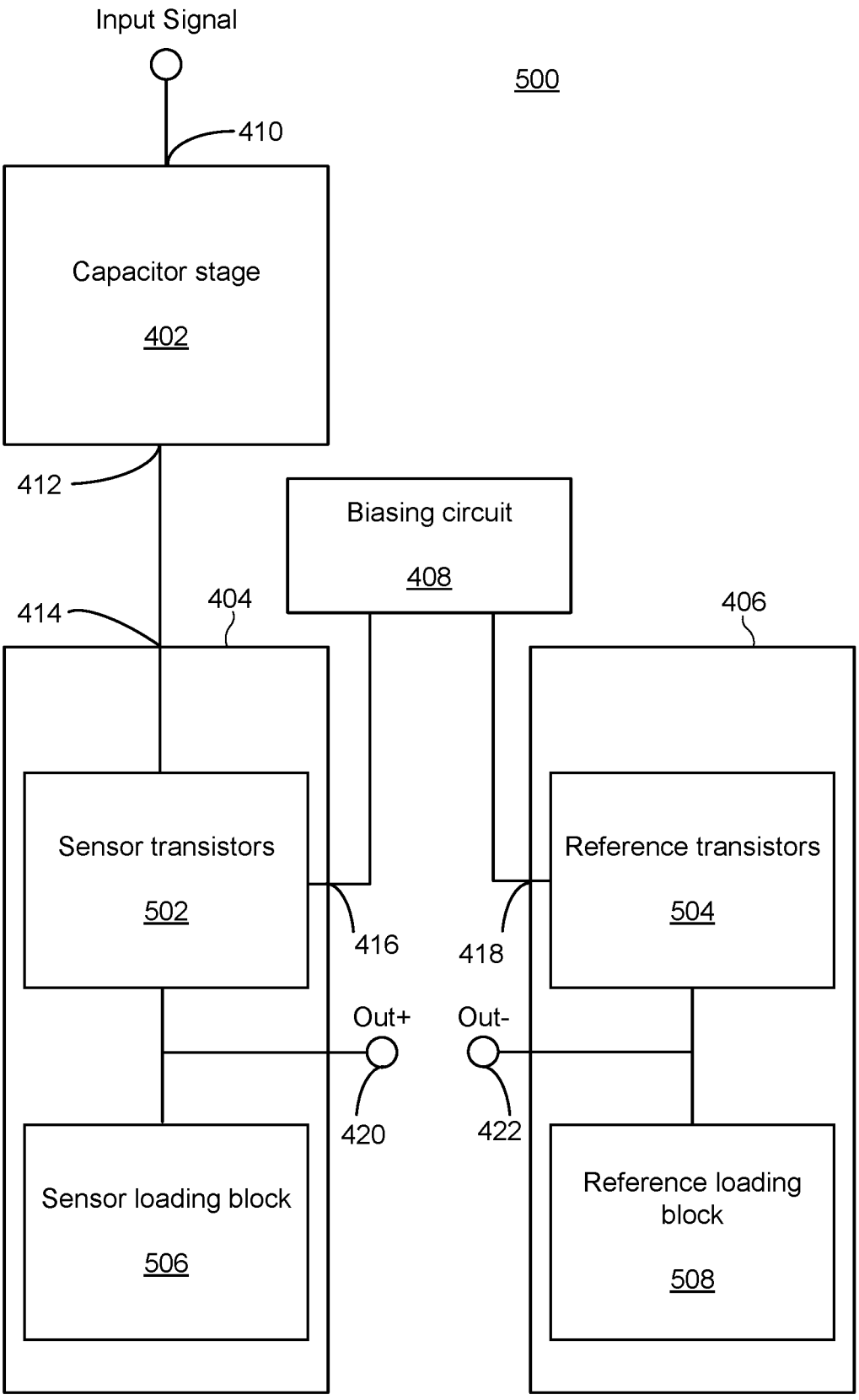
Input Signal
500
410
Capacitor stage
402
412
Biasing circuit
408
414
404
406
Sensor transistors
502
Reference transistors
504
416
418
Out+
Out-
420
422
Sensor loading block
506
Reference loading block
508

FIG. 5

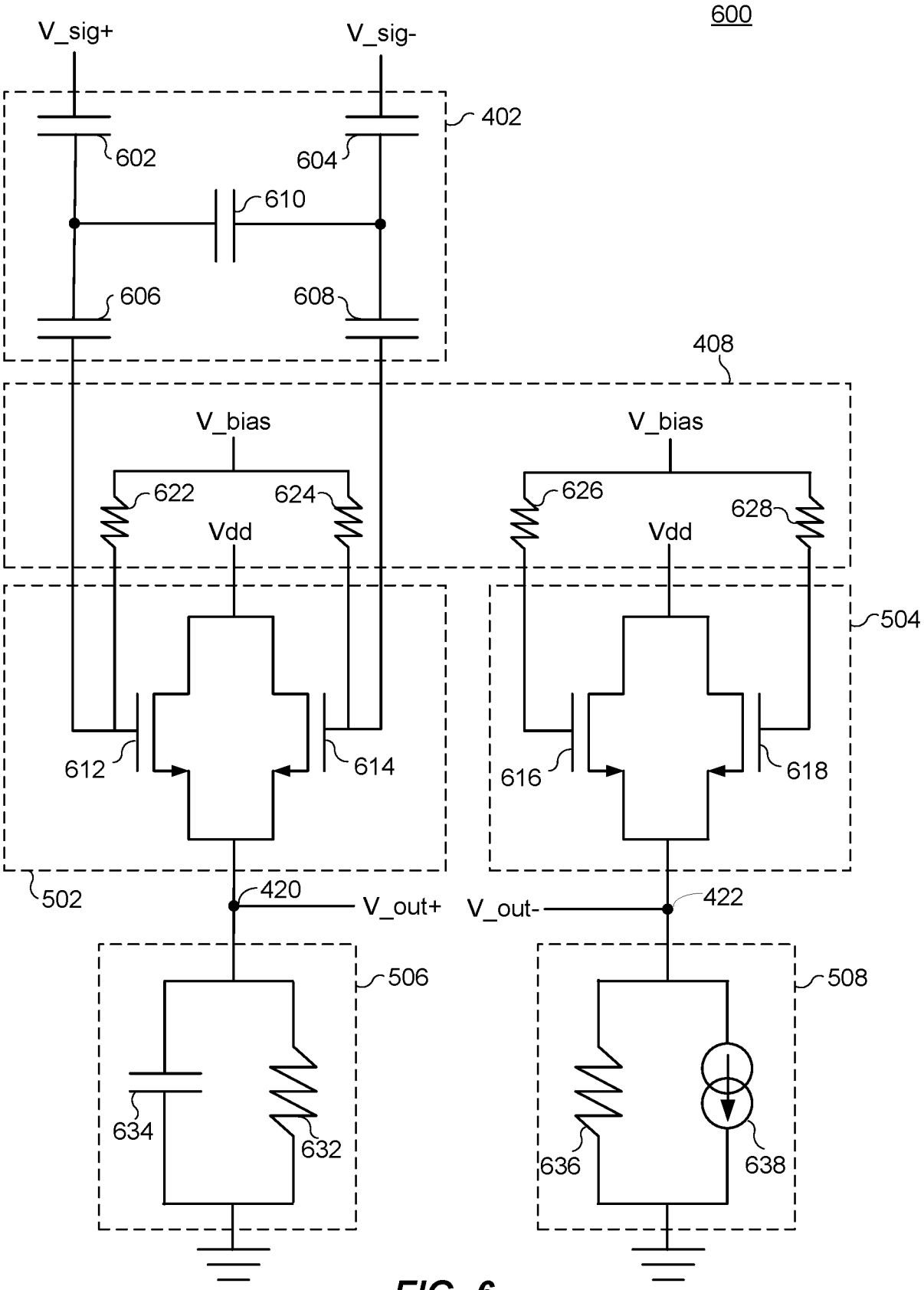
600
V_sig+
V_sig-
402
602
604
610
606
608
408
V_bias
V_bias
622
624
626
628
Vdd
Vdd
504
612
614
616
618
502
420
V_out+
V_out-
422
506
508
634
632
636
638

FIG. 6

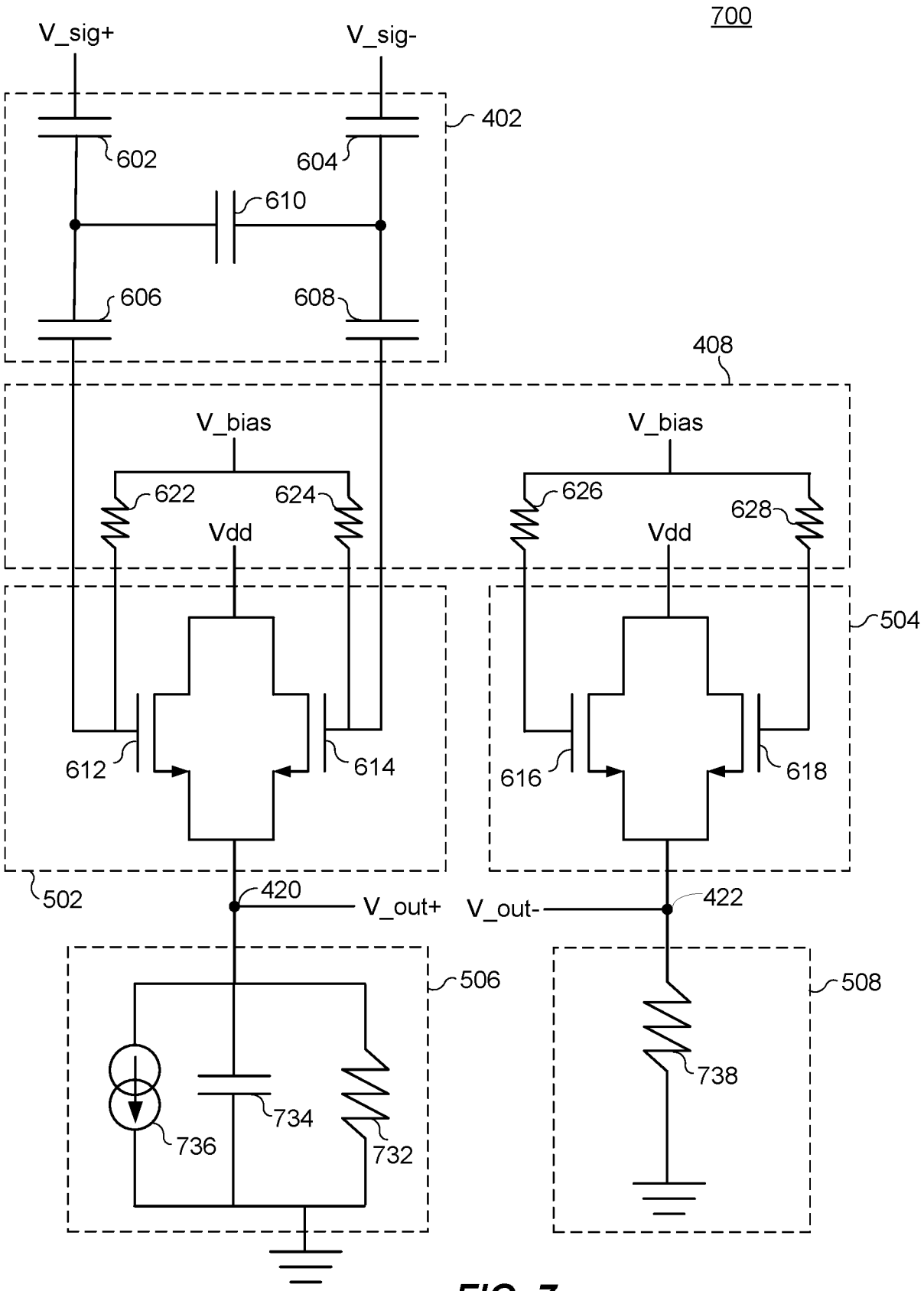
700
V_sig+
V_sig-
402
602
604
610
606
608
408
V_bias
V_bias
622
624
626
628
Vdd
Vdd
504
612
614
616
618
502
420
V_out+
V_out-
422
506
508
738
734
736
732

FIG. 7

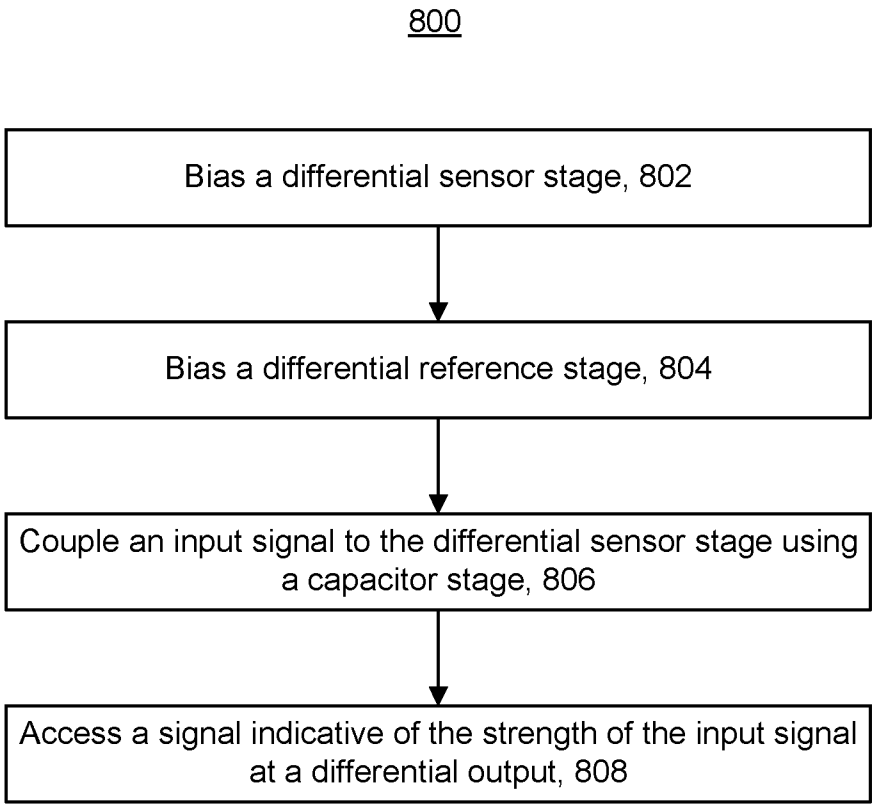
800
Bias a differential sensor stage, 802
Bias a differential reference stage, 804
Couple an input signal to the differential sensor stage using a capacitor stage, 806
Access a signal indicative of the strength of the input signal at a differential output, 808

FIG. 8

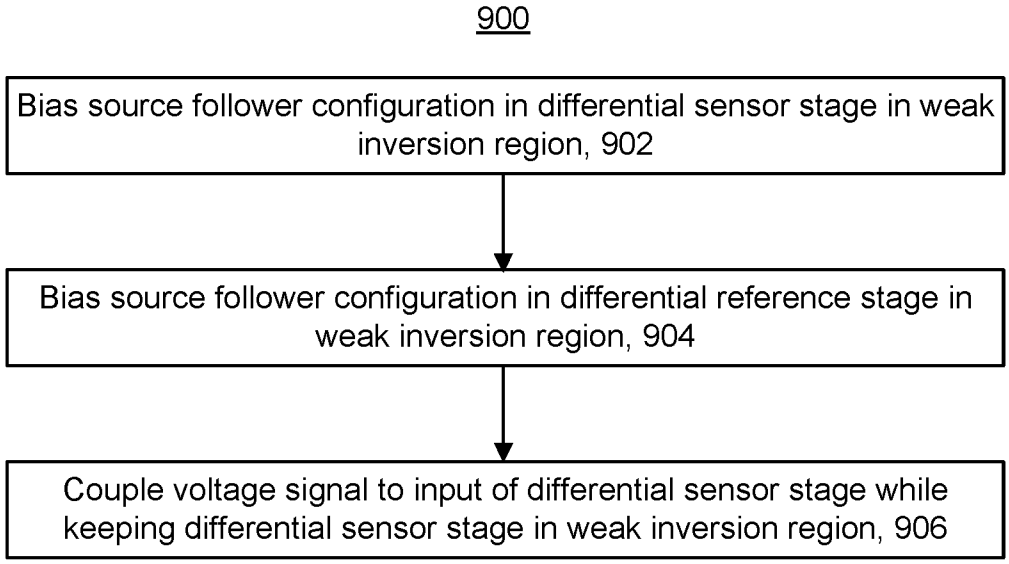
900
Bias source follower configuration in differential sensor stage in weak inversion region, 902
Bias source follower configuration in differential reference stage in weak inversion region, 904
Couple voltage signal to input of differential sensor stage while keeping differential sensor stage in weak inversion region, 906

FIG. 9

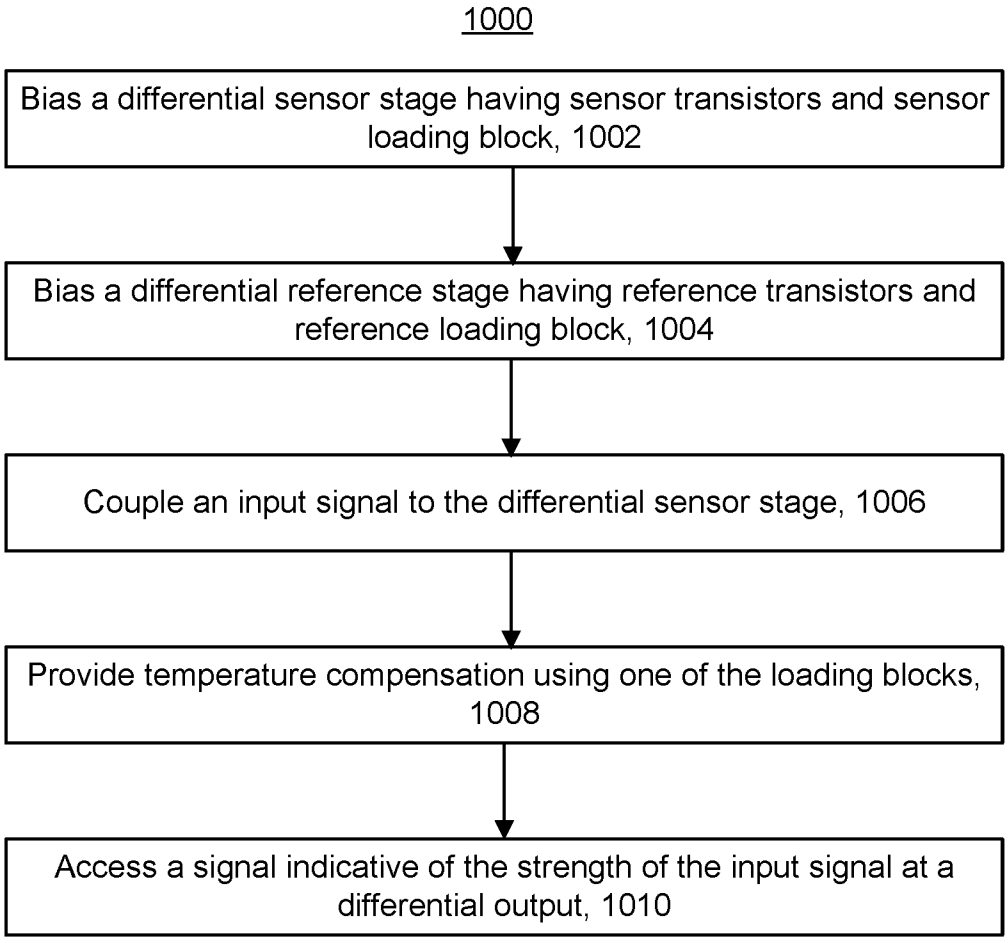
1000
Bias a differential sensor stage having sensor transistors and sensor loading block, 1002
Bias a differential reference stage having reference transistors and reference loading block, 1004
Couple an input signal to the differential sensor stage, 1006
Provide temperature compensation using one of the loading blocks, 1008
Access a signal indicative of the strength of the input signal at a differential output, 1010

FIG. 10

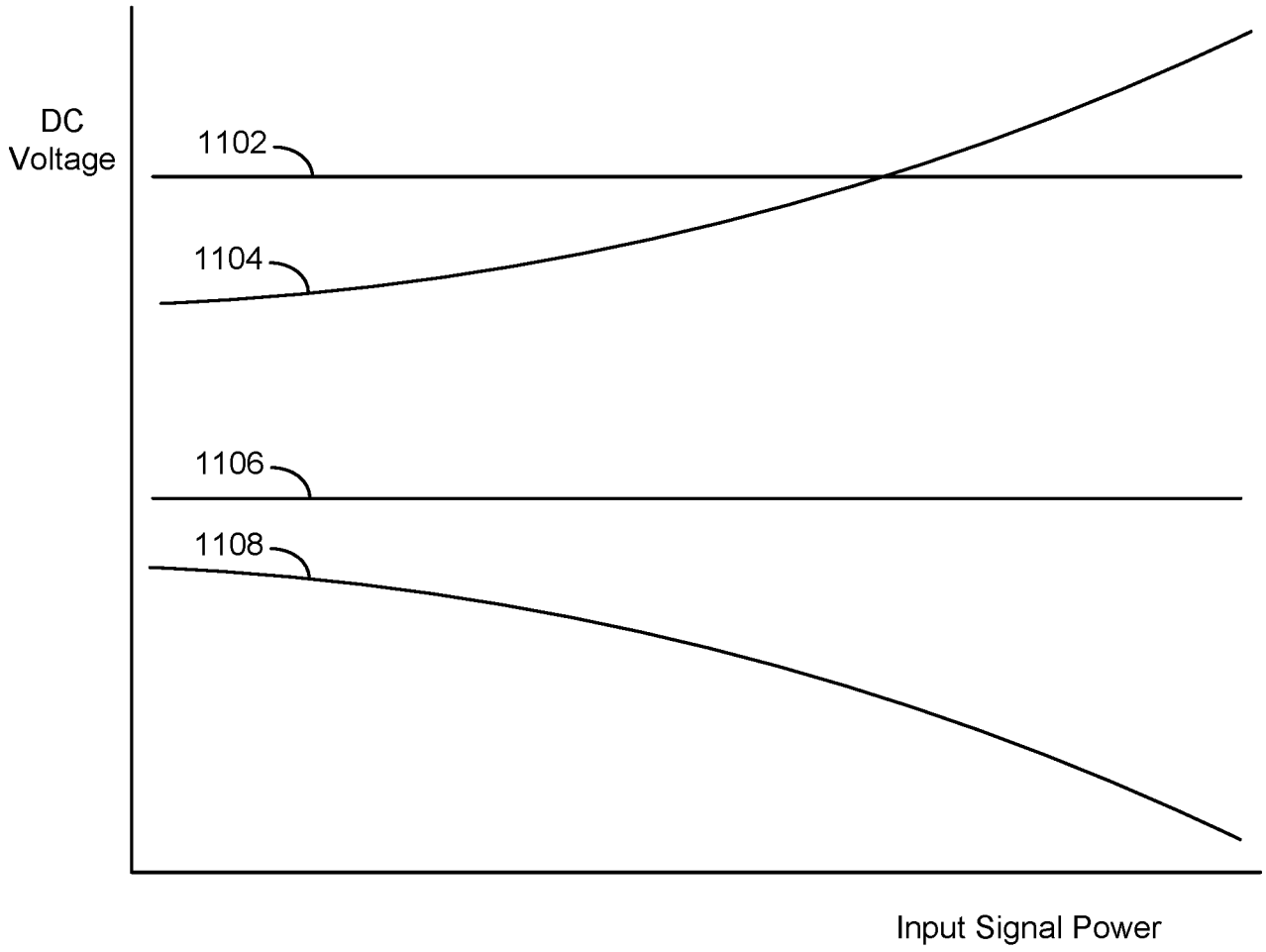

FIG. 11

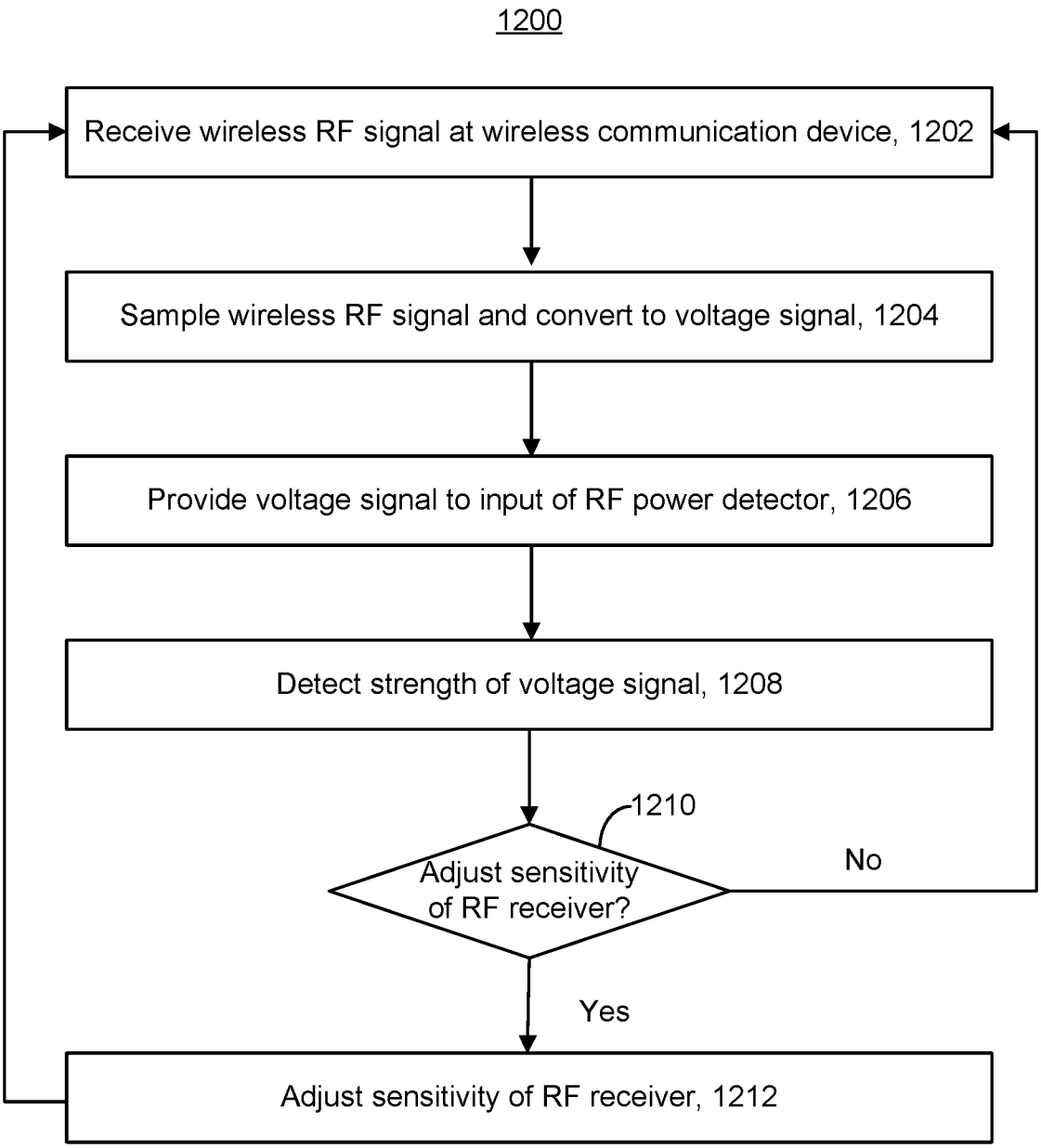
1200
Receive wireless RF signal at wireless communication device, 1202
Sample wireless RF signal and convert to voltage signal, 1204
Provide voltage signal to input of RF power detector, 1206
Detect strength of voltage signal, 1208
1210
Adjust sensitivity of RF receiver?
No
Yes
Adjust sensitivity of RF receiver, 1212

FIG. 12

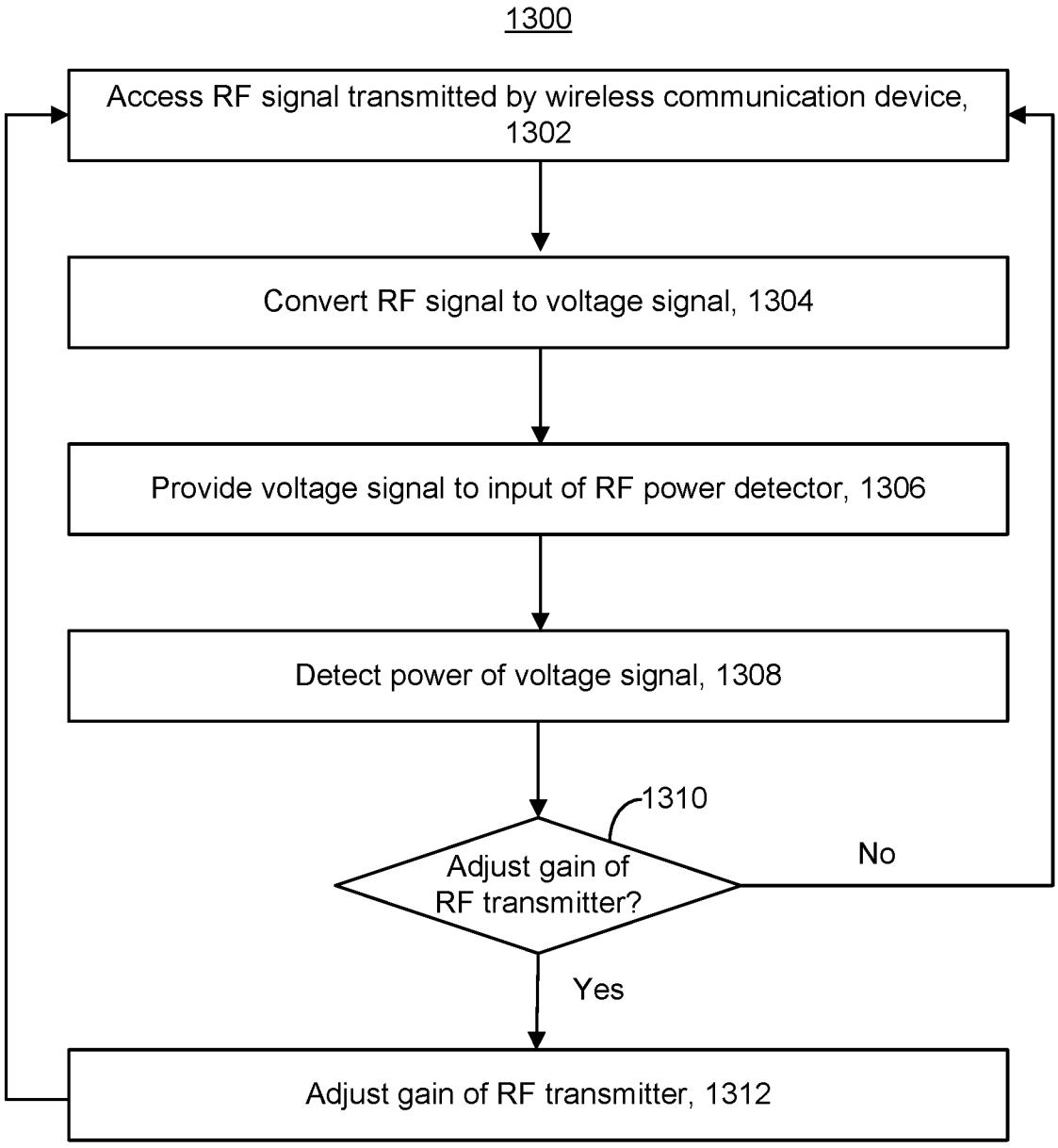
1300
Access RF signal transmitted by wireless communication device, 1302
Convert RF signal to voltage signal, 1304
Provide voltage signal to input of RF power detector, 1306
Detect power of voltage signal, 1308
1310
Adjust gain of RF transmitter?
No
Yes
Adjust gain of RF transmitter, 1312

FIG. 13