A structure. The structure includes a substrate. A first dielectric layer is on and in direct mechanical contact with the substrate. A first hard mask is on the first dielectric layer. A first and second trench is within the first dielectric layer and the first hard mask. The second trench is wider than the first trench. A first conformal liner is on sidewalls of the first and second trenches. The first conformal liner is in direct physical contact with the substrate, the first dielectric layer, and the first hard mask. A first conductive material that includes copper fills the first and second trenches. A planar surface of the first conductive material is coplanar with a top surface of the first conformal liner and a top surface of the first hard mask.
DAMASCENE FILAMENT WIRE STRUCTURE

This application is a Divisional of Ser. No. 10/906, 552, filed Feb. 24, 2005.

BACKGROUND OF THE INVENTION

1. Technical Field

The present invention relates generally to semiconductor devices, and more particularly, to a method of forming low capacitance back end of the line (BEOL) wiring, and the structure so formed.

2. Related Art

When forming CMOS, BiCMOS, SiGe, and other similar devices, it is desirable to minimize capacitance. Likewise, there is a continuing desire in the industry to reduce device size. Therefore, there is a need in the industry for a method of forming a semiconductor device that addresses these and other issues.

SUMMARY OF THE INVENTION

The present invention provides a method of forming a semiconductor device having a low wire capacitance and a high wire resistance, and the structure so formed, that solves the above-stated and other problems. The device comprises conductive wires having widths substantially smaller than the width of the printed and etched trench and/or via formed for the wire.

A first aspect of the invention provides a method of forming a semiconductor device, comprising: providing a substrate; depositing a first dielectric layer; depositing a hard mask on the first dielectric layer; forming an at least one first feature within the first dielectric layer and the hard mask; depositing a conformal dielectric liner over the hard mask and within the at least one feature, wherein the liner occupies more than at least 2% of a volume of the at least one feature; depositing a conductive material over the liner, and planarizing a surface of the device to remove excess conductive material.

A second aspect of the invention provides a method of forming a semiconductor device, comprising: providing a substrate; depositing a first dielectric layer; forming an at least one feature within the first dielectric layer; depositing a conformal dielectric liner over a surface of the device and within the at least one feature, wherein a thickness of the liner is at least approximately ½ a minimum width of the at least one feature; and metalizing the at least one feature.

A third aspect of the invention provides a semiconductor device, comprising: a substrate; a first dielectric layer on a surface of the substrate; a hard mask on the first dielectric layer; at least one first feature within the first dielectric layer and the hard mask; a conformal dielectric liner over the hard mask and within the at least one feature, wherein the liner occupies more than at least 2% of a volume of the at least one feature; and a conductive material within the at least one feature.

A fourth aspect of the present invention provides a method of forming a structure, and the structure so formed, comprising a dual damascene structure wherein a via of the dual damascene features may be formed having a width equal to, or up to ½ less than, a minimum trench width, and wherein a thickness of a conformal dielectric liner within the feature occupies more than at least approximately 2% of the feature volume.

The foregoing and other features and advantages of the invention will be apparent from the following more particular description of the embodiments of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

The embodiments of this invention will be described in detail, with reference to the following figures, wherein like designations denote like elements, and wherein:

FIG. 1 depicts a cross-sectional view of a device comprising a first dielectric layer, a first hard mask and a photoresist layer thereon, in accordance with embodiments of the present invention;

FIG. 2 depicts the device of FIG. 1 having trenches formed therein;

FIG. 3 depicts the device of FIG. 2 having a conformal liner thereon;

FIG. 4 depicts the device of FIG. 3 following an etch back process;

FIG. 5 depicts the device of FIG. 4 following metalization;

FIG. 6 depicts the device of FIG. 5 following planarization;

FIG. 7 depicts the device of FIG. 6 having a second dielectric layer, hardmask and photoresist layer;

FIG. 8 depicts the device of FIG. 7 having a plurality of trenches formed therein;

FIG. 9 depicts the device of FIG. 8 having a conformal liner thereon;

FIG. 10 depicts the device of FIG. 9 having a photoresist layer thereon;

FIG. 11 depicts the device of FIG. 10 following photoresist patterning;

FIG. 12 depicts the device of FIG. 11 having a plurality of narrow vias formed within the trenches;

FIG. 13 depicts the device of FIG. 12 following metalization;

FIG. 14 depicts the device of FIG. 13 following planarization;

FIG. 15 depicts the device of FIG. 11 having a plurality of wide vias formed within the trenches;

FIG. 16 depicts the device of FIG. 15 following metalization;

FIG. 17 depicts the device of FIG. 16 following planarization;

FIG. 18 depicts the device of FIG. 11 following photoresist patterning;

FIG. 19 depicts the device of FIG. 18 having a plurality of vias formed therein;
FIG. 20 depicts the device of FIG. 19 having a conformal liner deposited over the device;

[0033] FIG. 21 depicts the device of FIG. 20 having a plurality of layers deposited over the liner;

[0034] FIG. 22 depicts the device of FIG. 21 following photoresist patterning;

[0035] FIG. 23 depicts the device of FIG. 22 following etching;

[0036] FIG. 24 depicts the device of FIG. 23 following additional etching;

[0037] FIG. 25 depicts the device of FIG. 24 having trenches formed therein;

[0038] FIG. 26 depicts the device of FIG. 25 having a conformal liner deposited thereover;

[0039] FIG. 27 depicts the device of FIG. 26 following etching;

[0040] FIG. 28 depicts the device of FIG. 27 following metallization; and

[0041] FIG. 29 depicts the device of FIG. 28 following planarization.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0042] Although certain embodiments of the present invention will be shown and described in detail, it should be understood that various changes and modifications might be made without departing from the scope of the appended claims. The scope of the present invention will in no way be limited to the number of constituting components, the materials thereof, the shapes thereof, the relative arrangement thereof, etc. Although the drawings are intended to illustrate the present invention, the drawings are not necessarily drawn to scale.

[0043] FIG. 1 depicts a semiconductor device 10 having a substrate 12, which may comprise conventional features (not shown), such as, a plurality of shallow trench isolations (STI), a MOS transistor and spacers, a vertical NPN transistor, a plurality of contacts damascened into a dielectric, etc., as is known in the art. The substrate 12 is preferably substantially planar, as shown in FIG. 1.

[0044] In accordance with the present invention, a first dielectric layer 14 is deposited over a surface of the substrate 12. The first dielectric layer 14 may comprise a dielectric material having a low dielectric constant (k), wherein “low k” is defined as a dielectric constant (k) below 3.0, or in the range of approximately 1.5-2.7, such as porous poly(arylene) ether (e.g., porous SiLK (Dow Chemical)), porous SiCOH, porous SiO, teflon, or other similarly used material. The liner 24 may be deposited using PECVD, CVD, or other similar deposition techniques. The liner 24 may have a thickness of approximately 150-200 nm.

[0045] A hard mask 16 is then deposited over the first dielectric layer 14. The hard mask 16 may comprise a dielectric material, such as SiC, SiCN, SiCOH, SiO, SiN, etc. The hard mask 16 may be deposited using CVD, PECVD, etc., to a thickness of approximately 1-100 nm, e.g., 10 nm. The hard mask 16 protects the first dielectric layer 14 during subsequent processing, and is optional.

[0046] A photosist 18 is then applied over the hard mask 16, as illustrated in FIG. 1. The photosist 18 may be applied to a thickness in the range of approximately 50-3000 nm, e.g., 200 nm. The photosist 18 may comprise a positive or negative photosist 18 as desired. The photosist 18 is patterned, and the first dielectric layer 14 and hard mask 16 are etched using standard back end of the line (BEOL) exposure and reactive ion etch (RIE) formation techniques to form trenches 20a, 20b (FIG. 2). Narrower trenches 20a may be formed having an aspect ratio (height:width) in the range of approximately 2:1, and a minimum trench width 22a in the range of approximately 100-150 nm. Wider trenches 20b may be formed having any width, and a wide range of aspect ratios, e.g., an aspect ratio of approximately 1:2, 1:10, etc. The wider trenches 20b may also be formed with an optional “dummy fill” in the very large trenches 20b (e.g., a width greater than 2 microns) to reduce the patterned factor, as known in the art.

[0047] During the standard BEOL formation process the photosist 18 may be completely consumed during the RIE etch used in conjunction with a p-SiLK first dielectric layer 14, as illustrated in FIG. 2. Alternatively, a multi-layer hard mask may be used (not shown), such as a first lower hard mask layer, (SiC), and a second upper hard mask layer, (SiO). When using the multi-layer hard mask set the SiO is patterned and etched down to the SiC. The photosist used to pattern the SiO is removed. The SiO is then used to pattern and etch the SiC. The remaining combination of SiO and SiC are then used to pattern the underlying first dielectric layer 14, as known in the art.

[0048] As illustrated in FIG. 3, a conformal dielectric liner 24 is deposited over the surface of the device 10. The liner 24 may comprise a dielectric material having a low dielectric constant (k), wherein “low k” is defined as a dielectric constant (k) preferably below 3.0, or in the range of approximately 1.4-4.5, such as SiCOH, SiO, poly(arylene) ether (e.g., SiLK (Dow Chemical)), teflon, or other similarly used material. The liner 24 may be deposited using PECVD, CVD, or other similar deposition techniques. The liner 24 may have a thickness up to approximately ½ the width of the minimum trench width 22a, and preferably ½ the width of the minimum trench width 22a (FIG. 2: 100-200 nm), i.e., a thickness in the range of approximately 30-50 nm. As a result, the liner 24 occupies more than at least 2% of a trench volume, e.g., at least 50%, or more, of the trench volume. The liner 24 must be prevented from “pinching off” (filling in the opening of the trenches 20a, 20b) which would prevent subsequent metallization of the trenches 20a, 20b.

[0049] A spacer etch back process is performed to remove a portion of the liner 24 from a hole 31 of the trenches 20a, 20b, while leaving the liner 24 on the sidewalls 33 of the trenches 20a, 20b, as illustrated in FIG. 4.

[0050] As illustrated in FIG. 5, a conductive liner 26, a seed layer 28 and a conductive layer 30 are deposited during a standard metallization process. The conductive liner 26 may be deposited over the surface of the device 10 using sputtering techniques, such as plasma vapor deposition (PVD), ionized plasma vapor deposition (IPVD), self-ionized plasma (SIP), HCM, chemical vapor deposition (CVD), atomic layer deposition (ALD), metal organic chemical
vapor deposition (MOCVD), etc. Likewise, the seed layer 28 may be deposited over the conductive liner 26 using similar sputtering techniques, i.e., PVD, IPVD, SIP, HCM, CVD, ALD, MOCVD, etc. The conductive liner 26 may comprise one or more refractory metals or alloys, such as Ta, TaN, TiN, W, WN, TaSiN, WSiN, or other similarly used material. The conductive liner 26 may have a thickness in the range of approximately 1-200 nm, e.g., 5 nm. The seed layer 28 may comprise a copper seed material, or other similarly used material for the subsequent electroplating deposition. The seed layer 28 may have a thickness in the range of approximately 1-200 nm, e.g., 20 nm. The conductive layer 30 may comprise copper, or other similarly used material. The conductive layer 30 may be formed having a thickness in the range of approximately 50 nm-5 microns, e.g., 200 nm. It should be noted that the conductive layer 26 and the seed layer 28 are not drawn to scale for purposes of illustration.

[0051] Following deposition of the metallization, (the conductive layer 26, the seed layer 28 and the conductive layer 30), a planarization process is performed to remove the excess metallization on the surface of the device 10. A chemical mechanical polish (CMP) or other similarly used process may be used to planarize the surface of the device 10. The planarization process is performed down to the conformal dielectric liner 24, as illustrated in FIG. 6. Alternatively, the planarization process may be performed down to the hard mask 16 (not shown). A first metal wiring level 44, having a plurality of electrically conductive wires 32a, 32b therein, in this example comprising a single damascene wiring structure, is produced following the planarization process.

[0052] As illustrated in Table 1, infra, the present invention produces a device 10 having a capacitance far lower, and a wire resistance much higher, than that of similar devices formed using conventional formation methods.

| TABLE 1-continued Comparison of Capacitance and wire Resistance measurements normalized to the Conventional Device A. |
|---|---|---|
| **Comparison of Capacitance and wire Resistance measurements normalized to the Conventional Device A.** |
| **BEOL device dielectric** | **Resistance** | **Capacitance** | **Wire Resistance** |
| layer 14 liner 24 (wire dimensions) | per micron | per micron | levels per micron |
| (aspect ratio) | | | |
| **Conventional Device** | | | |
| A. SiCO (k = 2.7) | 1 | 1 | 1 |
| (140 nm x 200 nm) (1:1) | | | |
| **Present Invention** | | | |
| B. p-SiLK (k = 2.2) | 5 | 0.4 | 0.7 |
| SiCOH liner (k = 2.7) | | | |
| (50 nm x 150 nm) (3:1) | | | |
| C. p-OSG (k = 1.6) | 5 | 0.3 | 0.5 |
| SiCOH liner (k = 2.7) | | | |
| (50 nm x 150 nm) (3:1) | | | |

(* The “p-” indicates that the dielectric is a porous dielectric. The “k” stands for dielectric constant.)

[0053] As illustrated by examples B-D under the “Present Invention” in Table 1, using a low k dielectric material for the first dielectric layer 14, in conjunction with a low k dielectric liner 24 reduces the overall capacitance of the device 10 and increases the wire resistance. In fact, the lower the dielectric constant (k) of the first dielectric layer 14 the more the capacitance of the device is reduced (compare example B with examples C and D) and the more the wire resistance is increased.

[0054] As illustrated in FIG. 6, the wires 32a, 32b have a far smaller width 40a, 40b as compared to the trench widths 36a, 36b, respectively, made available for wire routing during patterning and etching. In fact, the wires 32a, 32b have a width 40a, 40b in the range of approximately 1/4-1/2 the widths 36a, 36b of the trench 20a, 20b, respectively. Typically this would be considered undesirable because it tends to increase wire resistance. The present invention, however, is not concerned with wire resistance, and may be used in conjunction with devices that are not affected by wire resistance, such as ultra low power CMOS devices, wherein the power consumption is determined primarily by the transistor driver resistance and the wire capacitance. By reducing the size (e.g., height 42 and width 40a, 40b) of the wires 32a, 32b, the capacitance of the device 10 can be reduced even further, (compare examples C and D of Table 1). Therefore, it is possible in the present invention to pattern and etch the trenches 20a, 20b having an aspect ratio of 2:1, but end up with much narrower conductive wires 32a, 32b within the trenches 20a, 20b having an aspect ratio of 5:1.

[0055] A dual damascene structure may also be formed in accordance with the present invention. As illustrated in FIG. 7, a second wiring level 45a may be formed on the first wiring level 44, in this example comprising a dual damascene wiring structure. First, a capping layer 46 is deposited over the first metal wiring level 44. The capping layer 46 may comprise SiCN, or other similarly used material. The capping layer 46 may be deposited using CVD, PECVD, etc., having a thickness in the range of approximately 5-100 nm, e.g., 20 nm. The purpose of the capping layer 46 is to prevent diffusion of copper from the conductive wire 32a, 32b formed in the first wiring level 44 into the dielectric layer 48 in the second wiring level 45a. The capping layer 46 may also optionally be used as an etch stop layer during patterning and etching of the vias in the second wiring level 45. Alternatively, the capping layer 46 could be replaced (not shown) by a selective conductive cap, such as electroless...
A second dielectric layer 48 is deposited over the capping layer 46. The second dielectric layer 48 may comprise a dielectric material having a low dielectric constant (k), wherein “low k” is defined as a dielectric constant (k) below 3.0, or in the range of approximately 1.5-2.7, such as porous poly(arylene) ether (e.g., porous Sil.K® (Dow Chemical)), porous SiCOH, porous SiO₂, teflon, amorphous carbon, etc. The second dielectric layer 48 may be deposited using CVD, PECVD, spin-on deposition, etc., to a thickness of approximately 100-3000 nm, e.g., 400 nm.

A hard mask 50 is then deposited over the second dielectric layer 48. The hard mask 50 may comprise a dielectric material, such as SiC, SiCN, SiCOH, SiO₂, Si₃N₄, etc. The hard mask 50 may be deposited using CVD, PECVD, etc., to a thickness of approximately 1-100 nm, e.g., 10 nm.

A photoresist 52 is then applied over the hard mask 50, as illustrated in FIG. 7. The photoresist 52 may be applied to a thickness in the range of approximately 50-3000 nm, e.g., 200 nm. The photoresist 52 may comprise a positive or negative photoresist 52 as desired. The photoresist 52 is then patterned and etched using standard BEOL exposure and RIE formation techniques to form trenches 54a, 54b (FIG. 8). Narrower trenches 54a may be formed having an aspect ratio of approximately 2:1, and a minimum trench width 56a in the range of approximately 100-150 nm. Wider trenches 54b may be formed having any width, and a wide range of aspect ratios, e.g., an aspect ratio of approximately 1:2, 1:10, etc. As described supra, the photoresist 52 may be completely consumed during the standard BEOL formation process when used in conjunction with a p-SiLK second dielectric layer 48. Alternatively, a multi-layer hard mask may be used (not shown), as described supra.

As illustrated in FIG. 9, a conformal dielectric liner 58 is deposited over the surface of the device 10. The liner 58 may comprise a dielectric material having a low dielectric constant (k), wherein “low k” is defined as a dielectric constant (k) preferably below 3.0, or in the range of approximately 1.4-4.5, such as SiCOH, SiO₂, poly(arylene) ether (e.g., Sil.K® (Dow Chemical)), teflon, or other similarly used material. The liner 58 may be deposited using PECVD, CVD, or other similar deposition techniques. The liner 58 may have a thickness up to approximately ½ the width of the minimum trench width 22a, and preferably ¼ the width of the minimum trench width 22a (100-150 nm), i.e., a thickness in the range of approximately 30-50 nm.

A photoresist layer 60 is then applied over the liner 58, as illustrated in FIG. 10. The photoresist 60 may be applied having a thickness in the range of approximately 50-3000 nm, e.g., 200 nm. The photoresist layer 60 over an optional anti-reflective layer (not shown) is then patterned using conventional positive or negative photolithography techniques, as illustrated in FIG. 11. A plurality of vias 62 may then be etched.

The vias 62 may be formed having different widths as desired. For example, as illustrated in FIGS. 12-14, narrower vias 62a may be formed having a width 64a approximately ½ the minimum trench width 56a, e.g., in the range of approximately 30-50 nm. The narrower vias 62a may be useful when forming devices having tighter device densities. Alternatively, wider vias 62b may be formed having a width 64b approximately the same size as the minimum trench width 56a, e.g., in the range of approximately 100-150 nm, as illustrated in FIGS. 15-17.

To form either vias 62a, 62b, the photoresist layer 60 is patterned, as known in the art (FIG. 11). Multiple etch chemistries are employed to then etch down through the conformal liner 58, the hard mask 50, the second dielectric layer 48, and the capping layer 46 to get down to the first wiring level 44 (FIGS. 12 and 15), using a RIE process as known in the art. The etching process may be performed until substantially all of the photoresist 60 is consumed.

As illustrated in FIG. 12, when forming the narrower vias 62a, the etch removes only a portion 72 of the liner 58 on the sidewalls 68a of the trenches 54a having the minimum trench width 56a. In contrast, when forming the wider vias 62b, the etch removes the conformal liner 58 on the sidewalls 68b of the trenches 54a having the minimum trench width 56a (FIG. 15).

Following via 62a, 62b formation, a cleaning process is performed and the metallization is deposited. As illustrated in FIGS. 13 and 16, a conductive liner 74, a seed layer 76 and a conductive layer 78 may be deposited as described supra in connection with the first wiring level 44. Again, the conductive liner 74 and the seed layer 76 are not drawn to scale for purposes of illustration.

Following deposition of the metallization, (the conductive liner 74, the seed layer 76 and the conductive layer 78), a planarization process is performed to remove the excess metallization on the surface of the second wiring level 45a. A CMP or other similarly used process may be used to planarize the surface of the second wiring level 45a. The planarization process is performed down to the conformal liner 58, as illustrated in FIGS. 14 and 17. Alternatively, the planarization process may be performed down to the hard mask 50 (not shown). Electrically conductive wires 80a, 80b are produced following planarization.

The method for forming the second wiring level 45a, described supra, was for a trench first, via second dual damascene feature formation. Alternatively, a second wiring level 45b may be formed using a via first, trench second dual damascene feature formation.

For example, following the formation of the device 10 illustrated in FIG. 7, as described supra, including the capping layer 46, the second dielectric layer 48, the second hard mask 50 and the photoresist layer 52, the photoresist layer 52 is patterned (FIG. 18). The second dielectric layer 48 and the hard mask 50 are then etched using standard BEOL exposure and RIE formation techniques to form vias 100, as illustrated in FIG. 19. The vias 100 may be formed having an aspect ratio of approximately 2:1, and a width 102 in the range of approximately 100-150 nm. As described supra, the photoresist 52 may be completely consumed during the standard BEOL formation process when used in conjunction with a p-SiLK second dielectric layer 48. Alternatively, a multi-layer hard mask may be used (not shown), as described supra.

As illustrated in FIG. 20, a conformal dielectric liner 104 is deposited over the surface of the device 10. The
liner 104 may comprise a dielectric material having a low dielectric constant (k), wherein “low k” is defined as a dielectric constant (k) preferably below 3.0, or in the range of approximately 1.4-4.5, such as SiCOH, SiO₂, poly(arylene) ether (e.g., Sil.K™ (Dow Chemical)), teflon, or other similarly used material. The liner 104 may be deposited using PECVD, CVD, or other similar deposition techniques. The liner 104 may have a thickness in the range of approximately 10-50 nm.

A gap filling organic anti-reflective coating (ARC) 106 is deposited over the surface of the device 10 filling the vias 100, as illustrated in FIG. 21. The ARC 106 may be deposited having a thickness in the range of approximately 100-300 nm, e.g., 200 nm, and may comprise organic or inorganic materials, such as polymers, spin-on glass, etc. The ARC 106 may be deposited using spin-on, CVD, or other similarly used methods. The ARC 106 provides a planar surface for further processing.

A third hard mask 108 is deposited over the ARC 106 using, a low temperature oxide deposited by PECVD at approximately 200°C. (so as not to damage the ARC 106), a spin-on oxide deposition with a low temperature cure (“low temperature” meaning a temperature below approximately 300°C), etc. The third hard mask 108 may comprise a dielectric material, such as SiC, SiCN, SiCOH, SiO₂, Si₃N₄, etc., and may be deposited to a thickness of approximately 1-100 nm, e.g., 10 nm.

A photoresist layer 110 is then applied over the third hard mask 108, as illustrated in FIG. 21. The photoresist 110 may be applied having a thickness in the range of approximately 5-3000 nm, e.g., 200 nm. An optional second ARC layer (not shown) may also be deposited over the photoresist layer 110 if desired. The photoresist layer 110 is then patterned using conventional positive or negative photolithography techniques, as illustrated in FIG. 22.

Various etch chemistries are used to remove portions of the third hard mask 108 and the ARC 106, as illustrated in FIG. 23. A portion of the ARC 106 remains within the vias 100 to prevent damage to the conductive material within the wires 32 of the first wiring level 44 during the subsequent etching process. A different etch chemistry is used to remove the liner 104 and the remaining hard mask 108, as illustrated in FIG. 24. Another etch chemistry is used to remove a portion of the second dielectric layer 48, thereby forming trenches 112 within the second wiring level 45/5, as illustrated in FIG. 25. As described supra, trenches 112a, 112b having different widths 114a, 114b may be formed.

As illustrated in FIG. 26, the remaining ARC 106 within the base of the vias 100 is removed using an ARC removal etch process. A conformal dielectric liner 116 is then deposited over the surface of the device 10. The liner 116 may comprise dielectric material having a low dielectric constant (k), wherein “low k” is defined as a dielectric constant (k) preferably below 3.0, or in the range of approximately 1.4-4.5, such as SiCOH, SiO₂, poly(arylene) ether (e.g., Sil.K™ (Dow Chemical)), teflon, or other similarly used material. The liner 116 may be deposited using PECVD, CVD, or other similar deposition techniques. The liner 116 may have a thickness up to approximately ½ the width of the minimum trench width 114a, and preferably ½ the width of the minimum trench width 114a (100-150 nm), i.e., a thickness in the range of approximately 30-50 nm.

Multiple etch chemistries are employed to etch down through the conformal liners 116, 50 and the capping layer 46 within the base of the vias 100 to get down to the first wiring level 44, as illustrated in FIG. 27.

A cleaning process is then performed and the metallization is deposited, as described supra. As illustrated in FIG. 28, a conductive liner 120, a seed layer 122 and a conductive layer 124 may be deposited as described supra in connection with the first wiring level 44. Again, the conductive liner 120 and the seed layer 122 are not drawn to scale for purposes of illustration.

Following deposition of the metallization, (the conductive liner 120, the seed layer 122 and the conductive layer 124), a planarization process is performed to remove the excess metallization on the surface of the second wiring level 45b, as illustrated in FIG. 29. A CMP or other similarly used process may be used to planarize the surface of the second wiring level 45b. Electrically conductive dual damascene wires 126a, 126b are produced following planarization.

I claim:

1. A structure, comprising:
   a substrate;
   a first dielectric layer on and in direct mechanical contact with a top surface of the substrate, wherein the first dielectric layer comprises a first dielectric material;
   a first hard mask on the first dielectric layer, wherein the first hard mask comprises a first lower hard mask layer and a second upper hard mask layer;
   a first trench and a second trench within the first dielectric layer and the first hard mask, wherein the second trench is wider than the first trench in a first direction that is parallel to the top surface of the substrate;
   a first conformal liner on sidewalls of the first trench and on sidewalls of the second trench, wherein the first conformal liner comprises a second dielectric material, wherein the first conformal liner is in direct physical contact with the top surface of the substrate, the first dielectric layer, the first hard mask; and
   a first conductive material filling the first and second trenches, wherein the first conductive material comprises copper, wherein a first portion of the first conformal liner is disposed between the first conductive material in the first trench and both first dielectric layer and the first hard mask, wherein a second portion of the first conformal liner is disposed between the first conductive material in the second trench and both first dielectric layer and the first hard mask, and wherein a planar surface of the first conductive material is parallel to the first direction and is coplanar with a top surface of the first conformal liner and a top surface of the first hard mask.

2. The structure of claim 1, further comprising:
   a capping layer on, and in direct mechanical contact with, the planar surface of the first conductive material, the top surface of the first hard mask, and the top surface of the first conformal liner;
   a second dielectric layer on, and in direct mechanical contact with, the capping layer, wherein the capping
layer comprises a continuously distributed capping material that prevents diffusion of copper from the first conductive material in both the first trench and the second trench to the second dielectric layer; and
a second hard mask on, and in direct mechanical contact with, the second dielectric layer.
3. The structure of claim 2, further comprising:
a third trench through the second hard mask and in the second dielectric layer, wherein the third trench is aligned directly above the first trench;
a fourth trench through the second hard mask and in the second dielectric layer, wherein the fourth trench is aligned directly above the second trench, and wherein the fourth trench is wider than the third trench in the first direction; and
a conformal dielectric liner on sidewalls of the third trench and on sidewalls of the fourth trench and on a top surface of the second hard mask and in direct mechanical contact with both the second hard mask and the second dielectric layer, wherein the conformal dielectric liner comprises a third dielectric material.
4. The structure of claim 3, wherein the third dielectric material has a dielectric constant in a range of 1.4 to 4.5.
5. The structure of claim 3, further comprising:
a photoresist layer on a top surface of the conformal dielectric liner and filling the fourth trench; and
a fifth trench in the conformal dielectric liner, wherein the fifth trench is above the third trench and is contiguous with the third trench, and wherein the fifth trench is wider than the third trench in the first direction.
6. The structure of claim 3, further comprising:
a sixth trench in the conformal dielectric liner, wherein the sixth trench is above the third trench and is contiguous with the third trench, wherein the sixth trench is wider than the third trench in the first direction, and wherein the third trench extends through the conformal dielectric layer, the second dielectric layer, and the capping layer to the planar surface of the substrate; and
a seventh trench extending through the conformal dielectric layer, the second dielectric layer, and the capping layer to the planar surface of the substrate, wherein the seventh trench is contiguous with the fourth trench, and wherein the fourth trench is wider than the seventh trench in the first direction.
7. The structure of claim 6, further comprising a conductive layer filling the sixth, third, fourth, and seventh trenches.
8. The structure of claim 7, wherein the conductive layer extends above the sixth and fourth trenches
9. The structure of claim 7, wherein a planar surface of the conductive layer is parallel to the first direction and coplanar with a top surface of the conformal dielectric liner.
10. The structure of claim 9, wherein the conformal dielectric liner is in direct mechanical contact with:
the conductive layer in the sixth trench;
the conductive layer in the third trench;
the conductive layer in the fourth trench; and
the conductive layer in the seventh trench;
11. The structure of claim 1, wherein the first dielectric material has a dielectric constant in a range of 1.4 to 2.7.
12. The structure of claim 1, wherein the second dielectric material has a dielectric constant in a range of 1.4 to 4.5.
13. The structure of claim 1, wherein the first lower hard mask layer includes SiC and the second upper hard mask layer includes SiO₂.

* * * * *