

- [54] **SORTING MACHINE WITH DIGITAL ERROR CORRECTION**
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- [73] Assignee: **Petty-Ray Geophysical, Inc.**, Houston, Tex.
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- [52] U.S. Cl. **209/111.6; 330/25; 330/96; 356/195**
- [51] Int. Cl.² **B07C 5/342**
- [58] Field of Search 209/111.6, 111.7; 250/222 R; 330/25, 96; 356/173, 195, 226

[56] **References Cited**

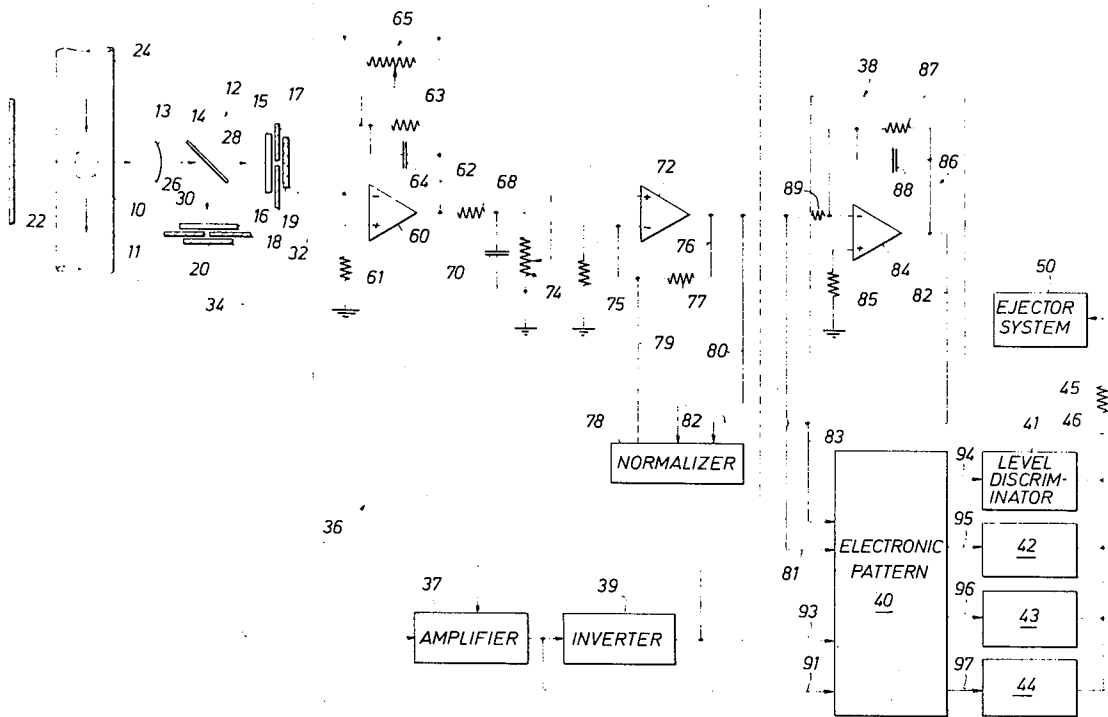
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Attorney, Agent, or Firm—Arnold, White & Durkee

[57] **ABSTRACT**

A sorting machine having direct coupled amplifier means is normalized to correct offset and drift errors due to component aging, dust buildup, and the like by digital error correction or normalizing circuit means. Error signals output by the amplifier means in response to application of a reference signal input are utilized with suitable control means to advance a digital counter, the output of which is coupled to a feedback loop of the amplifier means by way of a digital-to-analog converter to provide fixed levels of error correction signals corresponding to the stepwise output of the digital counter. The signal output by the digital normalizing circuit means is thus maintained at a constant level between normalizing cycles. In one embodiment of the present invention, the normalizing sequence may be programmed for periodic initiation at fixed time intervals.

8 Claims, 8 Drawing Figures



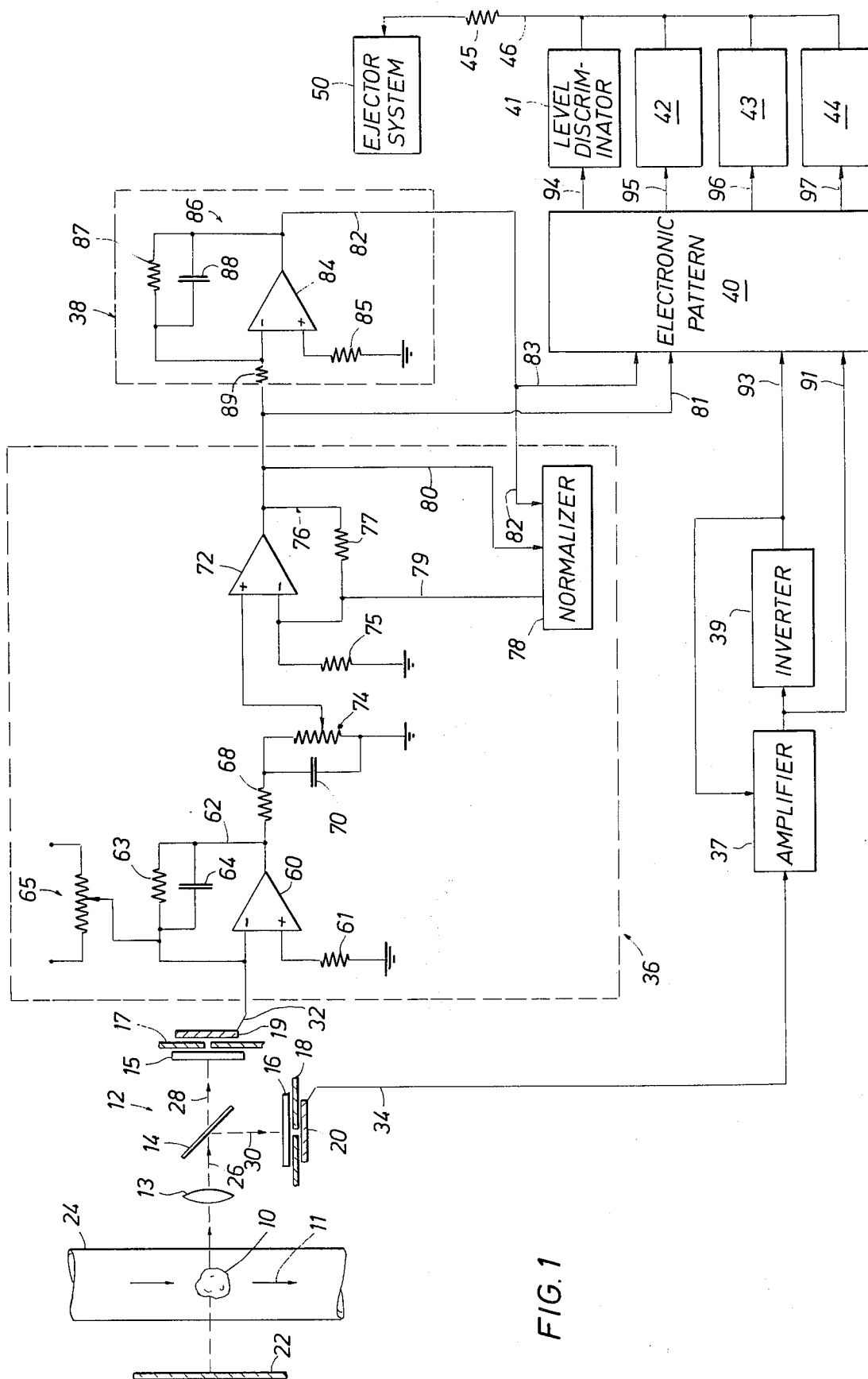


FIG. 1

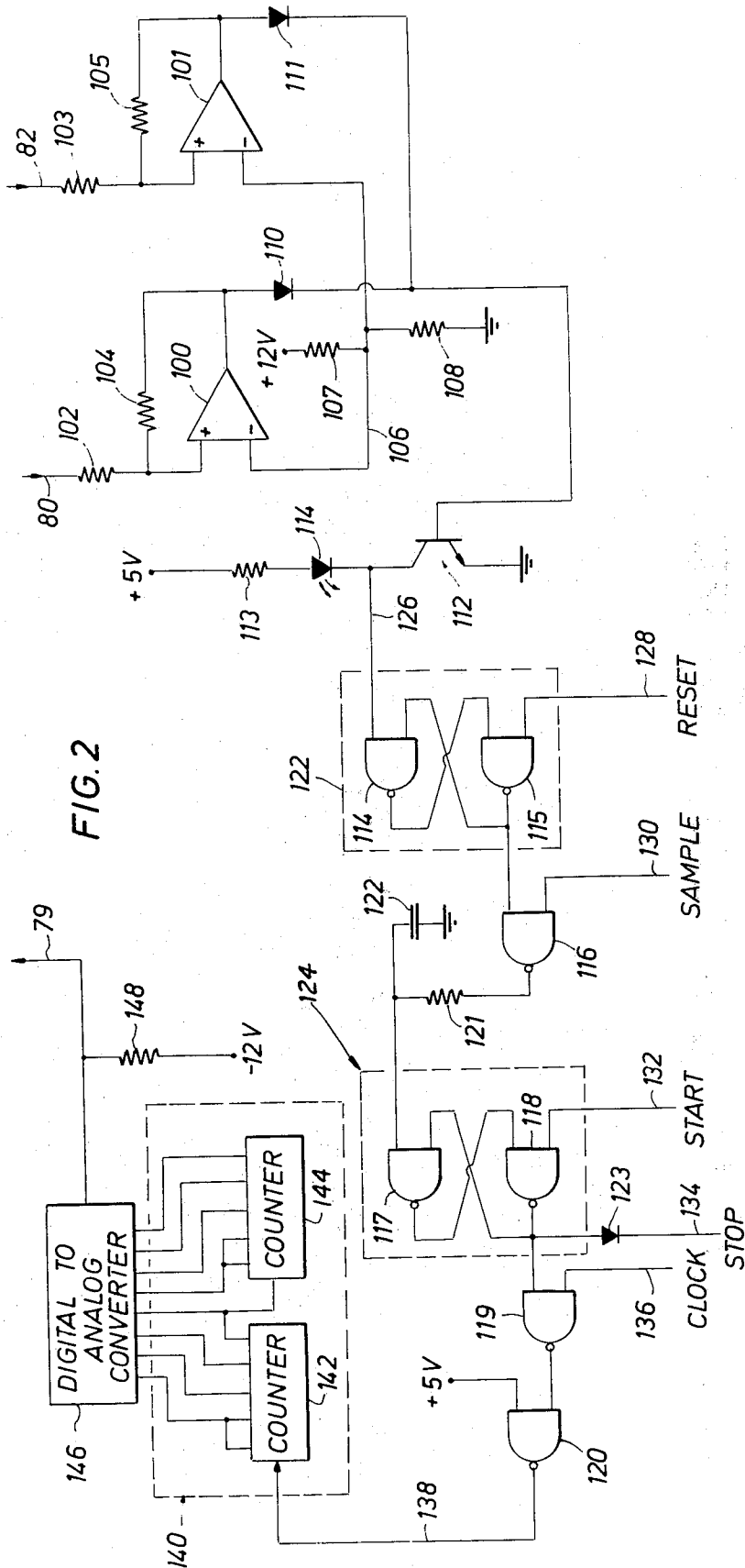
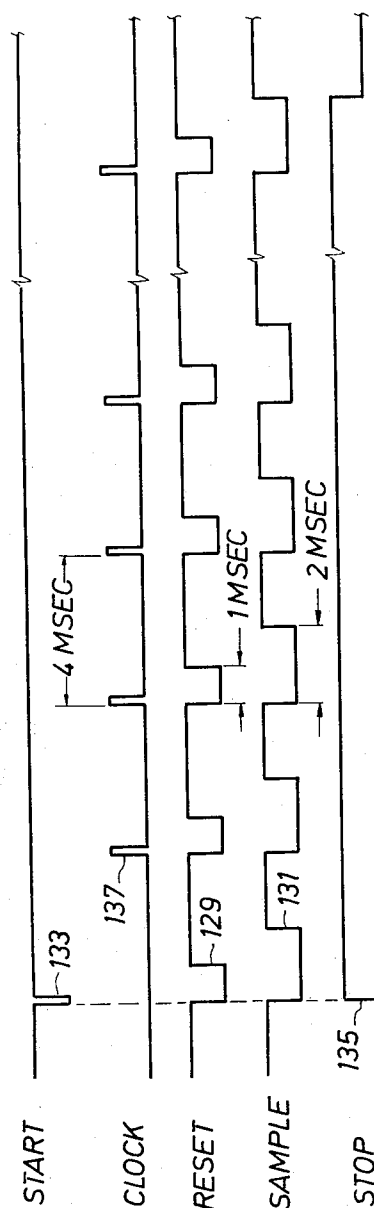


FIG. 3

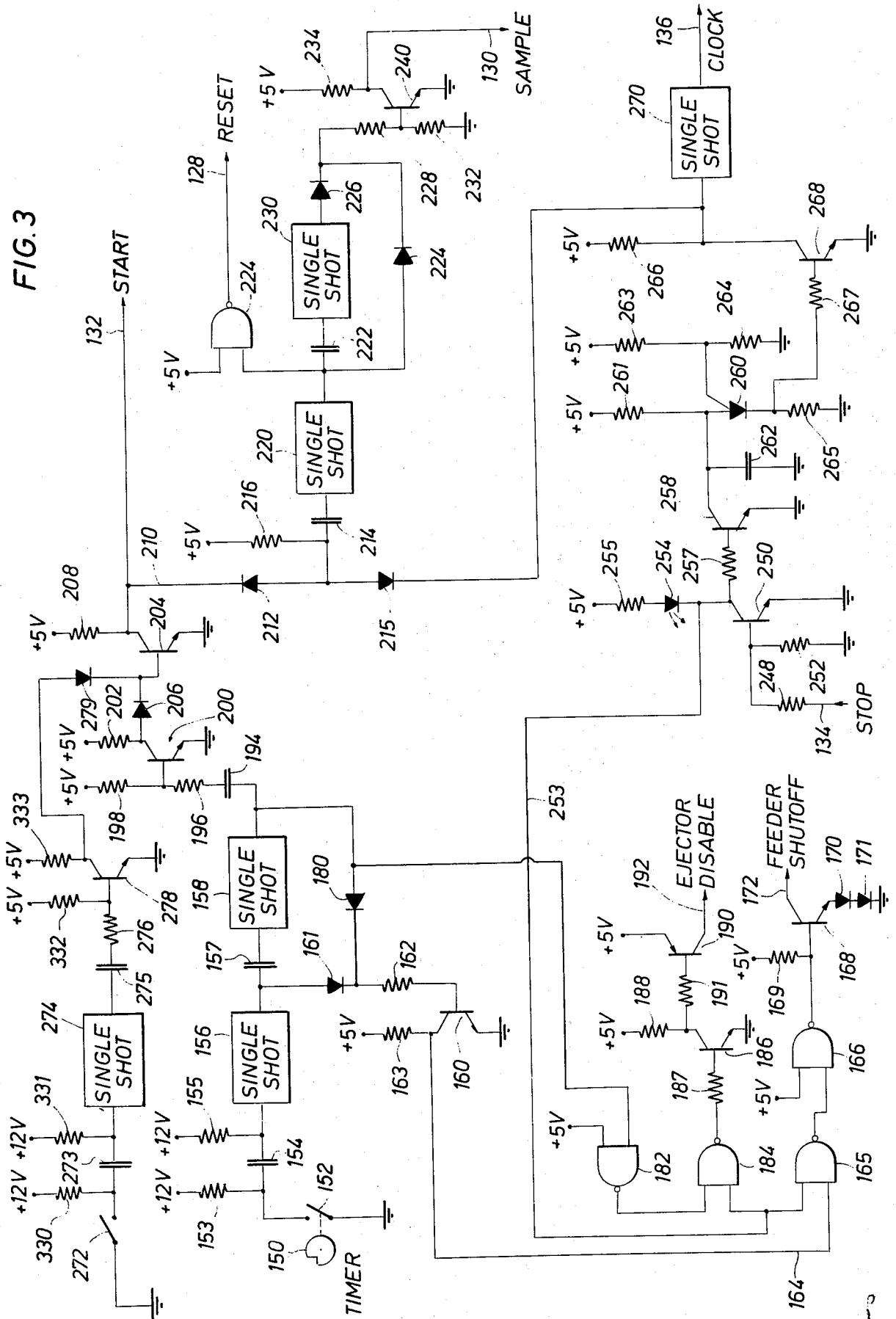


FIG. 5

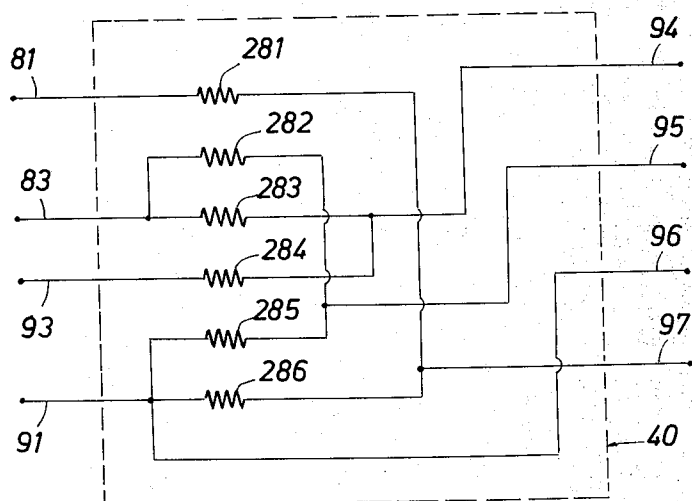


FIG. 6

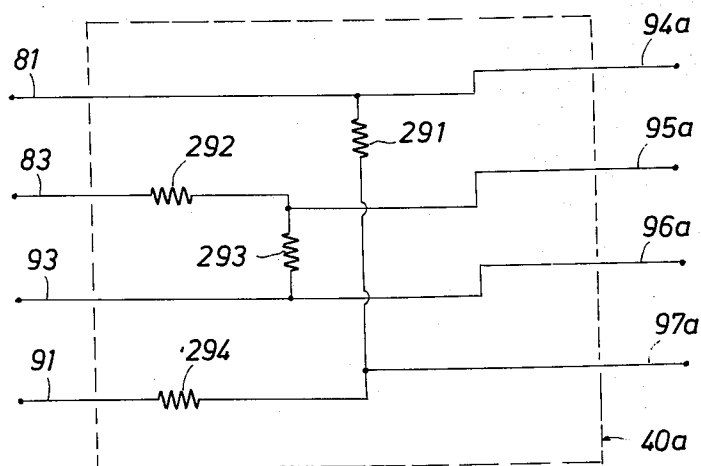
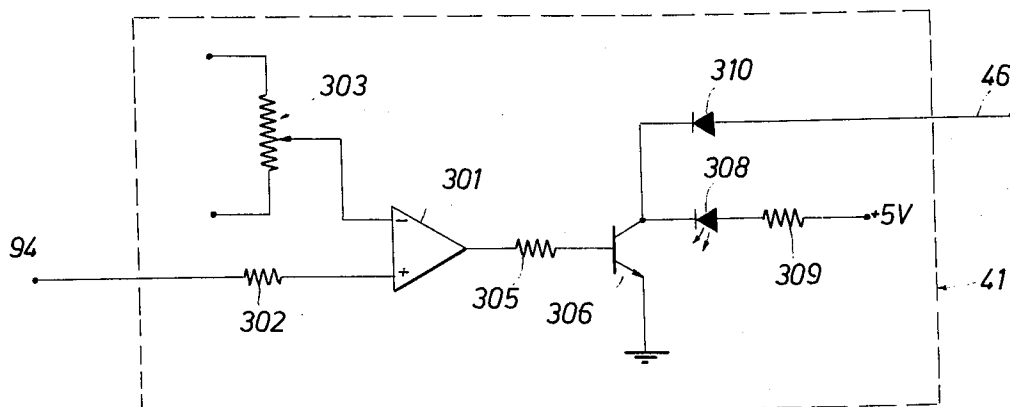


FIG. 7



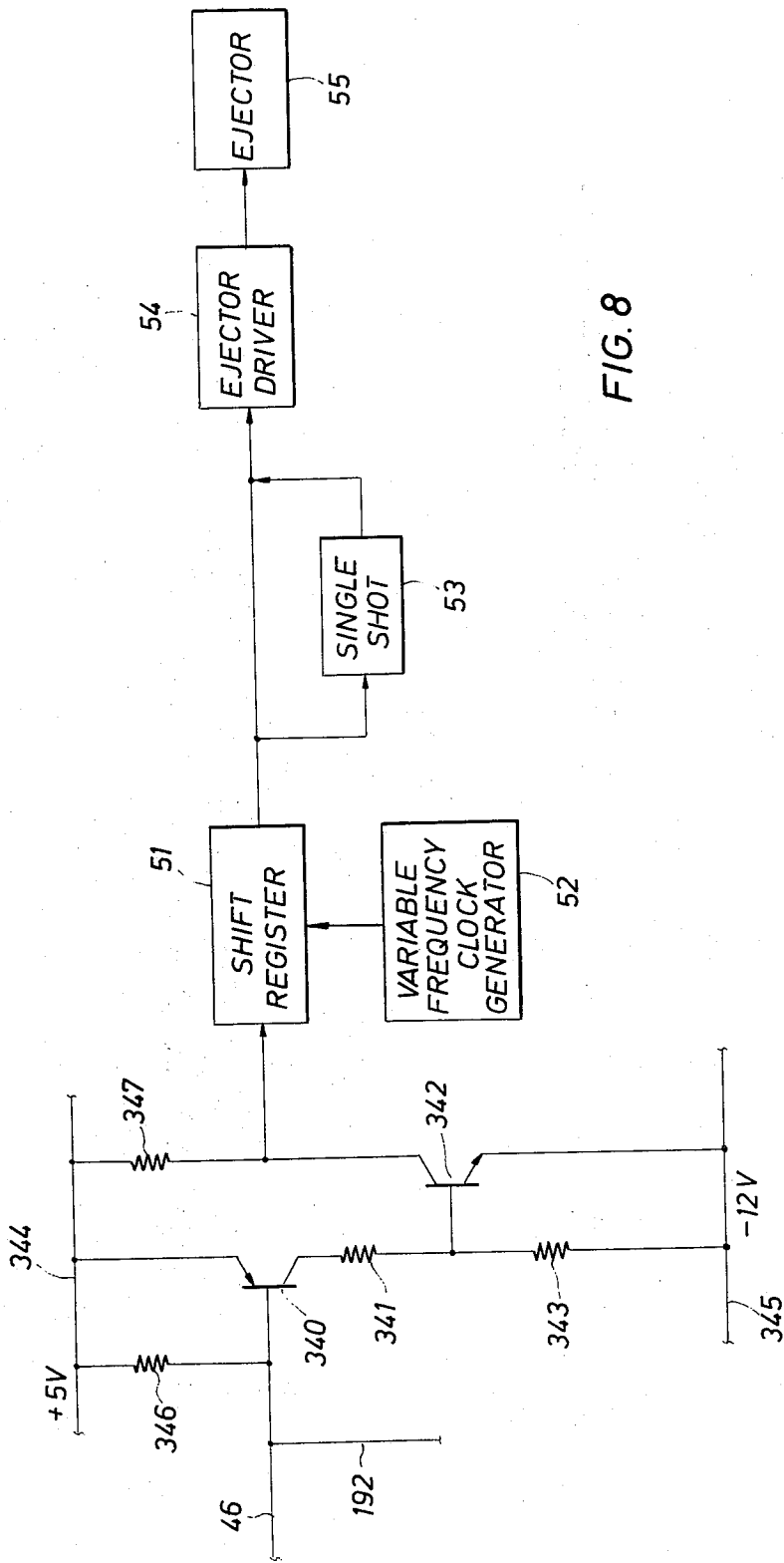


FIG. 8

SORTING MACHINE WITH DIGITAL ERROR CORRECTION

BACKGROUND OF THE INVENTION

The present invention relates to sorting machines, and, more particularly, to apparatus for sorting articles from one another responsive to differences in the intensity of light energy reflected therefrom at one or more predetermined wavelengths within the optical frequency spectrum.

In prior art color sorting machines in which light energy is reflected from the articles to be sorted and directed to one or more photosensitive elements to produce corresponding electrical signals, direct coupled amplifier systems have generally been used to obtain the necessary sensitivity discrimination between desired and undesired articles of many types. The offset and drift characteristics inherent in direct coupled amplifiers are well known, and frequent adjusting of the gain of such amplifiers has been required to compensate for such effects as component aging, temperature variations, buildup of dirt or dust in the optical system, and the like. This adjustment is referred to as "normalizing."

Normalizing of direct coupled amplifier systems in photoelectric sorting machines has heretofore involved intermittent charging or discharging of a capacitor to provide a bias voltage to an amplifier. This has often been accomplished by intermittent exposure of the various photosensitive elements of such apparatus to corresponding standard references, usually background elements which may be viewed in intervals between the passage of successive of the articles to be sorted through the machine's viewing area. This procedure requires a finite period of time during which no articles may be sorted, and frequent normalizing thereby significantly reduces the sorting capacity of the machine. The frequency with which prior art systems have required normalizing has been high, in some cases as often as between the viewing of each article to be sorted.

Efforts to overcome the foregoing offset and drift problem by utilization of capacity coupled amplifier systems have not been entirely satisfactory. Although such systems are typically far more stable and drift-free than direct coupled amplifier systems, they are inherently limited in their response to the random signal levels generated in response to undesired articles during optical color sorting. As a consequence, sorting machines utilizing capacity coupled amplifier systems have not provided the sensitivity and accuracy of sorting that has been desired in high capacity sorting of such articles as green coffee beans and the like.

Accordingly, it is one object of the present invention to provide a high capacity sorting machine which will accurately sort articles from one another on the basis of small color differences.

It is another object of this invention to provide an optical color sorting machine that will maintain sorting accuracy and constancy in calibration over a relatively extended period of operation while providing high capacity sorting capability.

Among the further objects of this invention is to provide a sorting machine capable of precise, sensitive, and accurate response to minute deviations in the light reflective properties of sorted articles from a predeter-

mined standard of comparison and to maintain such performance over substantial intervals of operation.

SUMMARY OF THE INVENTION

The present invention provides apparatus for sorting articles on the basis of small variations in their color, including direct coupled amplifiers employing digital normalizing means to provide a substantially drift-free calibration of the amplifiers over extended periods of operation.

In one aspect, the present invention includes a digital normalizer for periodically resetting the bias of a direct coupled amplifier, together with electronic control means for periodically determining the bias voltage necessary to compensate for offset and drift, means for setting this value in a digital counter, and digital-to-analog converter means for providing this value as a constant bias voltage to the feedback loop of the amplifier.

Further in accordance with this invention, an optical viewing system monitors the light energy reflected from articles passing through a viewing area or zone and produces electrical signals responsive to their color. The optical viewing system also monitors the light energy reflected from a background member supported in the viewing area such that the articles to be sorted pass between the background and the viewing system.

In one embodiment of the present invention, reference backgrounds corresponding to the color of acceptable articles to be sorted are viewed by each of three respective optical viewing assemblies. The light energy reflected from the respective backgrounds and from articles to be sorted as they pass between the respective backgrounds and optical viewing assemblies is passed through a beam splitter, one-half of the energy being directed to each of a pair of photosensitive elements through respective color filters. The filters limit to preselected wavelengths the light incident upon the respective photosensitive elements. Each of the photosensitive elements produces an electrical signal responsive to the intensity of the light incident upon it. Each of these signals is then input to corresponding direct coupled amplifier means.

During the normalizing sequence the feed of articles to the viewing zone is stopped and the background members are viewed as the reference standard. One output of each direct coupled amplifier means is directed to a first voltage level comparator and compared with a predetermined reference voltage. This output of the amplifier means is passed through a phase inverter and then to a second voltage level comparator, and compared with a second predetermined reference voltage. If the voltage input to either of the two voltage level comparators is outside the predetermined limit, as set by the corresponding reference voltages, a signal is output through suitable control logic to a digital counter. The counter advances in stepwise fashion with successive clock pulses to vary the digital signal input to a digital-to-analog converter. The output of the digital-to-analog converter is then provided to the corresponding amplifier feedback loop. The digital counter is advanced until the output of the amplifier system comes within the predetermined reference limits, at which time advancement of the counter is stopped and sorting operations are resumed. The output of the digital-to-analog converter is thus established at a fixed level corresponding to the output of the digital counter,

and remains at that level between successive normalizing sequences. In this manner the requirement for normalizing is limited to offset and drift variations occurring between successive normalizing sequences and, as the problems of capacitor leakage and the like in such circuits are overcome, apparatus in accordance with the various embodiments of the present invention will require normalizing much less frequently than has heretofore been necessary.

BRIEF DESCRIPTION OF THE DRAWINGS

A better understanding of the present invention will be afforded by the following detailed description considered in conjunction with the accompanying drawings.

FIG. 1 is a simplified block and schematic diagram illustrated one embodiment of the present invention.

FIG. 2 is a block and schematic diagram illustrating in greater detail a portion of the embodiment illustrated in FIG. 1.

FIG. 3 is a block and schematic diagram illustrating in greater detail another portion of the embodiment of FIG. 1.

FIG. 4 illustrates a series of waveforms which depict a timing sequence of the circuit of FIGS. 1-3.

FIGS. 5 and 6 are schematic circuit diagrams of electronic patterns useful in various embodiments of the present invention.

FIG. 7 is a schematic diagram of a level comparator suitable for the invention as illustrated in FIGS. 1-3.

FIG. 8 is a simplified block and schematic diagram of the ejector system of FIG. 1.

DETAILED DESCRIPTION OF THE INVENTION

Referring now to FIG. 1, articles to be sorted, such as a coffee bean 10, travel along a predetermined path indicated by reference numeral 11. The articles 10 may conveniently travel through a clear or transparent glass or plastic tube 24 to isolate the articles and any associated dust or debris from the viewing means of the sorting machine. The articles are illuminated by light sources (not shown), and the reflected light is collected in viewing means 12 by lens 13. Light path 26 is passed in part and reflected in part by a beam splitter 14, such as for example a half-silvered mirror, to define light paths 28 and 30 respectively. The light paths 28,30 are passed through respective color filters 15,16, each of which limits the wavelength of the light passed to a different predetermined wavelength within the optical frequency spectrum. For example, filter 15 might pass a red wavelength and filter 16 a blue wavelength. The light beams 28,30 are then passed through respective optical frames 17,18 and impinge upon respective photosensitive elements 19,20. Optical frames 17,18 are adjusted or "synchronized" so that the light incident upon the respective photosensitive elements is that reflected from the same viewed area of the article or product as it moves through tube 24.

The viewing means 12 views the background member 22 when there is no article 10 within its field of view. The background member 22 is preferably the color of the acceptable products 10, so that variations in the signals produced by photosensitive elements 19,20 represent deviations from the desired color of the products.

Photosensitive elements 19,20, which may for example be silicon solar cells, output electrical signals on lines 32 and 34 respectively. These signals are directed

to respective amplifier means 36 and 37. The outputs of the respective amplifier means are delivered in part to phase inverters 38,39 and then to an electronic pattern 40, and in part directly to the electronic pattern 40, which will be discussed below. Although a preferred embodiment of the present invention includes three optical viewing assemblies equally spaced in a single plane around the articles to be sorted, and each of these three assemblies outputs a pair of color signals, the present discussion is directed to but one such signal, the treatment of which is typical for all.

Referring in detail to the amplifier means indicated by reference numeral 36, the output of photosensitive element 19 is coupled to the negative input of a first operational amplifier 60. The positive input of amplifier 60 is coupled to ground through resistor 61. The output of the amplifier 60 is coupled to its negative input by a feedback loop 62 containing a filter defined by a resistor 63 and a capacitor 64. In addition, bias voltage is supplied to the feedback loop 62 through variable resistor 65.

The output of the first amplifier 60 is coupled to the noninverting input of a second operational amplifier 72 through a fixed resistor 68 and a variable resistor, or gain control potentiometer, 74. A capacitor 70 is coupled between the ground side of resistor 74 and the downstream side of resistor 68 to define a second filter. The negative input of amplifier 72 is grounded through a resistor 75. A feedback loop 76, including a resistor 77, is connected between the output and the negative input of amplifier 72. Normalizer means 78, which will be discussed in detail hereinafter, is coupled to the feedback loop 76 by line 79. The output of amplifier 72 is provided to normalizer means 78 by line 80.

The output of amplifier 72 increases with increasing intensity of the light energy passed by the filter 15, and constitutes the light trip signal for the color so defined. This output is coupled directly to the electronic pattern 40 by line 81.

The output of amplifier 72 is also coupled to phase inverter 38, the output of which is coupled to the electronic pattern 40 by line 83. The phase inverter 38 includes a unity gain amplifier 84, the positive input of which is coupled to ground through a resistor 85. A feedback loop 86 is coupled between the output and the negative input of amplifier 84 and includes a resistor 87 and a capacitor 88 defining a filter. The negative input line also includes a resistor 89. The output of amplifier 84 also is coupled to the normalizer means 78 by line 82. The output of amplifier 84 increases with decreasing intensity of the light energy passed by the filter 14, and is the dark trip signal for the color defined by the filter 15.

Corresponding light trip and dark trip signals representative of the light energy passed by the second filter 16 and the corresponding optical frame 18, and incident on photosensitive element 20, are similarly provided to electronic pattern 40 by lines 91 and 93 respectively. The respective filters 15,16 may be selected to define various color combinations, as is well known to those familiar with the art of bichromatic optical color sorting, depending upon the color properties of the articles or products to be sorted.

Electronic pattern 40 is coupled to level discriminators 41-44 by lines 94-97, respectively. The output of the level discriminators 41-44 is then coupled to an ejector system 50 through a resistor 45 by line 46. The

electronic pattern 40 will be discussed below in connection with FIGS. 5 and 6.

Referring now to FIG. 2, the normalizer means of FIG. 1 is illustrated in detail. The direct output of the second amplifier 72 on line 80 is coupled to a first level discriminator amplifier 100 through resistor 102. The negative input of the amplifier 100 is connected to a line 106 which represents a reference voltage determined by resistor 107 and 108 respectively connected line 106 to a positive 12-volt source and to ground. The output of inverter 38 on line 82 is coupled to a second level discriminator amplifier 101 through resistor 103. The negative input of amplifier 101 is also connected to the reference voltage line 106. The outputs of amplifiers 100 and 101 are connected to their respective positive inputs through resistors 104 and 105 respectively. The outputs of amplifiers 100 and 101 are also connected to the base of transistor 112 through diodes 110 and 111 respectively. As long as a signal is output by either amplifier 100 or amplifier 101, transistor 112 remains conductive creating a path from a 5-volt source through resistor 113 and light emitting diode 114 to ground. Line 126 remains at ground potential while transistor 112 is conductive.

NAND gates 114-120 are coupled as illustrated to provide control logic for directing clock pulses to counter 140. NAND gates 114 and 115 are coupled to define a latch 122. NAND gates 117 and 118 are similarly coupled to define a latch 124.

Reset, sample, start, and clock pulses are provided to NAND gates 115, 116, 118, and 119 respectively. One input to NAND gate 120 is coupled to a positive 5-volt source so that the NAND gate 120 operates as an inverter. The output of NAND gate 120 is provided by line 138 to an 8-bit digital binary counter 140. In the embodiment illustrated in FIG. 2, counter 140 includes a pair of 4-bit binary counters 142, 144 connected in cascade to provide the 8-bit counter. It will be appreciated, however, that other counter elements may be utilized if desired. The output of counter 140 is coupled to an 8-bit binary digital-to-analog converter (DAC) 146, and the analog signal output thereby is coupled to the feedback loop 76 of amplifier 72 by line 79. A portion of the current output by the DAC 146 is drawn off by resistor 148 to provide a staircase signal which will step through 256 steps to vary the voltage output of amplifier 72 over a preselected range, for example from plus 3 volts to minus 3 volts in approximately 23 millivolt increments. is coupled

Line 126 is coupled to the input of latch 122 defined by NAND gate 114, and line 128 is coupled to the input defined by NAND gate 115. The output of latch 122 is coupled to one input of NAND gate 116. The other input of NAND gate 116 is coupled to line 130. The output of NAND gate 116 is coupled through resistor 121 to the input of latch 124 defined by NAND gate 117. This input to NAND gate 117 is also coupled to ground through capacitor 122.

The input to latch 124 defined by NAND gate 118 is coupled to line 132. The output of latch 124 is connected to the anode of diode 123, the cathode of which is coupled to line 134. The output of latch 124 is also coupled to one input of NAND gate 119, the second input thereof being coupled to line 136. The output of NAND gate 119 is coupled to the second input of NAND gate 120.

Referring now to FIG. 3, the control circuit for the normalizer means of FIG. 2 is illustrated in schematic. A timer 150 periodically closes a switch 152 to ground, thereby firing a first monostable multivibrator, or single shot, 156 through capacitor 154. The left-hand side of capacitor 154 is connected to a positive 12-volt source through a resistor 153, and the right-hand side of capacitor 154 is connected to a positive 12-volt source through a resistor 155. The output of single shot 156 is coupled to a second single shot 158 through capacitor 157, and to the anode of diode 161. The cathode of diode 161 is coupled to the base of transistor 160 through a resistor 162. The collector of transistor 160 is connected to a 5-volt source through resistor 163, and the emitter of transistor 160 is coupled to ground. The output of single shot 158 is also coupled to the anode of diode 180. The cathode of diode 180 is connected to the base of transistor 160 through resistor 162.

The collector of transistor 160 is coupled to one input of NAND gate 165 by line 164. The output of NAND gate 165 is coupled to one input of NAND gate 166. The second input of NAND gate 166 is coupled to a positive 5-volt source, so that NAND gate 166 functions as an inverter. The output of NAND gate 166 is coupled to the base of transistor 168. The base of transistor 168 is also coupled to a positive 5-volt source through resistor 169. The collector of transistor 168 is coupled to a feeder shutoff control through line 172. The emitter of transistor 168 is grounded through diodes 170 and 171 in series.

The output of single shot 158 also is coupled directly to one input of NAND gate 182. The second input of NAND gate 182 is coupled to a positive 5-volt source. The output of NAND gate 182 is coupled to one input of NAND gate 184. The output of NAND gate 184 is coupled to the base of transistor 186 through resistor 187. The emitter of transistor 186 is grounded and the collector is coupled to a positive 5-volt source through resistor 188. The collector of transistor 186 also is coupled to the base of transistor 190 through resistor 191. The emitter of transistor 190 is coupled to a positive 5-volt source, and the collector to line 192 to disable the ejector, as will be discussed below.

The output of single shot 158 also is coupled to the base of transistor 200 through capacitor 194 and resistor 196. The base of transistor 200 is also coupled to a positive 5-volt source through resistor 198. The emitter of transistor 200 is grounded, while the collector is coupled to a positive 5-volt source through resistor 202. The collector of transistor 200 also is coupled to the anode of diode 206, the cathode of which is coupled to the base of transistor 204. The emitter of transistor 204 is grounded, while the collector is coupled to a positive 5-volt source through resistor 208. The collector of transistor 204 is further coupled to START signal line 132 and, through line 210, to the cathode of diode 212. The anode of diode 212 is coupled to a single shot 220 through capacitor 214. The left-hand side of capacitor 214 is coupled to a positive 5-volt source through resistor 216.

The output of single shot 220 is connected to the anode of diode 224, the cathode of which is connected to the base of transistor 240 through resistor 228. The base of transistor 240 is also grounded through resistor 232. The output of single shot 220 also is coupled to one input of NAND gate 224, the other input of which

is coupled to a positive 5-volt source. The output of NAND gate 224 appears on RESET signal line 128.

The output of single shot 220 also is coupled to single shot 230 through capacitor 222. The output of single shot 230 is coupled to the anode of diode 226, the cathode of which is also coupled to the base of transistor 240 through resistor 228. The emitter of transistor 240 is grounded, and the collector is coupled to a positive 5-volt source through resistor 234. The collector of transistor 240 is also coupled to SAMPLE signal line 130.

The output of NAND gate 118 (FIG. 2), appearing on STOP signal line 134, is coupled to the base of transistor 250 through resistor 248. The base of transistor 250 is also grounded through resistor 252. The collector of transistor 250 is coupled to the cathode of light emitting diode 254, the anode of which is coupled to a positive 5-volt source through resistor 255. The collector of transistor 250 is also coupled to the base of transistor 258 through resistor 257. The emitter of transistor 250 is grounded.

The emitter of transistor 258 is grounded, and the collector is coupled to a positive 5-volt source through resistor 261, to ground through capacitor 262, and to the anode of a programmable unijunction transistor, or relaxation oscillator, 260. The cathode of relaxation oscillator 260 is grounded through resistor 265, and also is connected to the base of transistor 268 through resistor 267. The gate of relaxation oscillator 260 is coupled to a positive 5-volt source through resistor 263 and to ground through resistor 264. The emitter of transistor 268 is grounded, and the collector is coupled to a positive 5-volt source through resistor 266, to the input of single shot 270, and to the cathode of diode 215. The anode of diode 215 is coupled to single shot 220 through capacitor 214. The output of single shot 270 appears as a CLOCK signal or pulse on line 136.

Referring again to transistor 204 of FIG. 3, the base of transistor 204 also is connected to the cathode of diode 279, the anode of which is connected to the collector of transistor 278 and to a positive 5-volt source through resistor 333. The emitter of transistor 278 is grounded. The base of transistor 278 is coupled to a positive 5-volt source through resistor 332, and to the output of single shot 274 through resistor 276 and capacitor 275. The input of single shot 274 is coupled to a first positive 12-volt source through resistor 331, and to a second positive 12-volt source through capacitor 273 and resistor 330. The left side of capacitor 273 may be grounded through switch 272 to start the countdown of single shot 274.

Referring now to FIG. 5, electronic pattern 40 is described in greater detail. Respective light trip input lines 81 and 91 are coupled to output 97 through resistors 281 and 286 respectively. Respective dark trip input lines 83 and 93 are coupled to output line 94 through resistors 283 and 284 respectively. Input lines 83 and 91 are coupled to output line 95 through resistors 282 and 285 respectively. Input line 91 also is coupled directly to output line 96.

Referring now to FIG. 6, an alternative embodiment of an electronic pattern suitable for utilization in the present invention is indicated by reference numeral 40a. Input line 81 is connected directly to output line 94a. Input lines 81 and 91 are connected to output line 97a through resistors 291 and 294 respectively. Input lines 83 and 93 are connected to output line 95a

through resistors 292 and 293 respectively. Input line 93 also is connected directly to output line 96a.

The purpose and effect of the various interconnections achieved by electronic pattern 40 may be more fully understood by reference to United States Patent 3,012,666, incorporated herein by reference, in which the results obtained by combining various light and dark trip circuit outputs through various mixing or pattern-defining resistor circuits is more fully discussed, and which further provides graphic illustration of exemplary of the "patterns" which may be obtained from such circuits.

FIG. 7 illustrates in detail one embodiment of a level discriminator 41 which is typical of the level discriminators 41-45 of FIG. 1. Input line 94 is coupled to the positive input of amplifier 301 through resistor 302. The negative input of amplifier 301 is coupled to a variable resistor 303, to provide a selectable reference voltage. The output of amplifier 301 is coupled to the base of transistor 306 through resistor 305. The emitter of transistor 306 is grounded. The collector of transistor 306 is coupled to the cathode of light emitting diode 308, the anode of which is coupled to a positive 5-volt source through resistor 309. The collector of transistor 306 is also coupled to the cathode of diode 310, the anode of which is coupled to the ejector system 50 of the sorting machine through resistor 45 by line 46 (FIG. 1).

Referring now to FIG. 8, the ejector system 50 of FIG. 1 is illustrated in greater detail. Lines 46 and 192 are coupled to the base of transistor 340, as well as to a positive 5-volt source through resistor 346. The emitter of transistor 340 is also coupled to a positive 5-volt source through line 344, and the collector is coupled to a negative 12-volt source through resistors 341 and 343. The base of transistor 342 is coupled between resistors 341 and 343, and the emitter is coupled to the negative 12-volt source. The collector of transistor 342 is coupled to a positive 5-volt source through resistor 247 and to shift register 51. A variable frequency clock generator 52 is operatively coupled to the shift register 51 to provide a variable clock signal to the shift register and thereby vary the countdown time of shift register 51 for corresponding variations in the resulting delay. The output of shift register 51 is coupled directly to a conventional ejector driver 54 and to the input of ejector driver 54 through single shot 53. The output of the ejector driver 54 is coupled to a conventional ejector 55.

Each of the foregoing circuit elements is of conventional construction and readily available on the commercial market. For example, amplifier 60 may be a type 709 low offset, low drift operational amplifier, while the remaining amplifiers may be type 741 operational amplifiers. The various single shots may be for example conventional model NE555V monostable multivibrators readily available from a variety of sources. Digital-to-analog converter 146 may be a Hybrid Systems' model DAC 371-8, and counters 142 and 144 may be model SN74L934-bit binary counters.

OPERATION

In operation, the normalization sequence may be initiated at predetermined intervals by timer 150. Closing switch 152 to ground fires single shot 156, the output of which immediately closes transistor 160, grounding input 164 to NAND gate 165. The high output of

NAND gate 165 produces a low output of NAND gate 166, opening transistor 168 and shutting off the product feeder through line 172.

As the output of single shot 156 returns to ground, it triggers single shot 158. The output of single shot 158 also maintains the feeder shutoff through transistor 160 and produces a low output into NAND gate 184 through inverter 182. The high output of NAND gate 184 closes transistor 186, which in turn closes transistor 190. When transistor 190 is closed, a 5-volt ejector disable signal is transmitted over line 192 to prevent firing of the ejector 55.

Transistor 200, which is normally biased to saturation through resistor 198, is momentarily opened by the trailing edge of the output of single shot 158. In turn closing transistor 204 through diode 206 and grounding line 132 to produce a START pulse 133 (FIG. 4). The closing of transistor 204 also initiates the countdown of single shot 220, the output of which is inverted by NAND gate 224 to produce a RESET pulse 129 (FIG. 4) on line 128. The output of single shot 220 also closes transistor 240 through diode 224 and resistor 228, and transistor 240 is held closed by the output of single shot 230, initiated by the trailing edge of the output of single shot 220, to produce a SAMPLE pulse 131 (FIG. 4) on line 130.

START pulse 133 is provided to NAND gate 118 (FIG. 2) by line 132, immediately producing a STOP pulse 135 (FIG. 4) on line 134. STOP pulse 135 is coupled to the base of transistor 250, causing the transistor to close and the light emitting diode 254 to fire. This grounds the second inputs of NAND gates 165 and 184 by way of line 253, maintaining the state of the ejector disable and feeder shutoff. The closing of transistor 250 opens transistor 258, initiating operation of the relaxation oscillator 260. Relaxation oscillator 260 periodically discharges, in this case every 4 milliseconds, to close transistor 268, grounding the inputs to single shots 270 and 220. Single shot 270 runs down at a very rapid rate, for example 0.1 millisecond, to produce corresponding CLOCK pulses 137 (FIG. 4) on line 136. As long as the output of latch 124 is high, each clock pulse input to NAND gate 119 produces a corresponding pulse output from inverter 120 over line 138 to counter 140, advancing counter 140 by one step.

During this period no product is fed to the viewing zone, and the optical system views only light reflected from background 22 as affected by dirt and dust accumulated in the system. The output of each of the photosensitive elements is amplified by the corresponding amplifiers and compared with the predetermined normalizer reference 106. As long as transistor 112 is held closed, counter 140 will advance with each clock pulse. The output of the digital-to-analog converter will correspondingly advance in fixed current steps of 1/256 of its full scale output, which may be, for example, 2 milliamperes. The output of DAC 146 is coupled through line 79 to feedback loop 76 of amplifier 72 to produce a corresponding staircase of fixed steps of voltages at the amplifier output. Note that as the DAC output increases, the amplifier output decreases.

When the output from the DAC to the feedback loop 76 is sufficient to bring the amplifier output within the predetermined range established at line 106, amplifiers 100 and 101 are simultaneously negative and transistor 112 is open. This puts line 126 in a high voltage state, thus ungrounding the corresponding input to latch 122.

If this condition holds for the 1 millisecond time interval between the low-to-high transitions on the RESET and SAMPLE waveforms, 129 and 131 (FIG. 4) respectively, then the output of latch 122 will still be in the high state when the SAMPLE waveform 131 goes high. When this condition is satisfied, the output of NAND gate 116 goes low into latch 124 through NAND gate 117. The output of latch 124 from NAND gate 118 then goes low into NAND gate 119, preventing clock pulses 137 from being input in inverter 120. Note that if line 126 goes low again at any time before the SAMPLE pulse 131 goes high, the output of latch 122 is set low and latch 124 cannot be reset during that particular 4-millisecond period of the clock.

When the output of NAND gate 118 goes low, STOP pulse 135 on line 134 (FIG. 3) also goes low, opening transistor 250 and sending line 253 high to NAND gates 184 and 165. This causes the respective outputs of NAND gates 184 and 165 to go low, terminating the ejector disable and turning on the feed, so that operation of the sorting machine will automatically resume.

It will be appreciated that the normalizing sequence also may be initiated by closing switch 272 (FIG. 3) to fire single shot 274. The trailing edge of the pulse from single shot 274 momentarily opens transistor 278, which in turn momentarily closes transistor 204 to generate the negative going START pulse on line 132 and to fire single shot 220. The remainder of the cycle will then be as previously described.

The operation of the ejector disable circuit may be understood by consideration of FIG. 8. The presence of an ejector disable input signal on line 192 will hold transistor 340 open. This will preclude the closing of transistor 342, and thereby prevent the counting down of shift register 51 to initiate an eject pulse, and no such pulse will be provided to ejector driver 54.

When there is no ejector disable signal on line 192, the ejector system is responsive to a negative-going pulse input on line 46 to close transistor 340, which in turn closes transistor 342. The closing of transistor 342 results in the input of a signal to shift register 51, the signal having a duration response to the time an unacceptable color is viewed by the respective viewing means.

The frequency of clock generator 52 is varied to adjust the delay between sensing of an unacceptable article or product and the firing of the ejector, which may be located slightly below the viewing zone. Adjustment of the clock frequency will then compensate for variations in location of the ejector with respect to the viewing zone and in rate of fall of the articles being sorted.

A single shot 53 is triggered by the output of the shift register to provide a minimum duration pulse to the ejector driver 54. If a large area of the article being sorted is of an unacceptable color, the pulse output by the shift register 51 may be of greater duration than that output by the single shot 53, in which event the former pulse would control shutdown of the ejector.

Although the present invention has been described herein with reference to the output of a single photosensitive element in one embodiment, it will be understood that normalization means may be provided for each of the respective viewing means and that the normalizing means will operate in each cycle until all of the amplifier means have been brought within the preset conditions. It will be apparent to those of skill in the optical color sorting arts that various modifications

may be made in the embodiment illustrated without departing from the spirit and scope hereof, and that the sorting machines may be operated with one or more viewing means, each of which may be monochromatic or bichromatic as desired or appropriate according to the articles to be sorted.

What we claim is:

1. Apparatus for sorting articles according to light-reflective properties, comprising:

viewing means for sensing light energy reflected from an article to be sorted, said viewing means producing an electrical signal indicative of the light-reflective properties of the article;

direct coupled amplifier means operatively coupled to said viewing means for amplifying said electrical signal;

ejector means operatively coupled to said amplifier means for deflecting an article having predetermined light-reflective properties responsive to a corresponding amplified electrical signal;

reference means for selectively providing a reference signal to said amplifier means; and

normalizing means operatively coupled to said amplifier means for introducing an error correction signal to said amplifier means, said normalizing means including digital counter means for defining discrete stepwise output signals corresponding to the error correction signal, digital-to-analog converter means for introducing the output signals from the digital counter means to said amplifier means as corresponding analog signals; and control means for automatically redetermining said error correction in said digital counter means at predetermined time intervals.

2. Apparatus for sorting articles as recited in claim 1, wherein said reference means comprise a background selectively viewed by said viewing means to provide the reference signal.

3. Apparatus for sorting articles as recited in claim 1, wherein said normalizing means includes means for comparing the amplified signal output from said amplifier means responsive to said reference signal with a predetermined standard and to produce a control signal when said signal output is greater than said standard, and means for advancing said digital counter means responsive to said control signal.

4. Apparatus for sorting articles as recited in claim 1, including phase inverter means coupled between said amplifier means and said ejector means and providing an inverted amplifier output signal to said normalizing means.

5. Apparatus for sorting articles according to light-reflective properties, comprising:

viewing means for sensing light energy reflected from an article to be sorted, said viewing means producing an electrical signal indicative of the light-

reflective properties of the article;

direct coupled amplifier means operatively coupled to said viewing means for amplifying said electrical signal;

ejector means operatively coupled to said amplifier means for deflecting an article having predetermined light-reflective properties responsive to a corresponding amplified electrical signal;

reference means for selectively providing a reference signal to said amplifier means;

normalizing means operatively coupled to said amplifier means for introducing an error correction signal to said amplifier means, said normalizing means including digital counter means for defining discrete stepwise output signals corresponding to the error correction signal and digital-to-analog converter means for introducing the output signals from the digital counter means to said amplifier means as corresponding analog signals; and

control means for clearing said viewing means of articles to be sorted, disabling said ejector means, providing said reference signal to said amplifier means, sensing the output of said amplifier means responsive to said reference signal, advancing said digital counter means until the output of said amplifier means is within a predetermined range of values, and resuming the sorting of said articles.

6. In a light-sensitive sorting machine having direct coupled amplifier means for amplifying electrical signals indicative of a light reflective property of an article to be sorted, the improvement comprising normalizing means operatively coupled to said amplifier means for introducing an error correction thereto, said normalizing means including means for setting said error correction in digital counter means, digital-to-analog converter means operatively coupled to said digital counter means for introducing said error correction to said amplifier means in analog format and means for redetermining the value of said error correction at selected intervals and resetting said predetermined error correction in said normalizing means.

7. Apparatus as recited in claim 6 wherein said normalizing means includes means for comparing the electrical signals output from said amplifier means with a predetermined value and means for advancing said digital counter means until said amplifier output responsive to a reference input signal is within the predetermined value.

8. Apparatus as recited in claim 6 wherein said normalizing means includes means for offsetting the error correction output by said digital-to-analog converter means to produce a desired range of outputs from said amplifier means when said digital counter means is stepped through a complete cycle.

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