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(54) **SEMICONDUCTOR DEVICE**

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(57) **ABSTRACT**

According to one embodiment, a semiconductor device includes a first element isolating area, a first element area surrounding the first element isolating area, a second element isolating area surrounding the first element area a first gate electrode provided on and across the first element isolating area, the first element area, and the second element isolating area, and a second gate electrode isolated from the first gate electrode and provided on and across the first element isolating area, the first element area, and the second element isolating area.

22 Claims, 12 Drawing Sheets

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H01L 21/8238 (2006.01)

(52) **U.S. Cl.**
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See application file for complete search history.

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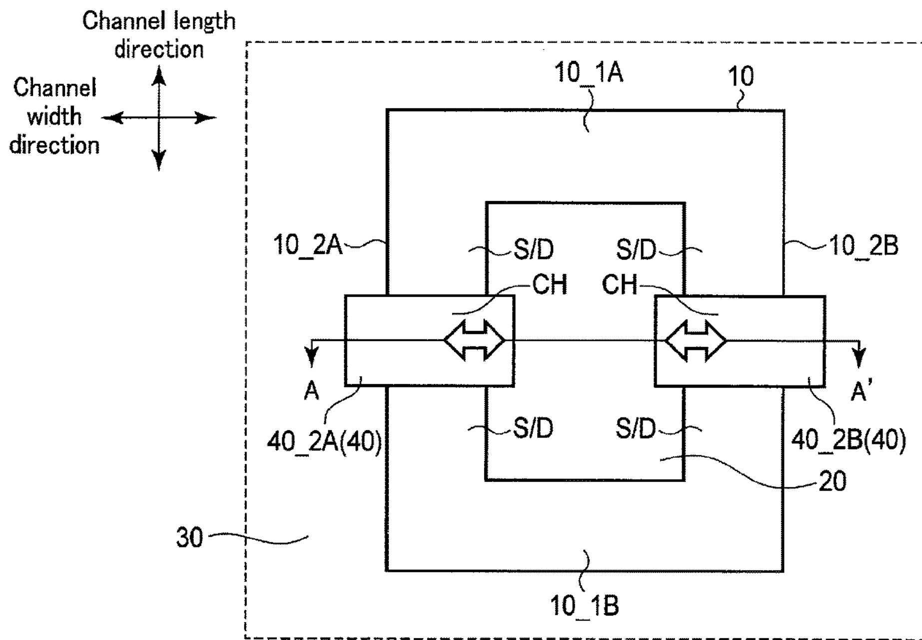

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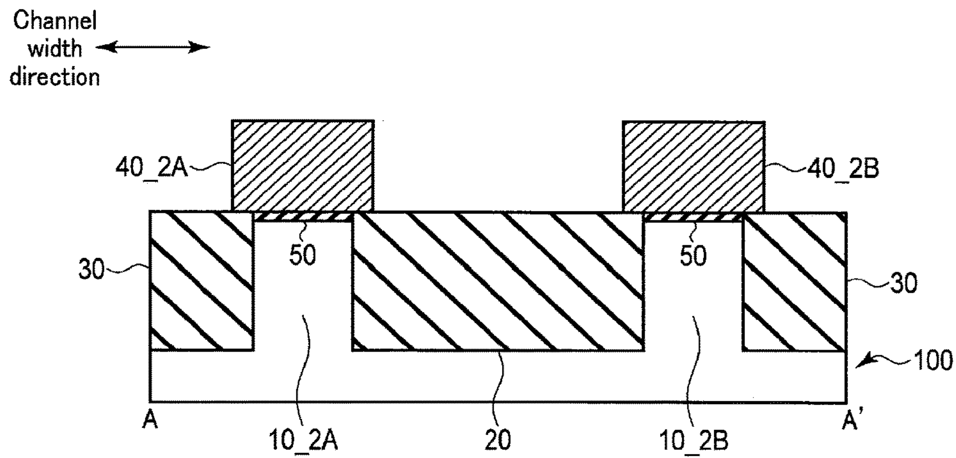

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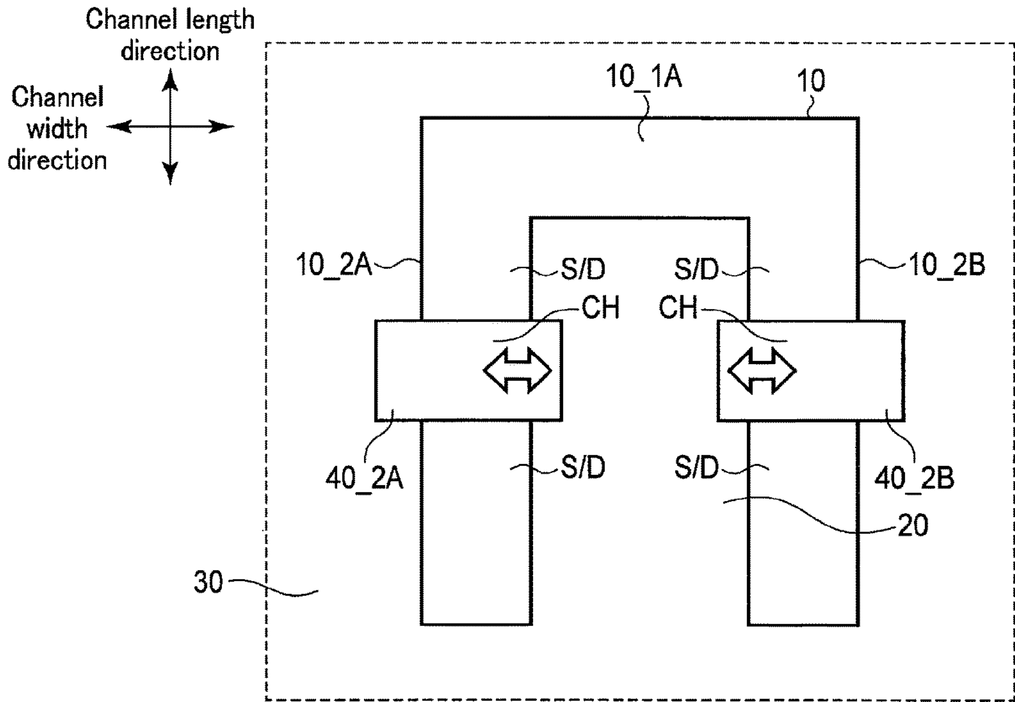

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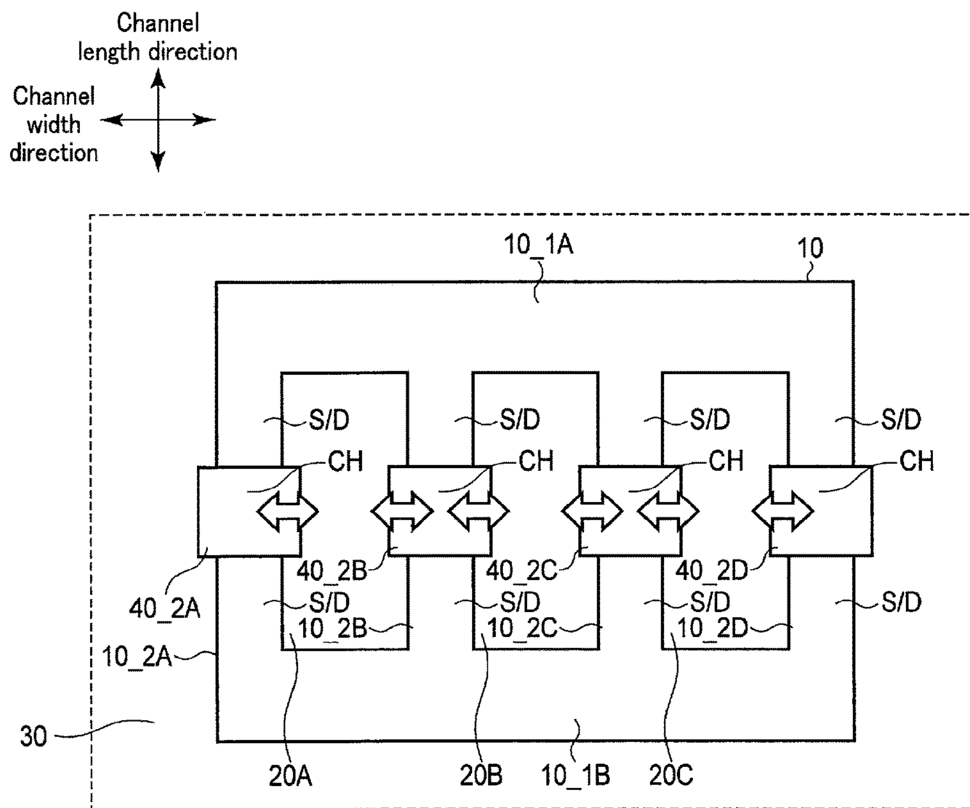

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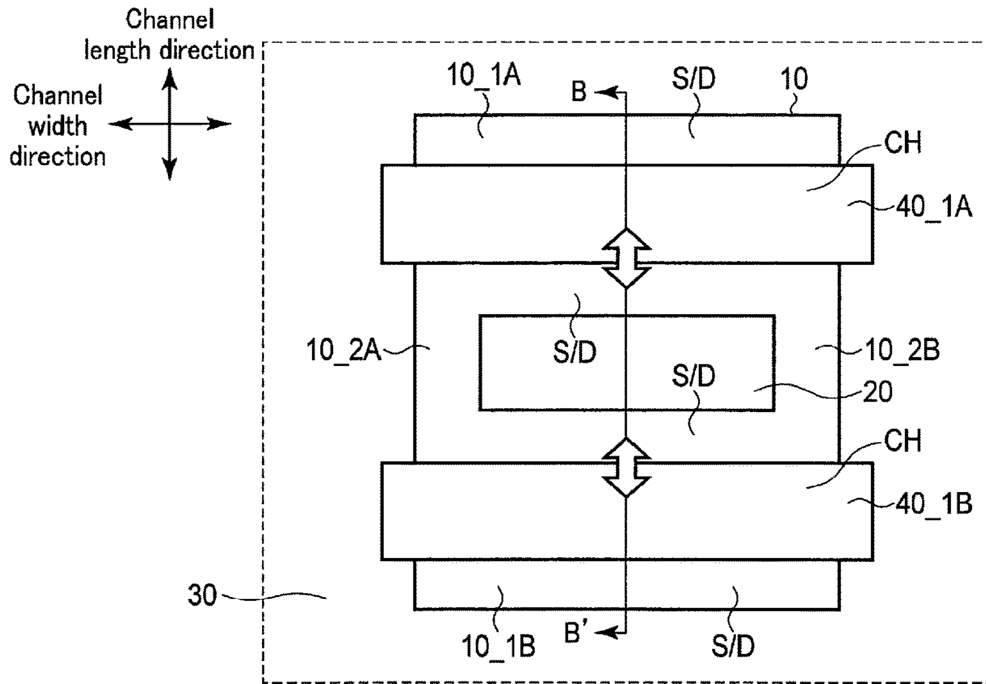

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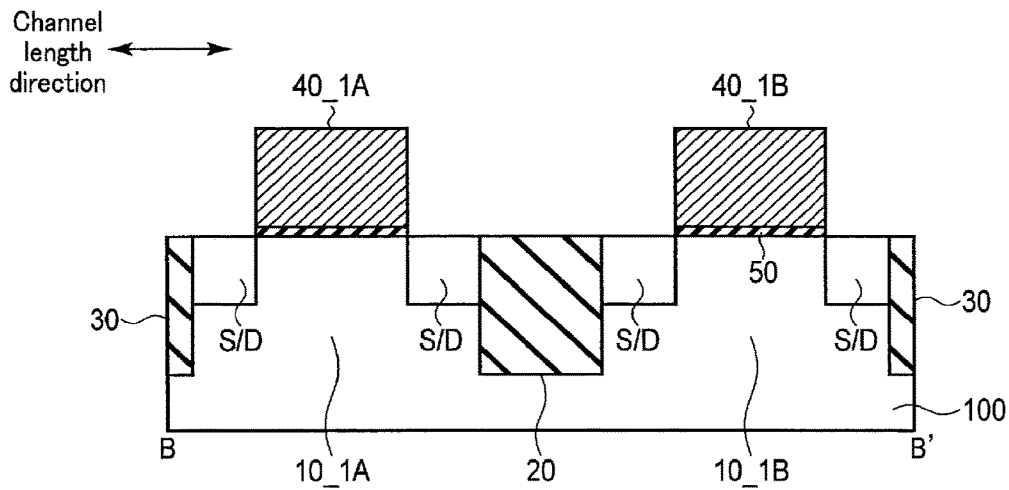

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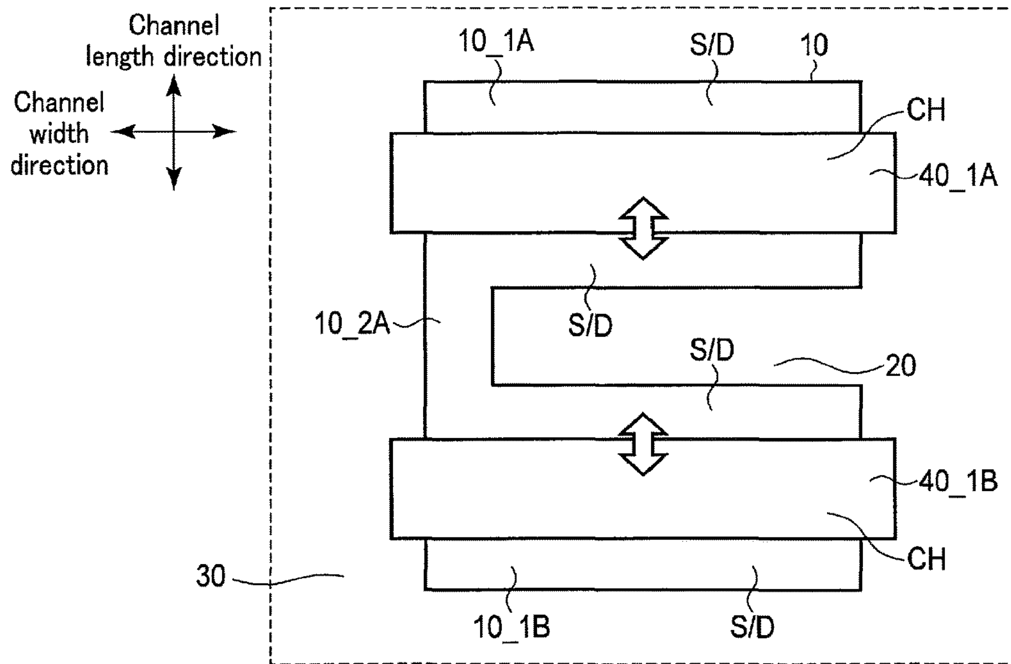

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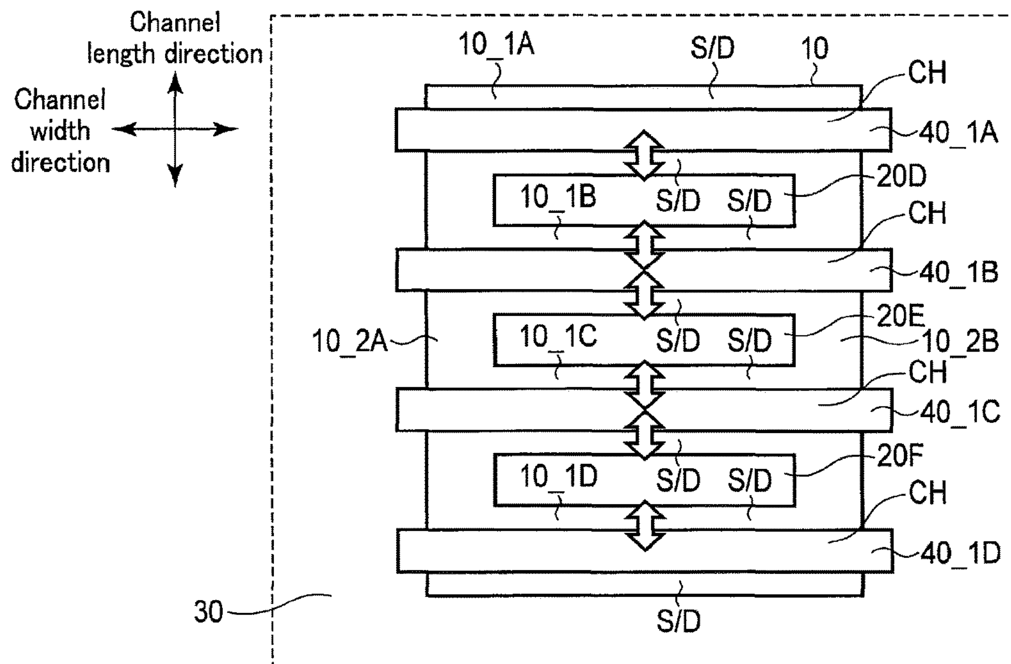


F I G. 8

Channel length direction
Channel width direction
10_1A
10
20A
20B
20C
S/D
CH
40_2A
40_2B
10_2B
10_1B
10_2C
40_2C
40_2D
40_1B
10_2D
20D
10_1C
10_2A
40_1C
20E
10_1D
40_1D
20F
10_1E
40_1E
30

F I G. 9

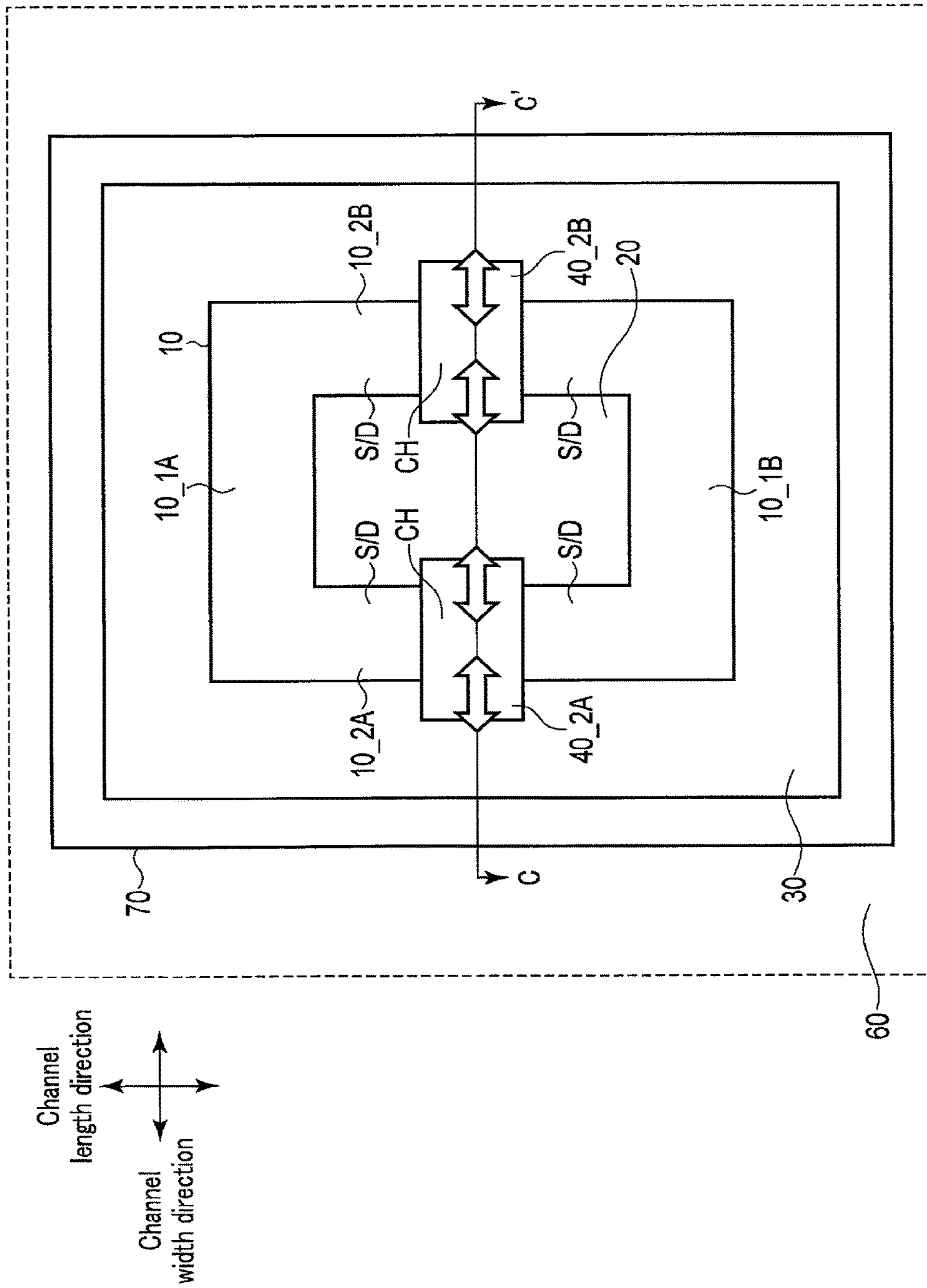


FIG. 10

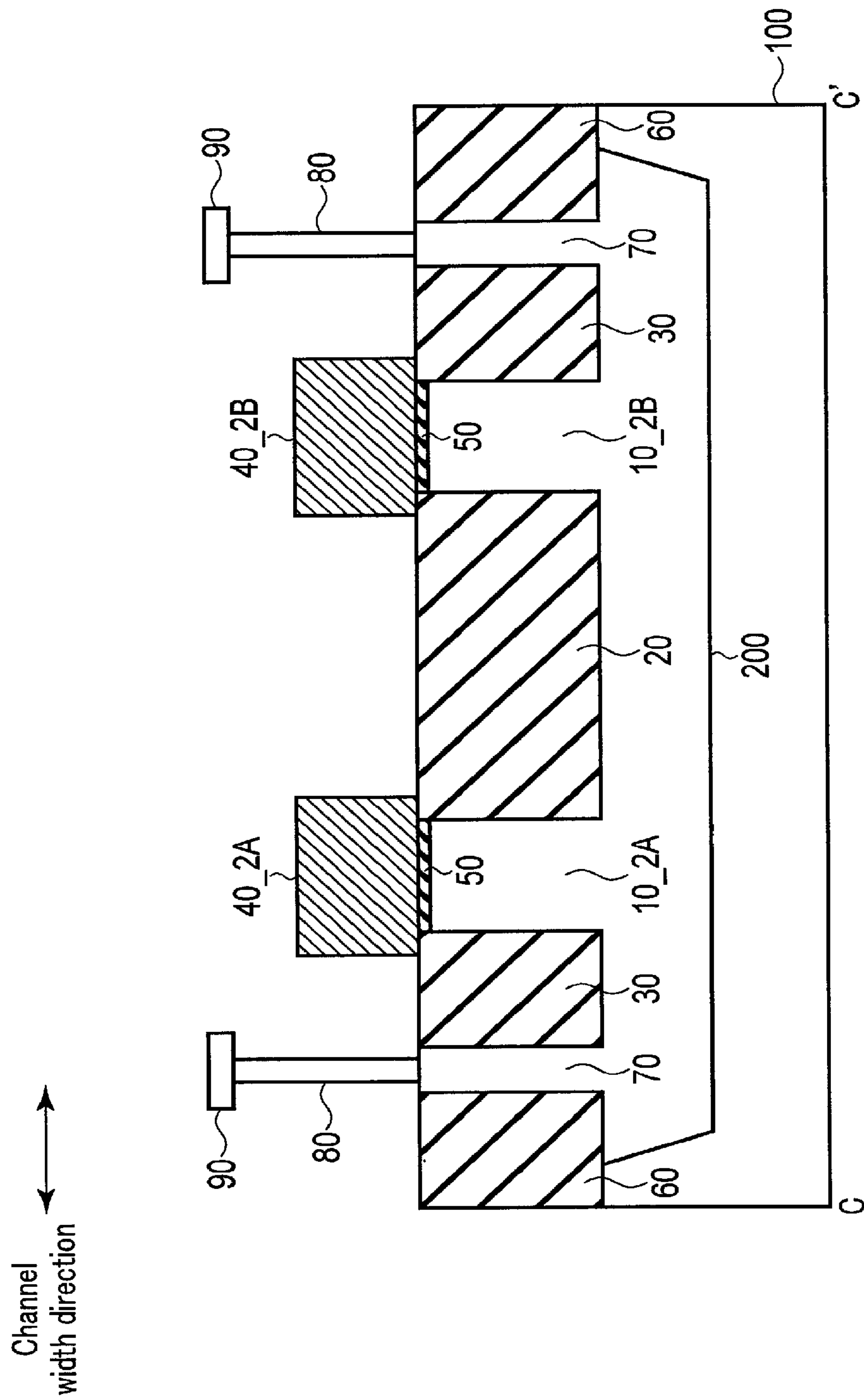
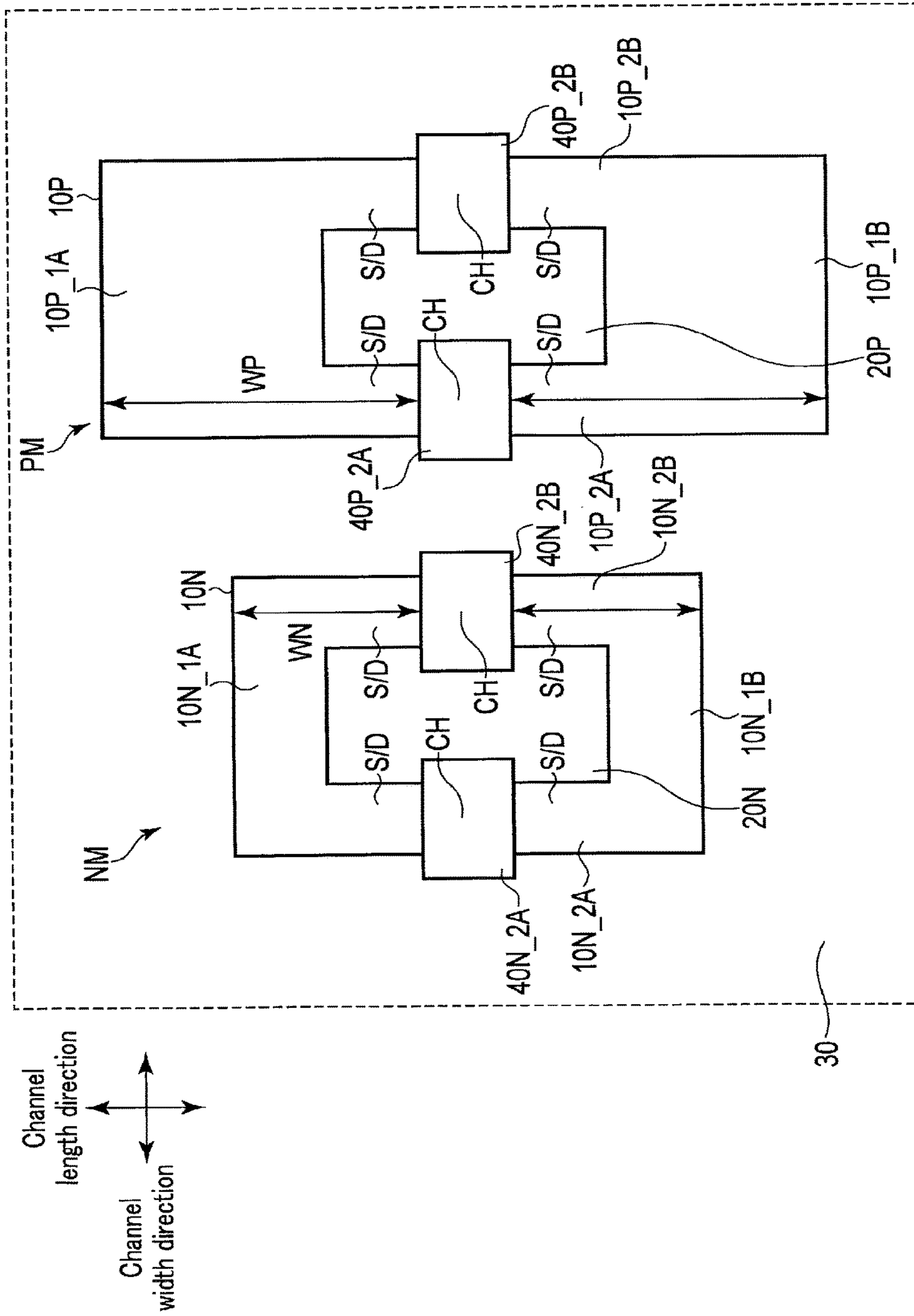
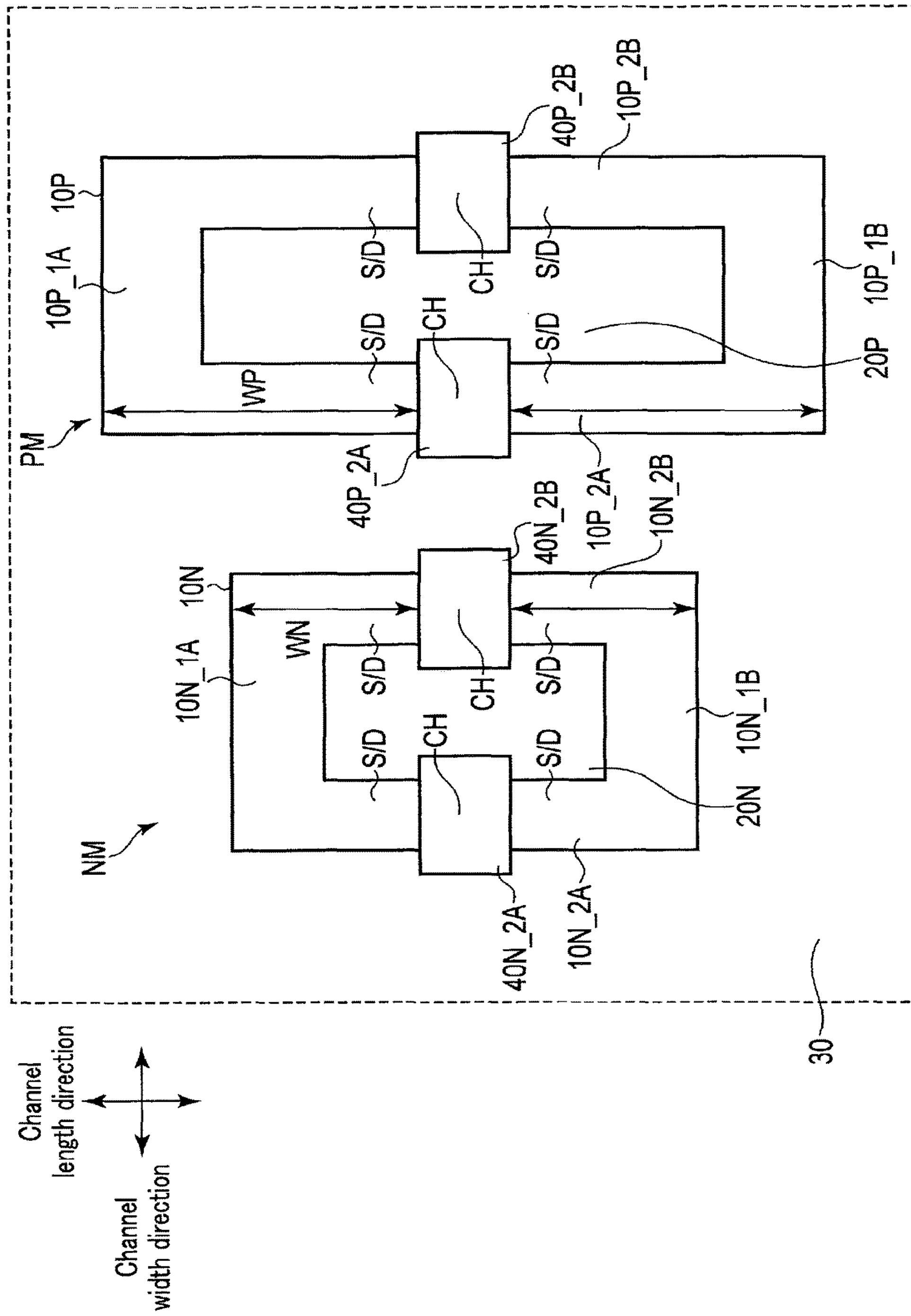


FIG. 11

FIG. 12



F I G. 13



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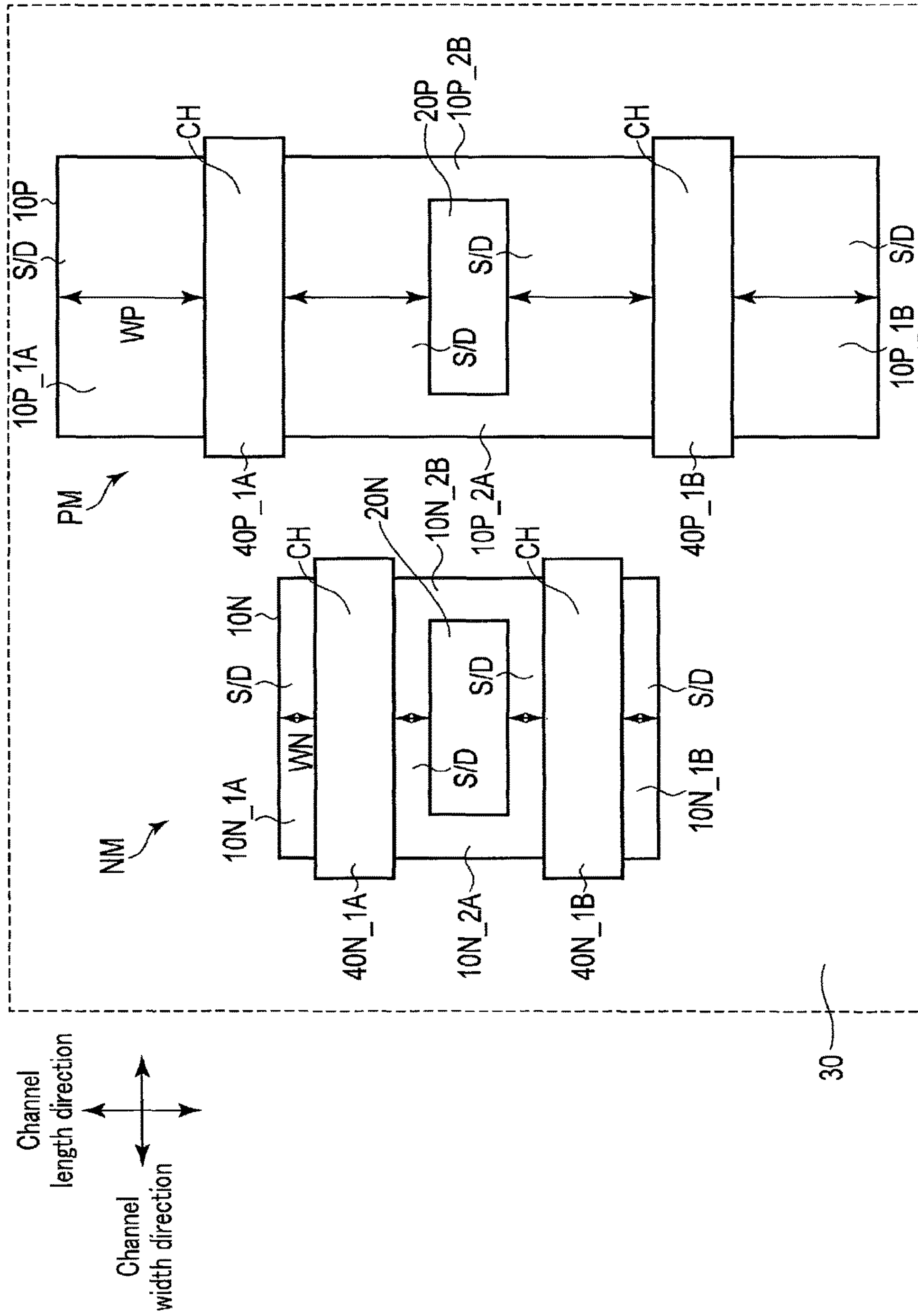

F I G. 15

SEMICONDUCTOR DEVICE

Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue; a claim printed with strikethrough indicates that the claim was canceled, disclaimed, or held invalid by a prior post-patent action or proceeding.

CROSS REFERENCE TO RELATED APPLICATIONS

This application *a Reissue of U.S. Pat. No. 10,043,905, issued Aug. 7, 2018, which* is based upon and claims the benefit of priority from U.S. Provisional Application No. 62/217,357, filed Sep. 11, 2015, the entire contents of all of which are incorporated herein by reference.

FIELD

The present embodiments relate to a semiconductor device.

BACKGROUND

As a technique to improve MOSFET current drivability, a method for applying distortion (stress) to a semiconductor substrate has been proposed. As stress applied to the semiconductor substrate, stress applied from STI (Shallow Trench Isolation) to an active area is known.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a layout diagram of a semiconductor device according to a first embodiment.

FIG. **2** is a cross-sectional view taken along A-A' of FIG. **1**.

FIG. **3** is a layout diagram of a modified example of the semiconductor device according to the first embodiment.

FIG. **4** is a layout diagram of a semiconductor device according to a second embodiment.

FIG. **5** is a layout diagram of a semiconductor device according to a third embodiment.

FIG. **6** is a cross-sectional view taken along B-B' of FIG. **5**.

FIG. **7** is a layout diagram of a modified example of the semiconductor device according to the third embodiment.

FIG. **8** is a layout diagram of a semiconductor device according to a fourth embodiment.

FIG. **9** is a layout diagram of a semiconductor device according to a fifth embodiment.

FIG. **10** is a layout diagram of a semiconductor device according to a sixth embodiment.

FIG. **11** is a cross-sectional view taken along C-C' of FIG. **10**.

FIG. **12** is a layout diagram of a semiconductor device according to a seventh embodiment.

FIG. **13** is a layout diagram of a semiconductor device according to an eighth embodiment.

FIG. **14** is a layout diagram of a modified example of the semiconductor device according to the eighth embodiment.

FIG. **15** is a layout diagram of a semiconductor device according to a ninth embodiment.

DETAILED DESCRIPTION

In general, according to one embodiment, a semiconductor device includes a first element isolating area, a first element area surrounding the first element isolating area, a second element isolating area surrounding the first element area a first gate electrode provided on and across the first element isolating area, the first element area, and the second element isolating area, and a second gate electrode isolated from the first gate electrode and provided on and across the first element isolating area, the first element area, and the second element isolating area.

Hereinafter, the present embodiments will be described with reference to the drawings. In the drawings, identical portions will be applied identical reference symbols.

First Embodiment

In the following, a semiconductor device according to a first embodiment will be explained with reference to FIG. **1** to FIG. **3**.

In the first embodiment, an annular active area **10** is provided in a manner surrounding an element isolating area **20**. By forming a MOS transistor on this active area **10**, a significant stress can be applied on a channel CH of the MOS transistor, thereby, improving mobility of an electric charge in the MOS transistor.

The first embodiment is explained in detail below.

Configuration Example in First Embodiment

FIG. **1** is a layout diagram of the semiconductor device according to the first embodiment. FIG. **2** is a cross-sectional view taken along A-A' of FIG. **1**.

As shown in FIG. **1** and FIG. **2**, the semiconductor device includes an active area (element area) **10**, element isolating areas **20** and **30**, and a gate electrode **40** (**40_2**A, **40_2**B).

The element isolating area **20** is an STI provided in a semiconductor substrate (Si substrate) **100**. The element isolating area **20** includes, for example, SiO_2. The circumference (four sides) of the element isolating area **20** is surrounded by the active area **10**.

The active area **10** is provided on a surface of the semiconductor substrate **100** in a manner which surrounds the circumference of the element isolating area **20**. More specifically, the active area **10** includes regions **10_1**A, **10_1**B, **10_2**A, and **10_2**B. Regions **10_1**A and **10_1**B extend in a channel width direction (horizontal direction of the drawing), and regions **10_2**A and **10_2**B extend in a channel length direction (vertical direction of the drawing). Region **10_2**A connects one end portion of region **10_1**A and one end portion of region **10_1**B, and region **10_2**B connects the other end portion of region **10_1**A and the other end portion of region **10_1**B. In other words, regions **10_1**A, **10_1**B, **10_2**A, and **10_2**B form a rectangular annular shape.

The element isolating area **30** is provided in a manner surrounding the active area **10**. The element isolating area **30** is isolated from the element isolating area **20**.

The gate electrode **40_2**A is provided on and across the element isolating area **30**, the active area **10** (region **10_2**A), and the element isolating area **20**. The gate electrode **40_2**A is orthogonal to the region **10_2**A. A gate insulation film **50** is provided between the gate electrode **40_2**A and the active area **10**. In this manner, a channel CH is formed on the active area **10** under the gate electrode **40_2**A. A source/drain S/D is provided on the active area **10** so as to sandwich this channel CH. In this manner, the gate electrode **40_2**A and the active area **10** form a MOS transistor.

The gate electrode **40_2**B is provided on and across the element isolating area **30**, the active area **10** (region **10_2**B),

and the element isolating area **20**. The gate electrode **40_2**B is orthogonal to the region **10_2**B. The gate electrode **40_2**B is isolated from the gate electrode **40_2**A. The gate insulation film **50** is provided between the gate electrode **40_2**A and the active area **10**. In this manner, the channel is formed on the active area **10** under the gate electrode **40_2**B. The source/drain S/D is provided on the active area **10** so as to sandwich this channel. In this manner, the gate electrode **40_2**B and the active area **10** form a MOS transistor.

In this manner, the active area **10** is in contact with the element isolating area **20**. This causes stress to be applied from the element isolating area **20** to the active area **10**. This stress is applied in a vertical direction with respect to a contact surface between the active area **10** and the element isolating area **20**. In other words, stress is applied to the channel CH in the channel width direction. In the present example, the circumference of the element isolating area **20** is surrounded (closed) by the active area **10**. Therefore, in comparison to the case in which the element isolating area **20** is opened, greater stress is applied to the active area **10**. In the case where the element isolating area **20** includes an expandable material, compressive stress is applied to the active area **10**. In the case where the element isolating area **20** includes a contractible material, tensile stress is applied to the active area **10**.

Although unillustrated, stress is also applied from the element isolating area **30** to the active area **10** in the channel width direction and the channel length direction.

Effect in First Embodiment

According to the first embodiment, the annular active area **10** is provided in a manner surrounding the element isolating area **20**. By closing the circumference of the element isolating area **20** by the annular active area **10**, the stress from the element isolating area **20** to the active area **10** becomes greater. The gate electrode **40** is provided on this active area **10** to form the MOS transistor. In this manner, significant stress may be applied to the channel CH of the MOS transistor, thereby, improving the mobility of an electric charge in the MOS transistor.

In the first embodiment, the gate electrode **40_2**A is provided on region **10_2**A, and the gate electrode **40_2**B is provided on region **10_2**B of the active area **10**. The gate electrode **40_2**A is orthogonal to the region **10_2**A, and the gate electrode **40_2**B is orthogonal to the region **10_2**B. The gate electrode **40_2**A and the gate electrode **40_2**B are provided in an isolated manner from each other, each forming the MOS transistor. In other words, the gate of the MOS transistor is divided into a plurality of nodes. In this manner, a complicated circuit with excellent electric properties may be realized.

Region **10_2**A and region **10_2**B are provided symmetrically. In this manner, the stress from the element isolating area **20** to region **10_2**A and region **10_2**B becomes equal. Therefore, the MOS transistor formed by the gate electrode **40_2**A and the gate electrode **40_2**B may have identical properties.

In the case where the active area **10** has a rectangular shape with a hollow space (STI) in its center as shown in FIG. **1**, strong stress is applied to corners of the active area **10** in the vertical and horizontal directions. Therefore, there is concern that crystal defects may occur. Crystal defects may lead to an increase in junction leakage and a deterioration in transistor properties. As a countermeasure, it is desirable to set the channel surface to (100) plane and the channel length direction to <100> direction in the MOS transistor. Generally, the widely-used <110> direction is more susceptible to defects than the <100> direction in terms of crystal construction. Using the <100> direction, makes it difficult for defects to occur, thereby reducing junction leakage. Furthermore, the <100> direction is more capable of improving current drivability of the transistor than the <110> direction.

Modified Example in First Embodiment

FIG. **3** is a layout diagram of a modified example of the semiconductor device according to the first embodiment.

As shown in FIG. **3**, according to the modified example, the three sides of the element isolating area **20** are surrounded by the active area **10**. The active area **10** includes regions **10_1**A, **10_2**A, and **20_2**B, and surrounds the three sides of the element isolating area **20**. In other words, the element isolating area **20** is opened at one side and is connected to the element isolating area **30**.

In this manner, the active area **10** is in contact with the element isolating area **20**. In the present example, the three sides of the element isolating area **20** are surrounded by the active area **10**. Therefore, in comparison to the case in which the circumference of the element isolating area **20** is opened, greater stress is applied to the active area **10**.

Second Embodiment

In the following, a semiconductor device according to a second embodiment will be explained with reference to FIG. **4**.

The second embodiment is an application example of the first embodiment, in which an annular active area **10** is provided in a manner surrounding a plurality of element isolating areas **20**A to **20**C aligned in a channel width direction. In this manner, significant stress may be applied to both sides of regions **10_2**B and **10_2**C, thereby, improving the mobility of an electric charge in a MOS transistor.

The second embodiment is explained in detail below. In the second embodiment, explanations on the matters which are the same as in the first embodiment are omitted, and mainly those matters which are different are explained.

Configuration Example in Second Embodiment

FIG. **4** is a layout diagram of the semiconductor device according to the second embodiment.

As shown in FIG. **4**, the semiconductor device includes an active area **10**, element isolating areas **20**A, **20**B, **20**C, and **30**, and a gate electrode **40** (**40_2**A, **40_2**B, **40_2**C, **40_2**D).

The circumference (four sides) of the element isolating areas **20**A, **20**B, and **20**C is surrounded by the active area **10**. The element isolating areas **20**A, **20**B, and **20**C are aligned along the channel width direction. The element isolating areas **20**A, **20**B, and **20**C are isolated from each other.

The active area **10** is provided in a manner surrounding the element isolating areas **20**A, **20**B, and **20**C. More specifically, the active area **10** includes regions **10_1**A, **10_1**B, **10_2**A, **10_2**B, **10_2**C, and **10_2**D. Regions **10_1**A and **10_1**B extend in a channel width direction (horizontal direction of the drawing), and regions **10_2**A, **10_2**B, **10_2**C, and **10_2**D extend in a channel length direction (vertical direction of the drawing). Regions **10_2**A, **10_2**B, **10_2**C, and **10_2**D are aligned along the channel width direction. Region **10_2**A connects one end portion of region **10_1**A and one end portion of region **10_1**B. Regions **10_23** and **10_2**C connect a part of region **10_1**A and a part of

region **10_1**B. Region **10_2**D connects the other end portion of region **10_1**A and the other end portion of region **10_1**B. In other words, regions **10_1**A, **10_1**B, **10_2**A, **10_2**B, **10_2**C, and **10_2**D form a ladder shape.

The element isolating area **20**A is surrounded by regions **10_1**A, **10_1**B, **10_2**A, and **10_2**B, the element isolating area **20**B is surrounded by regions **10_1**A, **10_1**B, **10_2**B, and **10_2**C, and the element isolating area **20**C is surrounded by regions **10_1**A, **10_1**B, **10_2**C, and **10_2**D.

The element isolating area **30** is provided in a manner surrounding the active area **10**. The element isolating area **30** is isolated from the element isolating areas **20**A, **20**B, and **20**C.

The gate electrode **40_2**A is provided on and across the element isolating area **30**, the active area **10_2**A, and the element isolating area **20**A. The gate electrode **40_2**A is orthogonal to the region **10_2**A. In this manner, the channel CH is formed on the active area **10** under the gate electrode **40_2**A. A source/drain S/D is provided on the active area **10** so as to sandwich this channel CH. In this manner, the gate electrode **40_2**A and the active area **10** form the MOS transistor.

The gate electrode **40_2**B is provided on and across the element isolating area **20**A, the active area **10_2**B, and the element isolating area **20**B. The gate electrode **40_2**B is orthogonal to the region **10_2**B. In this manner, the channel CH is formed on the active area **10** under the gate electrode **40_2**B. A source/drain S/D is provided on the active area **10** so as to sandwich this channel CH. In this manner, the gate electrode **40_2**B and the active area **10** form the MOS transistor.

The gate electrode **40_2**C is provided on and across the element isolating area **20**B, the active area **10_2**C, and the element isolating area **20**C. The gate electrode **40_2**C is orthogonal to the region **10_2**C. In this manner, the channel CH is formed on the active area **10** under the gate electrode **40_2**C. A source/drain S/D is provided on the active area **10** so as to sandwich this channel CH. In this manner, the gate electrode **40_2**C and the active area **10** form the MOS transistor.

The gate electrode **40_2**D is provided on and across the element isolating area **20**C, the active area **10_2**D, and the element isolating area **30**. The gate electrode **40_2**D is orthogonal to the region **10_2**D. In this manner, the channel CH is formed on the active area **10** under the gate electrode **40_2**D. A source/drain S/D is provided on the active area **10** so as to sandwich this channel CH. In this manner, the gate electrode **40_2**D and the active area **10** form the MOS transistor.

In the above manner, in the active area **10**, region **10_2**B is in contact with the element isolating area **20**A at one side, and the element isolating area **20**B at the other side. The circumference of the element isolating areas **20**A and **20**B is surrounded (enclosed) by the active area **10**. Therefore, significant stress is applied to both sides of region **10_2**B by the element isolating areas **20**A and **20**B. In the same manner, significant stress is applied to both sides of region **10_2**C by the element isolating areas **20**B and **20**C.

Meanwhile, significant stress is applied to one side of region **10_2**Aby the element isolating area **20**A. In the same manner, significant stress is applied on one side of region **10_2**D by the element isolating area **20**C.

Effect in Second Embodiment

According to the second embodiment, the annular active area **10** is provided in a manner surrounding a plurality of element isolating areas **20**A to **20**C. In this manner, one of the closed element isolating areas **20**A to **20**C is arranged on both sides of regions **10_23** and **10_2**C in the active area **10**. In this manner, significant stress can be applied to both sides of regions **10_2**B and **10_2**C. Therefore, greater stress can be applied to the channel CH of the MOS transistor than in the case of the first embodiment, thereby improving the mobility of an electric charge in the MOS transistor.

Meanwhile, significant stress is applied to one side of region **10_2**Aby the element isolating area **20**A. In the same manner, significant stress is applied on one side of region **10_2**D by the element isolating area **20**C. In other words, the applied stress is different between regions **10_2**A and **10_2**D and regions **10_2**B and **10_2**C. Therefore, the properties differ between the MOS transistors provided on regions **10_2**A and **10_2**D and the MOS transistors provided on regions **10_2**B and **10_2**C. Accordingly, in the case where the difference in the properties of the MOS transistors becomes a problem, the MOS transistors provided on regions **10_2**A and **10_2**D may be considered as dummy transistors.

Third Embodiment

In the following, a semiconductor device according to a third embodiment will be explained with reference to FIG. **5** to FIG. **7**.

In the third embodiment, a gate electrode **40_1**A is provided on region **10_1**A, and a gate electrode **40_1**B is provided on region **10_1**B in an active area **10**. The gate electrode **40_1**A is parallel to region **10_1**A, and the gate electrode **40_1**B is parallel to region **10_1**B. In this manner, significant stress may be applied to a channel CH of an MOS transistor in a channel length direction. By controlling the direction of stress as appropriate in the manner set forth in the present example, electric charge mobility with respect to various MOS transistors may be improved.

The third embodiment is explained in detail below. In the third embodiment, explanations on the matters which are the same as in the first embodiment are omitted, and mainly those matters which are different are explained.

Configuration Example in Third Embodiment

FIG. **5** is a layout diagram of the semiconductor device according to the third embodiment. FIG. **6** is a cross-sectional view taken along B-B' of FIG. **5**.

As shown in FIG. **5** and FIG. **6**, the semiconductor device includes an active area (element area) **10**, element isolating areas **20** and **30**, and a gate electrode **40** (**40_21**A, **40_1**B).

The gate electrode **40_1**A is provided on and across the element isolating area **30**, the active area **10** (region **10_1**A), and the element isolating area **30**. The gate electrode **40_1**A is parallel to region **10_1**A. A gate insulation film **50** is provided between the gate electrode **40_1**A and the active area **10**. In this manner, the channel CH is formed on the active area **10** under the gate electrode **40_1**A. A source/drain S/D is provided on the active area **10** so as to sandwich this channel CH. In this manner, the gate electrode **40_1**A and the active area **10** form the MOS transistor.

The gate electrode **40_1**B is provided on and across the element isolating area **30**, the active area **10** (region **10_1**B), and the element isolating area **30**. The gate electrode **40_1**B is parallel to region **10_1**B. The gate insulation film **50** is provided between the gate electrode **40_1**B and the active area **10**. In this manner, the channel CH is formed on the active area **10** under the gate electrode **40_1**B. A source/

drain S/D is provided on the active area **10** so as to sandwich this channel CH. In this manner, the gate electrode **40_1**B and the active area **10** form the MOS transistor.

In this manner, the active area **10** is in contact with the element isolating area **20**. This causes stress to be applied from the element isolating area **20** to the active area **10**. This stress is applied in a vertical direction with respect to a contact surface between the active area **10** and the element isolating area **20**. In other words, stress is applied in the channel length direction with respect to the channel CH.

Although unillustrated, stress is also applied from the element isolating area **30** to the active area **10** in the channel width direction and the channel length direction.

Effect in Third Embodiment

In the third embodiment, the gate electrode **40_1**A is provided on region **10_1**A, and the gate electrode **40_1**B is provided on region **10_1**B in the active area **10**. The gate electrode **40_1**A is parallel to region **10_1**A, and the gate electrode **40_1**B is parallel to region **10_1**B. In this manner, significant stress can be applied to a channel CH of a MOS transistor in a channel length direction. In other words, stress may be applied in a direction different from that of the first embodiment. In the MOS transistor, the stress direction for improving electric charge mobility is different depending on the condition of, such as, material. By controlling the direction of stress as appropriate in the manner set forth in the present example, electric charge mobility with respect to various MOS transistors can be improved.

Modified Example in Third Embodiment

FIG. **7** is a layout diagram of a modified example of the semiconductor device according to the third embodiment.

As shown in FIG. **7**, according to the modified example, the three sides of the element isolating area **20** are surrounded by the active area **10**. The active area **10** includes regions **10_1**A, **10_1**B, and **10_2**A, and surrounds the three sides of the element isolating area **20**. In other words, the element isolating area **20** is connected to the element isolating area **30** at one side.

In this manner, the active area **10** is in contact with the element isolating area **20**. In the present example, the three sides of the element isolating area **20** are surrounded by the active area **10**. Therefore, in comparison to the case in which the circumference of the element isolating area **20** is opened, greater stress is applied to the active area **10**.

Fourth Embodiment

In the following, a semiconductor device according to a fourth embodiment will be explained with reference to FIG. **8**.

The fourth embodiment is an application example of the third embodiment, in which the second embodiment is applied to the third embodiment. In the fourth embodiment, an annular active area **10** is provided in a manner surrounding a plurality of element isolating areas **20**D to **20**F aligned in a channel length direction. In this manner, significant stress may be applied to both sides of regions **10_1**B and **10_1**C, thereby improving the mobility of an electric charge in an MOS transistor.

The fourth embodiment is explained in detail below. In the fourth embodiment, explanations on the matters which are the same as in the third embodiment are omitted, and mainly those matters which are different are explained.

Configuration Example in Fourth Embodiment

FIG. **8** is a layout diagram of the semiconductor device according to the fourth embodiment.

As shown in FIG. **8**, the semiconductor device includes an active area **10**, element isolating areas **20**D, **20**E, **20**F, and **30**, and a gate electrode **40** (**40_1**A, **40_1**B, **40_1**C, **40_1**D).

The circumference (four sides) of the element isolating areas **20**D, **20**E, and **20**F is surrounded by the active area **10**. The element isolating areas **20**D, **20**E, and **20**F are aligned along the channel length direction. The element isolating areas **20**D, **20**E, and **20**F are isolated from each other.

The active area **10** is provided in a manner surrounding the element isolating areas **20**D, **20**E, and **20**F. More specifically, the active area **10** includes regions **10_1**A, **10_1**B, **10_1**C, and **10_1**D, **10_2**A, and **10_2**B. Regions **10_1**A, **10_1**B, **10_1**C, and **10_1**D extend in a channel width direction (horizontal direction of the drawing), and regions **10_2**A and **10_2**B extend in the channel length direction (vertical direction of the drawing). Regions **10_1**A, **10_1**B, **10_1**C, and **10_1**D are aligned along the channel width direction. Region **10_1**A connects one end portion of region **10_2**A and one end portion of region **10_2**B. Regions **10_1**B and **10_1**C connect a part of region **10_2**A and a part of region **10_2**B. Region **10_1**D connects the other end portion of region **10_2**A and the other end portion of region **10_2**B. In other words, regions **10_1**A, **10_1**B, **10_1**C, **10_1**D, **10_2**A, and **10_2**B form a ladder shape.

The element isolating area **20**D is surrounded by regions **10_1**A, **10_1**B, **10_2**A, and **10_2**B, the element isolating area **20**E is surrounded by regions **10_1**B, **10_1**C, **10_2**A, and **10_2**B, and the element isolating area **20**F is surrounded by regions **10_1**C, **10_1**D, **10_2**A, and **10_2**B.

The gate electrode **40_1**A is provided on and across the element isolating area **30**, the active area **10_2**A, and the element isolating area **30**. The gate electrode **40_1**A is parallel to region **10_1**A. In this manner, a channel CH is formed on the active area **10** under the gate electrode **40_1**A. A source/drain S/D is provided on the active area **10** so as to sandwich this channel CH. In this manner, the gate electrode **40_1**A and the active area **10** form the MOS transistor.

The gate electrode **40_1**B is provided on and across the element isolating area **30**, the active area **10_1**B, and the element isolating area **30**. The gate electrode **40_1**B is parallel to region **10_1**B. In this manner, the channel CH is formed on the active area **10** under the gate electrode **40_1**B. A source/drain S/D is provided on the active area **10** so as to sandwich this channel CH. In this manner, the gate electrode **40_1**B and the active area **10** form the MOS transistor.

The gate electrode **40_1**C is provided on and across the element isolating area **30**, the active area **10_1**C, and the element isolating area **30**. The gate electrode **40_1**C is parallel to region **10_1**C. In this manner, the channel CH is formed on the active area **10** under the gate electrode **40_1**C. A source/drain S/D is provided on the active area **10** so as to sandwich this channel CH. In this manner, the gate electrode **40_1**C and the active area **10** form the MOS transistor.

The gate electrode **40_1**D is provided on and across the element isolating area **30**, the active area **10_1**D, and the element isolating area **30**. The gate electrode **40_1**D is parallel to region **10_1**D. In this manner, the channel CH is

formed on the active area **10** under the gate electrode **40_1**D. A source/drain S/D is provided on the active area **10** so as to sandwich this channel CH. In this manner, the gate electrode **40_1**D and the active area **10** form the MOS transistor.

In this manner, in the active area **10**, region **10_1**B is in contact with the element isolating area **20**D at one side, and in contact with the element isolating area **20**E at the other side. The circumference of the element isolating areas **20**D and **20**E is surrounded (closed) by the active area **10**. Therefore, significant stress is applied to both sides of region **10_1**B by the element isolating areas **20**D and **20**E. In the same manner, significant stress is applied to both sides of region **10_1**C by the element isolating areas **20**E and **20**F.

Meanwhile, significant stress is applied to one side of region **10_1**A by the element isolating area **20**D. In the same manner, significant stress is applied to one side of region **10_1**D by the element isolating area **20**F.

Effect in Fourth Embodiment

In the fourth embodiment, the annular active area **10** is provided in a manner surrounding a plurality of element isolating areas **20**D to **20**F aligned in the channel length direction. In this manner, one of the closed element isolating areas **20**D to **20**F is arranged on both sides of regions **10_1**B and **10_1**C in the active area **10**. In this manner, significant stress may be applied to both sides of regions **10_1**B and **10_1**C. Therefore, greater stress may be applied to the channel CH of the MOS transistor than in the case of the third embodiment, thereby improving the mobility of an electric charge in the MOS transistor.

Meanwhile, significant stress is applied to one side of region **10_1**A by the element isolating area **20**D. In the same manner, significant stress is applied to one side of region **10_1**D by the element isolating area **20**F. In other words, the applied stress is different between regions **10_1**A and **10_1**D and regions **10_1**B and **10_1**C. Therefore, the properties differ between the MOS transistor provided on regions **10_1**A and **10_1**D and the MOS transistor provided on regions **10_1**B and **10_1**C. Accordingly, in the case where the difference in the properties of the MOS transistors become a problem, the MOS transistor provided on regions **10_1**A and **10_1**D may be considered as a dummy transistor.

Fifth Embodiment

In the following, a semiconductor device according to a fifth embodiment will be explained with reference to FIG. **9**.

The fifth embodiment is a combination of the second embodiment and the fourth embodiment. The fifth embodiment is capable of producing the same effects as the second and the fourth embodiments.

The fifth embodiment is explained in detail below. In the fifth embodiment, explanations on the matters which are the same as in the second and the fourth embodiments are omitted, and mainly those matters which are different are explained.

Configuration Example in Fifth Embodiment

FIG. **9** is a layout diagram of the semiconductor device according to the fifth embodiment.

As shown in FIG. **9**, the semiconductor device includes an active area **10**, element isolating areas **20**A, **20**B, **20**C, **20**D, **20**E, **20**F, and **30**, and a gate electrode **40** (**40_2**A, **40_2**B, **40_2**C, **40_2**D, **40_1**B, **40_1**C, **40_1**D, and **40_1**E).

The circumference (four sides) of the element isolating areas **20**A, **20**B, **20**C, **20**D, **20**E, and **20**F is surrounded by the active area **10**. The element isolating areas **20**A, **20**B, and **20**C are aligned along a channel width direction. The element isolating areas **20**D, **20**E, and **20**F are aligned along a channel length direction. The element isolating areas **20**A, **20**B, **20**C, **20**D, **20**E, and **20**F are isolated from each other.

The active area **10** is provided in a manner surrounding the element isolating areas **20**A, **20**B, **20**C, **20**D, **20**E, and **20**F. More specifically, the active area **10** includes regions **10_1**A, **10_1**B, **10_1**C, **10_1**D, **10_1**E, **10_2**A, **10_2**B, **10_2**C, and **10_2**D. Regions **10_1**A, **10_1**B, **10_1**C, **10_1**D, and **10_1**E extend in the channel width direction (horizontal direction of the drawing), and regions **10_2**A, **10_2**B, **10_2**C, and **10_2**D extend in the channel length direction (vertical direction of the drawing).

Regions **10_1**A, **10_1**B, **10_1**C, **10_1**D, and **10_1**E are aligned along the channel length direction. Region **10_1**A connects one end portion of region **10_2**A and one end portion of region **10_2**D. Regions **10_1**B, **10_1**C, and **10_1**D connect a part of region **10_2**A and a part of region **10_2**D. Region **10_1**E connects the other end portion of region **10_2**A and the other end portion of region **10_2**D.

Meanwhile, regions **10_2**A, **10_2**B, **10_2**C, and **10_2**D are aligned along the channel width direction. Region **10_2**A connects one end portion of region **10_1**A and one end portion of region **10_1**E. Regions **10_2**B and **10_2**C connect a part of region **10_1**A and a part of region **10_1**B. Region **10_2**D connects the other end portion of region **10_1**A and the other end portion of region **10_1**E.

The element isolating area **20**A is surrounded by regions **10_1**A, **10_1**B, **10_2**A, and **10_2**B, the element isolating area **20**B is surrounded by regions **10_1**A, **10_1**B, **10_2**B, and **10_2**C, and the element isolating area **20**C is surrounded by regions **10_1**A, **10_1**B, **10_2**C, and **10_2**D. The element isolating area **20**D is surrounded by regions **10_2**A, **10_2**D, **10_1**B, and **10_1**C, the element isolating area **20**E is surrounded by regions **10_2**A, **10_2**D, **10_1**C, and **10_1**D, and the element isolating area **20**F is surrounded by regions **10_2**A, **10_2**D, **10_1**D, and **10_1**E.

The gate electrode **40_2**A is provided on and across the element isolating area **30**, the active area **10_2**A, and the element isolating area **20**A. The gate electrode **40_2**A is orthogonal to the region **10_2**A. The gate electrode **40_2**B is provided on and across the element isolating area **20**A, the active area **10_2**B, and the element isolating area **20**B. The gate electrode **40_2**B is orthogonal to the region **10_2**B. The gate electrode **40_2**C is provided on and across the element isolating area **20**B, the active area **10_2**C, and the element isolating area **20**C. The gate electrode **40_2**C is orthogonal to the region **10_2**C. The gate electrode **40_2**D is provided on and across the element isolating area **20**C, the active area **10_2**D, and the element isolating area **30**. The gate electrode **40_2**D is orthogonal to the region **10_2**D.

The gate electrode **40_1**B is provided on and across the element isolating area **30**, the active area **10_1**B, and the element isolating area **30**. The gate electrode **40_1**B is parallel to region **10_1**B. The gate electrode **40_1**C is provided on and across the element isolating area **30**, the active area **10_1**C, and the element isolating area **30**. The gate electrode **40_1**C is parallel to region **10_1**C. The gate electrode **40_1**D is provided on and across the element isolating area **30**, the active area **10_1**D, and the element isolating area **30**. The gate electrode **40_1**D is parallel to region **10_1**D. The gate electrode **40_1**E is provided on and

across the element isolating area **30**, the active area **10_1**E, and the element isolating area **30**. The gate electrode **40_1**E is parallel to region **10_1**E.

Effect in Fifth Embodiment

In the fifth embodiment, the annular active area **10** is provided in a manner surrounding a plurality of element isolating areas **20**A to **20**C aligned in the channel length direction, and a plurality of element isolating areas **20**D to **20**F aligned in the channel width direction. In this manner, the fifth embodiment is capable of producing the same effects as the second and the fourth embodiments.

Sixth Embodiment

In the following, a semiconductor device according to a sixth embodiment will be explained with reference to FIG. **10** and FIG. **11**.

The sixth embodiment is an application example of the first embodiment, in which the circumference of the element isolating area **30** is surrounded by an active area **70**. In this manner, significant stress may be applied to both sides of regions **10_2**A and **10_2**B by element isolating areas **20** and **30**, thereby improving the mobility of an electric charge in an MOS transistor.

The sixth embodiment is explained in detail below. In the sixth embodiment, explanations on the matters which are the same as in the first embodiment are omitted, and mainly those matters which are different are explained.

Configuration Example in Sixth Embodiment

FIG. **10** is a layout diagram of the semiconductor device according to the sixth embodiment. FIG. **11** is a cross-sectional view taken along C-C' of FIG. **10**.

As shown in FIG. **10** and FIG. **11**, the semiconductor device includes active areas **10** and **70**, element isolating areas **20**, **30**, and **60**, and a gate electrode **40** (**40_2**A, **40_2**B).

The active area **70** is provided in a manner surrounding the element isolating area **30**. The active area **70** is isolated from the active area **10**. The active area **70** is electrically connected to a wiring layer **90** via a contact **80**. In this manner, the active area **70** supplies substrate voltage to a well **200** from the wiring layer **90**.

The element isolating area **60** is provided in a manner surrounding the active area **70**. The element isolating area **60** is isolated from the element isolating area **30**.

In this manner, regions **10_2**A and **10_2**B in the active area **10** are in contact with the element isolating area **20** at one side, and in contact with the element isolating area **30** at the other side. The circumference of the element isolating area **20** is surrounded by the active area **10**, and the circumference of the element isolating area **30** is surrounded by the active area **70**. Therefore, significant stress is applied to both sides of regions **10_2**A and **10_2**B by the element isolating areas **20** and **30**.

Effect in Sixth Embodiment

In the sixth embodiment, the circumference of the element isolating area **30** is surrounded by the active area **70**. In this manner, significant stress may be applied to both sides of regions **10_2**A and **10_2**B in the channel width direction by element isolating areas **20** and **30**. Therefore, greater stress can be applied to the channel CH of the MOS transistor in the channel width direction than in the case of the first embodiment, thereby, improving the mobility of an electric charge in the MOS transistor.

In the sixth embodiment, substrate voltage is supplied to the active area **70** from the wiring layer **90** via the contact **80**. In other words, by using the active area **70** as a substrate terminal, the substrate voltage can be supplied to the well **200**.

Seventh Embodiment

In the following, a semiconductor device according to a seventh embodiment will be explained with reference to FIG. **12**.

The seventh embodiment is an application example of the third embodiment, in which the sixth embodiment is applied to the third embodiment. In this manner, greater stress may be applied to the channel CH of the MOS transistor in the channel length direction than in the case of the third embodiment, thereby, improving the mobility of an electric charge in the MOS transistor.

The seventh embodiment is explained in detail below. In the seventh embodiment, explanations on the matters which are the same as in the third embodiment are omitted, and mainly those matters which are different are explained.

Configuration Example in Seventh Embodiment

FIG. **12** is a layout diagram of the semiconductor device according to the seventh embodiment.

As shown in FIG. **12**, the semiconductor device includes active areas **10** and **70**, element isolating areas **20**, **30**, and **60**, and a gate electrode **40** (**40_1**A, **40_1**B).

The active area **70** is provided in a manner surrounding the element isolating area **30**. The active area **70** is isolated from the active area **10**. In the same manner as FIG. **11** in the sixth embodiment, the active area **70** is electrically connected electrically to a wiring layer **90** via a contact **80**. In this manner, the active area **70** supplies substrate voltage to a well **200** from the wiring layer **90**.

The element isolating area **60** is provided in a manner surrounding the active area **70**. The element isolating area **60** is isolated from the element isolating area **30**.

In this manner, regions **10_1**A and **10_1**B in the active area **10** are in contact with the element isolating area **20** at one side, and in contact with the element isolating area **30** at the other side. The circumference of the element isolating area **20** is surrounded by the active area **10**, and the circumference of the element isolating area **30** is surrounded by the active area **70**. Therefore, significant stress is applied to both sides of regions **10_1**A and **10_1**B by the element isolating areas **20** and **30**.

Effect in Seventh Embodiment

In the seventh embodiment, the circumference of the element isolating area **30** is surrounded by the active area **70**. In this manner, significant stress can be applied to both sides of regions **10_1**A and **10_1**B by the element isolating areas **20** and **30**. Therefore, greater stress can be applied to the channel CH of the MOS transistor than in the case of the third embodiment, thereby improving the mobility of an electric charge in the MOS transistor.

Eighth Embodiment

In the following, a semiconductor device according to an eighth embodiment will be explained with reference to FIG. **13** and FIG. **14**.

The eighth embodiment is an application example of the first embodiment, in which an NMOS region NM and a PMOS region PM are provided. A dimension WN of a source/drain S/D of an NMOS transistor in the NMOS region NM and a dimension WP of a source/drain S/D of a PMOS transistor in the PMOS region PM are different. This allows the effect of stress to each transistor to be adjusted.

The eighth embodiment is explained in detail below. In the eighth embodiment, explanations on the matters which are the same as in the first embodiment are omitted, and mainly those matters which are different are explained.

Configuration Example in Eighth Embodiment

FIG. **13** is a layout diagram of the semiconductor device according to the eighth embodiment. FIG. **14** is a layout diagram of a modified example of the semiconductor device according to the eighth embodiment.

As shown in FIG. **13**, the semiconductor device includes an NMOS region NM and a PMOS region PM.

The NMOS region NM includes an active area (element area) **10**N (**10**N_1A, **10**N_1B, **10**N_2A, **10**N_2B), an element isolating area **20**N, and gate electrodes **40**N_2A and **40**N_2B. The PMOS region PM includes an active area (element area) **10**P (**10**P_1A, **10**P_1B, **10**P_2A, **10**P_2B), an element isolating area **20**P, and gate electrodes **40**P_2A and **40**P_2B.

Each of the NMOS region NM and the PMOS region PM in the eighth embodiment has the same configuration as in the first embodiment. In the NMOS region NM, the active area **10**N and the gate electrode **40**N form the NMOS transistor, and in the PMOS region PM, the active area **10**P and the gate electrode **40**P form the PMOS transistor.

Here, the dimension WN of the source/drain S/D of the NMOS transistor in a channel length direction in the NMOS region NM is smaller than the dimension WP of the source/drain S/D of the PMOS transistor in a channel length direction in the PMOS region PM. In other words, the distance from the channel CH of the NMOS transistor to the element isolating area **30** in the channel length direction is shorter than the distance from the channel CH of the PMOS transistor to the element isolating area **30** in the channel length direction. Therefore, the stress applied to the channel CH of the NMOS transistor in the channel length direction is greater than the stress applied to the channel CH of the PMOS transistor in the channel length direction

Effect in Eighth Embodiment

In some cases, the stress from the element isolating area **30** to the channel CH of the MOS transistor may improve mobility, however, may also degrade mobility. Even the stress in the same direction may, in some cases, for example, improve mobility for the NMOS transistor, however, mobility for the PMOS transistor may degrade. Therefore, a case in which stress is applied only to the NMOS transistor, not to the PMOS transistor, would become necessary.

To deal with this, the eighth embodiment is provided with the NMOS region NM and the PMOS region PM. The dimension WN of the source/drain S/D of the NMOS transistor in the NMOS region NM and the dimension WP of the source/drain S/D of the PMOS transistor in the PMOS region PM are different. For example, in the case where the stress from the element isolating area **30** causes favorable effects to the NMOS transistor, however, negative effects to the PMOS transistor, the dimension WP of the source/drain S/D of the PMOS transistor is made greater than the dimension WN of the source/drain S/D of the NMOS transistor. In this manner, the effect of stress to the channel CH from the element isolating area **30** in the channel length direction is lessened for the PMOS transistor than for the NMOS transistor. In other words, the effect of stress is used only for the NMOS transistor, and is lessened for the PMOS transistor. In this manner, by adjusting the effect of stress, it is possible to provide favorable effects caused by stress to the NMOS transistor and to avoid providing negative effects caused by stress to the PMOS transistor.

In the present example, the case in which the stress from the element isolating area **30** provides favorable effects to the NMOS transistor and negative effects to the PMOS transistor has been explained. However, the case is not limited to this. For example, in the case where the stress from the element isolating area **30** causes favorable effects to the PMOS transistor and negative effects to the NMOS transistor, the dimension WP of the source/drain S/D of the PMOS transistor may be made smaller than the dimension WN of the source/drain S/D of the NMOS transistor.

As shown in FIG. **13**, the dimension of an element isolating area **20**P in the channel length direction in the PMOS region PM may be equivalent to the dimension of an element isolating area **20**N in the channel length direction in the NMOS region NM, or may be different, as shown in FIG. **14**.

Ninth Embodiment

In the following, a semiconductor device according to a ninth embodiment will be explained with reference to FIG. **15**.

The ninth embodiment is an example of applying the eighth embodiment to the third embodiment.

The ninth embodiment is explained in detail below.

Configuration Example in Ninth Embodiment

FIG. **15** is a layout diagram of the semiconductor device according to the ninth embodiment.

As shown in FIG. **15**, the semiconductor device includes the NMOS region NM and the PMOS region PM.

The NMOS region NM includes an active area (element area) **10**N (**10**N_1A, **10**N_1B, **10**N_2A, **10**N_2B), an element isolating area **20**N, and gate electrodes **40**N_1A and **40**N_1B. The PMOS region PM includes an active area (element area) **10**P (**10**P_1A, **10**P_1B, **10**P_2A, **10**P_2B), an element isolating area **20**P, and gate electrodes **40**P_1A and **40**P_1B.

The NMOS region NM and the PMOS region PM in the ninth embodiment have the same configuration as in the third embodiment. In the NMOS region NM, the active area **10**N and the gate electrode **40**N form an NMOS transistor, and in the PMOS region PM, the active area **10**P and the gate electrode **40**P form a PMOS transistor.

Here, the dimension WN of the source/drain S/D of the NMOS transistor in the NMOS region NM in a channel length direction is smaller than the dimension WP of the source/drain S/D of the PMOS transistor in the PMOS region PM in a channel length direction. In other words, the distance from the channel CH of the NMOS transistor to the element isolating area **30** in the channel length direction is shorter than the distance from the channel CH of the PMOS transistor to the element isolating area **30** in the channel length direction. Therefore, the stress applied to the channel CH of the NMOS transistor in the channel length direction

is greater than the stress applied to the channel CH of the PMOS transistor in the channel length direction.

Effect in Ninth Embodiment

The ninth embodiment is provided with the NMOS region NM and the PMOS region PM. The dimension WN of the source/drain S/D of the NMOS transistor in the NMOS region NM and the dimension WP of the source/drain S/D of the PMOS transistor in the PMOS region PM are different. This allows the effect of stress from the element isolating areas **20** and **30** to each transistor to be adjusted.

While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the novel methods and systems described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the methods and systems described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the inventions.

What is claimed is:

1. A semiconductor device comprising:

a first element isolating area;

a first element area surrounding all sides of the first element isolating area, and including first to fourth regions, the first and second regions extending in a first direction, the third and fourth regions extending in a second direction different from the first direction, the first region being connected to one end portion of the third region and one end portion of the fourth region, the second region being connected to the other end portion of the third region and the other end portion of the fourth region;

a second element isolating area surrounding all sides of the first element area;

a first gate electrode provided on and across the first element isolating area, the first region, and the second element isolating area;

a second gate electrode isolated from the first gate electrode and provided on and across the first element isolating area, the second region, and the second element isolating area;

a first gate insulation film provided between the first region and the first gate electrode;

a second gate insulation film provided between the second region and the second gate electrode;

a third element isolating area;

a second element area surrounding all sides of the third element isolating area, all sides of the second element area surrounded by the second element isolating area;

a third gate electrode provided on and across the third element isolating area, the second element area, and the second element isolating area; and

a fourth gate electrode isolated from the third gate electrode and provided on and across the third element isolating area, the second element area, and the second element isolating area, wherein

the first gate electrode and the first element area forms a first transistor,

the second gate electrode and the first element area forms a second transistor, the first element area forms a rectangular annular shape,

the second element area forms a rectangular annular shape,

a transistor of a first conductive-type is formed by the first gate electrode and the first element area, and a transistor of a second conductive-type which is different from the first conductive-type is formed by the third gate electrode and the second element area, and

the first element area and the second element area are different from each other in outer dimension in the first direction.

2. The device of claim **1**, wherein the first gate electrode and the second gate electrode are aligned in a channel width direction.

3. The device of claim **1**, further comprising:

a first channel region provided under the first gate electrode and in the first element area;

a first source/drain region provided in the first element area in a manner sandwiching the first channel region;

a second channel region provided under the third gate electrode and in the second element area; and

a second source/drain region provided in the second element area in a manner sandwiching the second channel region,

wherein a dimension of the first source/drain region is smaller than a dimension of the second source/drain region.

4. The device of claim **1**, wherein the third region and the fourth region are provided symmetrically.

5. The device of claim **1**, wherein

a channel surface of the first and second transistor is set to (100) plane, and

a channel length direction of the first and second transistor is set to <100> direction.

6. The device of claim **1**, wherein

no control gate electrode is provided above the first gate electrode and the second gate electrode.

7. The device of claim **1**, wherein

no control gate electrode is provided above a drain of the first transistor, a source of the first transistor, a drain of the second transistor and a source of the second transistor.

8. The device of claim **1**, wherein

the first direction is a channel length direction of the first and second transistors.

9. The device of claim **8**, wherein

the first element area and the second element area are equal to each other in inner dimension in the first direction.

10. The device of claim **8**, wherein

the first element area and the second element area are different from each other in inner dimension in the first direction.

11. The device of claim **1**, wherein

the first and second element areas have outer and inner dimensions designed to adjust stress from the first and second element isolating areas to the first transistor and stress from the second and third element isolating areas to the second transistor.

12. A semiconductor device comprising:

a first element isolating area;

a first element area surrounding sides of the first element isolating area, and including first to fourth regions, the first and second regions extending in a first direction, the third and fourth regions extending in a second direction different from the first direction, the first region being connected to one end portion of the third region and one end portion of the fourth region, the

second region being connected to the other end portion of the third region and the other end portion of the fourth region;

a second element isolating area surrounding sides of the first element area;

a first gate electrode provided on and across the first element isolating area, the first region, and the second element isolating area;

a second gate electrode isolated from the first gate electrode and provided on and across the first element isolating area, the second region, and the second element isolating area;

a first gate insulation film provided between the first region and the first gate electrode;

a second gate insulation film provided between the second region and the second gate electrode;

a third element isolating area;

a second element area surrounding sides of the third element isolating area, sides of the second element area surrounded by the second element isolating area;

a third gate electrode provided on and across the third element isolating area, the second element area, and the second element isolating area; and

a fourth gate electrode isolated from the third gate electrode and provided on and across the third element isolating area, the second element area, and the second element isolating area, wherein

the first gate electrode and the first element area forms a first transistor,

the second gate electrode and the first element area forms a second transistor,

the first element area forms a substantially rectangular annular shape,

the second element area forms a substantially rectangular annular shape,

a transistor of a first conductive-type is formed by the first gate electrode and the first element area, and a transistor of a second conductive-type which is different from the first conductive-type is formed by the third gate electrode and the second element area, and

the first element area and the second element area are different from each other in outer dimension in the first direction.

13. The device of claim 12, wherein the first gate electrode and the second gate electrode are aligned in a channel width direction.

14. The device of claim 12, further comprising:

a first channel region provided under the first gate electrode and in the first element area;

a first source/drain region provided in the first element area in a manner sandwiching the first channel region;

a second channel region provided under the third gate electrode and in the second element area; and

a second source/drain region provided in the second element area in a manner sandwiching the second channel region,

wherein a dimension of the first source/drain region is smaller than a dimension of the second source/drain region.

15. The device of claim 12, wherein

the third region and the fourth region are provided symmetrically.

16. The device of claim 12, wherein

a channel surface of the first and second transistor is set to (100) plane, and

a channel length direction of the first and second transistor is set to <100> direction.

17. The device of claim 12, wherein

no control gate electrode is provided above the first gate electrode and the second gate electrode.

18. The device of claim 12, wherein

no control gate electrode is provided above a drain of the first transistor, a source of the first transistor, a drain of the second transistor and a source of the second transistor.

19. The device of claim 12, wherein

the first direction is a channel length direction of the first and second transistors.

20. The device of claim 19, wherein

the first element area and the second element area are equal to each other in inner dimension in the first direction.

21. The device of claim 19, wherein

the first element area and the second element area are different from each other in inner dimension in the first direction.

22. The device of claim 12, wherein

the first and second element areas have outer and inner dimensions designed to adjust stress from the first and second element isolating areas to the first transistor and stress from the second and third element isolating areas to the second transistor.

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