

(19) World Intellectual Property Organization  
International Bureau(43) International Publication Date  
8 January 2009 (08.01.2009)

PCT

(10) International Publication Number  
WO 2009/005903 A1(51) International Patent Classification:  
H01L 21/336 (2006.01) H01L 29/78 (2006.01)

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(21) International Application Number:  
PCT/US2008/064192

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(22) International Filing Date: 20 May 2008 (20.05.2008)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:  
11/771,721 29 June 2007 (29.06.2007) US(71) Applicant (for all designated States except US):  
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(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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## Published:

— with international search report

[Continued on next page]

(54) Title: METHOD FOR FORMING A DUAL METAL GATE STRUCTURE

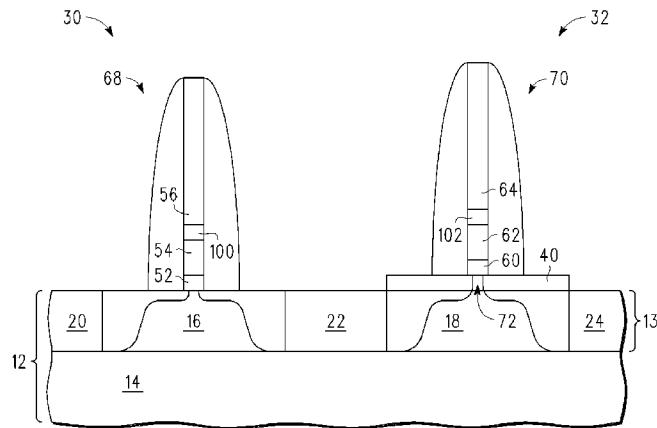


FIG. 13

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(57) Abstract: A method for forming a semiconductor structure (10) includes forming a channel region layer (40) over a semiconductor layer where the semiconductor layer includes a first and a second well region (16, 18), forming a protection layer (80) over the channel region layer, forming a first gate dielectric layer (26) over the first well region, forming a first metal gate electrode layer (28) over the first gate dielectric, removing the protection layer, forming a second gate dielectric layer (42) over the channel region layer, forming a second metal gate electrode layer (44) over the second gate dielectric layer, and forming a first gate stack (58) including a portion of each of the first gate dielectric layer and the first metal gate electrode layer over the first well region and forming a second gate stack (66) including a portion of each of the second gate dielectric layer and the second metal gate electrode layer over the channel region layer.



- *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

## **METHOD FOR FORMING A DUAL METAL GATE STRUCTURE**

### Background

#### Field

[0001] This disclosure relates generally to semiconductor processing, and more specifically, to a method for forming a dual metal gate structure.

#### Related Art

[0002] In the field of semiconductor processing, the use of polysilicon gate structures is becoming increasingly less feasible as gate dielectric thicknesses steadily decrease. As semiconductor processing moves away from the use of silicon dioxide as gate dielectrics in favor of dielectrics having a high dielectric constant (also referred to as high k dielectrics), polysilicon gates become more problematic. One solution to overcoming some of the problems introduced by polysilicon gates is to use metal gates. In dual metal gate processes, a first metal is used to form the gates for PMOS (p-channel metal oxide semiconductor) devices and second different metal is used to form NMOS (n-channel MOS) devices. Through the use of the different metals, the work functions can be optimized for each type of device. However, in conventional dual metal gate integrations, some processing steps, such as the metal etches and hard mask removals, can damage the high k gate dielectrics of the dual metal gate structures, thus degrading device performance.

### Brief Description of the Drawings

[0003] The present invention is illustrated by way of example and is not limited by the accompanying figures, in which like references indicate similar elements. Elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale.

[0004] FIG. 1 illustrates a cross-sectional view of a semiconductor structure having a channel region layer over a semiconductor layer, in accordance with one embodiment.

[0005] FIG. 2 illustrates a cross-sectional view of the semiconductor structure of FIG. 1 after formation of a protection layer over the semiconductor layer and over the channel region layer, and a patterned masking layer over the protection layer, in accordance with one embodiment.

[0006] FIG. 3 illustrates a cross-sectional view of the semiconductor structure of FIG. 2 after removing exposed portions of the protection layer, in accordance with one embodiment.

[0007] FIG. 4 illustrates a cross-sectional view of the semiconductor structure of FIG. 3 after removing the patterned masking layer formed in FIG. 2, in accordance with one embodiment.

[0008] FIG. 5 illustrates a cross-sectional view of the semiconductor structure of FIG. 4 after formation of a gate dielectric layer over the semiconductor layer and the protection layer, a gate electrode layer over the dielectric layer, a conductive layer over the gate electrode layer, and a patterned masking layer over the conductive layer, in accordance with one embodiment.

[0009] FIG. 6 illustrates a cross-sectional view of the semiconductor structure of FIG. 5 after patterning the gate dielectric layer, gate electrode layer, and conductive layer formed in FIG. 5 using the patterned masking layer formed in FIG. 5, in accordance with one embodiment.

[0010] FIG. 7 illustrates a cross-sectional view of the semiconductor structure of FIG. 6 after removal of the patterned masking layer formed in FIG. 5, in accordance with one embodiment.

[0011] FIG. 8 illustrates a cross-sectional view of the semiconductor structure of FIG. 7 after removal of the protection layer, in accordance with one embodiment.

[0012] FIG. 9 illustrates a cross-sectional view of the semiconductor structure of FIG. 8 after formation of a gate dielectric layer over the conductive layer and the channel region layer, a gate electrode layer over the gate dielectric layer, a conductive layer over the gate electrode layer, and a patterned masking layer over the gate electrode layer, in accordance with one embodiment.

[0013] FIG. 10 illustrates a cross-sectional view of the semiconductor structure of FIG. 9 after removing portions of the conductive layer, the gate electrode layer, and the gate dielectric layer formed in FIG. 9, in accordance with one embodiment.

[0014] FIG. 11 illustrates a cross-sectional view of the semiconductor structure of FIG. 10 after removing the patterned masking layer formed in FIG. 9, and after formation of a gate thickening layer over the conductive layers and a patterned masking layer over the gate thickening layer, in accordance with one embodiment.

[0015] FIG. 12 illustrates a cross-sectional view of the semiconductor structure of FIG. 11 after forming two gate stacks, in accordance with one embodiment.

[0016] FIG. 13 illustrates a cross-sectional view of the semiconductor structure of FIG. 12 after forming substantially completed semiconductor devices with the gate stacks of FIG. 12, in accordance with one embodiment.

#### Detailed Description

[0017] Dual metal gate integrations where a first metal gate is used for NMOS devices and a second different metal gate is used for PMOS devices may be used to address the problems associated with polysilicon gates and allows for the work functions to be optimized for each type of device. Also, performance of PMOS and NMOS devices can be further improved through the use of different materials for the channel regions of the devices. For example, an NMOS device may perform well when its channel region is formed in one semiconductor material (such as silicon) while a PMOS device may perform better when its channel region is formed in a different semiconductor material (such as silicon germanium). Therefore, one embodiment described below includes a dual metal integration which also allows for different types of channel regions for NMOS and PMOS devices.

[0018] FIG. 1 illustrates a semiconductor structure 10 having a semiconductor substrate 12. Semiconductor substrate 12 includes a buried oxide layer 14 and a semiconductor layer 13 over buried oxide layer 14. Semiconductor layer 13 includes an NMOS well region 16 which will be used to form an NMOS device and a PMOS well region 18 which will be used to form a PMOS device. Semiconductor layer 13 also includes isolations regions 20, 22, and 24 to isolate different well regions. Note that each well region, such as well regions 16 and 18, may be used to form any number of devices. In the illustrated embodiment, semiconductor substrate is illustrated as a semiconductor-on-insulator (SOI) substrate in which semiconductor layer 13 overlies buried oxide layer 14. However, in an alternate embodiment, substrate 12 can be a bulk semiconductor substrate where buried oxide layer 14 would not be present. Semiconductor layer 13 may include any semiconductor material. In one embodiment, semiconductor layer 13 is a silicon layer.

[0019] Semiconductor layer 13 includes an NMOS device region 30, in which one or more NMOS devices will be formed, and a PMOS device region 32, in which one or more PMOS devices will be formed. Note that NMOS device region 30 may include any number of NMOS well regions, such as NMOS well region 16, and PMOS device region 32 may include any number of PMOS well regions, such as PMOS well region 18.

[0020] FIG. 1 also illustrates a channel region layer 40 formed over PMOS well region 18 within PMOS device region 32. Channel region layer 40 is a layer which will contain a

channel region of a PMOS device. Therefore, channel region layer 40 may be a layer which includes a semiconductor material that is different from the semiconductor material of semiconductor layer 13 (or of NMOS well region 16) and which may be better suited for PMOS devices. For example, it may be a material which affects strain, bandgap, mobility, or the like, or any combination thereof. For example, in one embodiment, channel region layer 40 is a silicon germanium layer which allows for improved PMOS devices as compared to silicon. Therefore, in one embodiment, well regions 16 and 18 of semiconductor layer 13 may be silicon while channel region layer 40 may be silicon germanium. In one embodiment, the silicon germanium is epitaxially grown to a thickness in a range of approximately 2 to 15 nanometers at a temperature in range of approximately 550 to 700 degrees Celsius and has a germanium concentration in a range of approximately 10 to 50 percent.

[0021] FIG. 2 illustrates semiconductor structure 10 after the formation of a protection layer 80 over semiconductor layer 13 and over channel region layer 40. In one embodiment, protection layer 80 is formed by blanket depositing an oxide having a thickness in a range of approximately 5 to 20 nanometers. In an alternate embodiment, protection layer 80 may include a plasma enhanced nitride. FIG. 2 also illustrates a patterned masking layer 82 formed over protection layer 80 in PMOS device region 32. In one embodiment, patterned masking layer 82 may include photoresist. In one embodiment, conventional processing may be used to form patterned masking layer 82.

[0022] FIG. 3 illustrates semiconductor structure 10 after the removal of exposed portions of protection layer 80 using patterned masking layer 82. Therefore, note that through the use of patterned masking layer 82, those portions of protection layer 80 within NMOS device region 30 can be removed to expose NMOS well region 16 of semiconductor layer 13. In one embodiment, conventional etching processes and chemicals may be used to remove exposed portions of protection layer 80.

[0023] FIG. 4 illustrates semiconductor structure 10 after removal of patterned masking layer 82. In one embodiment, conventional processing is used to remove patterned masking layer 82.

[0024] FIG. 5 illustrates semiconductor structure 10 after formation of a gate dielectric layer 26 over semiconductor layer 13 and protection layer 80, a gate electrode layer 28 over gate dielectric layer 26, a conductive layer 84 over gate electrode layer 28, and a patterned masking layer 34 over conductive layer 84 in NMOS region 30. In one embodiment, gate dielectric layer 26 is blanket deposited over semiconductor layer 13 and protection layer 80,

and gate electrode layer 28 is blanket deposited over gate dielectric layer 26. In one embodiment, gate dielectric layer 26 is a high k gate dielectric including, for example, hafnium oxide or hafnium zirconium oxide. (Note that, as used herein, a high k dielectric refers to a dielectric having a dielectric constant, k, greater than that of silicon dioxide.) Furthermore, gate dielectric layer 26 may include more than one layer, such as a high k dielectric layer capped with an oxide. In one embodiment, gate dielectric layer 26 may have a thickness in a range of approximately 1 to 5 nanometers. In one embodiment, gate electrode layer 28 includes a metal such as, for example, tantalum carbide, tantalum nitride, titanium nitride, or the like. In one embodiment, gate electrode layer 28 has a thickness in a range of approximately 2 to 10 nanometers. In the illustrated embodiment, note that gate dielectric layer 26 and gate electrode layer 28 are the gate dielectric layer and gate electrode layer, respectively, that will be used to form an NMOS device in NMOS device region 30.

[0025] Still referring to FIG. 5, in one embodiment, conductive layer 84 is an in-situ doped polycrystalline silicon layer. In one embodiment, conductive layer 84 has a thickness in a range of approximately 2 to 20 nanometers. In an alternate embodiment, conductive layer 84 is not present. Also, in one embodiment, patterned masking layer 34 includes photoresist and may be formed using conventional processing.

[0026] FIG. 6 illustrates semiconductor structure 10 after removal of exposed portions of gate dielectric layer 26, gate electrode layer 28, and conductive layer 84 using patterned masking layer 34. Therefore, note that through the use of patterned masking layer 34, those portions of gate dielectric layer 26, gate electrode layer 28, and conductive layer 84 within PMOS device region 32 can be removed. In one embodiment, a dry etch may be used to etch through at least conductive layer 84 while a wet or dry etch may be used to etch through gate electrode layer 28 and gate dielectric layer 26. Note that, in the illustrated embodiment, protection layer 80 protects channel region 40 during the etch of gate dielectric layer 26, gate electrode layer 28, and conductive layer 84 within PMOS device region 32.

[0027] FIG. 7 illustrates semiconductor structure 10 after removal of patterned masking layer 34. In one embodiment, conventional processing can be used to remove patterned masking layer 34.

[0028] FIG. 8 illustrates semiconductor structure 10 after the removal of protection layer 80. In one embodiment, a hydrofluoric acid (HF) is used to remove protection layer 80 in PMOS device region 32.

[0029] FIG. 9 illustrates semiconductor structure 10 after the formation of a gate dielectric layer 42 over conductive layer 84 in NMOS device region 30 and over channel region layer 40 in PMOS device region 32, a gate electrode layer 44 over gate dielectric layer 42, a conductive layer 92 over gate electrode layer 44, and a patterned masking layer 46 over conductive layer 92 in PMOS device region 32. In one embodiment, gate dielectric layer 42 is blanket deposited over conductive layer 84, semiconductor layer 13, and channel region 40, and gate electrode layer 44 is blanket deposited over gate dielectric layer 42. In one embodiment, gate dielectric layer 42 is a high  $k$  gate dielectric including, for example, hafnium oxide or hafnium zirconium oxide. (Note that, in one embodiment, gate dielectric layer 42 is formed using a different high  $k$  dielectric than gate dielectric 26.) Furthermore, gate dielectric layer 42 may include more than one layer, such as a high  $k$  dielectric layer capped with an oxide. In one embodiment, gate dielectric layer 42 may have a thickness in a range of approximately 1 to 5 nanometers. In one embodiment, gate electrode layer 44 includes a metal such as, for example, molybdenum nitride, ruthenium, or the like. Also, in one embodiment, gate electrode layer 44 is formed with a metal that is different from the metal of gate electrode layer 28. In one embodiment, gate electrode layer 44 has a thickness in a range of approximately 2 to 10 nanometers. In the illustrated embodiment, note that gate dielectric layer 42 and gate electrode layer 44 are the gate dielectric layer and gate electrode layer, respectively, that will be used to form a PMOS device in PMOS device region 32.

[0030] Still referring to FIG. 9, in one embodiment, conductive layer 92 is an in-situ doped polycrystalline silicon layer. In one embodiment, conductive layer 92 has a thickness in a range of approximately 3 to 15 nanometers. In an alternate embodiment, conductive layer 92 is not present. Also, in one embodiment, patterned masking layer 46 includes photoresist and may be formed using conventional processing.

[0031] Note that NMOS device region 30 may be referred to as a first device region, and similarly, NMOS well region 16 may be referred to as a first well region, and PMOS device region 32 may be referred to as a second device region, and similarly, PMOS well region 18 may be referred to as a second well region. Also, note that the polarities may be reversed, such that the first device region corresponds to a PMOS device region and the second device region corresponds to an NMOS device region. Similarly, in this embodiment, the first well region corresponds to a PMOS well region and the second well region corresponds to an NMOS well region. Also, in this case, gate dielectric layer 26 and gate electrode layer 28 would correspond to the gate dielectric layer and gate electrode layer, respectively, that would be used to form a PMOS device while gate dielectric layer 42 and gate electrode layer

44 would correspond to the gate dielectric layer and gate electrode layer, respectively, that would be used to form an NMOS device.

[0032] FIG. 10 illustrates semiconductor structure 10 after removing exposed portions conductive layer 92, gate electrode layer 44, and gate dielectric layer 42 in NMOS device region 30 using patterned masking layer 46. Therefore, note that through the use of patterned masking layer 46, those portions of conductive layer 92, gate electrode layer 44, and gate dielectric layer 42, within NMOS device region 30 can be etched where, in one embodiment, conductive layer 86 operates as an etch stop layer for the etch and operates to protect underlying gate electrode layer 28 during the etch. In an alternate embodiment, conductive layer 84 is not present. In this alternate embodiment, gate electrode layer 28 may be made thicker where a top portion of gate electrode layer 28 would be removed during the etch of conductive layer 92, gate electrode layer 44, and gate dielectric layer 42. In this manner, a remaining portion of gate electrode layer 44 would have a thickness sufficient to operate appropriately as a gate electrode. In one embodiment, conventional etching may be used to remove the portions of conductive layer 92, gate electrode layer 44, and gate dielectric layer 42.

[0033] FIG. 11 illustrates semiconductor structure 10 after removing patterned masking layer 46. Note that conductive layer 92 operates to protect underlying gate electrode layer 44 during removal of patterned masking layer 46. In one embodiment, an ash or "Piranha" clean may be used to remove patterned masking layer 46, where the ash or "Piranha" may damage gate electrode layer 44 if conductive protection layer 92 were not present. In an alternate embodiment, conductive layer 92 may not be present. For example, in one embodiment, patterned masking layer 46 may be removed with a solvent which may not damage an underlying layer such as gate electrode layer 44.

[0034] FIG. 11 also illustrates semiconductor structure 10 after formation of a gate thickening layer 48 over conductive layer 84 and 92 and after formation of a patterned masking layer 50 over gate thickening layer 48. Note that if conductive layer 84 is not present, then gate thickening layer 48 is formed directly on gate electrode 28 and if conductive layer 92 is not present, gate thickening layer 48 is formed directly on gate electrode 44. In one embodiment, gate thickening layer 48 includes a conductive material, such as, for example, polycrystalline silicon, and may therefore also be referred to as a conductive gate thickening layer. Also, gate thickening layer 48 may include one or more layers of conductive materials. In one embodiment, gate thickening layer 48 operates to thicken the gate stacks of the devices being formed so that when source and drain implants are performed, the gate stacks are thick enough to block the implants in the channel region.

In an alternate embodiment, no gate thickening layers may be formed. Patterned masking layer 50 defines locations corresponding to the gate stacks of the devices being formed. In the illustrated embodiment, patterned masking layer 50 defines a gate stack location in NMOS device region 30 and a gate stack location in PMOS device region 32. In one embodiment, patterned masking layer 50 includes photoresist. In one embodiment, conventional processing may be used to form gate thickening layer 48 and patterned masking layer 50.

[0035] FIG. 12 illustrates semiconductor structure 10 after the formation of gate stacks 58 and 66 using patterned masking layer 50 and after subsequent removal of patterned masking layer 50. Therefore, using patterned masking layer 50, exposed portions of gate thickening layer 48 are removed from device regions 30 and 32, portions of conductive layer 84, gate electrode layer 28, and gate dielectric layer 26 are removed from NMOS device region 30, and portions of conductive layer 92, gate electrode layer 44, and gate dielectric layer 42 are removed from PMOS device region 32, thus resulting in gate stack 58 in NMOS device region 30 and gate stack 66 in PMOS device region 32. Note that during the etch of the embodiment illustrated in FIG. 13, both metal gate electrode layers (gate electrode layers 28 and 44) are etched simultaneously. In one embodiment, the thicknesses of gate electrode layers 28 and 44 can be adjusted depending on their relative etch rates so that both the layers can be etched in the same total time. In one embodiment, conventional processing may be used to form gate stacks 58 and 66 and patterned masking layer 50.

[0036] As illustrated in FIG. 13, gate stack 58 includes a gate dielectric 52 (formed from gate dielectric layer 26) over NMOS well region 16, a gate electrode 54 (formed from gate electrode layer 28) over gate dielectric 52, a conductive layer 100 (formed from conductive layer 84) over gate electrode 54, and a gate thickener 56 (formed from gate thickening layer 48) over gate electrode 54. Gate stack 66 includes a gate dielectric 60 (formed from gate dielectric layer 42) over channel region layer 40, a gate electrode 62 (formed from gate electrode layer 44) over gate dielectric 60, a conductive layer 102 (formed from conductive layer 92) over gate electrode 62, and a gate thickener 64 (formed from gate thickening layer 48) over gate electrode 62.

[0037] FIG. 14 illustrates semiconductor structure 10 after the formation of substantially completed NMOS device 68 and PMOS device 70. NMOS device 68 is formed using gate stack 58 in NMOS device region 30 and PMOS device is formed using gate stack 66 in PMOS device region 32. For each device, conventional processing may be used to form spacers and source/drain regions. Note that a channel region is formed between source/drain regions of NMOS device 68 under gate dielectric 52 in NMOS well regions 16

of semiconductor layer 13. However, a channel region of PMOS device 70 is located between source/ drain regions of PMOS device 70 under gate dielectric 60 in channel region layer 40 rather than in semiconductor layer 13. In this manner, NMOS and PMOS devices 68 and 70 may include different metal gate electrodes and be formed having different semiconductor materials for the channel regions. Therefore, the NMOS and PMOS devices can each be optimized separately through the selection of different metal gate electrodes and different channel region materials.

[0038] Therefore, it can be appreciated that through the use of protection layer 80, gate electrode layer 28 and gate dielectric layer 26 (and conductive layer 84, if present) can be etched from device region 32 without damaging previously formed channel region layer 40. Furthermore, the use of conductive layers 84 and 92, underlying layers, such as gate electrode layers 28 and 44, respectively, can be protected during subsequent processing (such as during removal of overlying layers) needed to form a dual metal gate structure. In this manner, a channel region layer can be formed that is better suited for the particular type of device being formed in device region 32 (whether it be a PMOS or an NMOS device) while allowing for a dual metal integration that does not damage the channel region/gate dielectric interface.

[0039] In an alternate embodiment, note that a channel region layer such as channel region layer 40 may be used for forming an NMOS device rather than a PMOS device. In yet another embodiment, a channel region layer such as channel region layer 40 may be used for forming both an NMOS and a PMOS device. For example, a channel region layer may also be formed over well region 16 prior to the formation of gate dielectric layer 26.

[0040] One embodiment relates to a method for forming a semiconductor structure including forming a channel region layer over a semiconductor layer where the semiconductor layer includes a first well region and a second well region and where the channel region layer is formed over the second well region, forming a protection layer over the channel region layer, forming a first gate dielectric layer over the first well region, forming a first metal gate electrode layer over the first gate dielectric, removing the protection layer after the forming the first metal gate electrode layer, forming a second gate dielectric layer over the channel region layer, forming a second metal gate electrode layer over the second gate dielectric layer where the second metal gate electrode layer is a different metal than the first metal gate electrode layer, and forming a first gate stack including a portion of each of the first gate dielectric layer and the first metal gate electrode layer over the first well region and forming a second gate stack including a portion of each of the second gate dielectric

layer and the second metal gate electrode layer over the channel region layer and over the second well region.

[0041] In a further embodiment, the method further includes forming a first device having a first conductivity type using the first gate stack and forming a second device having a second conductivity type different from the first conductivity type, using the second gate stack, where a channel region of the second device is in the channel region layer.

[0042] In another further embodiment, prior to the forming the first gate stack and the second gate stack, the method further includes forming a conductive gate thickening layer over each of the first metal gate electrode layer and the second metal gate electrode layer.

[0043] In another further embodiment, the forming the channel region layer includes growing a semiconductor material that is different from a semiconductor material of the semiconductor layer. In yet a further embodiment, the forming the channel region layer includes epitaxially growing silicon germanium over the second well region.

[0044] In another further embodiment, the forming the protection layer includes depositing a material selected from a group consisting of an oxide and a nitride.

[0045] In another further embodiment, the forming the first gate dielectric layer includes forming a first high k dielectric layer and forming the second gate dielectric layer includes forming a second high k dielectric layer which includes a different high k dielectric than the first high k dielectric layer.

[0046] In another embodiment, a method for forming a semiconductor structure includes forming a channel region layer over a semiconductor layer where the semiconductor layer includes a first well region and a second well region and where the channel region layer is formed over the second well region and not over the first well region, forming a protection layer over the channel region layer, forming a gate dielectric layer over the semiconductor layer and the protection layer, forming a first metal gate electrode layer over the first gate dielectric layer, removing portions of the first gate dielectric layer and the first metal gate electrode layer which overlie the protection layer, removing the protection layer, forming a second gate dielectric layer over the first gate electrode layer and the channel region layer, forming a second metal gate electrode layer over the second gate dielectric layer where the second metal gate electrode layer is a different metal than the first metal gate electrode layer, removing portions of the second metal gate electrode layer and the second gate dielectric layer which overlie the first gate electrode layer, and forming a first gate stack including a portion of each of the first gate dielectric layer and the first metal gate electrode

layer over the first well region and forming a second gate stack including a portion of each of the second gate dielectric layer and the second metal gate electrode layer over the channel region layer and over the second well region.

[0047] In a further embodiment of the another embodiment, the forming the protection layer includes depositing a material selected from a group consisting of an oxide and a nitride.

[0048] In another further embodiment of the another embodiment, forming a first device having a first conductivity type using the first gate stack and forming a second device having a second conductivity type different from the first conductivity type, using the second gate stack, where a channel region of the second device is in the channel region layer

[0049] In another further embodiment of the another embodiment, the forming the channel region layer includes growing a semiconductor material that is different from a semiconductor material of the semiconductor layer. In a further embodiment, the forming the channel region layer includes epitaxially growing silicon germanium over the second well region.

[0050] In another further embodiment of the another embodiment, the forming the first gate dielectric layer includes forming a first high k dielectric layer and the forming the second gate dielectric layer includes forming a second high k dielectric layer which includes a different high k dielectric than the first high k dielectric layer.

[0051] In another further embodiment of the another embodiment, the method further includes forming a conductive layer over the first gate electrode layer where the forming a second gate dielectric layer over the first gate electrode layer and the channel region layer includes forming the second gate dielectric layer over the conductive layer and the channel region layer. In yet a further embodiment, the removing the portions of the second metal gate electrode layer and the second gate dielectric layer which overlie the first gate electrode layer includes using the conductive layer as an etch stop layer.

[0052] In another further embodiment of the another embodiment, the method further includes forming a conductive layer over the second metal gate electrode layer.

[0053] In yet another embodiment, a method for forming a semiconductor structure includes forming a channel region layer over a semiconductor layer where the semiconductor layer includes a first well region and a second well region and where the channel region layer is formed over the second well region, forming a protection layer over

the channel region layer, forming a first high k gate dielectric layer over the first well region, forming a first metal gate electrode layer over the first high k gate dielectric, removing the protection layer after the forming the first metal gate electrode layer, forming a second high k gate dielectric layer over the channel region layer where the second high k gate dielectric layer has a different high k dielectric than the first high k gate dielectric layer, forming a second metal gate electrode layer over the second high k gate dielectric layer where the second metal gate electrode layer is a different metal than the first metal gate electrode layer, forming a first gate stack including a portion of each of the first high k gate dielectric layer and the first metal gate electrode layer over the first well region and forming a second gate stack including a portion of each of the second high k gate dielectric layer and the second metal gate electrode layer over the channel region layer and over the second well region, and forming a first device having a first conductivity type using the first gate stack and forming a second device having a second conductivity type different from the first conductivity type, using the second gate stack, where a channel region of the second device is in the channel region layer.

[0054] In a further embodiment of the yet another embodiment, prior to the forming the first gate stack and the second gate stack, the method further includes forming a conductive gate thickening layer over each of the first metal gate electrode layer and the second metal gate electrode layer.

[0055] In another further embodiment of the yet another embodiment, the forming the channel region layer includes growing a semiconductor material that is different from a semiconductor material of the semiconductor layer.

[0056] In another further embodiment of the yet another embodiment, the forming the protection layer includes depositing a material selected from a group consisting of an oxide and a nitride.

[0057] Although the invention has been described with respect to specific conductivity types or polarity of potentials, skilled artisans appreciated that conductivity types and polarities of potentials may be reversed.

[0058] Moreover, the terms "front," "back," "top," "bottom," "over," "under" and the like in the description and in the claims, if any, are used for descriptive purposes and not necessarily for describing permanent relative positions. It is understood that the terms so used are interchangeable under appropriate circumstances such that the embodiments of

the invention described herein are, for example, capable of operation in other orientations than those illustrated or otherwise described herein.

[0059] Although the invention is described herein with reference to specific embodiments, various modifications and changes can be made without departing from the scope of the present invention as set forth in the claims below. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of the present invention. Any benefits, advantages, or solutions to problems that are described herein with regard to specific embodiments are not intended to be construed as a critical, required, or essential feature or element of any or all the claims.

[0060] Furthermore, the terms "a" or "an," as used herein, are defined as one or more than one. Also, the use of introductory phrases such as "at least one" and "one or more" in the claims should not be construed to imply that the introduction of another claim element by the indefinite articles "a" or "an" limits any particular claim containing such introduced claim element to inventions containing only one such element, even when the same claim includes the introductory phrases "one or more" or "at least one" and indefinite articles such as "a" or "an." The same holds true for the use of definite articles.

[0061] Unless stated otherwise, terms such as "first" and "second" are used to arbitrarily distinguish between the elements such terms describe. Thus, these terms are not necessarily intended to indicate temporal or other prioritization of such elements.

CLAIMS

What is claimed is:

1. A method for forming a semiconductor structure, the method comprising:  
forming a channel region layer over a semiconductor layer, the semiconductor layer comprising a first well region and a second well region, and the channel region layer being formed over the second well region;  
forming a protection layer over the channel region layer;  
forming a first gate dielectric layer over the first well region;  
forming a first metal gate electrode layer over the first gate dielectric;  
removing the protection layer after the forming the first metal gate electrode layer;  
forming a second gate dielectric layer over the channel region layer;  
forming a second metal gate electrode layer over the second gate dielectric layer, wherein the second metal gate electrode layer is a different metal than the first metal gate electrode layer; and  
forming a first gate stack comprising a portion of each of the first gate dielectric layer and the first metal gate electrode layer over the first well region and forming a second gate stack comprising a portion of each of the second gate dielectric layer and the second metal gate electrode layer over the channel region layer and over the second well region.
2. The method of claim 1, further comprising:  
forming a first device having a first conductivity type using the first gate stack and  
forming a second device having a second conductivity type different from the first conductivity type, using the second gate stack, wherein a channel region of the second device is in the channel region layer.
3. The method of claim 1, further comprising, prior to the forming the first gate stack and the second gate stack, forming a conductive gate thickening layer over each of the first metal gate electrode layer and the second metal gate electrode layer.
4. The method of claim 1, wherein the forming the channel region layer comprises growing a semiconductor material that is different from a semiconductor material of the semiconductor layer.

5. The method of claim 4, wherein the forming the channel region layer comprises epitaxially growing silicon germanium over the second well region.
6. The method of claim 1, wherein the forming the protection layer comprises depositing a material selected from a group consisting of an oxide and a nitride.
7. The method of claim 1, wherein the forming the first gate dielectric layer comprises forming a first high k dielectric layer and forming the second gate dielectric layer comprises forming a second high k dielectric layer which includes a different high k dielectric than the first high k dielectric layer.
8. A method for forming a semiconductor structure, the method comprising:  
forming a channel region layer over a semiconductor layer, the semiconductor layer comprising a first well region and a second well region, and the channel region layer being formed over the second well region and not over the first well region;  
forming a protection layer over the channel region layer;  
forming a gate dielectric layer over the semiconductor layer and the protection layer;  
forming a first metal gate electrode layer over the first gate dielectric layer;  
removing portions of the first gate dielectric layer and the first metal gate electrode layer which overlie the protection layer;  
removing the protection layer;  
forming a second gate dielectric layer over the first gate electrode layer and the channel region layer;  
forming a second metal gate electrode layer over the second gate dielectric layer, wherein the second metal gate electrode layer is a different metal than the first metal gate electrode layer;  
removing portions of the second metal gate electrode layer and the second gate dielectric layer which overlie the first gate electrode layer; and  
forming a first gate stack comprising a portion of each of the first gate dielectric layer and the first metal gate electrode layer over the first well region and forming a second gate stack comprising a portion of each of the second gate dielectric layer and the second metal gate electrode layer over the channel region layer and over the second well region.
9. The method of claim 8, wherein the forming the protection layer comprises depositing a material selected from a group consisting of an oxide and a nitride.

10. The method of claim 8, further comprising:
  - forming a first device having a first conductivity type using the first gate stack and
  - forming a second device having a second conductivity type different from the first conductivity type, using the second gate stack, wherein a channel region of the second device is in the channel region layer.
11. The method of claim 8, wherein the forming the channel region layer comprises growing a semiconductor material that is different from a semiconductor material of the semiconductor layer.
12. The method of claim 11, wherein the forming the channel region layer comprises epitaxially growing silicon germanium over the second well region.
13. The method of claim 8, wherein the forming the first gate dielectric layer comprises forming a first high k dielectric layer and the forming the second gate dielectric layer comprises forming a second high k dielectric layer which includes a different high k dielectric than the first high k dielectric layer.
14. The method of claim 8, further comprising forming a conductive layer over the first gate electrode layer, wherein the forming a second gate dielectric layer over the first gate electrode layer and the channel region layer comprises forming the second gate dielectric layer over the conductive layer and the channel region layer.
15. The method of claim 14, wherein the removing the portions of the second metal gate electrode layer and the second gate dielectric layer which overlie the first gate electrode layer comprises using the conductive layer as an etch stop layer.
16. The method of claim 8, further comprising forming a conductive layer over the second metal gate electrode layer.
17. A method for forming a semiconductor structure, the method comprising:
  - forming a channel region layer over a semiconductor layer, the semiconductor layer comprising a first well region and a second well region, and the channel region layer being formed over the second well region;
  - forming a protection layer over the channel region layer;
  - forming a first high k gate dielectric layer over the first well region;
  - forming a first metal gate electrode layer over the first high k gate dielectric;

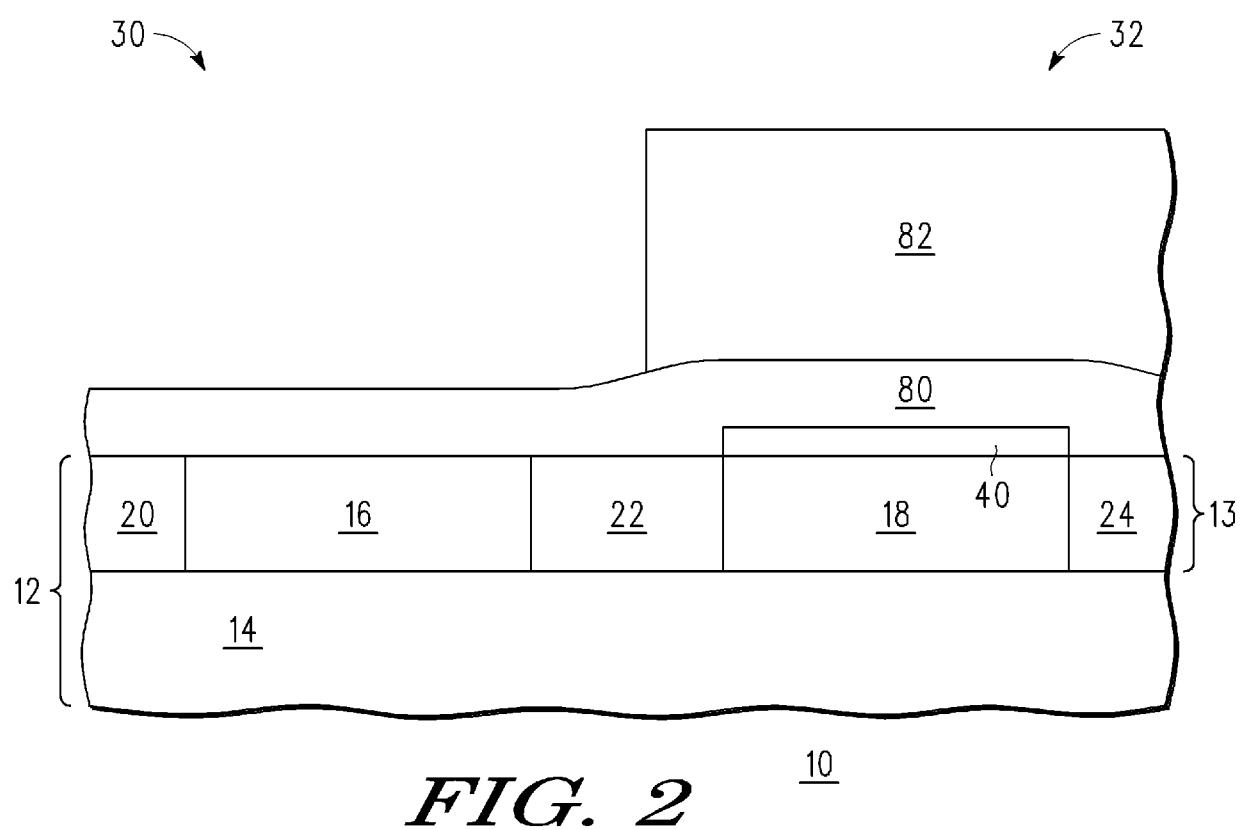
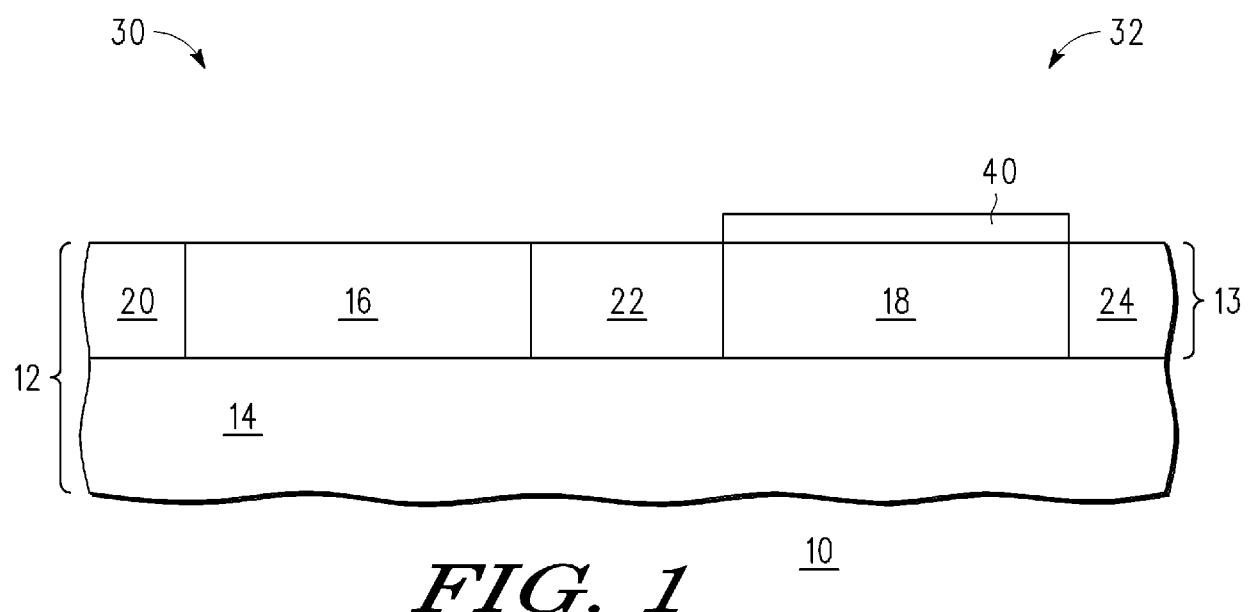
removing the protection layer after the forming the first metal gate electrode layer; forming a second high k gate dielectric layer over the channel region layer, the second high k gate dielectric layer having a different high k dielectric than the first high k gate dielectric layer; forming a second metal gate electrode layer over the second high k gate dielectric layer, wherein the second metal gate electrode layer is a different metal than the first metal gate electrode layer; forming a first gate stack comprising a portion of each of the first high k gate dielectric layer and the first metal gate electrode layer over the first well region and forming a second gate stack comprising a portion of each of the second high k gate dielectric layer and the second metal gate electrode layer over the channel region layer and over the second well region; and forming a first device having a first conductivity type using the first gate stack and forming a second device having a second conductivity type different from the first conductivity type, using the second gate stack, wherein a channel region of the second device is in the channel region layer.

18. The method of claim 17, further comprising, prior to the forming the first gate stack and the second gate stack, forming a conductive gate thickening layer over each of the first metal gate electrode layer and the second metal gate electrode layer.

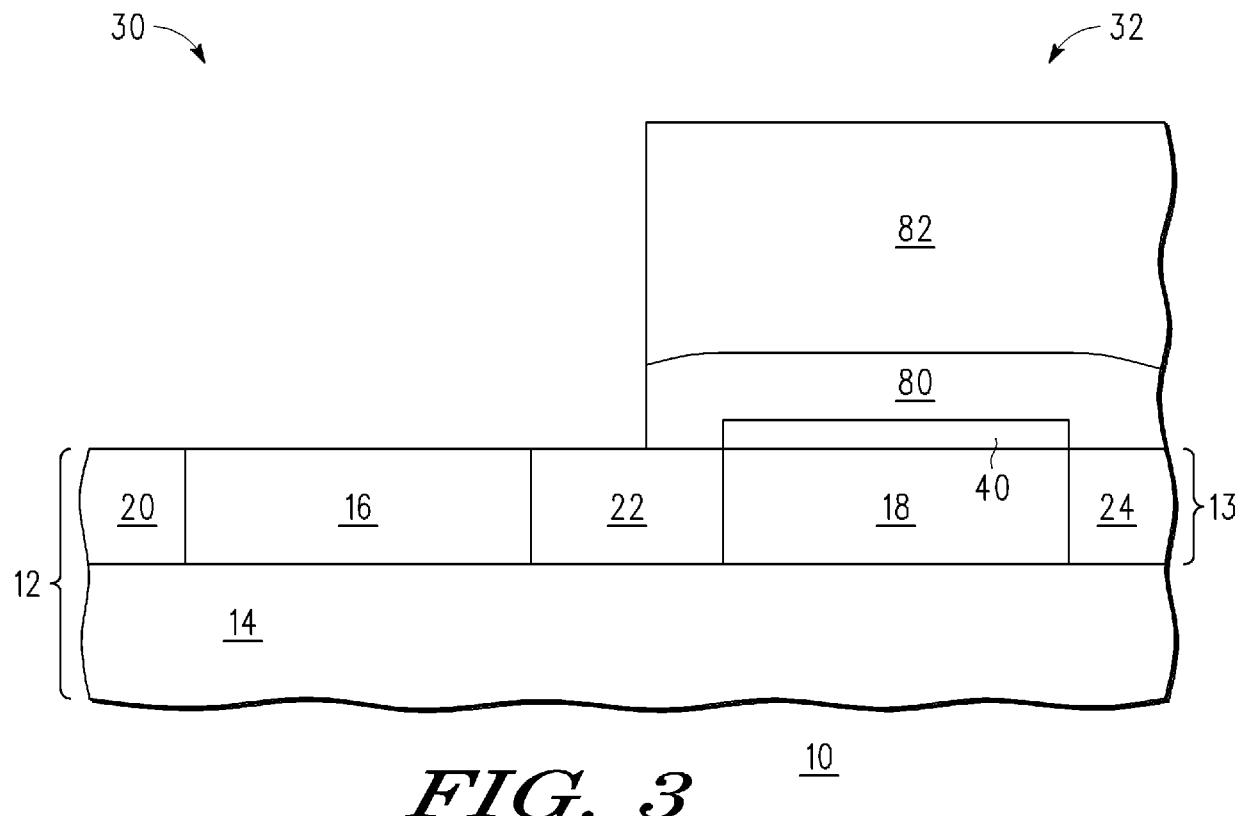
19. The method of claim 17, wherein the forming the channel region layer comprises growing a semiconductor material that is different from a semiconductor material of the semiconductor layer.

20. The method of claim 17, wherein the forming the protection layer comprises depositing a material selected from a group consisting of an oxide and a nitride.

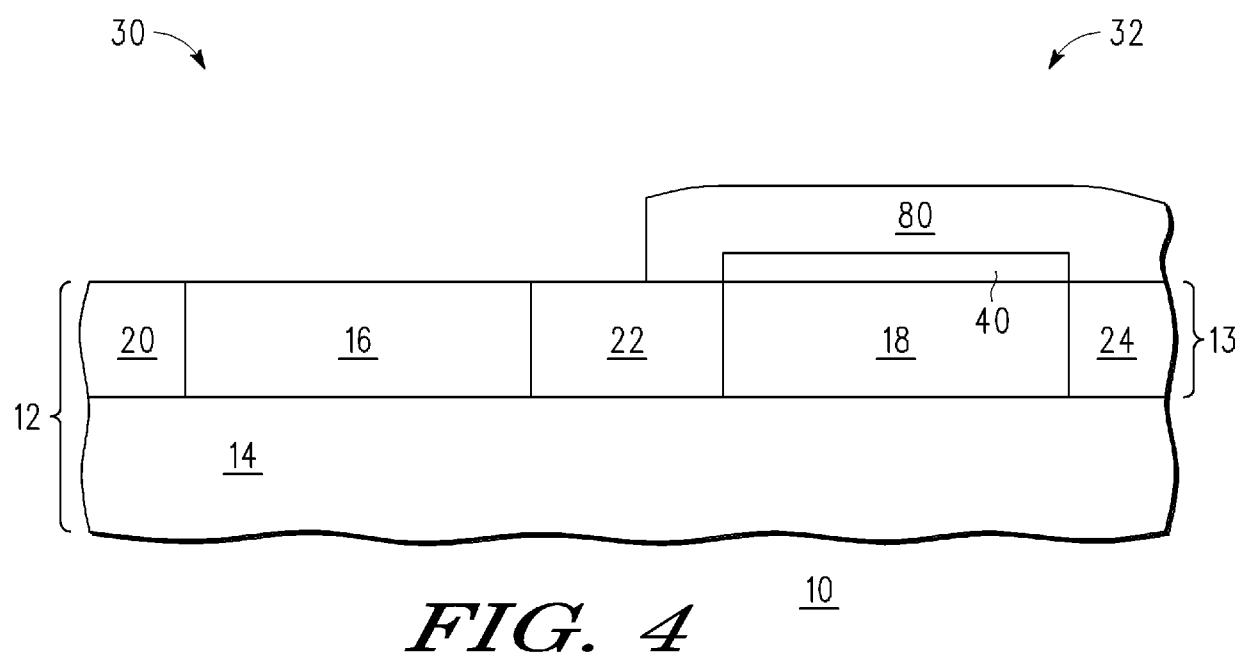
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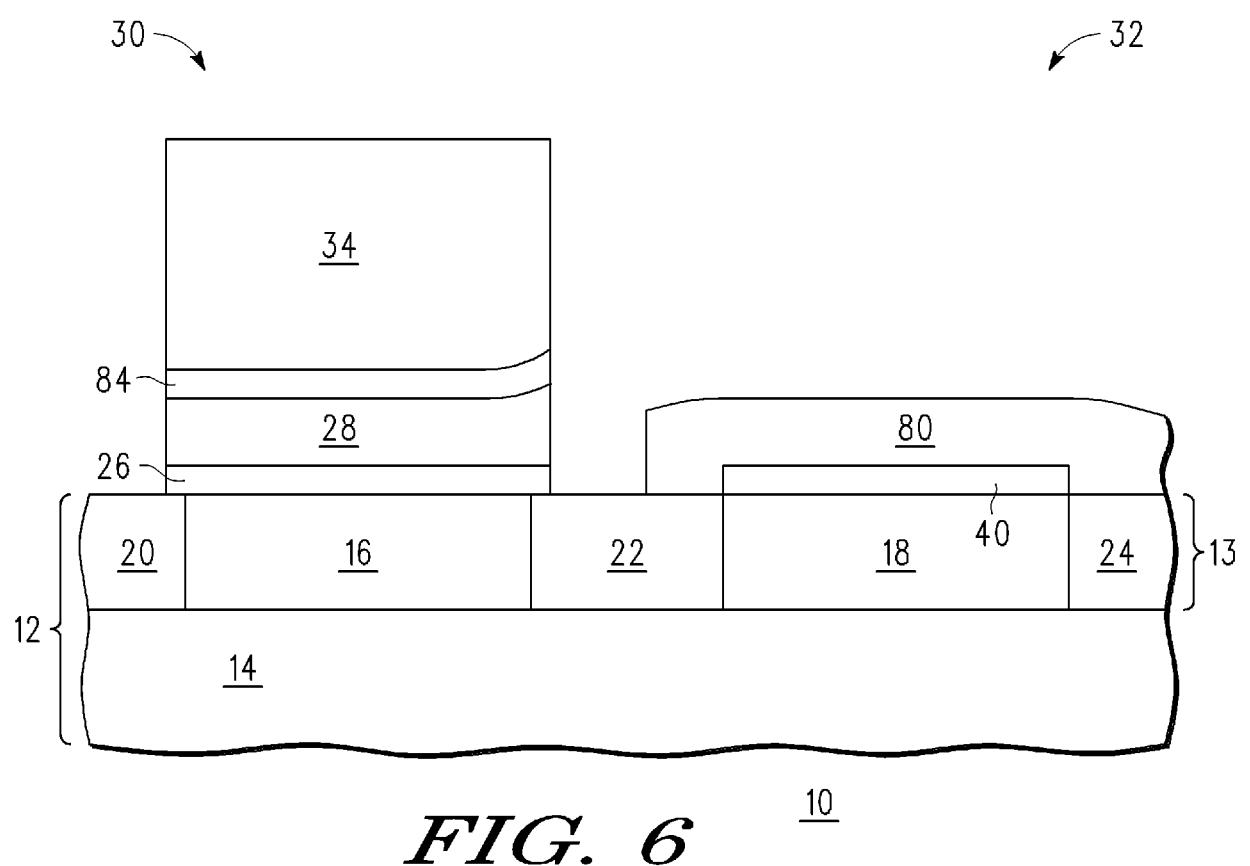
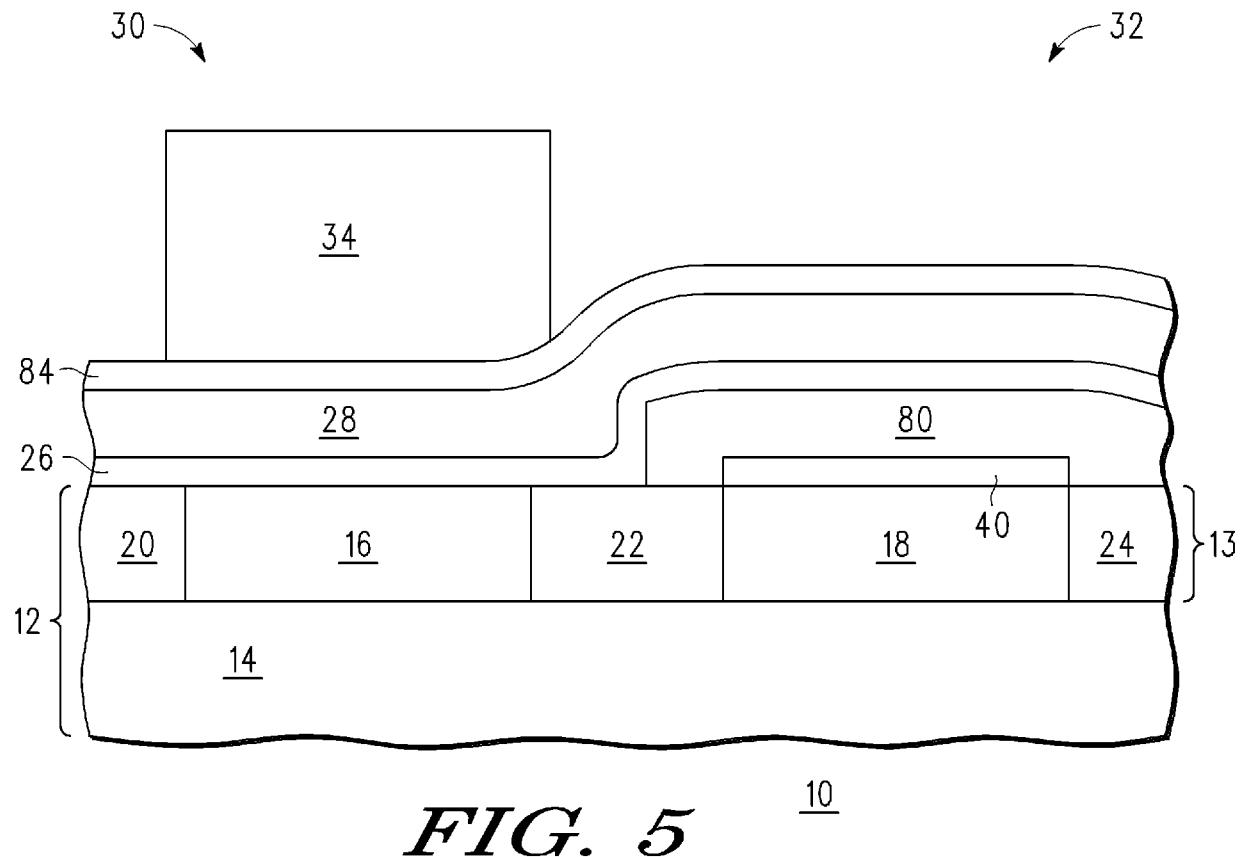


**FIG. 3** 10

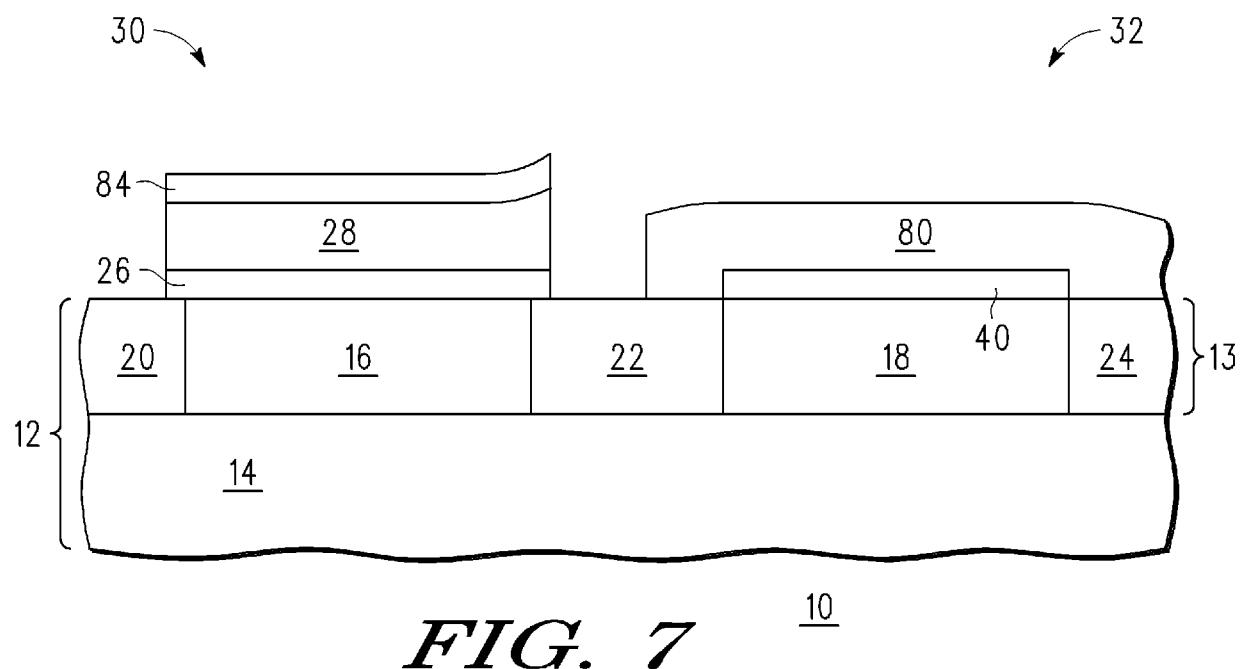


**FIG. 4** 10

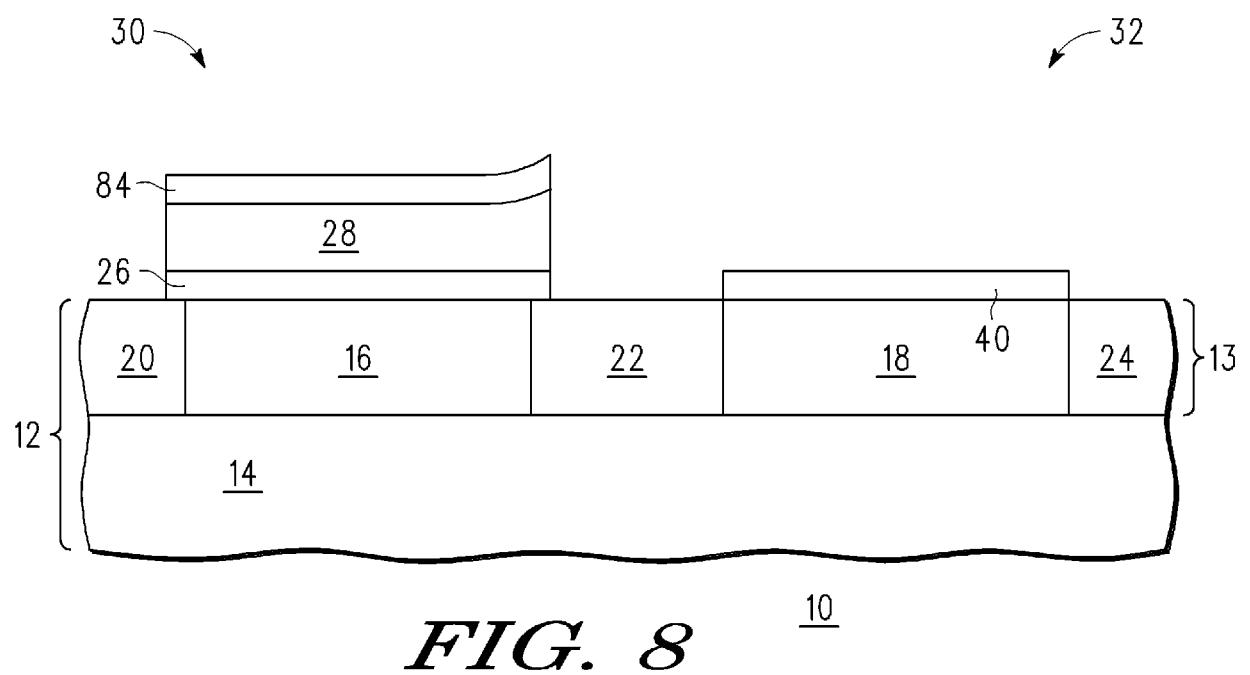
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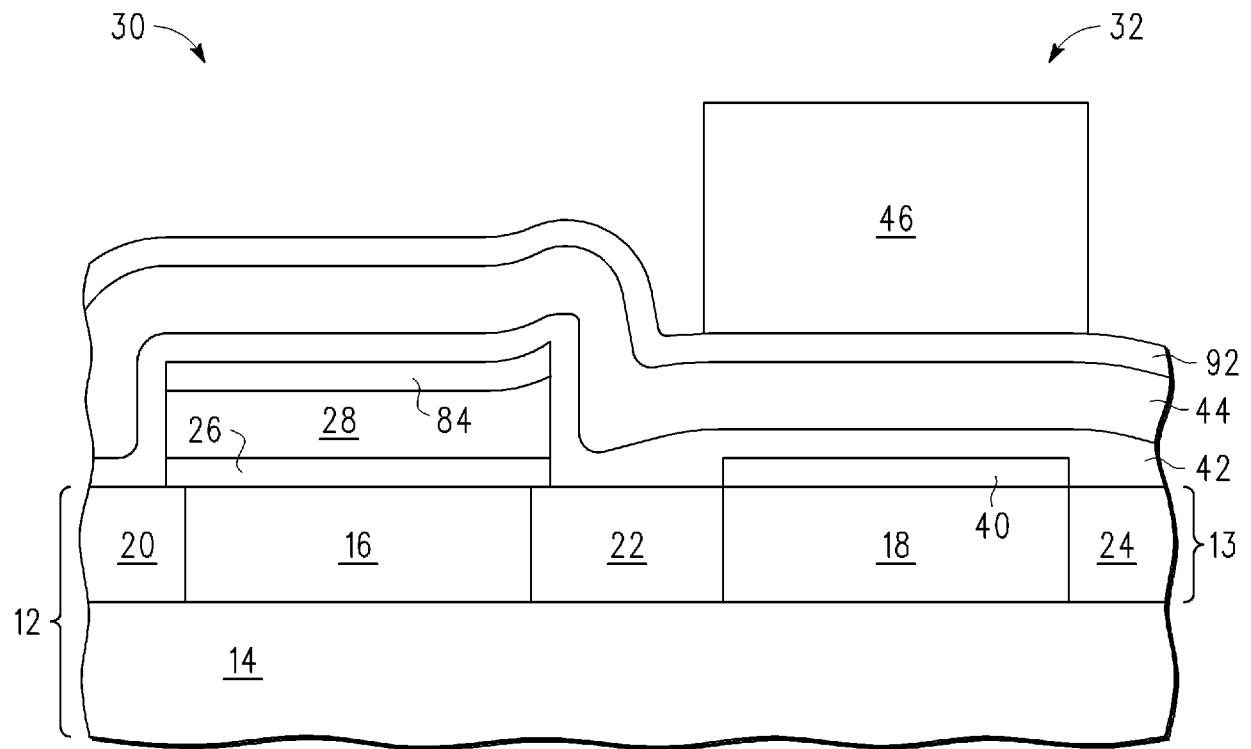


***FIG. 7***

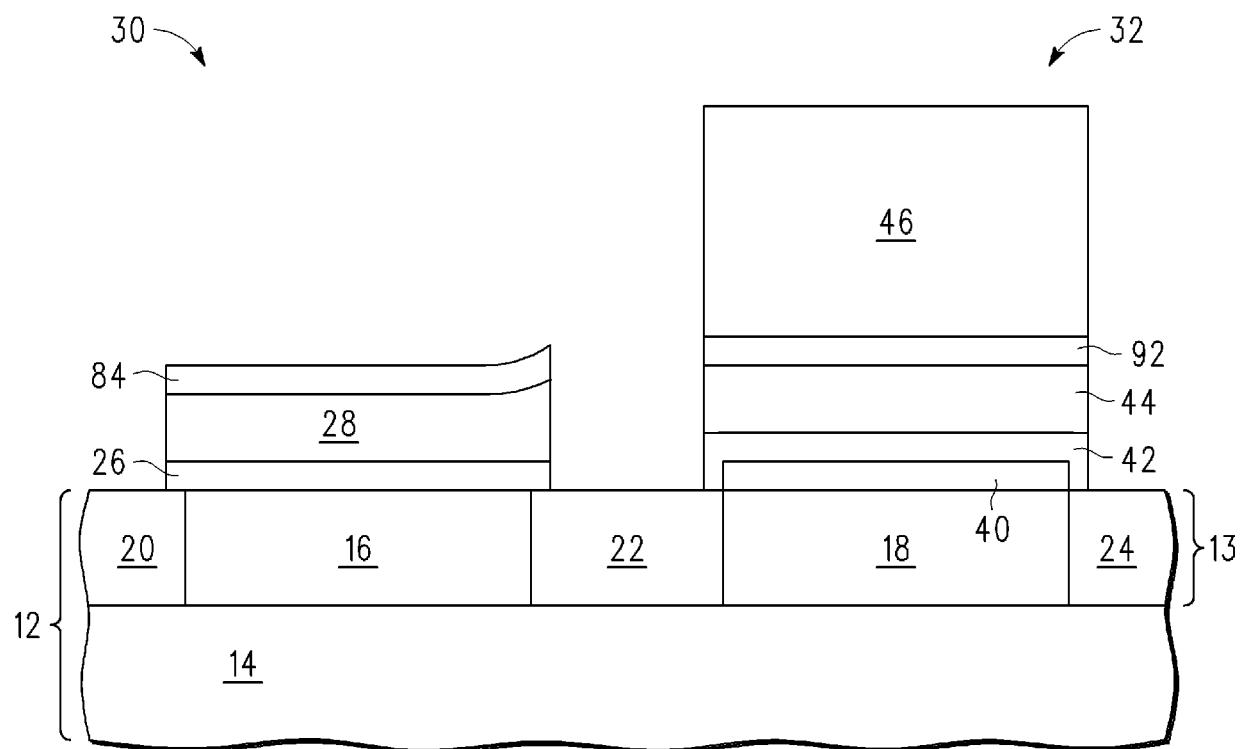


***FIG. 8***

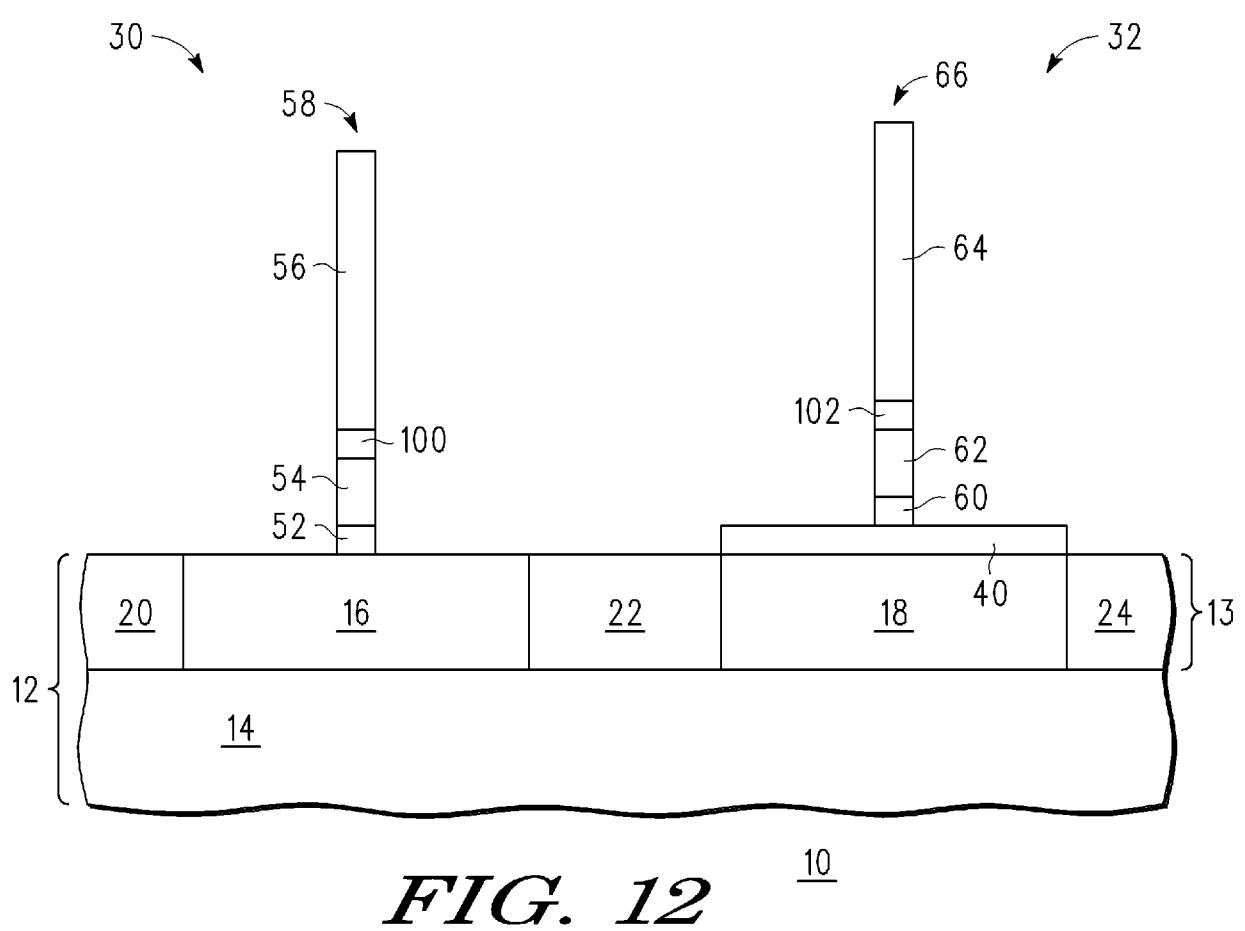
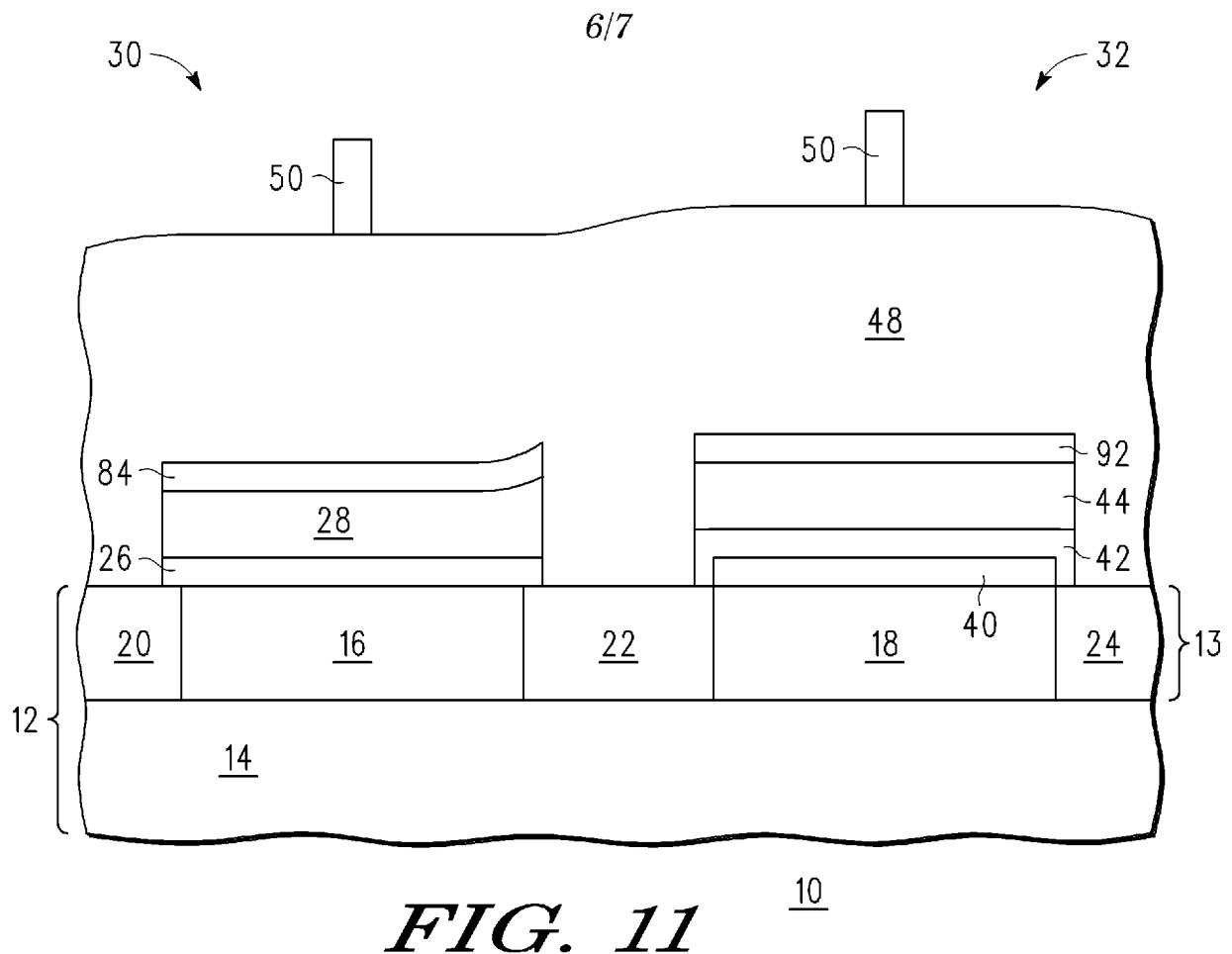
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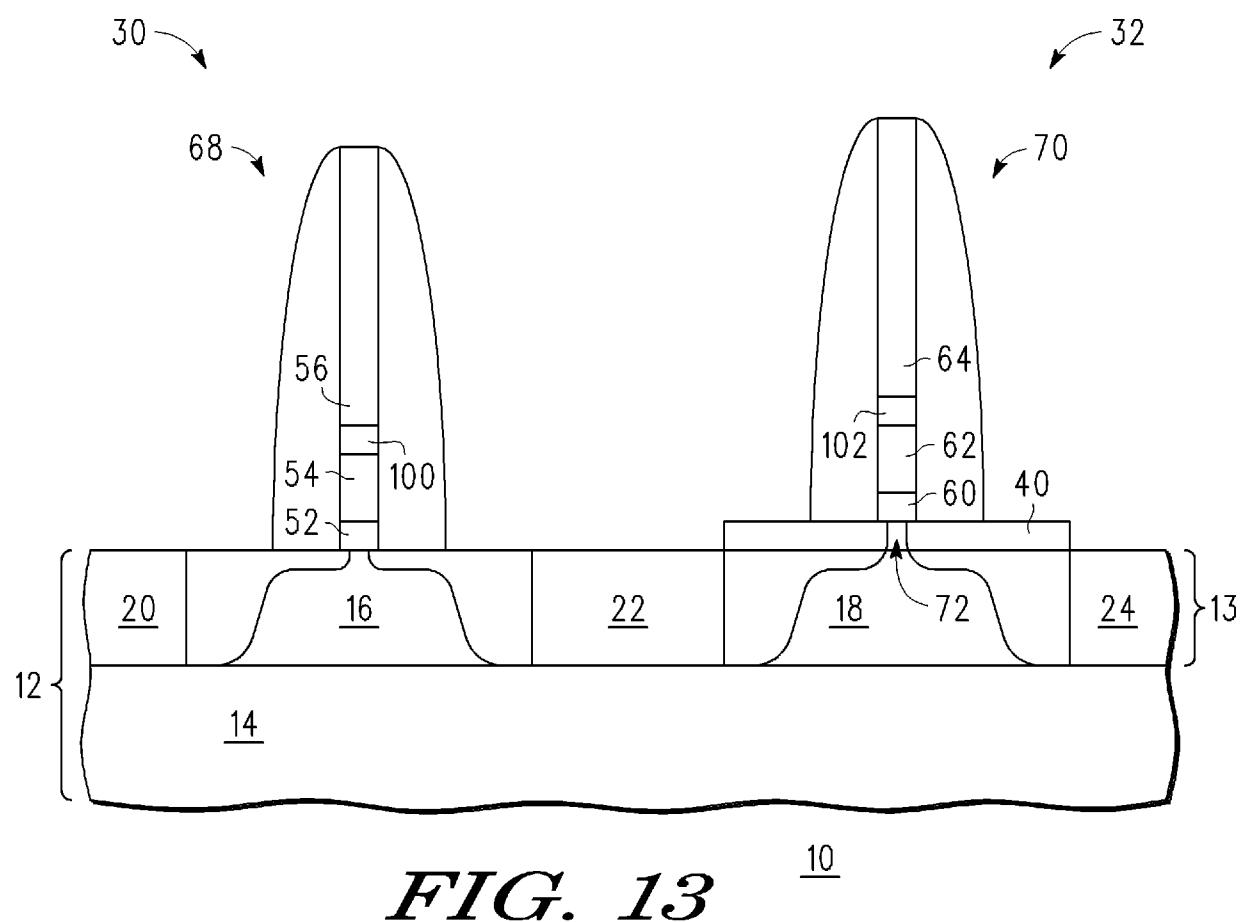
*FIG. 9*



*FIG. 10*



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## INTERNATIONAL SEARCH REPORT

International application No.  
**PCT/US2008/064192****A. CLASSIFICATION OF SUBJECT MATTER*****H01L 21/336(2006.01)i, H01L 29/78(2006.01)i***

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

IPC 8 : as above

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched  
Korean Utility Models and application for Utility Models since 1975  
Japanese Utility models and applications for Utility Models since 1975Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)  
eKIPASS(KIPO internal) "dual", "gate"**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 2004095527 A2(FREESCALE SEMICONDUCTOR INC.) 04 NOVEMBER 2004 See claims and figs 3-7	1-20
A	US 20060157796 A1(KIM, MIN-JOO et al.) 20 JULY 2006 See claims and figs 1-6	1-20
A	US 20070111453 A1(LEE, HYE-LAN et al.) 17 MAY 2007 See claims and figs 2-5	1-20
A	US 6794252 B2(ANTONIO L.P.ROTONDARO; MARK R. VISOKAY) 21 SEPTEMBER 2004 See claims and figs 1A-1D	1-20

 Further documents are listed in the continuation of Box C. See patent family annex.

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Date of the actual completion of the international search  
26 NOVEMBER 2008 (26.11.2008)

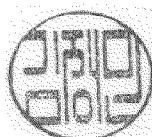
Date of mailing of the international search report

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KIM Jung Min

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**INTERNATIONAL SEARCH REPORT**

Information on patent family members

International application No.

**PCT/US2008/064192**

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