

TUNING OF FLOATING GATE SELECT TRANSISTOR IN NAND-STRING**BACKGROUND**

5 [0001] This application relates to the operation of re-programmable non-volatile memory systems such as semiconductor flash memory which record data using charge stored in charge storage elements of memory cells.

10 [0002] Solid-state memory capable of nonvolatile storage of charge, particularly in the form of EEPROM and flash EEPROM packaged as a small form factor card, has recently become the storage of choice in a variety of mobile and handheld devices, notably information appliances and consumer electronics products. Unlike RAM (random access memory) that is also solid-state memory, flash memory is non-volatile, and retains its stored data even after power is turned off. Also, unlike ROM (read only memory), flash memory is rewritable similar to a disk storage device. In spite of the higher cost, flash memory is increasingly being used in mass storage
15 applications.

[0003] Flash EEPROM is similar to EEPROM (electrically erasable and programmable read-only memory) in that it is a non-volatile memory that can be erased and have new data written or “programmed” into their memory cells. Both utilize a floating (unconnected) conductive gate, in a field effect transistor structure,
20 positioned over a channel region in a semiconductor substrate, between source and drain regions. A control gate is then provided over the floating gate. The threshold voltage characteristic of the transistor is controlled by the amount of charge that is retained on the floating gate. That is, for a given level of charge on the floating gate, there is a corresponding voltage (threshold) that must be applied to the control gate
25 before the transistor is turned “on” to permit conduction between its source and drain regions. Flash memory such as Flash EEPROM allows entire blocks of memory cells to be erased at the same time.

[0004] The floating gate can hold a range of charges and therefore can be programmed to any threshold voltage level within a threshold voltage window. The
30 size of the threshold voltage window is delimited by the minimum and maximum threshold levels of the device, which in turn correspond to the range of the charges that can be programmed onto the floating gate. The threshold window generally

depends on the memory device's characteristics, operating conditions and history. Each distinct, resolvable threshold voltage level range within the window may, in principle, be used to designate a definite memory state of the cell.

[0005] In order to improve read and program performance, multiple charge storage elements or memory transistors in an array are read or programmed in parallel. Thus, a "page" of memory elements are read or programmed together. In existing memory architectures, a row typically contains several interleaved pages or it may constitute one page. All memory elements of a page are read or programmed together.

[0006] Nonvolatile memory devices are also manufactured from memory cells with a dielectric layer for storing charge. Instead of the conductive floating gate elements described earlier, a dielectric layer is used. Such memory devices utilizing dielectric storage element have been described by Eitan et al., "NROM: A Novel Localized Trapping, 2-Bit Nonvolatile Memory Cell," IEEE Electron Device Letters, vol. 21, no. 11, November 2000, pp. 543-545. An ONO dielectric layer extends across the channel between source and drain diffusions. The charge for one data bit is localized in the dielectric layer adjacent to the drain, and the charge for the other data bit is localized in the dielectric layer adjacent to the source. For example, United States patents nos. 5,768,192 and 6,011,725 disclose a nonvolatile memory cell having a trapping dielectric sandwiched between two silicon dioxide layers. Multi-state data storage is implemented by separately reading the binary states of the spatially separated charge storage regions within the dielectric.

SUMMARY OF THE INVENTION

[0007] Examples of the present invention relate to schemes to monitor select transistors and dummy transistors and to return their threshold voltages to desired ranges if they deviate from those ranges. In certain 3-dimensional memory arrays, select transistors include charge storage elements that may come to contain some charge (even if charge is never deliberately stored there). In order to maintain select transistors in a specified range, threshold voltages of select transistors may be determined, and charge may be added or removed as needed. Similarly, dummy cells may have their threshold voltages checked and restored to a desired range.

[0008] An example of a method of operating a 3-D charge-storage memory array

includes: determining a threshold voltage of a select transistor that is connected in series with a string of memory cells; comparing the threshold voltage of the select transistor with a desirable range of select transistor threshold voltage; and in response to determining that the threshold voltage of the select transistor is outside of the desirable range of select transistor threshold voltage, performing an operation to change the threshold voltage of the select transistor.

[0009] The operation to change the threshold voltage may add charge to a charge storage element of the select transistor. The operation to change the threshold voltage may remove charge from the charge storage element of the select transistor. The operation to change the threshold voltage may first remove charge from a charge storage element of the select transistor and may then add charge to the charge storage element of the select transistor. A threshold voltage of a dummy memory cell that is connected in series with the string of memory cells may also be determined, the dummy memory cell containing no data. The determining, the comparing, and the performing may be steps in an initialization for the 3-D charge-storage memory array. The determining, the comparing, and the performing may be steps performed in response to a triggering event after the 3-D charge storage memory array has been used for a period of time. The triggering event may be either: (a) the period of time exceeds a predetermined threshold, (b) the select transistor experiences wear that exceeds a predetermined amount, or (c) Error Correction Code (ECC) results indicate increased errors in the string of memory cells that is connected in series with the select transistor.

[0010] An example of a method of operating a 3-D charge-storage memory array includes: determining a threshold voltage of a dummy memory cell that is not used to store data, the dummy memory cell connected in series in a string of memory cells that are used to store data, and with at least one select transistor that is used to selectively connect the string of memory cells to conductive lines; comparing the threshold voltage of the dummy memory cell with a desirable range of dummy memory cell threshold voltage; and in response to determining that the threshold voltage of the dummy memory cell is outside of the desirable range of dummy memory cell threshold voltage, performing an operation to change the threshold

voltage of the dummy memory cell.

[0011] The operation to change the threshold voltage may add charge to a charge storage element of the dummy memory cell. The operation to change the threshold voltage may remove charge from the charge storage element of the dummy memory cell. The operation to change the threshold voltage may first remove charge from a charge storage element of the dummy memory cell and then add charge to the charge storage element of the dummy memory cell. The determining, the comparing, and the performing may be steps in an initialization for the 3-D charge-storage memory array. The determining, the comparing, and the performing may be steps performed in response to a triggering event after the 3-D charge storage memory array has been used for a period of time. The triggering event may be either: (a) the period of time exceeds a predetermined threshold, (b) the select transistor experiences wear that exceeds a predetermined amount, or (c) Error Correction Code (ECC) results indicate increased errors in the string of memory cells that is connected in series with the select transistor.

[0012] An example of a 3-D charge-storage memory array includes: a plurality of NAND strings that extend in a direction that is perpendicular to a surface of a substrate, each of the plurality of NAND strings having a select transistor at each end; a plurality of select lines that are connected to gates of the select transistors to selectively connect the plurality of strings to conductive lines; and resolving circuits that are configured to resolve a threshold voltage of a select transistor.

[0013] Charge-increasing circuits may be configured to increase the threshold voltage of the select transistor. Charge-decreasing circuits may be configured to decrease the threshold voltage of the select transistor.

[0014] An example of a 3-D charge-storage memory array includes: a plurality of NAND strings that extend in a direction that is perpendicular to a surface of a substrate, each of the plurality of NAND strings having a number N of cells for storing data, and at least one dummy cell that does not store data; a dummy word line that is coupled to the dummy cells; and resolving circuits that are configured to resolve threshold voltages of the dummy cells.

[0015] Charge-increasing circuits may be configured to increase the threshold voltage of the dummy cells. Charge-decreasing circuits may be configured to decrease the threshold voltage of the dummy cells.

5 [0016] Various aspects, advantages, features and embodiments of the present invention are included in the following description of exemplary examples thereof, which description should be taken in conjunction with the accompanying drawings. All patents, patent applications, articles, other publications, documents and things referenced herein are hereby incorporated herein by this reference in their entirety for all purposes. To the extent of any inconsistency or conflict in the definition or use of
10 terms between any of the incorporated publications, documents or things and the present application, those of the present application shall prevail.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] **FIG. 1** illustrates schematically the main hardware components of a memory system suitable for implementing the present invention.

15 [0018] **FIG. 2** illustrates schematically a non-volatile memory cell.

[0019] **FIG. 3** illustrates the relation between the source-drain current I_D and the control gate voltage V_{CG} for four different charges Q_1 - Q_4 that the floating gate may be selectively storing at any one time at fixed drain voltage.

20 [0020] **FIG. 4A** illustrates schematically a string of memory cells organized into a NAND string.

[0021] **FIG. 4B** illustrates an example of a NAND array 210 of memory cells, constituted from NAND strings 50 such as that shown in **FIG. 4A**.

[0022] **FIG. 5** illustrates a page of memory cells, organized in the NAND configuration, being sensed or programmed in parallel.

25 [0023] **FIGs. 6A-6C** illustrate an example of programming a population of 4-state memory cells.

[0024] **FIG. 7** shows an example of a physical structure of a 3-D memory array.

[0025] FIG. 8 shows detail of a physical structure of a 3-D memory array.

[0026] FIG. 9 shows an example of a NAND string with select transistors and dummy cells.

5 [0027] FIGS. 10A-10D show examples of threshold voltage distributions for select transistors.

[0028] FIG. 11 illustrates a scheme for select transistor monitoring.

[0029] FIG. 12 illustrates a scheme for increasing threshold voltage.

[0030] FIG. 13 illustrates a scheme for decreasing threshold voltage.

10 [0031] FIG. 14 shows an example of hardware for managing select transistors and dummy cells.

DETAILED DESCRIPTION

MEMORY SYSTEM

[0032] FIG. 1 illustrates schematically the main hardware components of a memory system suitable for implementing the present invention. The memory system 90 typically operates with a host 80 through a host interface. The memory system is typically in the form of a memory card or an embedded memory system. The memory system 90 includes a memory 102 whose operations are controlled by a controller 100. The memory 102 comprises one or more array of non-volatile memory cells distributed over one or more integrated circuit chip. The controller 100 may include interface circuits 110, a processor 120, ROM (read-only-memory) 122, RAM (random access memory) 130, programmable nonvolatile memory 124, and additional components. The controller is typically formed as an ASIC (application specific integrated circuit) and the components included in such an ASIC generally depend on the particular application.

25 Physical Memory Structure

[0033] FIG. 2 illustrates schematically a non-volatile memory cell. The memory cell 10 can be implemented by a field-effect transistor having a charge storage unit 20,

such as a floating gate or a dielectric layer. The memory cell 10 also includes a source 14, a drain 16, and a control gate 30.

[0034] There are many commercially successful non-volatile solid-state memory devices being used today. These memory devices may employ different types of memory cells, each type having one or more charge storage element.

[0035] Typical non-volatile memory cells include EEPROM and flash EEPROM. Examples of EEPROM cells and methods of manufacturing them are given in United States patent no. 5,595,924. Examples of flash EEPROM cells, their uses in memory systems and methods of manufacturing them are given in United States patents nos. 5,070,032, 5,095,344, 5,315,541, 5,343,063, 5,661,053, 5,313,421 and 6,222,762. In particular, examples of memory devices with NAND cell structures are described in United States patent nos. 5,570,315, 5,903,495, 6,046,935. Also, examples of memory devices utilizing dielectric storage elements have been described by Eitan et al., "NROM: A Novel Localized Trapping, 2-Bit Nonvolatile Memory Cell," IEEE Electron Device Letters, vol. 21, no. 11, November 2000, pp. 543-545, and in United States patents nos. 5,768,192 and 6,011,725.

[0036] In practice, the memory state of a cell is usually read by sensing the conduction current across the source and drain electrodes of the cell when a reference voltage is applied to the control gate. Thus, for each given charge on the floating gate of a cell, a corresponding conduction current with respect to a fixed reference control gate voltage may be detected. Similarly, the range of charge programmable onto the floating gate defines a corresponding threshold voltage window or a corresponding conduction current window.

[0037] Alternatively, instead of detecting the conduction current among a partitioned current window, it is possible to set the threshold voltage for a given memory state under test at the control gate and detect if the conduction current is lower or higher than a threshold current (cell-read reference current). In one implementation the detection of the conduction current relative to a threshold current is accomplished by examining the rate the conduction current is discharging through the capacitance of the bit line.

[0038] FIG. 3 illustrates the relation between the source-drain current I_D and the

control gate voltage V_{CG} for four different charges Q1-Q4 that the floating gate may be selectively storing at any one time. With fixed drain voltage bias, the four solid I_D versus V_{CG} curves represent four of seven possible charge levels that can be programmed on a floating gate of a memory cell, respectively corresponding to four possible memory states. As an example, the threshold voltage window of a population of cells may range from 0.5V to 3.5V. Seven possible programmed memory states “0”, “1”, “2”, “3”, “4”, “5”, “6”, and an erased state (not shown) may be demarcated by partitioning the threshold window into regions in intervals of 0.5V each. For example, if a reference current, I_{REF} of 2 μA is used as shown, then the cell programmed with Q1 may be considered to be in a memory state “1” since its curve intersects with I_{REF} in the region of the threshold window demarcated by $V_{CG} = 0.5V$ and 1.0V. Similarly, Q4 is in a memory state “5”.

[0039] As can be seen from the description above, the more states a memory cell is made to store, the more finely divided is its threshold window. For example, a memory device may have memory cells having a threshold window that ranges from -1.5V to 5V. This provides a maximum width of 6.5V. If the memory cell is to store 16 states, each state may occupy from 200mV to 300mV in the threshold window. This will require higher precision in programming and reading operations in order to be able to achieve the required resolution.

20 NAND Structure

[0040] FIG. 4A illustrates schematically a string of memory cells organized into a NAND string. A NAND string 50 comprises a series of memory transistors M1, M2, ... Mn (e.g., n= 4, 8, 16 or higher) daisy-chained by their sources and drains. A pair of select transistors S1, S2 controls the memory transistor chain's connection to the external world via the NAND string's source terminal 54 and drain terminal 56 respectively. In a memory array, when the source select transistor S1 is turned on, the source terminal is coupled to a source line (see FIG. 4B). Similarly, when the drain select transistor S2 is turned on, the drain terminal of the NAND string is coupled to a bit line of the memory array. Each memory transistor 10 in the chain acts as a memory cell. It has a charge storage element 20 to store a given amount of charge so as to represent an intended memory state. A control gate 30 of each memory transistor allows control over read and write operations. As will be seen in FIG. 4B,

the control gates 30 of corresponding memory transistors of a row of NAND string are all connected to the same word line. Similarly, a control gate 32 of each of the select transistors S1, S2 provides control access to the NAND string via its source terminal 54 and drain terminal 56 respectively. Likewise, the control gates 32 of
5 corresponding select transistors of a row of NAND string are all connected to the same select line.

[0041] When an addressed memory transistor 10 within a NAND string is read or is verified during programming, its control gate 30 is supplied with an appropriate voltage. At the same time, the rest of the non-addressed memory transistors in the
10 NAND string 50 are fully turned on by application of sufficient voltage on their control gates. In this way, a conductive path is effectively created from the source of the individual memory transistor to the source terminal 54 of the NAND string and likewise for the drain of the individual memory transistor to the drain terminal 56 of the cell. Memory devices with such NAND string structures are described in United
15 States patent nos. 5,570,315, 5,903,495, 6,046,935.

[0042] **FIG. 4B** illustrates an example of a NAND array 210 of memory cells, constituted from NAND strings 50 such as that shown in **FIG. 4A**. Along each column of NAND strings, a bit line such as bit line 36 is coupled to the drain terminal 56 of each NAND string. Along each bank of NAND strings, a source line such as
20 source line 34 is coupled to the source terminals 54 of each NAND string. Also the control gates along a row of memory cells in a bank of NAND strings are connected to a word line such as word line 42. The control gates along a row of select transistors in a bank of NAND strings are connected to a select line such as select line 44. An entire row of memory cells in a bank of NAND strings can be addressed by
25 appropriate voltages on the word lines and select lines of the bank of NAND strings.

[0043] **FIG. 5** illustrates a page of memory cells, organized in the NAND configuration, being sensed or programmed in parallel. **FIG. 5** essentially shows a bank of NAND strings 50 in the memory array 210 of **FIG. 4B**, where the detail of each NAND string is shown explicitly as in **FIG. 4A**. A physical page, such as the
30 page 60, is a group of memory cells enabled to be sensed or programmed in parallel. This is accomplished by a corresponding page of sense amplifiers 212. The sensed results are latched in a corresponding set of latches 214. Each sense amplifier can be

coupled to a NAND string via a bit line. The page is enabled by the control gates of the cells of the page connected in common to a word line 42 and each cell accessible by a sense amplifier accessible via a bit line 36. As an example, when respectively sensing or programming the page of cells 60, a sensing voltage or a programming voltage is respectively applied to the common word line WL3 together with appropriate voltages on the bit lines.

Physical Organization of the Memory

[0044] One important difference between flash memory and other of types of memory is that a cell must be programmed from the erased state. That is the floating gate must first be emptied of charge. Programming then adds a desired amount of charge back to the floating gate. It does not support removing a portion of the charge from the floating gate to go from a more programmed state to a lesser one. This means that updated data cannot overwrite existing data and must be written to a previous unwritten location.

[0045] Furthermore erasing is to empty all the charges from the floating gate and generally takes appreciable time. For that reason, it will be cumbersome and very slow to erase cell by cell or even page by page. In practice, the array of memory cells is divided into a large number of blocks of memory cells. As is common for flash EEPROM systems, the block is the unit of erase. That is, each block contains the minimum number of memory cells that are erased together. While aggregating a large number of cells in a block to be erased in parallel will improve erase performance, a large size block also entails dealing with a larger number of update and obsolete data.

[0046] Each block is typically divided into a number of physical pages. A logical page is a unit of programming or reading that contains a number of bits equal to the number of cells in a physical page. In a memory that stores one bit per cell, one physical page stores one logical page of data. In memories that store two bits per cell, a physical page stores two logical pages. The number of logical pages stored in a physical page thus reflects the number of bits stored per cell. In one embodiment, the individual pages may be divided into segments and the segments may contain the fewest number of cells that are written at one time as a basic programming operation. One or more logical pages of data are typically stored in one row of memory cells. A

page can store one or more sectors. A sector includes user data and overhead data.

All-bit, Full-Sequence MLC Programming

[0047] FIG. 6A – 6C illustrate an example of programming a population of 4-state memory cells. FIG. 6A illustrates the population of memory cells programmable into four distinct distributions of threshold voltages respectively representing memory states “0”, “1”, “2” and “3”. FIG. 6B illustrates the initial distribution of “erased” threshold voltages for an erased memory. FIG. 6C illustrates an example of the memory after many of the memory cells have been programmed. Essentially, a cell initially has an “erased” threshold voltage and programming will move it to a higher value into one of the three zones demarcated by verify levels vV_1 , vV_2 and vV_3 . In this way, each memory cell can be programmed to one of the three programmed states “1”, “2” and “3” or remain un-programmed in the “erased” state. As the memory gets more programming, the initial distribution of the “erased” state as shown in FIG. 6B will become narrower and the erased state is represented by the “0” state.

[0048] A 2-bit code having a lower bit and an upper bit can be used to represent each of the four memory states. For example, the “0”, “1”, “2” and “3” states are respectively represented by “11”, “01”, “00” and “10”. The 2-bit data may be read from the memory by sensing in “full-sequence” mode where the two bits are sensed together by sensing relative to the read demarcation threshold values rV_1 , rV_2 and rV_3 in three sub-passes respectively.

3-D NAND structure

[0049] An alternative arrangement to a conventional two-dimensional (2-D) NAND array is a three-dimensional (3-D) array. In contrast to 2-D NAND arrays, which are formed along a planar surface of a semiconductor wafer, 3-D arrays extend up from the wafer surface and generally include stacks, or columns, of memory cells extending up from the wafer surface. Various 3-D arrangements are possible. In one arrangement a NAND string is formed vertically with one end (e.g. source) at the wafer surface and the other end (e.g. drain) on top. In another arrangement a NAND string is formed in a U-shape so that both ends of the NAND string are accessible on top, thus facilitating connections between such strings. Examples of such NAND strings and their formation are described in U.S. Patent Publication Number

2012/0220088.

[0050] FIG. 7 shows a physical implementation of a 3-D NAND array. The bit line extends as a continuous conductor (e.g. metal line) in the y-direction with vertical connections formed between the bit line and drains of strings. Below the bit line, common source lines extend perpendicular to the cross section shown (i.e. extend in the x-direction) and connect sources of neighboring strings. Source select lines extend in the x-direction and form source select gates (SGS) where they intersect vertical columns. Drain select lines extend in the x-direction and form drain select gates (SGD) where they intersect vertical columns. Word lines WL0-WL63 extend in the x-direction and form control gates of memory cells where they intersect vertical columns. Dummy word lines are provided between word lines and select gates, with one dummy word line WLDS between the source select gate and word lines, and another dummy word line WLDD between the drain select gate and word lines. In one example, word lines, including dummy word lines, are formed from conductive layers separated by dielectric layers, with channels of memory cells being formed in vertical holes (“memory holes”) that extend through the conductive layers and dielectric layers.

[0051] FIG. 8 shows the structure of a stack of layers in the memory holes that form memory cells. It can be seen that a blocking dielectric “Block” is deposited on the walls of the memory hole to provide electrical isolation. A Charge Trapping Layer (CTL) is deposited on the blocking dielectric. The CTL forms charge storage elements where the CTL is in close proximity to polysilicon word lines. A tunnel dielectric is deposited to provide electrical isolation and to allow charge to tunnel into the CTL under certain conditions. A channel material is deposited to form the channel of the memory cells along the string. A core material is deposited that forms the core of the column that is located in the memory hole.

[0052] When a NAND string is made using a memory hole, layers are deposited within the cylindrical memory hole so that the memory hole is filled in a substantially uniform manner with all deposited layers being present in at all levels (though some variation in memory hole diameter and other dimensions may occur). In contrast to planar NAND, where films deposited on a substrate surface can be patterned by photolithography, films deposited within a memory hole are generally not exposed in

a manner that allows such patterning.

Select Transistors

[0053] One result of a uniform cylindrical structure like that shown in FIG. 8 is that select transistors are formed that contain charge storage elements. In planar NAND it is common to form select gates without charge storage elements. Two polysilicon layers (corresponding to floating gate layer and control gate layer) may be connected to form a single gate in a select transistor. Such connection requires an additional patterning step to form openings in inter-poly dielectric in select transistors (while leaving inter-poly dielectric intact in memory cells). Alternatively, a portion of a floating gate polysilicon or charge trapping layer may be removed from a select transistor. This also requires some patterning. Such additional patterning may not be possible in many 3-D memories. In general, there is no easy way to remove a portion of a charge trapping layer or otherwise eliminate a charge storage element from a select transistor in 3-D memory. Therefore, a select transistor may contain a charge storage element. While such a transistor may not be programmed with any data, the charge storage element may acquire or lose charge because of memory operations directed to memory cells (e.g. because of biases applied to the select gate and channel during read, write, or erase operations directed to memory cells).

[0054] FIG. 9 is a schematic showing a U-shaped NAND string similar to those of FIG. 7. (Not all cells are shown for clarity of illustration; dashed lines indicate omitted memory cells.) Source and drain transistors connect either end of the string to external terminals and a back gate "BG" connects the two sides of the U-shaped NAND string. Two dummy cells, D0 and D1, are provided at the source end of the string, and two dummy cells, D2 and D3, are provided at the drain end of the string, for a total of four dummy cells in the string (in contrast, FIG. 7 showed one dummy cell at each end for a total of two dummy cells per string). Other examples may have different numbers of dummy cells. For example, where sub-block erase is used, dummy cells may be located along boundaries between sub-blocks.

[0055] Source and drain select transistors are provided at either end of the string to allow the string to be selectively connected to external connections for reading, writing, and erasing. A source select transistor is configurable (through a voltage

applied to the source select line) to connect the source end of the NAND string to a source terminal (e.g. to a common source line). A drain select transistor is configurable (through a voltage applied to the drain select line) to connect the drain end of the NAND string to a drain terminal (e.g. to a bit line). In contrast to the select transistors S1 and S2 of FIG. 4A, these select transistors include charge storage elements (as indicated by dotted line). Charge that is trapped in such charge storage elements may affect the threshold voltages of the select transistors in the same way that charge trapped in charge storage elements of memory cells affects memory cell threshold voltage.

10 [0056] In some cases, the threshold voltage of a select transistor may be tuned to a desired range so that it turns on and off when corresponding voltages are applied to its select line. This means bringing the threshold voltage to a desired range that may be similar to one of the ranges shown in FIG. 6, or may be different. FIG. 10A shows an example of a distribution of select transistors in a desirable threshold voltage range
15 that is between V_1 and V_2 . If the threshold voltage of a select transistor changes significantly from this range then the select transistor may not turn on and off as required. If charge in the charge storage element either increases or decreases so that the charge is outside a specified range the select transistor may no longer operate as specified. In order to have all strings operating correctly as their gates are driven by
20 predetermined voltages it is necessary to have threshold voltages of select gates within a certain window (i.e. a reasonably narrow distribution). If select transistors lose charge (threshold voltage distribution shifts down) as shown in FIG. 10B or gain charge (threshold voltage distribution shifts up) as shown in FIG. 10C, or if select transistors have random changes in charge levels (threshold voltage distribution
25 becomes wider) as shown in FIG. 10D then problems may occur.

[0057] As in planar NAND, the current through a string under different word line bias conditions is used to determine the state of memory cells along the selected word line. Thus, source and drain select transistors, which are connected in series with the memory cells may affect how a memory cell is read. In principle, all unselected word
30 lines and the source and drain select gates of a string have high voltages applied to make the unselected memory cells and the select transistors turn on. However, if select transistors have acquired significant charge in their charge storage elements

then they may not fully turn on and may provide significant series resistance. Such series resistance may cause a misreading. Similarly, during programming along a selected string, additional resistance from select transistors may affect verification and thus cause cells to be incorrectly programmed.

- 5 [0058] Source and drain select transistors are also required to turn off in order to isolate strings from source terminals and drain terminals at certain times (e.g. isolating unselected strings during reading of a selected string). If a select transistor threshold voltage is too low then the select transistor may not turn off adequately thus keeping some connection between an unselected string and source and/or drain terminals. This
10 may allow some current through unselected strings which affects bit line current and may cause data to be misread. Various other problems may result from failure of select transistors to turn on or turn off as required.

- [0059] In order to maintain the threshold voltage of a select transistor within a desired range, the threshold voltage may be monitored to see if it is within the predetermined
15 range and restore it to the predetermined range if it is no longer within the predetermined range. The threshold voltage may be monitored periodically during the lifecycle of the memory (e.g. based on a time stamp or other time indicator), or may be monitored in response to some triggering event. Hot count (the number of write/erase cycles) may be used to trigger monitoring. For example, select transistors
20 may be monitored every N cycles (e.g. every 1000 cycles). Alternatively, monitoring may be performed in response to increasing numbers of ECC errors so that when the number of ECC errors exceeds a threshold number then monitoring is performed. Other triggering events may also be used.

- [0060] FIG. 11 shows an example of a scheme to monitor a select transistor 141.
25 Initially, the threshold voltage of a select transistor is determined 143. This determination may be performed in a similar manner to reading a memory cell (e.g. memory cells are turned on and a sense amplifier is used to sense current or voltage on the bit line while one or more voltages are applied to the select line that controls the select transistor). If the threshold voltage is below the specified range 145 then an
30 operation may be carried out to increase the threshold voltage 147. If the threshold voltage is above the specified range 149 then an operation may be carried out to reduce the threshold voltage 151. If the threshold voltage is within the specified range

(neither above nor below the specified range) then the monitoring operation ends 153 and the select transistor may continue to be used without change.

5 [0061] Where the desirable threshold voltage range of a select transistor is greater than zero (i.e. some charge on the charge storage element is desirable) the threshold voltage may fall below the desired range through current leakage. Such leakage corresponds to similar leakage in memory cells which is related to data retention issues. Loss of charge through such leakage may be counteracted by adding charge in an operation that is analogous to a programming operation applied to a memory cell.

10 [0062] FIG. 12 shows an example of an operation to increase the threshold voltage of a select transistor 261 by a series of steps. A programming voltage is supplied to the select line that connects to the gate of the select transistor while the channel is kept at a low voltage 263. The programming may be performed by applying one or more pulses, with different pulses having the same or different voltages. After a given pulse, or series of pulses, a verification step determines if the threshold voltage is
15 outside the specified range 265. If it remains outside the specified range then another pulse, or series of pulses, is applied. If the threshold voltage is within the specified range then the operation ends 267 and the select transistor is ready for use.

[0063] The operation of FIG. 12 may be used as part of memory configuration or initialization. For example, where the desirable range of threshold voltage is not the
20 threshold voltage of a newly-manufactured select transistor then an operation may be performed after manufacturing, prior to use, to bring the threshold voltage within the desired range. Such initial tuning of the select transistor threshold voltage may be performed at the factory, or later, after the product is shipped, for example when it is first powered on.

25 [0064] If the threshold voltage of the select transistor is too high then it may be reduced as shown in FIG. 13. A threshold voltage reduction operation 381 may be considered to be analogous to an erase operation applied to a memory cell. An erase voltage is applied to the select line of the select transistor 383. This may be a low voltage. At the same time a positive voltage is applied to the channel of the NAND
30 string. After this step, a determination is made as to whether the select transistor is fully erased 385. The steps are repeated until it is determined to be fully erased. In

many cases, the desired threshold voltage range is not the erased state, so that the erase operation is followed by increasing the threshold voltage 387 (e.g. according to FIG. 12) in order to return the threshold voltage to the desired range. In some schemes, tuning always includes erasing prior to increasing the threshold voltage by
5 adding charge. In other schemes, charge may be added without necessarily erasing first. Once the desired threshold voltage range is achieved, the process ends 389.

[0065] Monitoring and tuning select transistor threshold voltage may be performed on any grouping of select transistors. For example, all select transistors of a block may be monitored and tuned together, or monitoring and tuning may be performed on a select
10 line by select line basis. In some cases, multiple blocks may be treated together as a unit for monitoring and tuning of select transistor threshold voltages.

[0066] In many cases, patterns of change may be observed in threshold voltages of select transistors. For example, all select transistors of a block may show an increase, or decrease, in threshold voltage at a reasonably predictable rate. In such cases, it may
15 not be necessary to perform tuning on a transistor-by-transistor, or line-by-line basis. One or more sample transistors may be taken as representative of a group of transistors. Conditions that return the sample transistors to the desired threshold voltage range may be assumed to return other similar transistors to the desired threshold voltage range. Thus, one select line in a block may be considered as a
20 sample that is subject to erase until it is confirmed that select transistors along the line have threshold voltages corresponding to an erased condition. Other select transistors may be subjected to the same erase conditions without separate erase verification (i.e. it may be assumed that they will be similarly erased by the same conditions). One or more select lines may similarly be considered as samples when increasing threshold
25 voltage also, with verification applied to only sample transistors, and other transistors simply subjected to the same conditions without necessarily being separately verified.

Dummy Cells

[0067] In some cases, one or more memory cells in a NAND string may be considered as dummy cells that are not used to store data. For example, as shown in
30 FIGs. 7 and 9, a memory cell, or two memory cells immediately adjacent to a select transistor may be dummy cells. These cells may be considered unreliable for storage

of data because of the effects of adjacent select transistors. Thus, rows of dummy cells may be formed, connected by dummy word lines. In many cases, such dummy cells are largely ignored during operation of a memory array as they do not contain data (no data is programmed or read in such cells). However, charge storage elements of such cells may acquire or lose charge during access to other cells. Therefore, their threshold voltages may shift over time. As a result, such cells may not respond as expected when a voltage is applied to their control gate. For example, they may fail to turn on fully when required. Where dummy word lines are over-driven to boost channel voltage, changes in dummy cell threshold voltages may affect boosting and thus, for example, impact unselected strings during programming.

[0068] In general, the approach described above, that is used to tune threshold voltages of select transistors, may also be used to tune threshold voltages of dummy cells. For example, dummy cells may be subject to an initialization procedure that adds charge to their charge storage elements so that their threshold voltages fall within a desirable range. Dummy cells may be subject to monitoring of their threshold voltages and may be returned to their specified threshold voltage ranges when monitoring indicates that their threshold voltages are outside of a specified range. Monitoring, threshold voltage increasing, and threshold voltage reduction in dummy cells may be performed as in FIGs. 11, 12, and 13 respectively.

[0069] While select transistors and dummy memory cells may be similarly monitored and may have their threshold voltages similarly tuned, these operations may be performed separately (although performing them together may be convenient in some cases). For example, monitoring of select transistors may be triggered by a first triggering event while monitoring of dummy cells may be triggered by a different event. Select transistors may be tuned to a first threshold voltage range, while dummy memory cells are tuned to a second threshold voltage range. Where multiple dummy word lines are present in a string they may be separately monitored and tuned, or may be monitored and tuned together. Select transistor and dummy cell tuning may be done in conjunction with operations directed to the memory cells (e.g. when a block is garbage collected) or may be done independently, e.g. while the memory cells continue to hold valid data. Select transistor and dummy cell monitoring and tuning may be performed as background operations that are performed when the memory

array is idle, or may be performed in the foreground with a signal provided to indicate that the memory is busy.

[0070] Various hardware may be used to carry out aspects of the present invention. FIG. 14 shows one example where peripheral circuits 401 on a memory chip 403 include threshold voltage resolving circuits 405 to resolve the threshold voltages of select transistors and/or dummy cells in a 3-D NAND array 406 (different embodiments may have one or the other, or both). Such circuits may be similar in configuration to reading circuits used to read memory cells. Also shown are charge-increasing circuits 407, which also may be for select transistors and/or dummy cells. Charge-increasing circuits may be similar to programming circuits used to program data to memory cells. However, charge-increasing circuits generally add charge uniformly to select transistors or dummy cells to bring them to a uniform specified level, whereas programming circuits program memory cells to various levels that reflect data to be stored. Also shown are charge-decreasing circuits 409, which may be for select transistors and/or dummy cells. Charge-decreasing circuits may be similar to erase circuits used to erase memory cells.

Conclusion

[0071] The foregoing detailed description of the invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Many modifications and variations are possible in light of the above teaching. The described embodiments were chosen in order to best explain the principles of the invention and its practical application, to thereby enable others skilled in the art to best utilize the invention in various embodiments and with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the claims appended hereto.

IT IS CLAIMED:

1. A method of operating a 3-D charge-storage memory array comprising:
determining a threshold voltage of a select transistor that is connected
5 in series with a string of memory cells;
comparing the threshold voltage of the select transistor with a desirable range of select transistor threshold voltage; and
in response to determining that the threshold voltage of the select transistor is outside of the desirable range of select transistor threshold
10 voltage, performing an operation to change the threshold voltage of the select transistor.
2. The method of claim 1 wherein the operation to change the threshold voltage adds charge to a charge storage element of the select
15 transistor.
3. The method of claim 1 wherein the operation to change the threshold voltage removes charge from the charge storage element of the select transistor.
20
4. The method of claim 1 wherein the operation to change the threshold voltage first removes charge from a charge storage element of the select transistor and then adds charge to the charge storage element of the select transistor.
25
5. The method of claim 1 further comprising determining a threshold voltage of a dummy memory cell that is connected in series with the string of memory cells, the dummy memory cell containing no data.
6. The method of claim 1 wherein the determining, the comparing, and the performing are steps in an initialization for the 3-D charge-storage memory array.
30

7. The method of claim 1 wherein the determining, the comparing, and the performing are steps performed in response to a triggering event after the 3-D charge storage memory array has been used for a period of time.

5

8. The method of claim 7 wherein the triggering event is either: (a) the period of time exceeds a predetermined threshold, (b) the select transistor experiences wear that exceeds a predetermined amount, or (c) Error Correction Code (ECC) results indicate increased errors in the string of memory cells that is connected in series with the select transistor.

10

9. A method of operating a 3-D charge-storage memory array comprising:

15

determining a threshold voltage of a dummy memory cell that is not used to store data, the dummy memory cell connected in series in a string of memory cells that are used to store data, and with at least one select transistor that is used to selectively connect the string of memory cells to conductive lines;

20

comparing the threshold voltage of the dummy memory cell with a desirable range of dummy memory cell threshold voltage; and

in response to determining that the threshold voltage of the dummy memory cell is outside of the desirable range of dummy memory cell threshold voltage, performing an operation to change the threshold voltage of the dummy memory cell.

25

10. The method of claim 9 wherein the operation to change the threshold voltage adds charge to a charge storage element of the dummy memory cell.

30

11. The method of claim 9 wherein the operation to change the threshold voltage removes charge from the charge storage element of the dummy memory cell.

12. The method of claim 9 wherein the operation to change the threshold voltage first removes charge from a charge storage element of the dummy memory cell and then adds charge to the charge storage element of the dummy memory cell.

5

13. The method of claim 9 wherein the determining, the comparing, and the performing are steps in an initialization for the 3-D charge-storage memory array.

10

14. The method of claim 9 wherein the determining, the comparing, and the performing are steps performed in response to a triggering event after the 3-D charge storage memory array has been used for a period of time.

15

15. The method of claim 14 wherein the triggering event is either: (a) the period of time exceeds a predetermined threshold, (b) the select transistor experiences wear that exceeds a predetermined amount, or (c) Error Correction Code (ECC) results indicate increased errors in the string of memory cells that is connected in series with the select transistor.

20

16. A 3-D charge-storage memory array comprising:
a plurality of NAND strings that extend in a direction that is perpendicular to a surface of a substrate, each of the plurality of NAND strings having a select transistor at each end;

25

a plurality of select lines that are connected to gates of the select transistors to selectively connect the plurality of strings to conductive lines;
and

resolving circuits that are configured to resolve a threshold voltage of a select transistor.

30

17. The 3-D charge-storage memory array of claim 16 further comprising charge-increasing circuits that are configured to increase the threshold voltage of the select transistor.

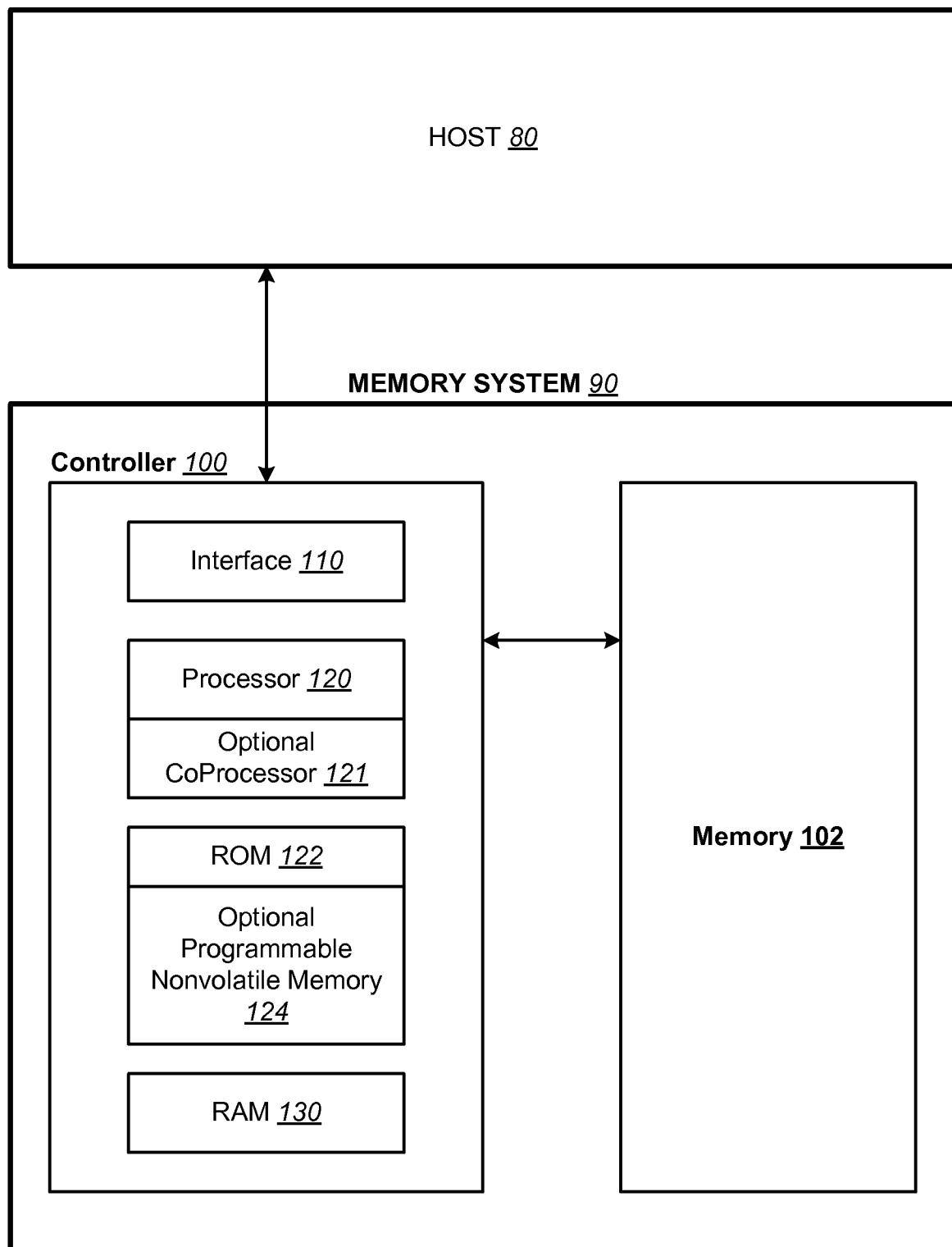
18. The 3-D charge-storage memory array of claim 16 further comprising charge-decreasing circuits that are configured to decrease the threshold voltage of the select transistor.

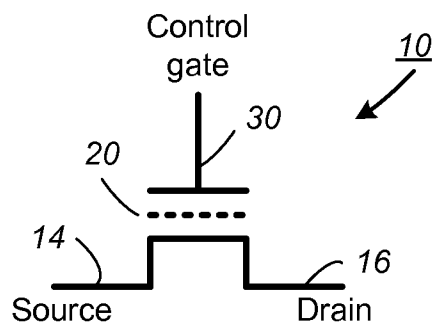
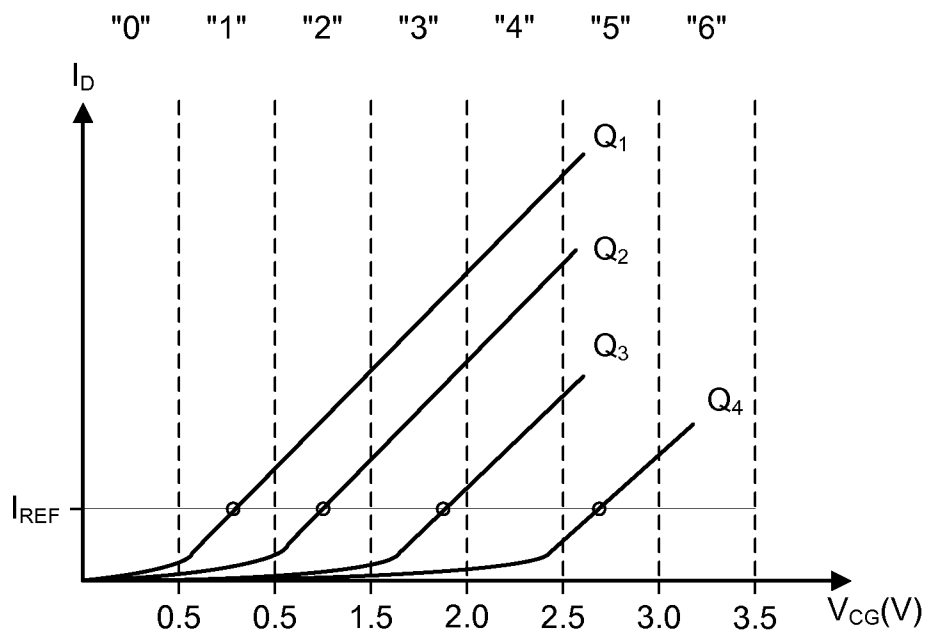
5 19. A 3-D charge-storage memory array comprising:
a plurality of NAND strings that extend in a direction that is perpendicular to a surface of a substrate, each of the plurality of NAND strings having a number N of cells for storing data, and at least one dummy cell that does not store data;
10 a dummy word line that is coupled to the dummy cells; and
resolving circuits that are configured to resolve threshold voltages of the dummy cells.

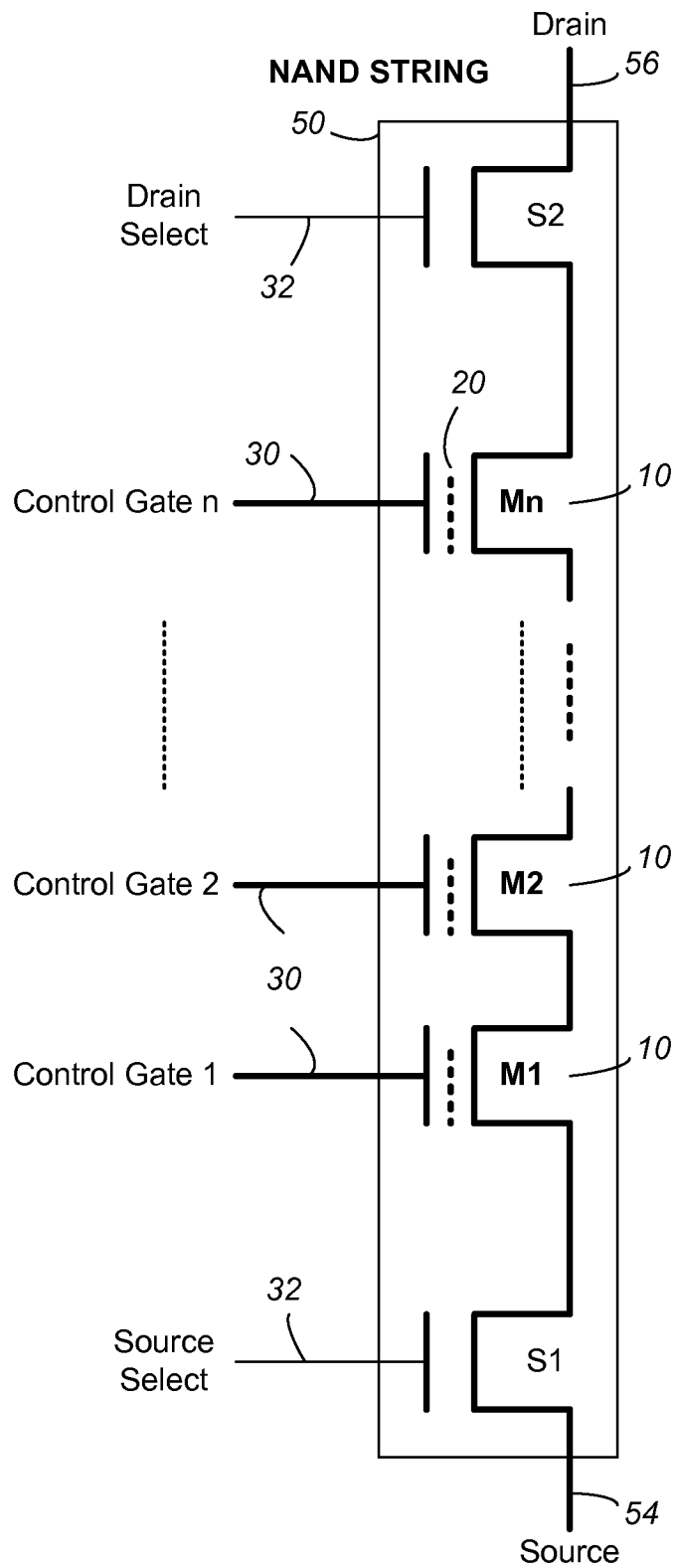
20. The 3-D charge-storage memory array of claim 19 further
15 comprising charge-increasing circuits that are configured to increase the threshold voltage of the dummy cells.

21. The 3-D charge-storage memory array of claim 19 further
20 comprising charge-decreasing circuits that are configured to decrease the threshold voltage of the dummy cells.

25

**FIG. 1**

**FIG. 2****FIG. 3**

**FIG. 4A**

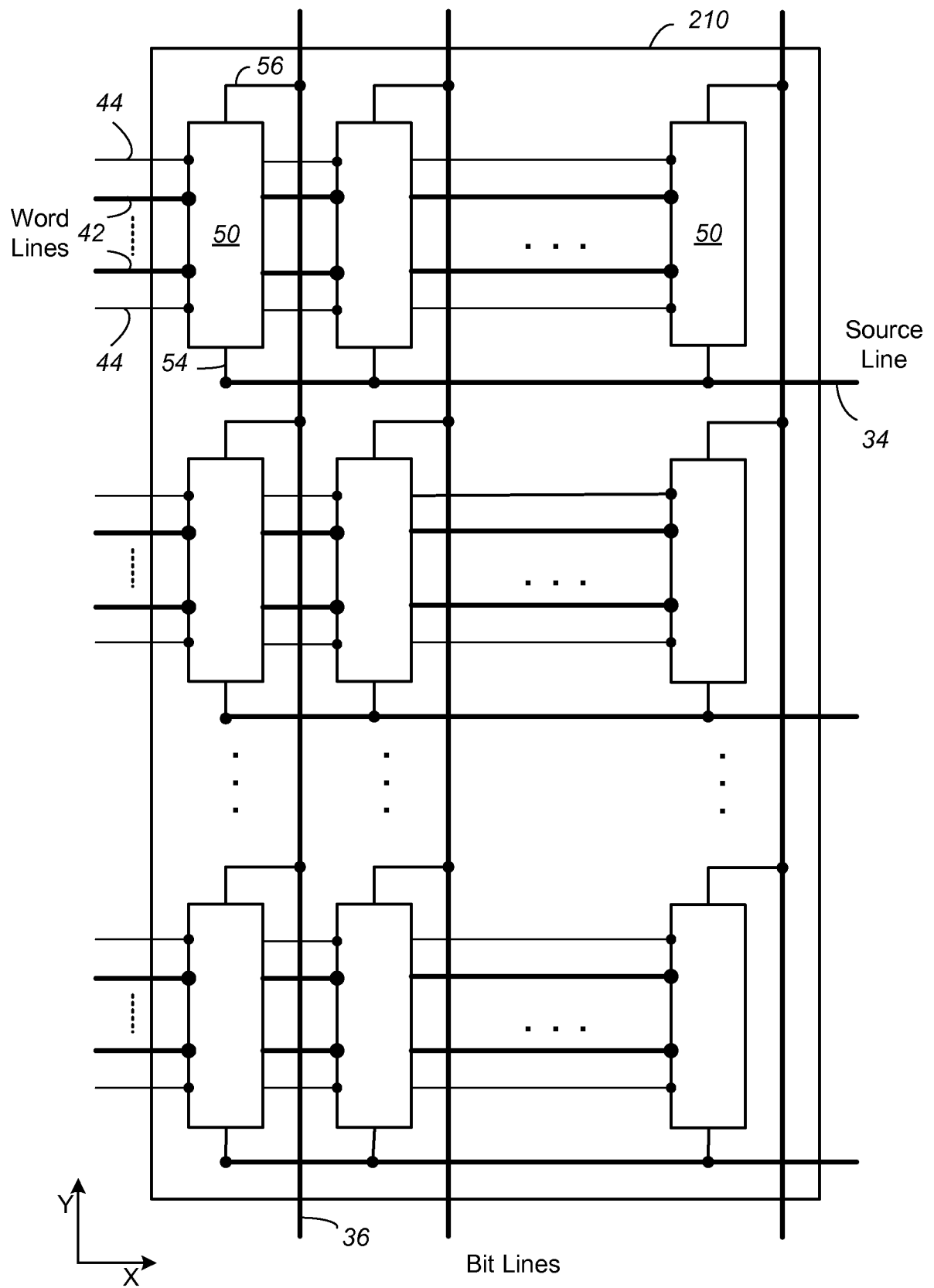
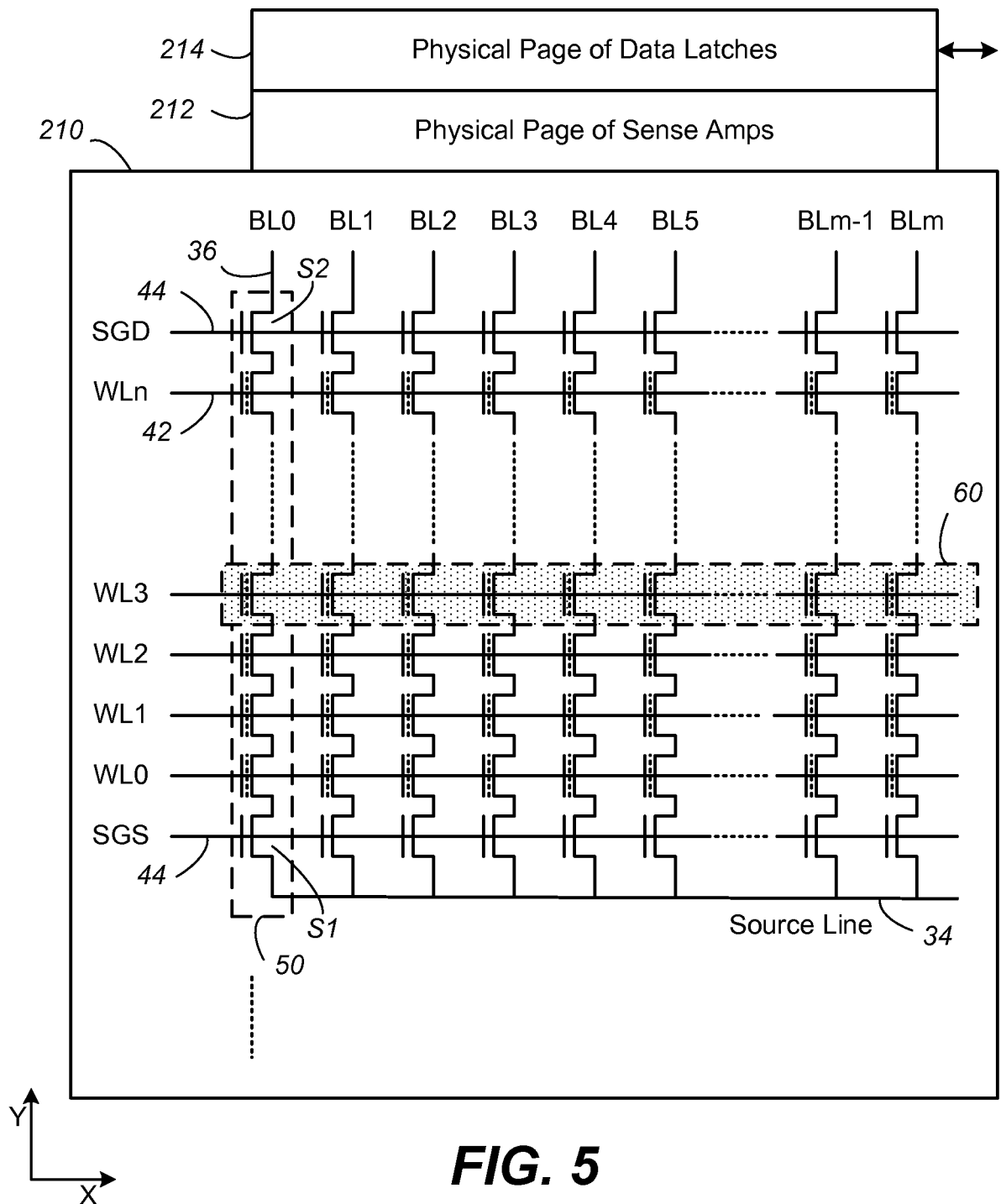
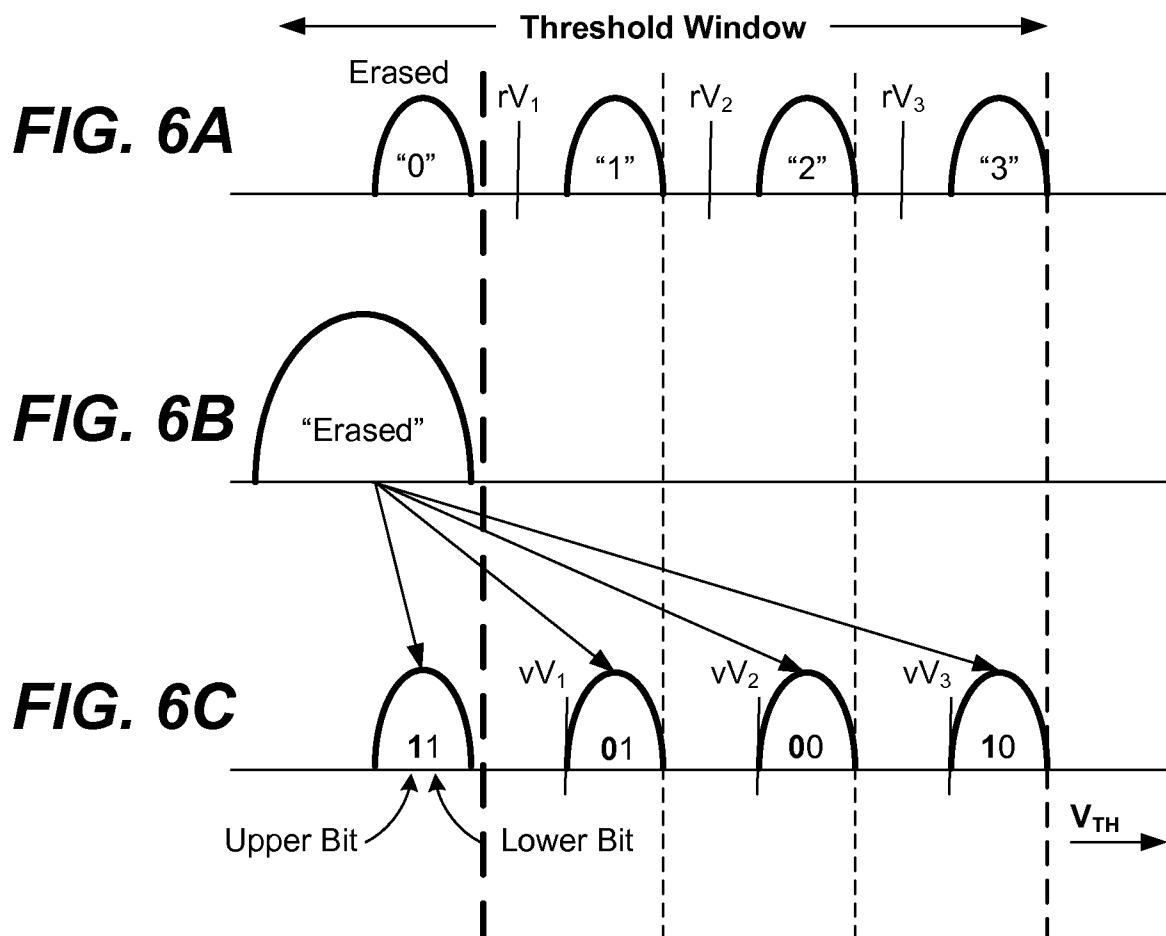


FIG. 4B





Programming into four states represented by a 2-bit code

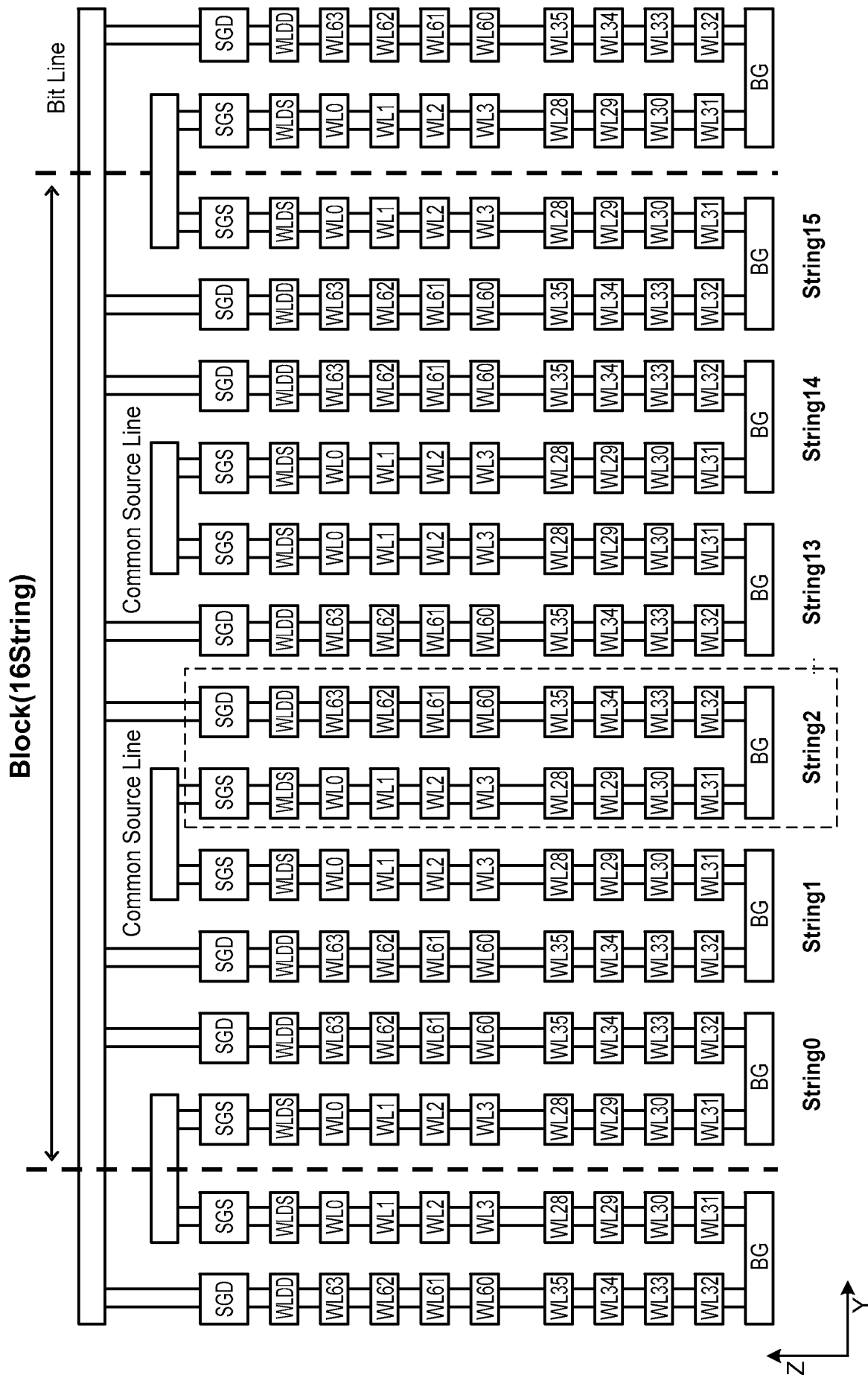
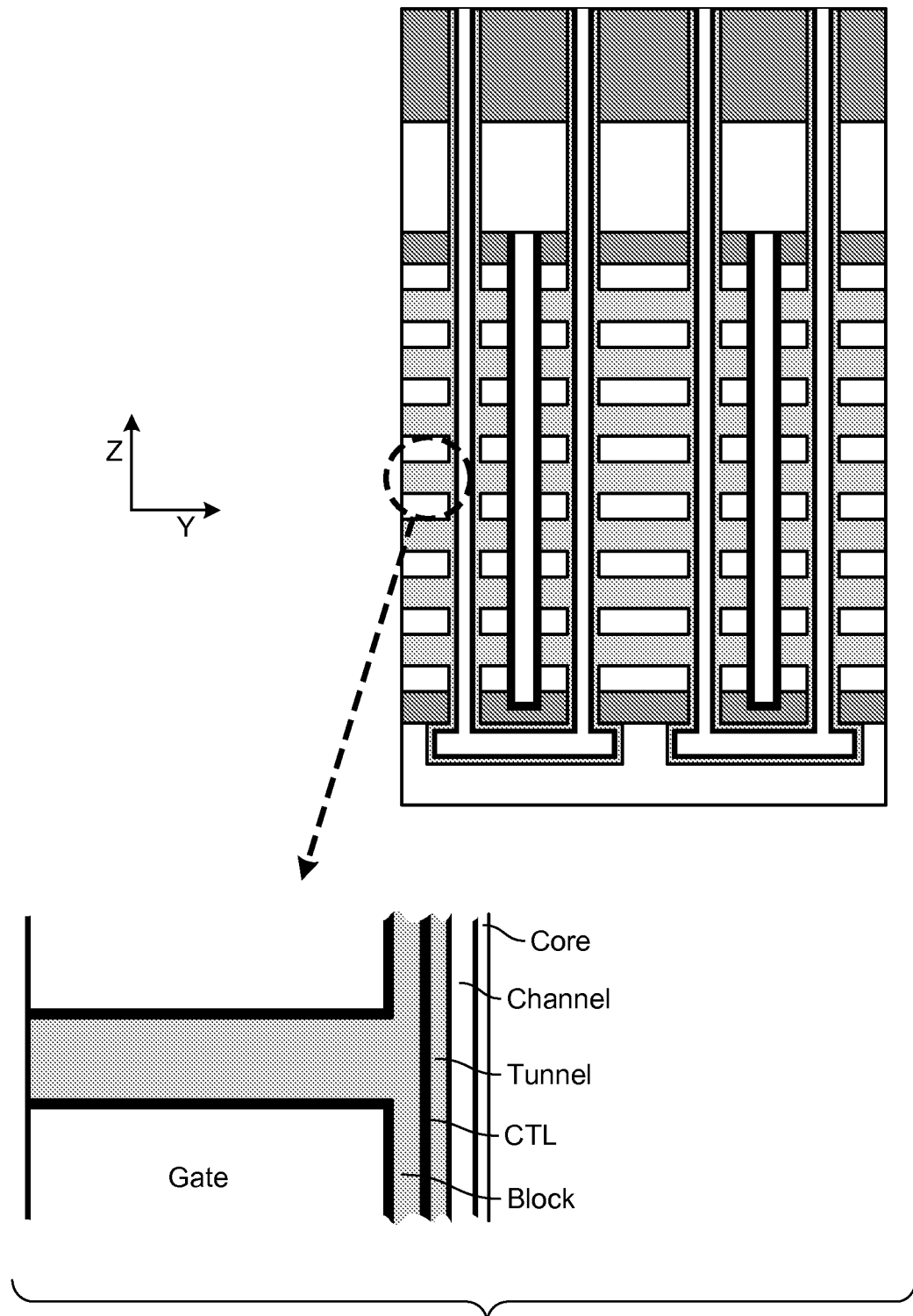
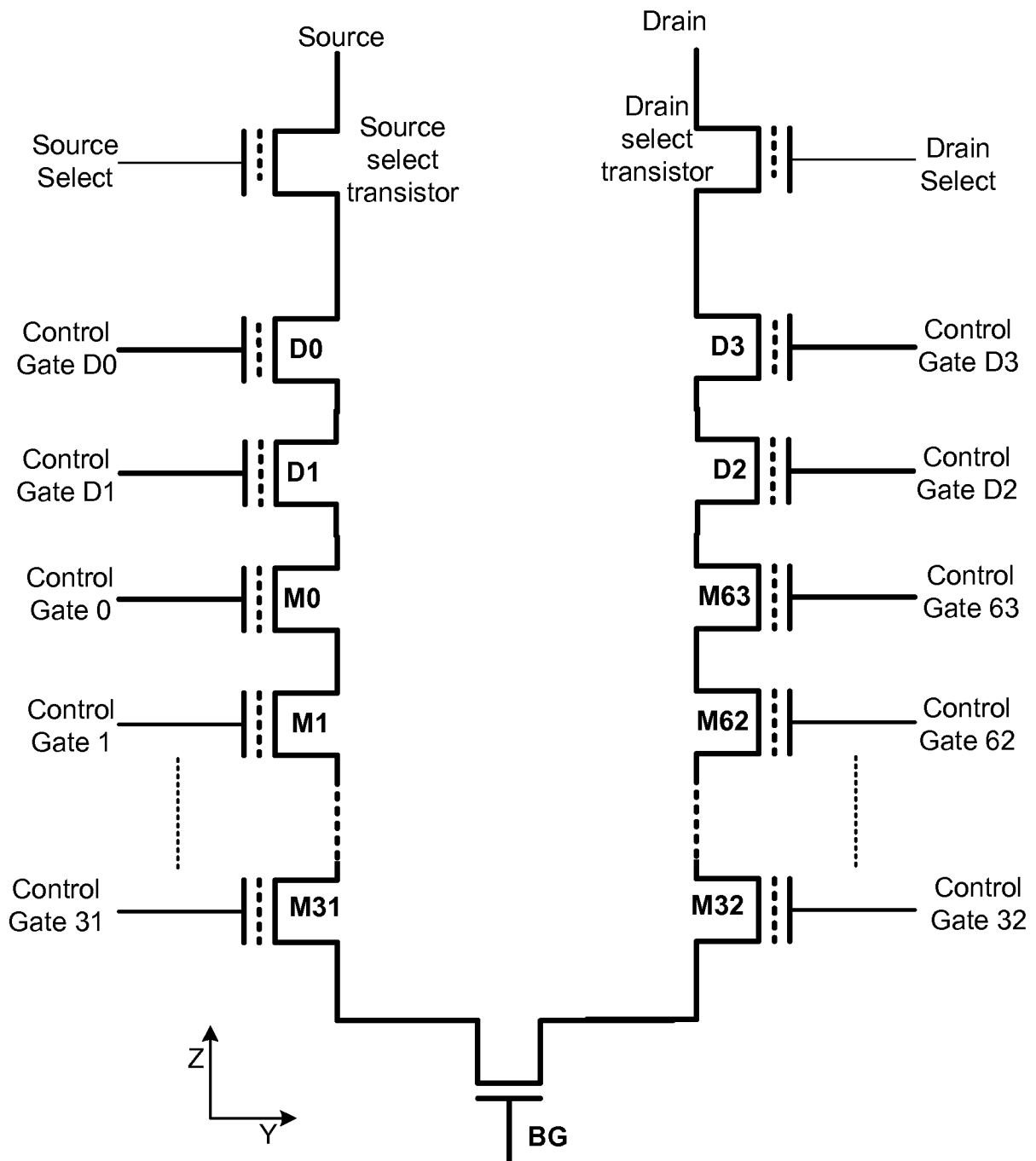
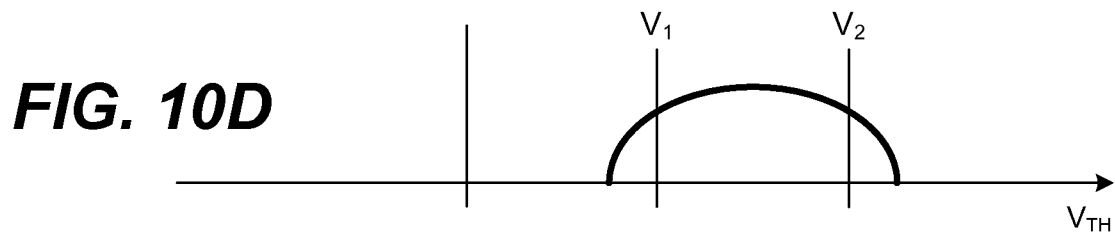
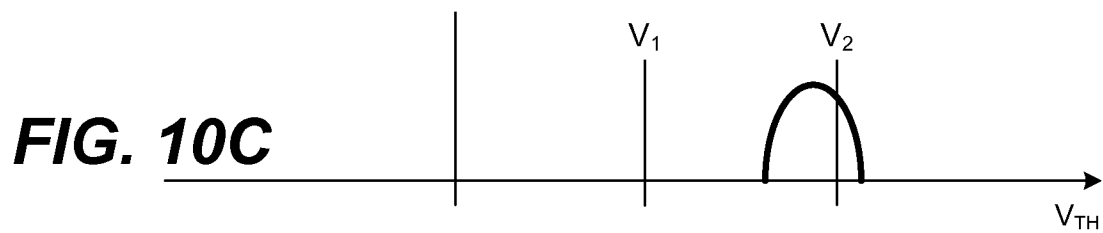
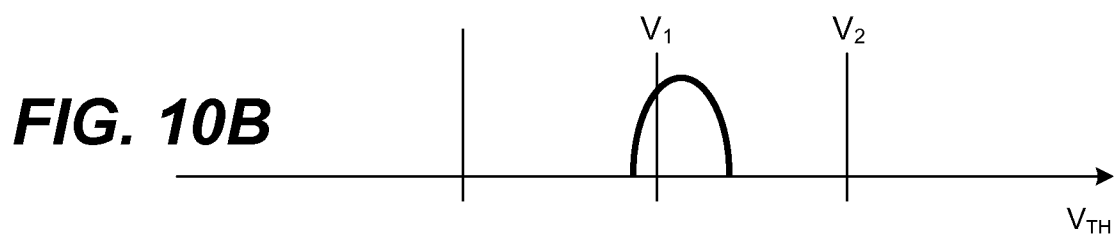
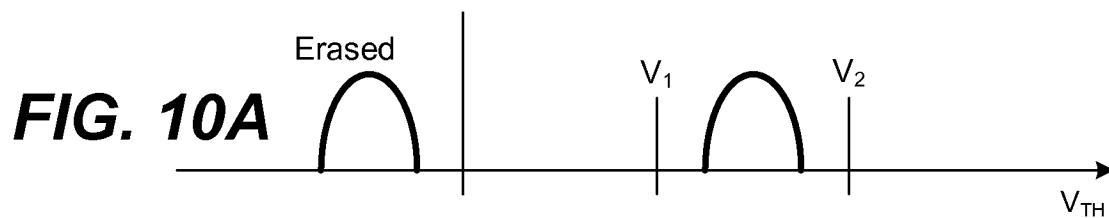
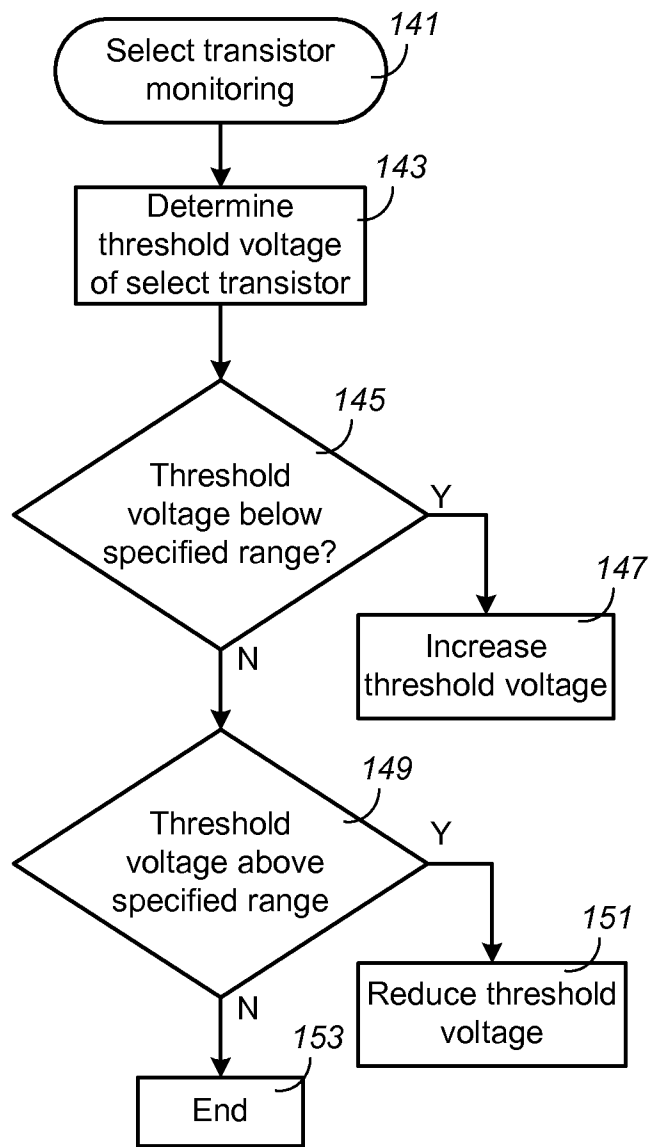
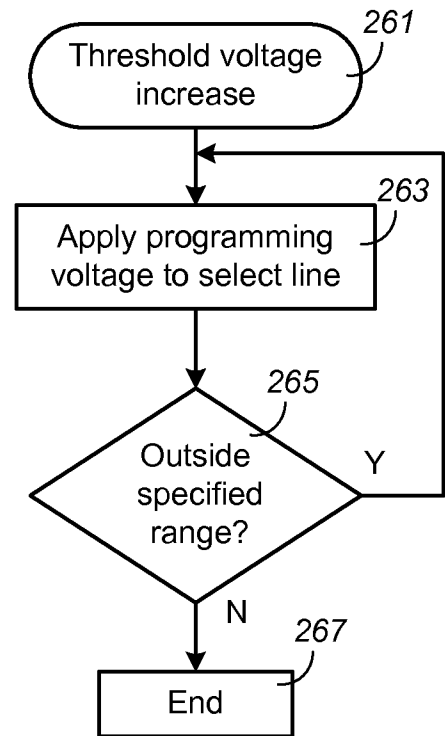
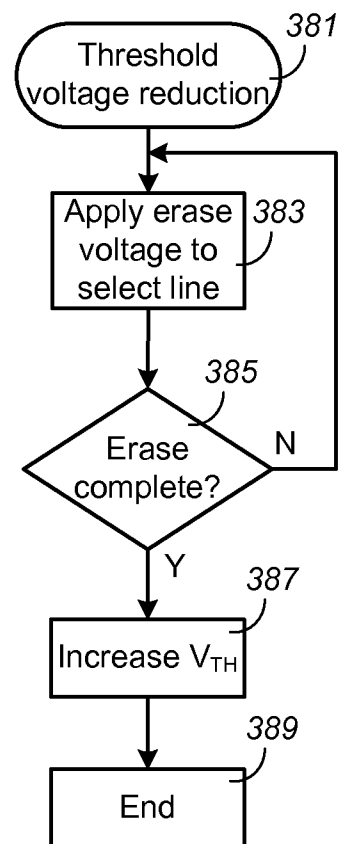


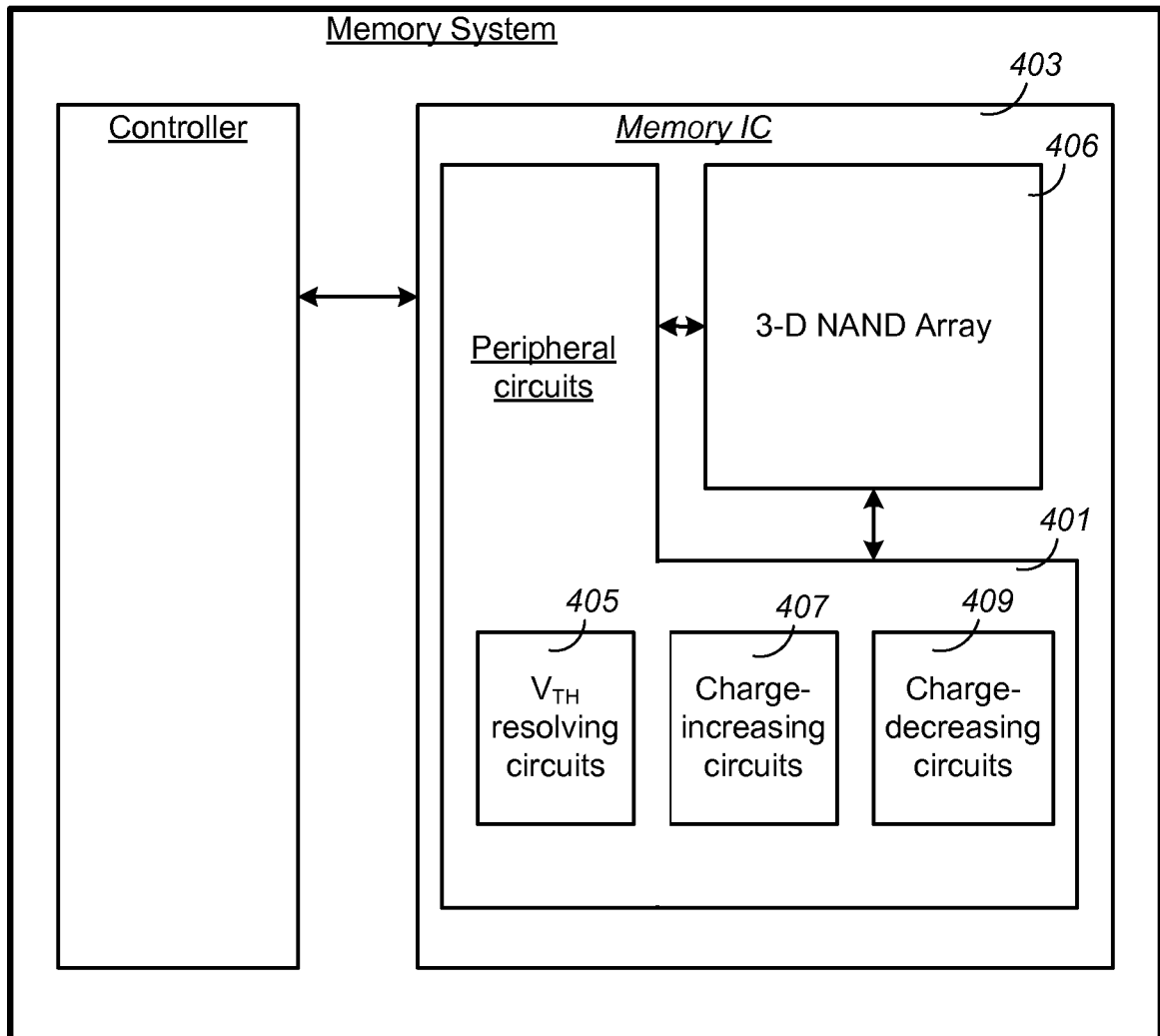
FIG. 7

**FIG. 8**

**FIG. 9**



**FIG. 11****FIG. 12****FIG. 13**

**FIG. 14**

INTERNATIONAL SEARCH REPORT

International application No

PCT/US2013/073120

A. CLASSIFICATION OF SUBJECT MATTER

INV. G11C29/02 G11C16/24
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2011/249503 A1 (YAMADA SHIGEKAZU [JP] ET AL) 13 October 2011 (2011-10-13) paragraph [0005] - paragraph [0008]; figures 1,2	1-8, 16-18
Y	US 2012/170375 A1 (SIM JAESUNG [KR] ET AL) 5 July 2012 (2012-07-05) abstract; figure 7	1-4,6-8, 16-18
X	US 2011/211392 A1 (KIM JAE-HO [KR] ET AL) 1 September 2011 (2011-09-01)	9-15, 19-21
Y	paragraph [0006] - paragraph [0024] paragraph [0114] - paragraph [0116]; figure 13	5
A	US 2010/124118 A1 (HSU F; HSU F C; LEE P W) 20 May 2010 (2010-05-20) abstract; figure 2	1-21
	-/--	



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

17 March 2014

Date of mailing of the international search report

27/03/2014

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040,
Fax: (+31-70) 340-3016

Authorized officer

Wolff, Norbert

INTERNATIONAL SEARCH REPORT

International application No

PCT/US2013/073120

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2009/135656 A1 (PARK KI-TAE [KR]) 28 May 2009 (2009-05-28) paragraph [0069] - paragraph [0072] paragraph [0079] - paragraph [0083]; figure 5 -----	9-15, 19-21

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2013/073120

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2011249503 A1	13-10-2011	US 2011249503 A1	13-10-2011
		US 2014003151 A1	02-01-2014

US 2012170375 A1	05-07-2012	KR 20120078959 A	11-07-2012
		US 2012170375 A1	05-07-2012

US 2011211392 A1	01-09-2011	KR 20110098119 A	01-09-2011
		US 2011211392 A1	01-09-2011

US 2010124118 A1	20-05-2010	TW 201023189 A	16-06-2010
		US 2010124118 A1	20-05-2010
		WO 2010056259 A1	20-05-2010

US 2009135656 A1	28-05-2009	NONE	
