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(54) **Driving circuit of a liquid crystal display and driving method thereof**

Steuereinrichtung eines Flüssigkristallanzeigegeräts und Ansteuerverfahren dafür

Circuit de commande d'un dispositif d'affichage à cristaux liquides et sa méthode de commande

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- **PATENT ABSTRACTS OF JAPAN vol. 017, no. 147 (P-1508), 24 March 1993 (1993-03-24) -& JP 04 318516 A (CASIO COMPUT CO LTD), 10 November 1992 (1992-11-10)**

EP 1 528 534 B1

Description

[0001] The invention relates to a driving circuit of a liquid crystal display and a driving method thereof according to the pre-characterizing clauses of claims 1 and 6. Such a method and circuit are disclosed in US 2002/0196218 A1. Further, EP 1 443 486 A1 discloses a liquid crystal display and driving method having features corresponding to features (h) and (i) defined in claim 2.

[0002] A liquid crystal display (LCD) has advantages of light weight, low power consumption, and low divergence, and is applied to various portable equipment, such as notebook computers and personal digital assistants (PDA). In addition, LCD monitors and LCD televisions are gaining in popularity as a substitute for traditional cathode ray tube (CRT) monitors and televisions. However, an LCD still has some disadvantages. Because of the limitations of physical characteristics, the liquid crystal molecules should be twisted and rearranged when changing input data, and the images will be delayed. For satisfying the rapid switching requirements of multimedia equipment, improving the response speed of liquid crystal is desired.

[0003] With these problems in mind, the present invention aims at providing a driving circuit of a liquid crystal display and a driving method thereof to solve the above-mentioned problem.

[0004] This is achieved by the present invention by a driving method of a liquid crystal display as claimed in claim 1 and a driving circuit for driving a liquid crystal display as claimed in claim 6. The dependent claims pertain to preferred embodiments thereof.

[0005] The invention is illustrated by way of example with reference to the accompanying drawings, in which

Fig.1 is a timing diagram of pixel voltage and transmission rate according to prior art,
Fig.2 is another timing diagram of pixel voltage and transmission rate according to prior art using an over-driving method,
Fig.3 is a diagram of liquid crystal display,
Fig. 4 is a block diagram of one embodiment of the present invention,
Fig.5 is a reference table used for the lookup table in Fig.4,
Fig.6 is a block diagram of another application of the present invention,
Fig.7 is a reference table used for the lookup table in Fig. 6,
Fig.8 is a block diagram of another application of the present invention, and
Fig.9 is a reference table used for the lookup table in Fig. 8.

[0006] The prior art is disclosed in U.S. published application No. 2002/0050965. The U.S. published application No. 2002/0050965 discloses an over-driving method using a brief table to store the over-driving image data. The brief table only includes part of the over-driving image data for driving the pixels switched from one gray level to another. When the driving circuit receives the image data from the input terminal, a processor is used to perform an interpolation operation to expand the brief table. Hence, an extra algorithm is needed in the conventional over-driving method and the algorithm will slow down the response speed.

[0007] Please refer to Fig.1, which is a timing diagram of the pixel voltage and the transmission rate V1 according to a prior art LCD. In Fig. 1, the pixel voltage is shown with the straight lines, and the transmission rate V1 is shown with a dotted line. In Fig.1, frame N means a frame period, and frame N+1, N+2... mean the following frame periods. When the pixel voltage is switched from a data voltage C1 to a data voltage C2, due to the physical characteristics of liquid crystal molecules, the liquid crystal molecules cannot be twisted to a predetermined angle within a frame period and fail to perform a predetermined transmission rate. As the curve of the transmission rate V1 shows, the transmission rate V1 cannot reach a predetermined transmission rate until the frame period of frame N+2. The delayed switch will cause blurring on the LCD.

[0008] An over-driving method is utilized to improve the delayed switch. Please refer to Fig.2, which is a timing diagram of the pixel voltage and the transmission rate V2 according to a prior art LCD using an over-driving method. When the pixel voltage is switched from the data voltage C1 to the data voltage C2, an over-driving data voltage C3 is added to accelerate the response speed of the liquid crystal molecules. Since a higher data voltage can obtain a faster response speed of the liquid crystal molecules, the data voltage C3 higher than the data voltage C2 can improve the delayed switch to reach the predetermined transmission rate in a frame period. As Fig.2 shows, the curve of the transmission rate V2 can reach the predetermined transmission rate in frame N.

[0009] Please refer to Fig.3, which is a diagram of a general LCD 30. The LCD 30 comprises a liquid crystal panel 31, and the liquid crystal panel 31 comprises a plurality of scan lines 32, a plurality of data lines 34, and a plurality of pixels 36. Each pixel 36 is connected to a corresponding scan line 32 and a corresponding data line 34, and each pixel 36 has a switching device 38 and a pixel electrode 39. The switching device 38 is connected to the corresponding scan line 32 and the corresponding data line 34.

[0010] The driving method of the LCD 30 provides scan voltages to the scan lines 32 to open the switching devices 38, and data voltages are provided to the data lines 34 and transferred to the pixel electrodes 30 through the switching devices 38. When scan voltages are provided to the scan lines 32 to open the switching devices 38, data voltages on the data lines 34 will charge the pixel electrodes 39 through the switch devices 38, and twist the liquid crystal molecules. When scan voltages on the

scan lines 32 are removed to close the switching devices 38, the electrical connections between the data lines 34 and the pixel 36 will be cut and the pixel electrodes 39 will remain charged. The scan lines 32 control the switching devices 38 to repeatedly open and close, and thus the pixel electrodes 39 can be repeatedly charged. Different data voltages will cause different twisting angles and show different transmission rates. Hence, the LCD 30 displays different images.

[0011] Please refer to Fig. 4, which is a block diagram of the first embodiment. A driving circuit 40 is utilized for driving the LCD 30 in Fig.3. The driving circuit 40 comprises an image data input terminal 41, a bit processor 42, an image memory 43, a comparison circuit 44, a lookup table (LUT) 45, a multiplexer 46, a data line driving circuit 47, a memory 48, a table selector 49, and a temperature detector 51. In this embodiment, the image memory 43 is a 16-bit (5,6,5 or 5,5,5) memory having the necessary circuitry to read/write the memory cells. The image data input terminal 41 transfers 3 image data (RGB) to the bit processor 42, and each image data is 8 bits for controlling the gray levels of the pixel 30. Each color has 256 (2^8) gray levels, so the 3 image data need 24 bits (8X3) to determine a RGB image. For using the 16-bit image memory 43 in this embodiment, the bit processor 42 is used to extract most significant bits (MSB) of the 3 RGB image data. For example, extracting 5 MSB of the R image data, 6 MSB of the G image data, and 5 MSB of the B image data, and storing the extracted data in the image memory 43. It is of course possible that 5 or other quantities MSB can be extracted from 3 RGB image data as long as the total extracted bits are not more than 16.

[0012] In this embodiment, one of the 3 RGB image data is representative to explain the present invention. The image data input terminal 41 transfers an 8-bit image data D8 to the bit processor 42. The bit processor 42 processes the 8-bit image data D8 and outputs a 6-bit second extracted image data D6 and a current 8-bit image data D8. The second extracted image data D6 is the 6 MSB extracted from the current 8-bit image data D8 by the bit processor 42, and the second extracted image data D6 is stored in the image memory 43 to delay a frame period. After delayed a frame period, the second extracted image data D6 is outputted as a first extracted image data D6' . In Fig. 4, the first extracted image data D6' and the second extracted image data D6 received by the comparison circuit 44 belong to different frame cycles as they differ one frame period.

[0013] The bit processor 42 transfers the second extracted image data D6 to the comparison circuit 44 and transfers the current 8-bit image data D8 to the multiplexer 46. The image memory 43 transfers the first extracted image data D6' to the comparison circuit 44. The first extracted image data D6' and the second extracted image data D6 are compared in the comparison circuit 44. A result value of 0 or 1 is determined after comparing the first extracted image data D6' and the second extracted image data D6. The result value 0 means that the first extracted image data D6' and the second extracted image data D6 are the same, and the result value 1 means that they are different. Since the first extracted image data D6' and the second extracted image data D6 are extracted from two different 8-bit image data D8, the result value 0 means that the differences between these two 8-bit image data D8 is less than 4.

[0014] For example, if the values of the first extracted image data D6' and the second extracted image data D6 are both 2 (000010), the result value of the comparison circuit 44 is 0, and the two corresponding 8-bit image data D8 are 8~11 (00001000~00001011). When the result value is 0, the pixel 36 does not need the over-driving control. On the other hand, if the result value is 1, the difference between these two 8-bit image data D8 is at least 4 and the pixel 36 needs the over-driving control. For example, if the value of the first extracted image data D6' is 2 (000010) and the value of the second extracted image data D6 is 5 (000101), the two corresponding 8-bit image data D8 are 8~11 (00001000~00001011) and 20~23 (00010100~00010111). In this situation, the pixel 36 needs the over-driving control.

[0015] The lookup table 45 comprises a reference table, and the lookup table 45 is operated in accordance with the reference table. Please refer to Fig.5, which illustrates a reference table 50 of the lookup table 45 in Fig.4. The reference table 50 is recorded with (2^6 x 2^6) or (2^5 x 2^5) 8-bit image data values 52, and each image data value 52 corresponds to different first extracted image data D6' and second extracted image data D6. When the result value is 1, meaning the first extracted image data D6' and the second extracted image data D6 are different, the first extracted image data D6' and the second extracted image data D6 are transferred to the lookup table 45. Then the lookup table 45 selects a corresponding 8-bit image data value 52 from the reference table 50 as a first image value D8' according to the first extracted image data D6' and the second extracted image data D6, and transfers the first image value D8' to the multiplexer 46.

[0016] For example, when the value of the first extracted image data D6' is 2 (000010) and the value of the second extracted image data D6 is 3 (000011), the lookup table 45 selects 25 (00011001) from the reference table 50 as the first image value D8' , and transfers the first image value D8' to the multiplexer 46.

[0017] In addition, the result value of the comparison circuit 44 is transferred to the multiplexer 46 to control the operation of the multiplexer 46. If the result value is 0, the multiplexer 46 will output the current 8-bit image data D8. If the result value is 1, the multiplexer 46 will output the over-driving image data D8'. The output Dout of the multiplexer 46 is transferred to the data line driving circuit 47, and the data line driving circuit 47 produces a corresponding data voltage in accordance with the output Dout (D8 or D8') of the multiplexer 46. The data voltage is applied to the corresponding data line 34 to control the

pixel 36.

[0018] For example, if the values of the first extracted image data D6' and the second extracted image data D6 are both 2 (000010) and the value of the current 8-bit image data D8 is 10 (00001010), the output Dout of the multiplexer 46 will be 10 (00001010) and the data line driving circuit 47 will produce a first data voltage corresponding to the output Dout. If the value of the first extracted image data D6' is 2 (000010) and the value of the second extracted image data D6 is 63 (111111) , the over-driving image data D8' outputted by the lookup table 45 will be 255 (11111111), the output Dout will be 255, and the data line driving circuit 47 will produce a second data voltage corresponding to the output Dout.

[0019] Fig. 6 shows a similar embodiment of the present invention. In this situation, the bit processor 42 extracts different MSBs of the 8-bit image data D8. For example, 5 and 6 MSBs of the 8-bit image data D8 are extracted to be the first extracted image data D5' and the second extracted image data D6 respectively. As with the previous embodiment, the comparison circuit 44 compares the first extracted image data D5' and the second extracted image data D6 and determines the result value. When comparing the first extracted image data D5' and the second extracted image data D6, the comparison circuit fills the least significant bits (LSB) of the first extracted image data D5' with 0 and compares the filled first extracted image data D5' with the second extracted image data D6. For example, if the first extracted image data D5' is 7 (00111) and the second extracted image data D6 is 10 (001010), the LSB of the first extracted image data D5' is filled with 0 so that the filled first extracted image data D5' becomes 14 (001110). Then, 14 (001110) is compared with 10 (001010). Again, if the result value is 0, the pixel 36 does not need the over-driving control. If the result value is 1, the pixel 36 needs the over-driving control.

[0020] In addition, when comparing the first extracted image data D5' and the second extracted image data D6, the comparison circuit 44 can delete the LSB of the second extracted image data D6 and compare the first extracted image data D5' with the modified second extracted image data D6. For example, if the first extracted image data D5' is 7 (00111) and the second extracted image data D6 is 10 (001010), the LSB of the second extracted image data D6 is deleted, and the modified second extracted image data D6 is 5 (00101). Then, 7 (00111) is compared with 5 (00101). Similarly, if the result value is 0, the pixel 36 does not need the over-driving control. If the result value is 1, the pixel 36 needs the over-driving control.

[0021] In this embodiment, the reference table used in the lookup table 45 is different. Please refer to Fig.7, which is a reference table 70 used for the lookup table 45 in this situation. The reference table 70 is recorded with (2^5 x 2^6) 8-bit image data values 72. When the result value is 1, meaning that the first extracted image data D5' and the second extracted image data D6 are different, the first extracted image data D5' and the second extracted image data D6 are transferred to the lookup table 45. Then the lookup table 45 selects a corresponding 8-bit image data value 72 from the reference table 70 as a first image value D8' according to the first extracted image data D5' and the second extracted image data D6, and transfers the first image value D8' to the multiplexer 46.

[0022] For saving power, the comparison.circuit 44 can further output a LUT enable signal to the lookup table 45. When the result value is 1, the LUT enable signal will turn on the lookup table 45. When the result value is 0, the LUT enable signal will turn off the lookup table 45.

[0023] In this embodiment, the bit processor 42 extracts N and P MSBs of the 8-bit image data D8 to form the first extracted image data and the second extracted image data. As described above, the combination of (N, P) is (6,6) or (5,6), and can be other suitable values such as (5, 5). Please refer to Fig. 8 and Fig.9. Fig.8 is a block diagram of an embodiment where (N,P) is (5,5), and Fig. 9 is a reference table 90 used for the lookup table 45 in Fig.8. The operation where (N,P) is (5, 5) is similar to that where (N,P) is (6,6), and the only difference is whether 5 or 6 MSBs of the 8-bit image data D8 is extracted. When (N,P) is (5, 5), the first extracted image data D5' and the second extracted image data D5 are both 5-bit image data, and the reference table 90 is stored with (2^5 x 2^5) 8-bit image data 92. The lookup table 45 selects a corresponding 8-bit image data value 92 from the reference table 90 according to the first extracted image data D5' and the second extracted image data D5 to control the followed operation of the data line driving circuit 47.

[0024] In contrast to the prior art, the reference tables in the present invention are built by actually measuring the over-driving voltages needed for properly driving the liquid crystal panel in a frame period. The reference tables include all of the over-driving image data that drives the pixels from any gray level to another, so the processor used to expand the brief table is not needed, and the efficiency can be improved. Additionally, the driving circuit and the driving method of the present invention extract LSB or MSB of a general bit length, so the management of the image memory can be more convenient and efficient.

Claims

1. A driving method of a liquid crystal display (30), the liquid crystal display (30) comprising:

   a liquid crystal panel (31), the liquid crystal panel (31) comprising:

   a plurality of scan lines (32);
   a plurality of data lines (34); and
   a plurality of pixels (36), each pixel (36) is connected to a corresponding scan line (32) and a corresponding data line (34), and

each pixel (36) has a switching device (38) connected to the corresponding scan line (32) and the corresponding data line (34);

the driving method comprises:

(a) continuously providing scan voltages to the scan lines (32);
(b) receiving an M-bit image data from an image data input terminal (41);
(c) extracting N most significant bits of the M-bit image data to form an N-bit image data, N being smaller than M;
(d) delaying the N-bit image data by a frame period to form an N-bit delayed image data;
(e) comparing P most significant bits of a current M-bit image data with the N-bit delayed image data to determine a result value;
(f) if the result value equals a first result value, selecting a first image value (52, 72, 92) from a reference table (50, 70, 90) used in a look up table (45) in accordance with the P MSB and the N-bit delayed image data and forming a first data voltage according to the first image value (52, 72, 92), and providing the first data voltage to the corresponding data line (34) ; and
(g) if the result value equals a second result value, forming a second data voltage in accordance with the current M-bit image data and providing the second data voltage to the corresponding data line (34);

characterized by:

(f1) if the result value equals the first result value, output a look up table enable signal to turn on the look up table (45); and
(g1) if the result value equals the second result value, output a look up table enable signal to turn off the look up table (45).

2. The driving method of claim 1 **characterized in that** the driving method further comprises:

(h) producing a temperature compensation signal in accordance with temperature of the liquid crystal panel (31); and
(i) selecting the reference table (50, 70, 90) to be used in the look up table (45) in step (f) from a plurality of tables (54) in accordance with the temperature compensation signal.

3. The driving method of claim 1 **characterized in that** the reference table (50, 70, 90) is recorded with 2^N x 2^P image values (52, 72, 92).

4. The driving method of claim 1 **characterized in that** P is greater than N.

5. The driving method of claim 1 **characterized in that** P equals N.

6. A driving circuit (40) for driving a liquid crystal display (30), the liquid crystal display (30) comprising:

a liquid crystal panel (31), the liquid crystal panel (31) comprising:

a plurality of scan lines (32);
a plurality, of data lines (34); and
a plurality of pixels (36), each pixel (36) is connected to a corresponding scan line (32) and a corresponding data line (34), and each pixel (36) has a switching device (38) connected to the corresponding scan line (32) and the corresponding data line (34);

the driving circuit (40) comprises:

a scan line driving circuit for continuously providing scan voltages to the scan lines (32);
an image data input terminal (41) for receiving an M-bit image data;
a bit processor (42) for extracting N most significant bits from the M-bit image data to form an N-bit image data, N is smaller than M;
an image memory (43) for storing the N-bit image data and delaying the N-bit image data by a frame period;
a comparison circuit (44) for comparing P most significant bits of a current M-bit image data with the N-bit delayed image data to determine a result value;
a lookup table (45) for outputting an image value (52, 72, 92) from a reference table (50, 70, 90) in accordance with the P MSB and the N-bit delayed image data;
a multiplexer (46) for outputting the image value (52, 72, 92) or outputting the M-bit image data in accordance with the result value; and
a data line driving circuit (47) for forming a data voltage in accordance with output of the multiplexer (46), and providing the data voltage to the corresponding data line (34),

characterized in that:

the comparison circuit (44) further outputs a lookup table enable signal to the lookup table (45) to turn on the lookup table (45) when the multiplexer (46) should output the image value

(52, 72, 92) and to turn off the lookup table (45) when the multiplexer (46) should output the M-bit image data.

7. The driving circuit (40) of claim 6 **characterized in that** the driving circuit (40) further comprises:

a temperature detector (51) for detecting temperature of the liquid crystal panel (31), and producing a temperature compensation signal in accordance with temperature of the liquid crystal panel (31);
a memory (48) for storing a plurality of tables (54); and
a selector (49) for selecting a reference table (50, 70, 90) from the plurality of tables (54) stored in the memory (48) in accordance with the temperature compensation signal, and transferring the selected reference table (50, 70, 90) to the look up table (45) to make the look up table (45) output the image value (52, 72, 92) in accordance with the selected reference table (50, 70, 90).

8. The driving circuit (40) of claim 6 **characterized in that** the reference table (50, 70, 90) is recorded with 2^N x 2^P image values (52, 72, 92).

9. The driving circuit (40) of claim 6 **characterized in that** P is greater than N.

10. The driving circuit (40) of claim 6 **characterized in that** P equals N.

Patentansprüche

1. Ansteuerverfahren einer Flüssigkristallanzeige (30), wobei die Flüssigkristallanzeige (30) umfasst:

ein Flüssigkristall-Panel (31), wobei das Flüssigkristall-Panel (31) umfasst:

eine Vielzahl von Abtastzeilen (32);
eine Vielzahl von Datenzeilen (34); und
eine Vielzahl von Pixeln (36), wobei jedes Pixel (36) mit einer korrespondierenden Abtastzeile (32) und einer korrespondierenden Datenzeile (34) verbunden ist, und jedes Pixel (36) eine Umschaltvorrichtung (38) aufweist, die mit der korrespondierenden Abtastzeile (32) und der korrespondierenden Datenzeile (34) verbunden ist;

wobei das Ansteuerverfahren umfasst:

(a) kontinuierliches Bereitstellen von Abtastspannungen an die Abtastzeilen (32);
(b) Empfangen von M-Bit-Bilddaten von einem Bilddaten-Eingabeterminal (41);
(c) Entnehmen von N höchstwertigen Bits der M-Bit-Bilddaten, um N-Bit-Bilddaten zu bilden, wobei N kleiner als M ist;
(d) Verzögern der N-Bit-Bilddaten um eine Vollbilddauer, um verzögerte N-Bit-Bilddaten zu bilden;
(e) Vergleichen von P höchstwertigen Bits aktueller M-Bit-Bilddaten mit den verzögerten N-Bit-Bilddaten, um einen Ergebniswert zu bestimmen;
(f) wenn der Ergebniswert gleich einem ersten Ergebniswert ist, Auswählen eines ersten Bildwerts (52, 72, 92) aus einer Referenztabelle (50, 70, 90), die in einer Nachschlagtabelle (45) verwendet wird, gemäß den P höchstwertigen Bits und den verzögerten N-Bit-Bilddaten und Ausbilden einer ersten Datenspannung gemäß dem ersten Bildwert (52, 72, 92) und Bereitstellen der ersten Datenspannung an die korrespondierende Datenzeile (34); und
(g) wenn der Ergebniswert gleich einem zweiten Ergebniswert ist, Ausbilden einer zweiten Datenspannung gemäß den aktuellen M-Bit-Bilddaten und Bereitstellen der zweiten Datenspannung an die korrespondierende Datenzeile (34);

gekennzeichnet durch:

(f1) wenn der Ergebniswert gleich dem ersten Ergebniswert ist, Ausgeben eines Nachschlagtabellen-Aktivierungssignals, um die Nachschlagtabelle (45) einzuschalten; und
(g1) wenn der Ergebniswert gleich dem zweiten Ergebniswert ist, Ausgeben eines Nachschlagtabellen-Aktivierungssignals, um die Nachschlagtabelle (45) abzuschalten.

2. Ansteuerverfahren nach Anspruch 1, **dadurch gekennzeichnet, dass** das Ansteuerverfahren ferner umfasst:

(h) Erzeugen eines Temperaturkompensationssignals gemäß einer Temperatur des Flüssigkristall-Panels (31); und
(i) Auswählen der Referenztabelle (50, 70, 90), die in der Nachschlagtabelle (45) in Schritt (f) verwendet werden soll, aus einer Vielzahl von Tabellen (54) gemäß dem Temperaturkompensationssignal.

3. Ansteuerverfahren nach Anspruch 1, **dadurch gekennzeichnet, dass** die Referenztabelle (50, 70, 90) mit $2^N \times 2^P$ Bildwerten (52, 72, 92) aufgezeichnet ist.

4. Ansteuerverfahren nach Anspruch 1, **dadurch gekennzeichnet dass** P größer als N ist.

5. Ansteuerverfahren nach Anspruch 1, **dadurch gekennzeichnet, dass** P gleich N ist.

6. Steuerschaltung (40) zum Ansteuern einer Flüssigkristallanzeige (30), wobei die Flüssigkristallanzeige (30) umfasst:

ein Flüssigkristall-Panel (31), wobei das Flüssigkristall-Panel (31) umfasst:

eine Vielzahl von Abtastzeilen (32);
eine Vielzahl von Datenzeilen (34); und
eine Vielzahl von Pixeln (36), wobei jedes Pixel (36) mit einer korrespondierenden Abtastzeile (32) und einer korrespondierenden Datenzeile (34) verbunden ist, und jedes Pixel (36) eine Umschaltvorrichtung (38) aufweist, die mit der korrespondierenden Abtastzeile (32) und der korrespondierenden Datenzeile (34) verbunden ist;

wobei die Steuerschaltung (40) umfasst:

eine Abtastzeilen-Treiberschaltung zum kontinuierlichen Bereitstellen von Abtastspannungen an die Abtastzeilen (32);
ein Bilddaten-Eingabeterminal (41) zum Empfangen von M-Bit-Bilddaten;
einen Bitprozessor (42) zum Entnehmen von N höchstwertigen Bits aus den M-Bit-Bilddaten, um N-Bit-Bilddaten zu bilden, wobei N kleiner als M ist;
einen Bildspeicher (43) zum Speichern der N-Bit-Bilddaten und zum Verzögern der N-Bit-Bilddaten um eine Vollbilddauer;
eine Vergleichsschaltung (44) zum Vergleichen von P höchstwertigen Bits aktueller M-Bit-Bilddaten mit den verzögerten N-Bit-Bilddaten, um einen Ergebniswert zu bestimmen;
eine Nachschlagtabelle (45) zum Ausgeben eines Bildwerts (52, 72, 92) aus einer Referenztabelle (50, 70, 90) gemäß den P höchstwertigen Bits und den verzögerten N-Bit-Bilddaten;
einen Multiplexer (46) zum Ausgeben des Bildwerts (52, 72, 92) oder Ausgeben der M-Bit-Bilddaten gemäß dem Ergebniswert; und
eine Datenzeilen-Treiberschaltung (47) zum Ausbilden einer Datenspannung gemäß der Ausgabe des Multiplexers (46), und Bereitstellen der Datenspannung an die korrespondierende Datenzeile (34).

dadurch gekennzeichnet, dass
die Vergleichsschaltung (44) ferner ein Nachschlagtabellen-Aktivierungssignal an die Nachschlagtabelle (45) ausgibt, um die Nachschlagtabelle (45) einzuschalten, wenn der Multiplexer (46) den Bildwert (52, 72, 92) ausgeben sollte, und um die Nachschlagtabelle (45) abzuschalten, wenn der Multiplexer (46) die M-Bit-Bilddaten ausgeben sollte.

7. Steuerschaltung (40) nach Anspruch 6, **dadurch gekennzeichnet, dass** die Steuerschaltung (40) ferner umfasst:

einen Temperaturdetektor (51) zum Erfassen einer Temperatur des Flüssigkristall-Panels (31) und zum Erzeugen eines Temperaturkompensationssignals gemäß der Temperatur des Flüssigkristall-Panels (31);
einen Speicher (48) zum Speichern einer Vielzahl von Tabellen (54); und
eine Auswahleinrichtung (49) zum Auswählen einer Referenztabelle (50, 70, 90) aus der Vielzahl von Tabellen (54), die im Speicher (48) gespeichert sind, gemäß dem Temperaturkompensationssignal, und Übertragen der ausgewählten Referenztabelle (50, 70, 90) zur Nachschlagtabelle (45), damit die Nachschlagtabelle (45) den Bildwert (52, 72, 92) gemäß der ausgewählten Referenztabelle (50, 70, 90) ausgibt.

8. Steuerschaltung (40) nach Anspruch 6, **dadurch gekennzeichnet, dass** die Referenztabelle (50, 70, 90) mit 2^N x 2^P Bildwerten (52, 72, 92) aufgezeichnet ist.

9. Steuerschaltung (40) nach Anspruch 6, **dadurch gekennzeichnet dass** P größer als N ist.

10. Steuerschaltung (40) nach Anspruch 6, **dadurch gekennzeichnet, dass** P gleich N ist.

Revendications

1. Procédé de pilotage d'un afficheur à cristaux liquides (30), l'afficheur à cristaux liquides (30) comprenant :

un panneau à cristaux liquides (31), le panneau à cristaux liquides (31) comprenant :

une pluralité de lignes de balayage (32) ;
une pluralité de lignes de données (34) ; et
une pluralité de pixels (36), chaque pixel (36) est connecté à une ligne de balayage correspondante (32) et à une ligne de données correspondante (34), et chaque pixel (36) a un dispositif de commutation (38) connecté à la ligne de balayage correspondante (32) et à la ligne de données correspondante (34) ;
le procédé de pilotage comprend :

(a) la fourniture continue de tensions de balayage aux lignes de balayage (32) ;
(b) la réception d'une donnée d'image à M bit en provenance d'une borne d'entrée de données d'image (41) ;
(c) l'extraction de N bits de poids fort de la donnée d'image à M bit afin de former une donnée d'image à N bit, N étant inférieur à M ;
(d) le retardement de la donnée d'image à N bit d'une période de trame afin de former une donnée d'image retardée à N bit ;
(e) la comparaison des P bits de poids fort d'une donnée d'image à M bit actuelle avec la donnée d'image retardée à N bit afin de déterminer une valeur de résultat ;
(f) si la valeur de résultat est égale à une première valeur de résultat, la sélection d'une première valeur d'image (52, 72, 92) à partir d'une table de référence (50, 70, 90) utilisée dans une table de consultation (45) conformément aux P bits de poids fort et à la donnée d'image retardée à N bit et la formation d'une première tension de données selon la première valeur d'image (52, 72, 92), et la fourniture de la première tension de données à la ligne de données correspondante (34) ; et
(g) si la valeur de résultat est égale à une seconde valeur de résultat, la formation d'une seconde tension de données conformément à la donnée d'image à M bit actuelle et la fourniture de la seconde tension de données à la ligne de données correspondante (34) ;

caractérisé par :

(f1) si la valeur de résultat est égale à la première valeur de résultat, la sortie d'un signal d'activation de table de consultation mettant en fonction la table de consultation (45) ; et
(g1) si la valeur de résultat est égale à la seconde valeur de résultat, la sortie d'un signal d'activation de table de consultation mettant hors fonction la table de consultation (45).

2. Procédé de pilotage selon la revendication 1, **caractérisé en ce que** le procédé de pilotage comprend en outre :

(h) la production d'un signal de compensation de température conformément à la température du panneau à cristaux liquides (31) ; et
(i) la sélection de la table de référence (50, 70, 90) devant être utilisée dans la table de consultation (45) à l'étape (f) parmi une pluralité de tables (54) conformément au signal de compensation de température.

3. Procédé de pilotage selon la revendication 1, **caractérisé en ce que** la table de référence (50, 70, 90) est enregistrée avec 2^N x 2^P valeurs d'image (52, 72, 92).

4. Procédé de pilotage selon la revendication 1, **caractérisé en ce que** P est supérieur à N.

5. Procédé de pilotage selon la revendication 1, **caractérisé en ce que** P est égal à N.

6. Circuit de pilotage (40) pour piloter un afficheur à cristaux liquides (30), l'afficheur à cristaux liquides (30) comprenant :

un panneau à cristaux liquides (31), le panneau à cristaux liquides (31) comprenant :

une pluralité de lignes de balayage (32) ;
une pluralité de lignes de données (34) ; et
une pluralité de pixels (36), chaque pixel (36) est connecté à une ligne de balayage correspondante (32) et à une ligne de données correspondante (34), et chaque pixel (36) a un dispositif de commutation (38) connecté à la ligne de balayage correspondante (32) et à la ligne de données correspondante (34) ;

le circuit de pilotage (40) comprend :

un circuit de pilotage de ligne de balayage pour fournir de manière continue des tensions de balayage aux lignes de balayage (32) ;
une borne d'entrée de données d'image (41) pour recevoir une donnée d'image à M bit ;
un processeur de bit (42) pour extraire N bits de poids fort de la donnée d'image à M bit afin de former une donnée d'image à N bit, N est inférieur à M ;
une mémoire d'image (43) pour stocker la donnée d'image à N bit et retarder la donnée d'image à N bit d'une période de trame ;
un circuit de comparaison (44) pour comparer P bits de poids fort d'une donnée d'image à M bit actuelle avec la donnée d'image retardée à N bit afin de déterminer une valeur de résultat ;
une table de consultation (45) pour sortir

une valeur d'image (52, 72, 92) à partir d'une table de référence (50, 70, 90) conformément aux B bits de poids fort et à la donnée d'image retardée à N bit ;
un multiplexeur (46) pour sortir la valeur d'image (52, 72, 92) ou sortir la donnée d'image à M bit conformément à la valeur de résultat ; et
un circuit de pilotage de ligne de données (47) pour former une tension de données conformément à la sortie du multiplexeur (46), et fournir la tension de données à la ligne de données correspondante (34),

caractérisé en ce que :

le circuit de comparaison (44) sort en outre un signal d'activation de table de consultation vers la table de consultation (45) pour mettre en fonction la table de consultation (45) lorsque le multiplexeur (46) devrait sortir la valeur d'image (52, 72, 92) et pour mettre hors fonction la table de consultation (45) lorsque le multiplexeur (46) devrait sortir la donnée d'image à M bit.

7. Circuit de pilotage (40) selon la revendication 6, **caractérisé en ce que** le circuit de pilotage (40) comprend en outre :

un détecteur de température (51) pour détecter la température du panneau à cristaux liquides (31), et produire un signal de compensation de température conformément à la température du panneau à cristaux liquides (31) ;
une mémoire (48) pour stocker une pluralité de tables (54) ; et
un sélecteur (49) pour sélectionner une table de référence (50, 70, 90) parmi la pluralité de tables (54) stockées dans la mémoire (48) conformément au signal de compensation de température, et transférer la table de référence sélectionnée (50, 70, 90) à la table de consultation (45) pour amener la table de consultation (45) à sortir la valeur d'image (52, 72, 92) conformément à la table de référence sélectionnée (50, 70, 90).

8. Circuit de pilotage (40) selon la revendication 6, **caractérisé en ce que** la table de référence (50, 70, 90) est enregistrée avec $2^N \times 2^P$ valeurs d'image (52, 72, 92).

9. Circuit de pilotage (40) selon la revendication 6, **caractérisé en ce que** P est supérieur à N.

10. Circuit de pilotage (40) selon la revendication 6, **caractérisé en ce que** P est égal à N.

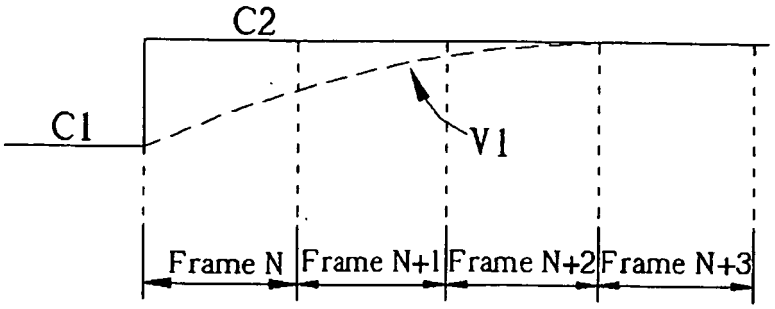


Fig. 1 Prior art

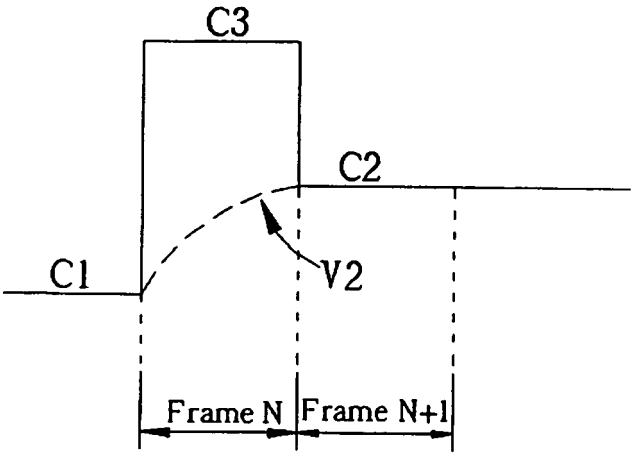


Fig. 2 Prior art

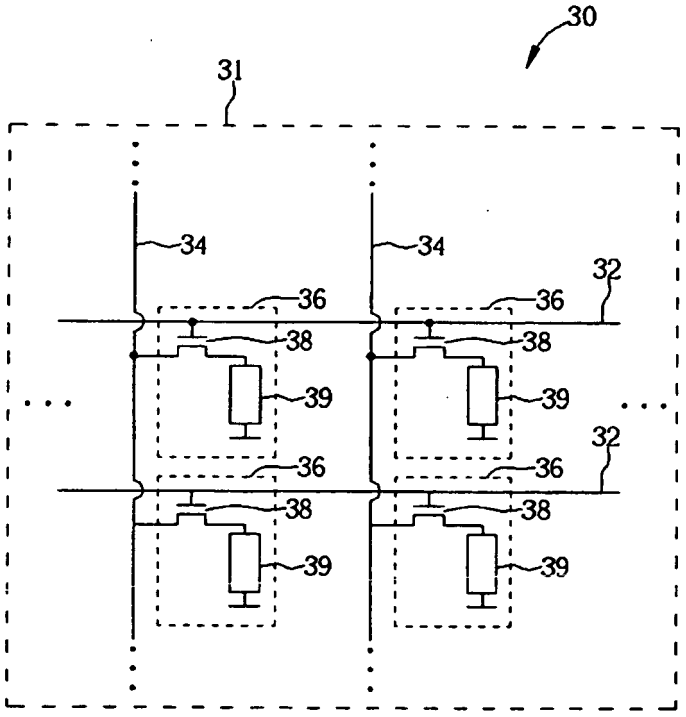


Fig. 3 Prior art

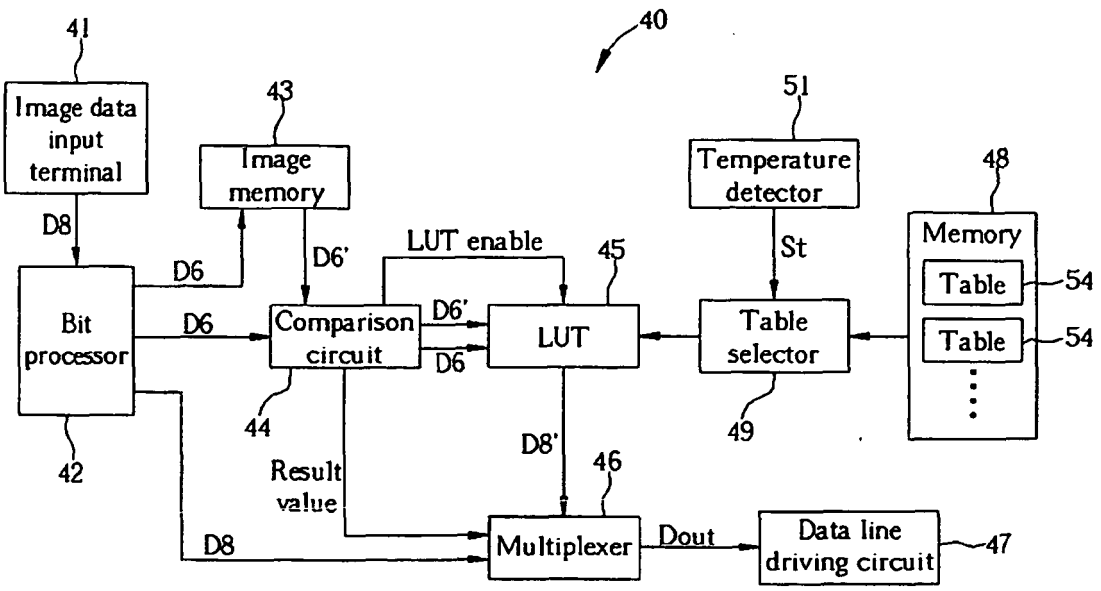

40
41
Image data input terminal
43
Image memory
51
Temperature detector
48
Memory
Table
Table
54
54
D8
D6
D6'
LUT enable
45
St
Bit processor
D6
Comparison circuit
D6'
D6
LUT
Table selector
44
49
42
Result value
D8'
46
D8
Multiplexer
Dout
Data line driving circuit
47

Fig. 4

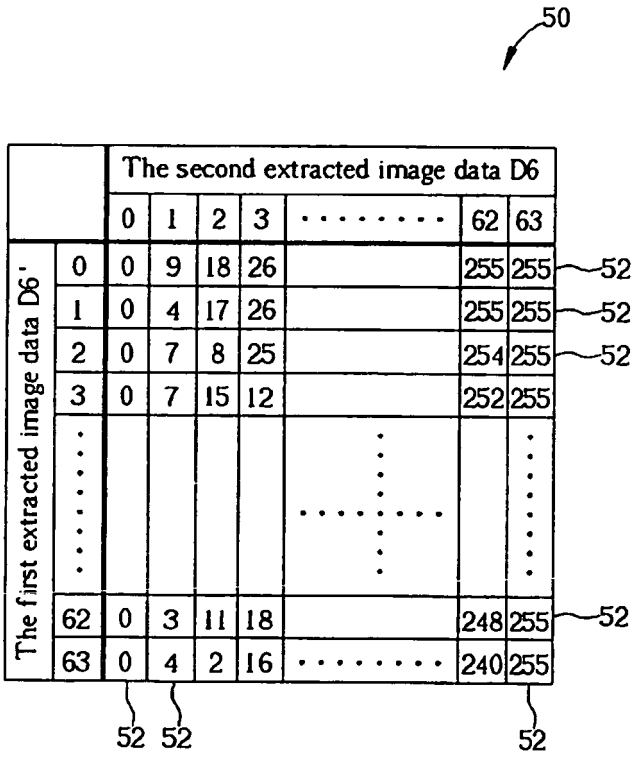

50
The second extracted image data D6
0 1 2 3 ..... 62 63
The first extracted image data D6'
0 0 9 18 26 ..... 255 255 52
1 0 4 17 26 ..... 255 255 52
2 0 7 8 25 ..... 254 255 52
3 0 7 15 12 ..... 252 255
62 0 3 11 18 ..... 248 255 52
63 0 4 2 16 ..... 240 255
52 52 52

Fig. 5

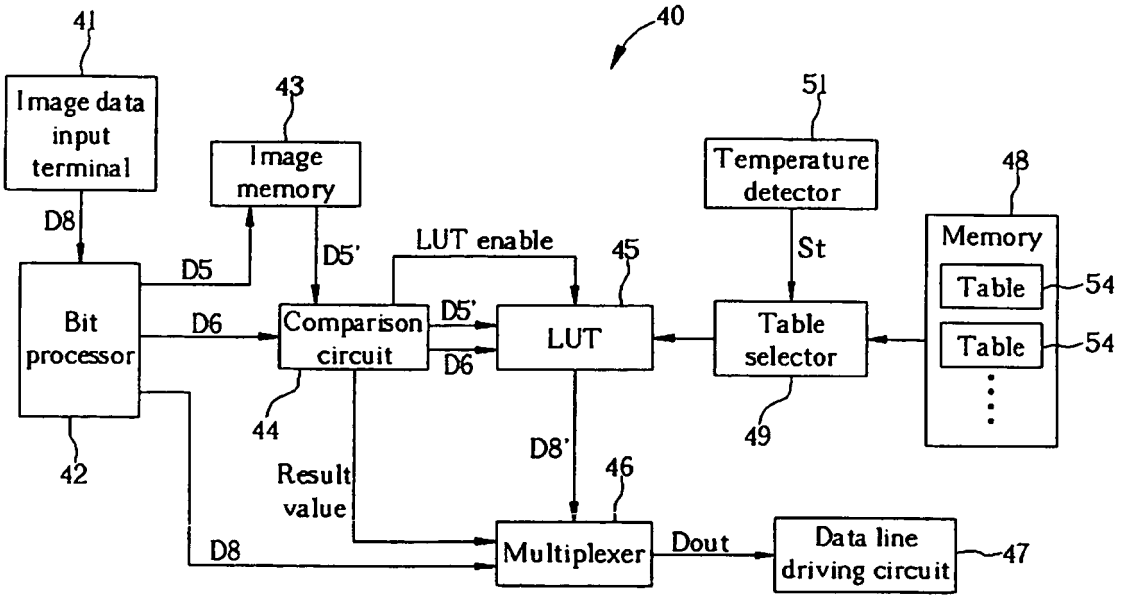
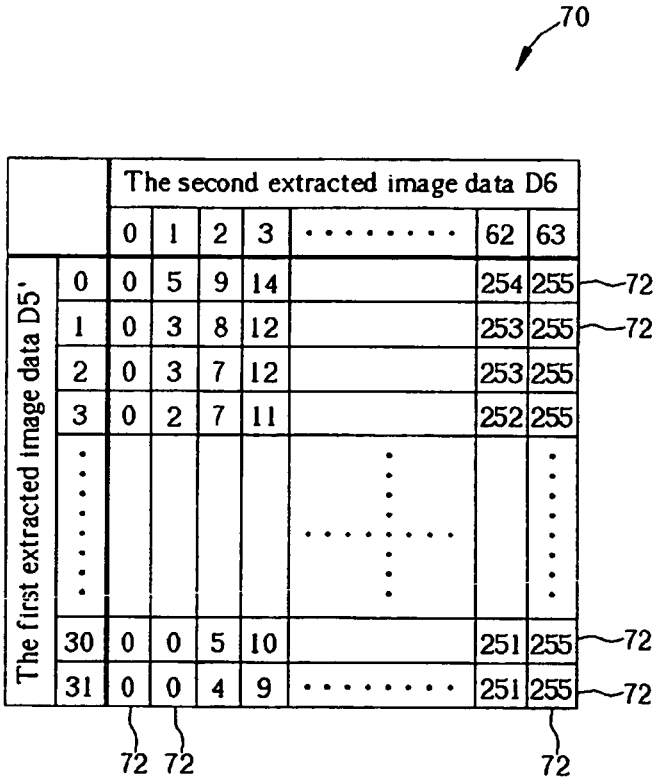

41
40
Image data input terminal
43
Image memory
51
Temperature detector
48
Memory
D8
D5
D5'
LUT enable
45
St
Table
54
Bit processor
D6
Comparison circuit
D5'
LUT
Table selector
Table
54
D6
44
49
42
D8'
46
Result value
D8
Multiplexer
Dout
Data line driving circuit
47

Fig. 6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The second extracted image data D6
0 1 2 3 62 63
The first extracted image data D5'
0 0 5 9 14 254 255 72
1 0 3 8 12 253 255 72
2 0 3 7 12 253 255
3 0 2 7 11 252 255
30 0 0 5 10 251 255 72
31 0 0 4 9 251 255 72
72 72 72

Fig. 7

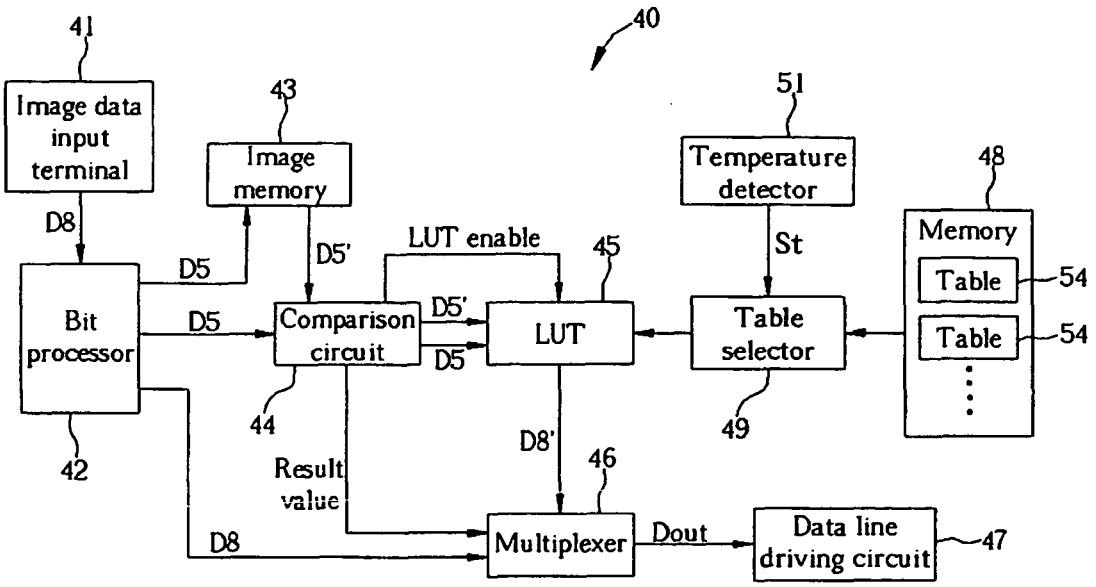
41
40
Image data input terminal
43
Image memory
51
Temperature detector
48
Memory
D8
D5
D5'
LUT enable
45
St
Table
54
Bit processor
D5
Comparison circuit
D5'
D5
LUT
Table selector
Table
54
44
49
42
D8'
46
Result value
D8
Multiplexer
Dout
Data line driving circuit
47

Fig. 8

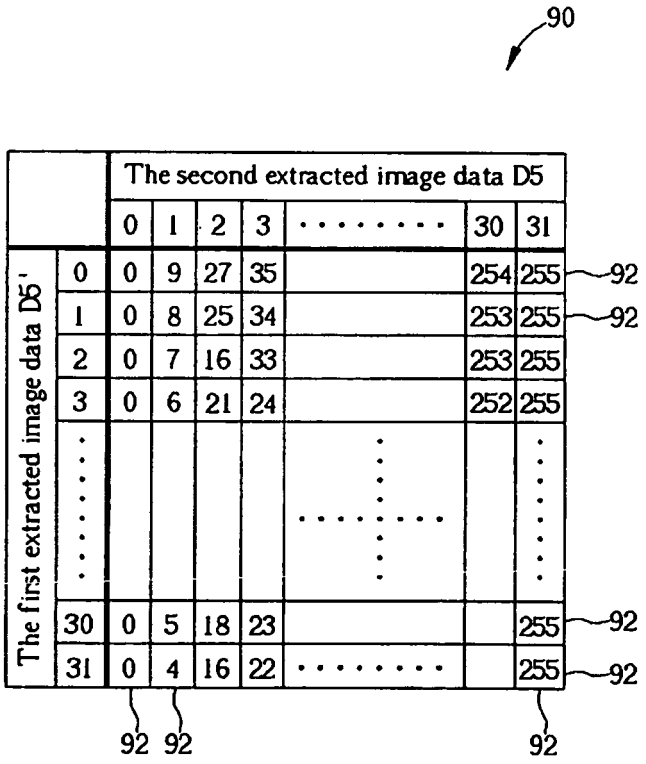
90
The second extracted image data D5
0 1 2 3 30 31
The first extracted image data D5'
0 0 9 27 35 254 255 92
1 0 8 25 34 253 255 92
2 0 7 16 33 253 255
3 0 6 21 24 252 255
30 0 5 18 23 255 92
31 0 4 16 22 255 92
92 92 92

Fig. 9

REFERENCES CITED IN THE DESCRIPTION

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- EP 1443486 A1 **[0001]**
- US 20020050965 A **[0006]**