United States Patent

Bryden et al.

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[54] **VISUAL DISPLAY SYSTEM**

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[21] Appl. No.: **19,190**

[52] **U.S. Cl.**.....**340/172.5,** 340/324 A

[51] **Int. Cl.**.....**G06f 3/14**

[58] **Field of Search**.....340/172.5, 324.1

[56] **References Cited**

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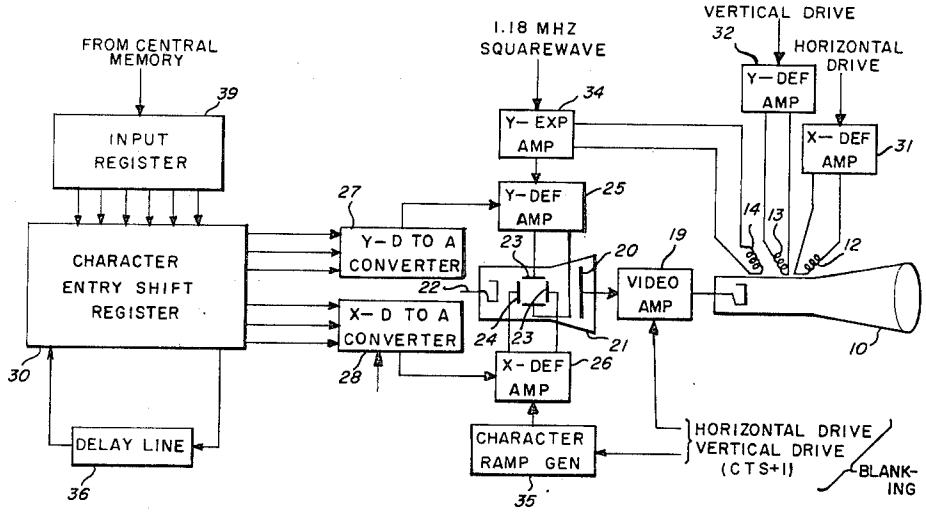
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[57] **ABSTRACT**

A cathode ray display system in which characters are generated by a monoscope and in which the character address information for the entire raster of a cathode ray tube display is stored in a dynamic memory which is continuously read and regenerated by character entry and read-out logic which controls the monoscope scanning to supply the proper characters to the cathode ray tube as it scans in a raster.

34 Claims, 6 Drawing Figures



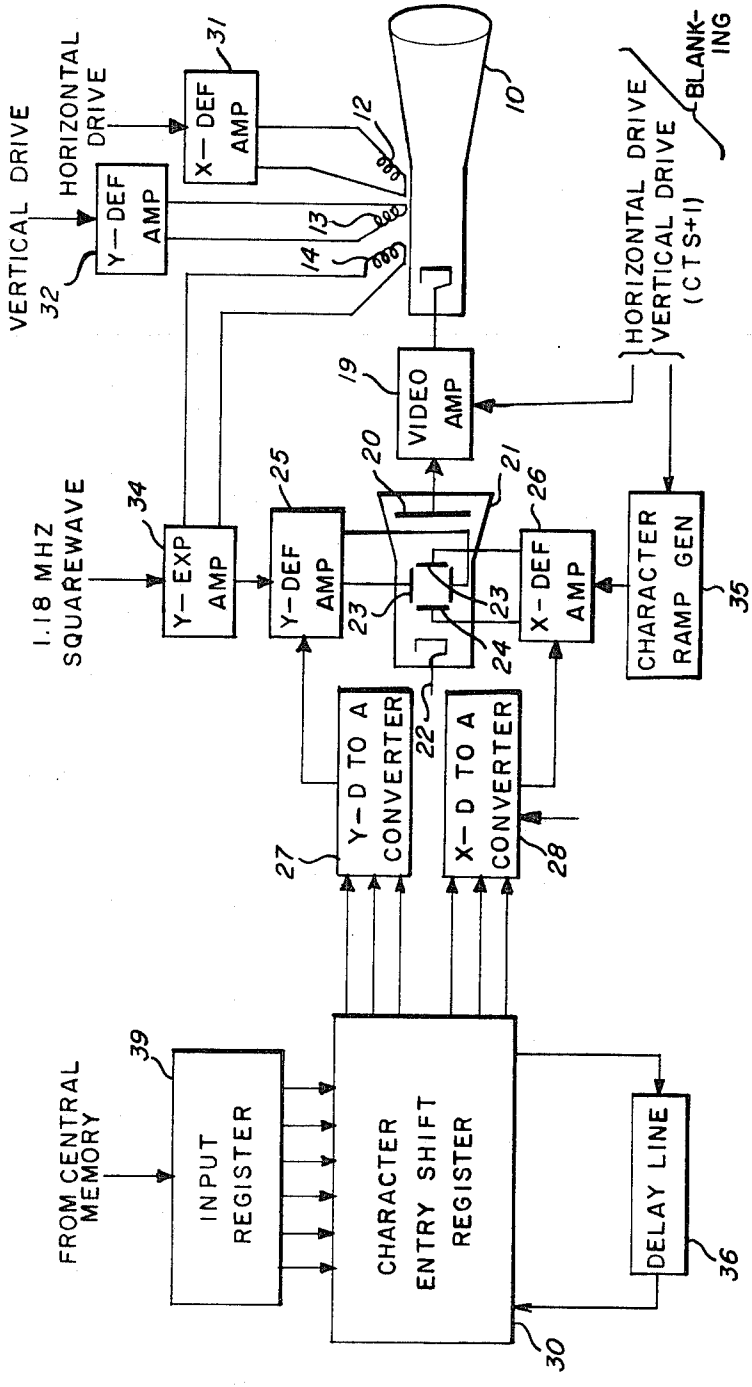


FIG. 1

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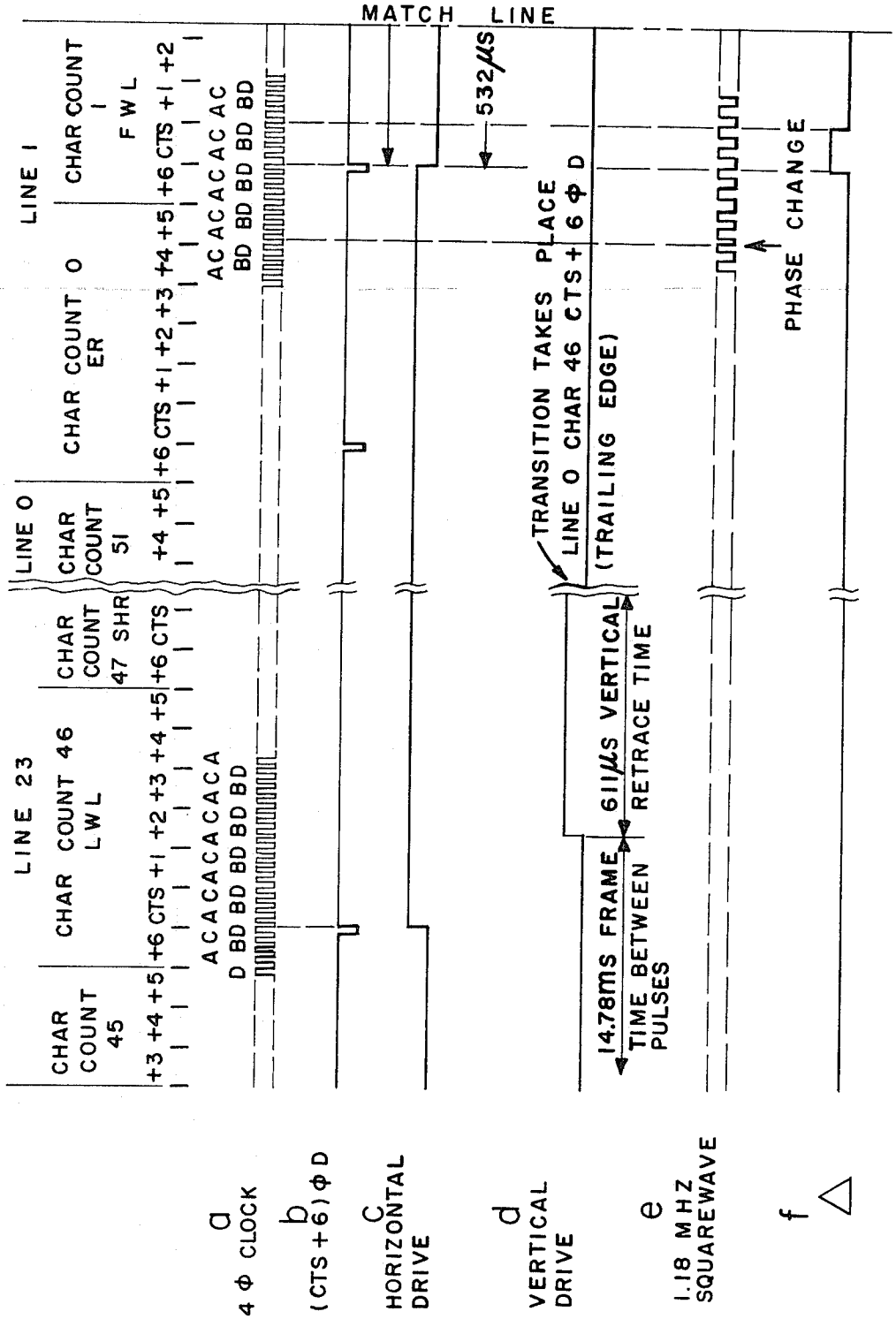


FIG. 2

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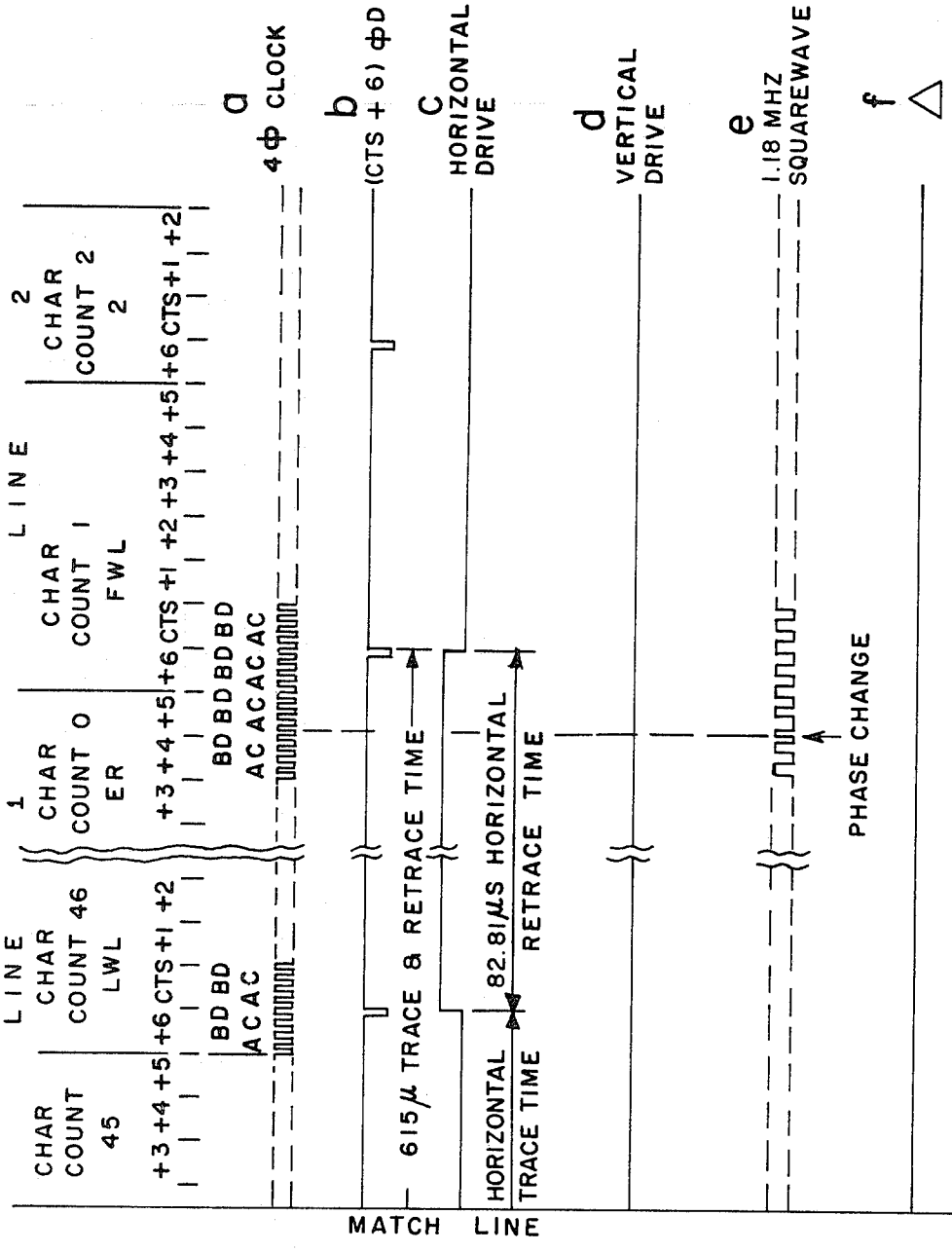


FIG. 3

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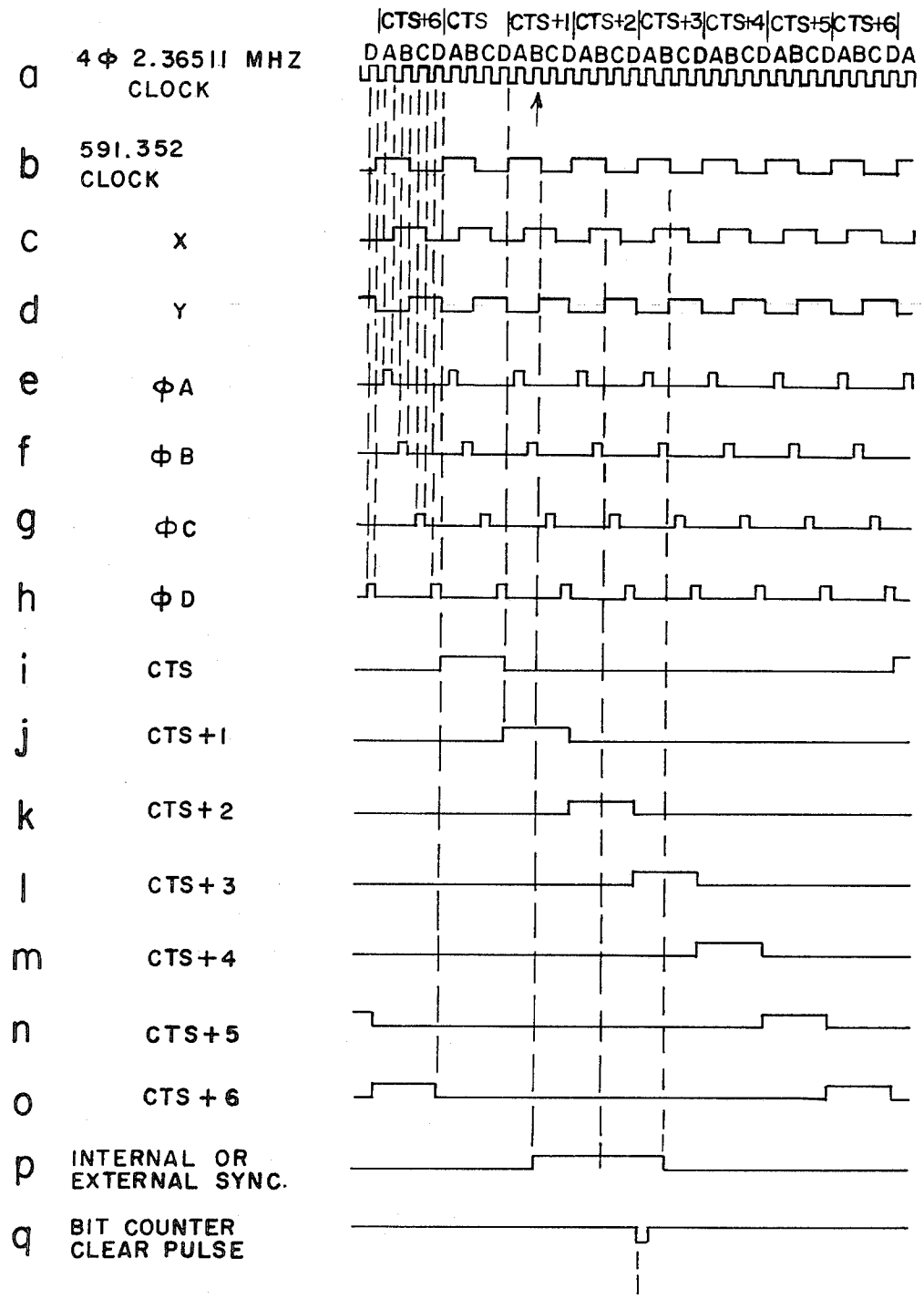


FIG. 4

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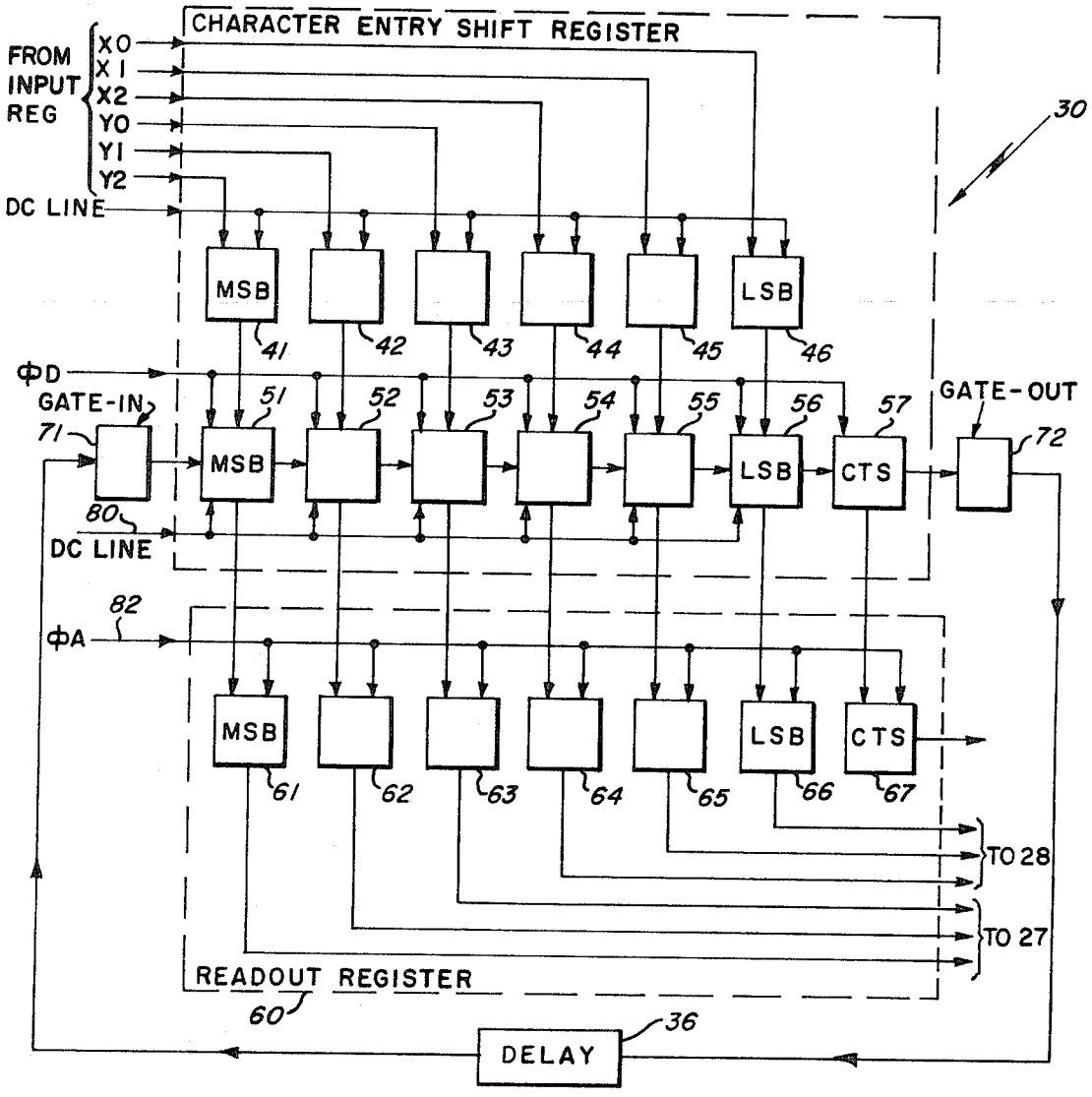


FIG. 5

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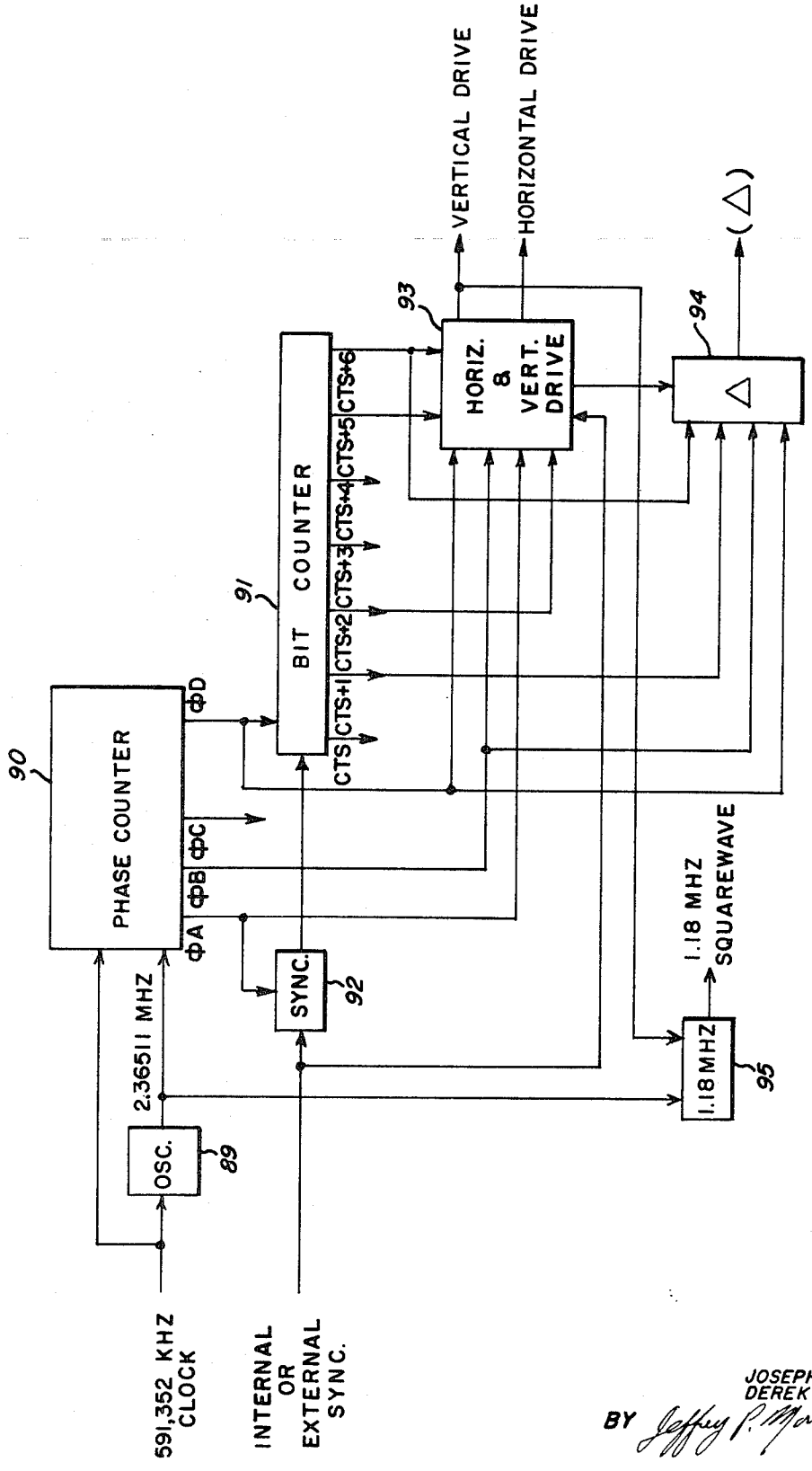


FIG. 6

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VISUAL DISPLAY SYSTEM

BACKGROUND OF THE INVENTION

This invention relates to display systems and, more particularly, to cathode ray tube display systems for displaying characters representing data from large computer systems. Many prior art systems are available for displaying output data from a computer on a cathode ray tube, some of which use a monoscope with the characters to be displayed imprinted thereon. The monoscope output is fed to a cathode ray tube, whereby the individual characters on the monoscope are scanned to produce a composite raster of output information on the cathode ray tube. In such systems, the monoscope address and retrace data come from large central storage systems using complex programming or from permanent memory devices, such as magnetic drums, with a resulting high overall system cost. Other systems provide for displays in which every elemental area of the cathode ray tube face is scanned and the required elements are illuminated by a pulse derived from a computer. However, such systems require very substantial memories to hold a composite raster of information.

SUMMARY OF THE INVENTION

This invention discloses a system wherein the information for display of a complete raster or frame of a cathode ray tube picture may be stored in a dynamic delay device, such as a mechanical vibrator delay line, so that the entire contents of the delay line are fed through a read-out circuit which continuously supplies the stored information to the deflection circuitry of a monoscope for generating characters for display on the cathode ray tube. The read-out circuit also recirculates the stored information through the delay line so that it is resupplied to the monoscope deflection circuitry at the frame scan rate of the cathode ray tube which is, for example, in excess of 60 scans per second so that objectionable flicker does not occur on the cathode ray tube face.

The specific delay line employed consists of a length of coiled wire into which torsional vibrations are introduced and extracted by magnetostrictive transducers so as to provide a delay of, for example, approximately 15 milliseconds. While such dynamic delay systems have been used to store a portion of the displayed character information, as a practical matter the storage capacity of a delay line is limited. The detailed storage of every character for a full frame of displayed information would require a delay line of relatively large capacity; therefore, in prior art systems, only a single line or single character of information has been stored. In the present invention, only the addresses of the detailed storage for every character are stored in digital form in the delay line; that is, the locations of the characters in the monoscope are stored in the delay line. This arrangement results in a reduction of the required delay capacity by a factor of 10 to 100.

It is, therefore, an object of this invention to provide a recirculating memory for a character display system including a delay line wherein character address information for an entire display frame is stored and recirculated.

An additional object of this invention is the provision of a continuously regenerative memory for use in a character generator.

A further object of this invention is the provision of a vertical deflection character scanning signal which has a predetermined phase between successive cathode ray tube frame scans.

Yet a further object of this invention is the provision of an information regeneration or reformation shift register which is capable of providing entry, regeneration, and non-destructive transfer of character address information.

Other objects and advantages of this system will be brought out in the description to follow. This description is accompanied by drawings wherein:

FIG. **1** is a block diagram showing preferred embodiment of the invention;

FIG. **2** is a waveform diagram showing some of the important waveforms present in the system;

FIG. **3** is an additional waveform diagram continuing from FIG. **2**;

FIG. **4** is a further waveform diagram;

FIG. **5** shows the regenerative recirculating memory and delay line of the present invention; and

FIG. **6** is a block diagram of the timing circuitry.

Referring now to FIGS. **1** through **6**, there is shown a cathode ray tube display system embodying the invention. Cathode ray tube **10** is of the conventional type and includes a fluorescent screen **11**, horizontal deflection coil **12**, vertical deflection coil **13**, high-frequency auxiliary vertical deflection coil **14**, cathode **15**, control grid, focus and auxiliary electrodes, and a high voltage anode (not shown). These elements of the cathode ray tube are supplied with biasing voltages and currents in accordance with well-known practice. Cathode **15** is fed negative video signals and positive blanking signals from the output of a video amplifier **19** which may have a video band-pass characteristic of from 15 to 50 megacycles or greater, depending upon the desired writing speed. A video preamplifier (not shown) amplifies incoming signals to the video amplifier and is fed from the target electrode **20** of monoscope **21** which is conventional design having a cathode **22**, vertical deflection plates **23**, horizontal deflection plates **24**, and grid, focusing and auxiliary electrodes (not shown). An electron beam, originating at the cathode **22**, is accelerated toward a target anode **20** at the other end of the tube. The target anode may be, for example, in accordance with well-known practice an aluminum oxide disc with alphanumeric and other special symbol characters deposited thereon in carbon or other desired material. When the electron beam from cathode **22** scans an area of target **20**, the secondary emission characteristics will vary depending on whether the beam strikes the aluminum oxide target or a portion of a carbon character positioned thereon to produce an output signal. The vertical deflection plates **23** of the monoscope **21** are fed from a vertical or Y deflection amplifier **25**, while the horizontal deflection plates **24** are fed from a horizontal or X deflection amplifier **26**.

The purpose of the monoscope deflection amplifier is to convert digital character codes into analog voltages for deflecting the monoscope scan. Y deflection amplifier **25** has an output derived from a Y axis digital-to-analog converter **27**, while X deflection amplifier **26** is fed from an X axis digital-to-analog converter **28**. Digital-to-analog converters **27** and **28** include well-known storage registers (not shown) which

are parallel fed from character entry shift register 30, so that when a digital code passes through the character entry shift register, it is nondestructively read into the storage registers of the digital-to-analog converters 27 and 28. The digital character code is a six-bit binary code, the three most significant bits of which are fed to the X axis digital-to-analog converter 28 for positioning the monoscope scan on the X axis, while the three least significant bits are fed to the Y axis digital-to-analog converter 27 for positioning the monoscope scan on the Y axis.

The six-bit character code is derived from an input register 39, which may be a keyboard including a diode matrix for producing the requisite digital code. The code, once formed, is parallel transferred into the character entry shift register 30. The digital code may also originate in the central memory of the computer and may, through a suitable buffer, be parallel or serially transferred into the character entry register. Whether a digital character code originates at the input register 39 or at a central memory, once the code is in the character entry shift register 30 it is continuously serially shifted out of the character entry shift register into delay line 36. The character code is also parallel transferred to the appropriate storage register in the X and Y axis digital-to-analog converters 27 and 28 to provide the analog voltages necessary to position the monoscope beam, thereby providing the intensity modulation through video amplifier 19 which generates the character on the cathode ray tube screen.

The character code serial output is delayed for a period of time corresponding to the frame scan time in the delay line and serially fed to the input of shift register 30. In the present embodiment, the frame time is approximately 67 scans per second, which requires a delay of 14.78 milliseconds. The frame time is the time required for the cathode ray tube beam to scan through a complete raster on the screen; that is, from one character position through a complete scan cycle and back to the same character position. Thus, the sum of the delay time of delay line 36 and of shift register 30 represents the total frame time. One character time after the character code is serially shifted out of the character entry shift register 30, register 30 is cleared, the last bit of the character code has entered the delay line, and the cathode ray tube scan has moved to the next character position on the screen. Thus, the delay line refresh memory loop refreshes the register 30; hence, the display 67 times a second.

The horizontal drive timing signal, shown in FIGS. 2*c* and 3*c*, fed to X deflection amplifier 30 from a central timing source, is an 83-microsecond gate pulse which represents the horizontal line retrace time and is equivalent to seven character times. A 532-microsecond deflection pulse which corresponds to the horizontal trace time required to enter 45 characters into the memory follows the 83-microsecond horizontal line retrace gate pulse. Thus, the 83-microsecond gate signals occur at 615-microsecond intervals, which is the combined horizontal line trace and retrace period. When the X deflection amplifier receives this horizontal drive timing pulse, a sawtooth generator in the X deflection amplifier is triggered and the resulting sawtooth is amplified and applied to the horizontal deflection coil 12 as a linearly increasing current that moves the electron beam horizontally across the cathode ray tube screen.

The vertical drive timing or vertical retrace signal shown in FIGS. 2*d* and 3*d* is fed to the vertical deflection amplifier 31 from the central timing source, triggering a sawtooth generator similar to that used in the horizontal amplifier. The resulting sawtooth is combined with a portion of the sawtooth from the horizontal deflection amplifier and applied to vertical deflection coil 13. Thus, the sawtooth that drives the sweep downward has a horizontal step for each horizontal line during the time that the horizontal sweeps occur. The horizontal sweep applied to the vertical amplifier is used to correct any slant of the horizontal line caused by the vertical deflection. In this way, the stepped sawtooth maintains a constant vertical deflection until the end of a horizontal sweep resulting in perfectly horizontal sweeps. The vertical drive pulse is a gate pulse 611 microseconds wide which corresponds to one horizontal line time and is the vertical retrace time. These gates are approximately 14.78 milliseconds apart, which represents the frame time or the time necessary to generate 23 horizontal line pulses plus the vertical retrace time. The frame scan rate or refresh time in the embodiment illustrated is 67 cycles per second.

As shown in FIGS. 2*c* and 3*c*, the leading edge of the horizontal gate pulse occurs in the character time slot plus six, phase D (CTS + 6 ϕD) of the 46 characters counted (the end of a line) and the trailing edge occurs at the first character count of the line in the (CTS + 6 ϕD) timing slot. The leading edge of the vertical drive pulse occurs at (CTS + 2 ϕB) during character count 46, line 23 (the last character of the last line). The timing will be explained in more detail with reference to FIG. 6.

A Y axis expansion amplifier 34 drives high-frequency auxiliary vertical deflection coil 13 with a sinusoidal waveform at 1.18 megacycles in the embodiment shown although the frequency used may lie in the one megacycle plus or minus a fraction range. A square wave signal developed in the timing circuitry is shown in FIGS. 2*e* and 3*e*. This square wave is phase shifted, for example 180°, on alternate cathode ray tube scans and is applied to the Y axis expansion amplifier, then to the auxiliary deflection coil 14 which is a resonant circuit that changes the square wave signal to a sine wave which occurs at the rate of 12 times per character and which, when applied to coil 14, increases the horizontal line height, thereby increasing the character height on the cathode ray tube. Each horizontal line is made a width equal to the excursion produced by the high-frequency vertical deflection coil 13. The Y axis expansion amplifier output is also combined with the Y axis analog voltage in Y deflection amplifier 25 causing the monoscope beam to sweep up and down across a character symbol. This painting effect is shifted by 180° on alternate cathode ray tube scans so that effectively the character symbol is canned 24 times, 12 times per frame, although frequency interlacing phases other than 180° may be employed. This technique also causes the painting of individual characters to occur at the same phase each time with a resulting elimination of excess jitter. A signal applied to horizontal deflection amplifier 26 from character ramp generator 35 which

produces a sawtooth waveshape develops a ramp voltage that will drive the monoscope electron beam across the character to be painted. No sawtooth is present during horizontal or vertical retrace due to blanking.

The blank pulse is composed of three distinct pulses, (CTS + 1), horizontal drive and vertical drive shown on FIGS. 4*j*; 2*c* and 3*c*; and 2*d* and 3*d*, respectively. When a (CTS + 1) pulse is present on the blank pulse line in combination with either a horizontal drive pulse or a vertical drive pulse, blanking occurs. When no vertical or horizontal drive pulses are present, the sawtooth generated in the character ramp generator **35** drives the beam horizontally across the character. The blanking pulse is also applied to the video amplifier during retrace and during intercharacter time (CTS), shown in FIG. 4*i*, thereby synchronizing the operation of the monoscope with the cathode ray tube sweep and the intensity modulation of the cathode ray tube cathode **15** to reproduce the characters on the cathode ray tube face.

The refresh memory loop shown in FIG. **5** consists of the character entry shift register **30**, delay **36** and associated entry and exit gates **71** and **72**, respectively. The purpose of the refresh memory loop is to provide a constant refresh of characters on the cathode ray tube screen.

Digital character codes, whether entered from input register **39** or from the central memory, enter the refresh memory loop at the character entry shift register **39** wherein the code is serially shifted bit by bit out of register **30** and into delay line **36** while substantially simultaneously parallel transferred into parallel storage registers in the X and Y digital-to-analog converters **27** and **28**. A complete raster of information comprising upwards of 1,500 character address signals may be dynamically stored in the recirculating delay line. Character entry register **30** is a seven-bit shift register comprising flip-flops **51**, **52**, **53**, **54**, **55**, **56**, and **57** which performs the dual function of input register interface through data entry gates **41**, **42**, **43**, **44**, **45**, and **46** and refresh memory access through data entry and exit gates **71** and **72**, respectively.

When a six-bit character address code is available for entry from input register **39**, the code is entered into register **30** only during the coincidence of a specified character bit time slot and a recirculating bit in the entry shift register. This bit is constantly recirculated and appears in the character entry register **30** only once per frame during (CTS), which is one bit time of a character word time slot, or approximately once every 14.78 milliseconds. This time slot is derived from the system clock, as will be explained with reference to FIG. **6**.

The recirculating bit is used when editing is desired; however, the editing as such does not form a part of this invention and is not desired. The CTS time slot is used in the present invention without editing in the intercharacter time, and is shown in FIG. 4*i*. Whenever a character code is available for entry, a DC signal is produced immediately after the formation of the character code on line **80** which clears flip-flops **51**, **52**, **53**, **54**, **55**, and **56** for entry of the character code and allows the recirculating bit to be located in register **30** in flip-flop **57**. Since register **30** is series connected to the delay line, one of the characters or retrace characters circulating in the loop is always present in the register. For editing operations, the recirculating bit must be attached to the character code in the entry register; however, this bit is not needed when no editing is to be performed, as in the present invention. The six bits contained in flip-flops **51**, **52**, **53**, **54**, **55**, and **56** are parallel transferred to flip-flops **61**, **62**, **63**, **64**, **65**, and **66** of the storage registers in X and Y digital-to-analog converters **27** and **28**. Should editing be performed, a logical one would be present in flip-flop **57** which would be parallel transferred with the six-bit digital code to flip-flop **67**, from which flip-flop an output would be produced which would control the editing.

As previously described, delay line data enters register **30** through input gate **71**. Phase D clock pulses shown in FIG. 4*e* from the central timing source shown in FIG. **6** are applied to register **30** along line **81**, and characters are transferred least significant bit first. Then, the seventh bit, intercharacter time (CTS), is the first to enter register **30** and is clocked into flip-flop **51** during the CTS time slot shown in FIG. 4i. The next six successive phase D pulses shift the six-bit character code into the register until after a total of seven bit times a complete character is held in the register. At phase A of the character time slot inputted on line **82**, the character code is parallel transferred into the X and Y digital-to-analog storage read-out registers, shown as register **60** which comprises flip-flops **61**, **62**, **63**, **64**, **65**, **66**, and **67**. Thus, the transfer is practically simultaneous with character entry into register **30**, since phase A is just one-quarter of a character time from phase D.

The character codes are held in the storage register for one character time for read-out, during which time the monoscope beam is deflected to a specific position on target **20** to produce a visual character on the cathode ray tube screen in accordance with the character code held in the read-out storage register **60**. The six-bit code is divided into two three-bit segments, three MSB's going to the X digital-to-analog converter **28**, and the three LSB's to the Y digital-to-analog converter **27**. The output of flip-flop **67** is applied to a line which is used when editing is desired.

The purpose of delay **36** is to dynamically store the character address signals which are recirculated in the refresh memory loop. Delay **36** is an internal storage device of the ultrasonic or sonic type with a magnetostrictive transducer input and output, although other dynamic delays of well-known design may be used. Amplifiers (not shown) are coupled to the input and output of delay **36** to compensate for attenuation incurred in the delay line. Two or more delays rather than one may be employed with appropriate pulse reforming amplifiers between them in the event that additional delay is needed for more character address codes. In any event, an entire frame, which may consist of 1,500 or more characters, may be delayed on the delay line. In the present embodiment, upwards of 1,200 characters and retrace characters must be delayed approximately 15 milliseconds and refreshed approximately 67 times per second.

The specific delay means which is well known consists of 50 to 100 feet of coiled wire into which a magnetostrictive transducer, which converts electrical into mechanical energy, applies a torsional vibration at one

end of the wire. This vibration travels down the wire at about 9 microseconds per inch and appears at the other end after a delay time which is dependent upon the length of wire used. At the output end, the torsional movement is reconverted into electrical energy after a delay of, for example, 7 to 15 milliseconds by a second magnetostrictive transducer.

The central timing source is shown in FIG. 6 and produces timing pulses for controlling data transfer and all other internal logical operations performed by the display terminal. All timing signals in the display terminal are originated by a 2.365411 MHZ clock in the timing circuits, the waveform of which is shown in FIG. 4*a*. This clock is synchronized by 591.352 KHZ clock which may be contained internally or externally when more than one unit is involved. This 591.352 KHZ waveform is shown in FIG. 4*b*.

There are six timing circuits: (1) the phase counter, (2) the 1.18 MHZ square wave circuit, (3) the bit counter, (4) the horizontal drive or retrace, (5) the vertical drive or retrace, and (6) the delta (Δ) circuit which times the first character of the first line on the cathode ray tube.

Phase counter 90 in FIG. 6 consists of dual flip-flops and decode gates. In phase counter 90, the 591 KHZ sync pulses enter and are serially clocked through the phase counter flip-flops by the synchronized 2.365411 MHZ clock signal developed in oscillator 89 to produce outputs X and Y, the waveforms of which are shown in FIGS. 4*c* and 4*d*, respectively, and which are decoded along with the 2.365411 MHZ clock signal to produce timing signals ϕA, ϕB, ϕC, and ϕD, respectively, the waveforms of which are shown in FIGS. 4*e*, 4*f*, 4*g*, and 4*h*, respectively.

As is apparent from FIGS. 4*a* and 4*p*, sync pulses being in ϕC and are used to develop the horizontal and vertical drive signals shown in FIGS. 2*c* and 3*c*, and 2*d* and 3*d*, respectively. The outputs from phase counter 90 are used throughout the display terminal to clock various operations during specific bit times, as will become apparent. The specific bit time may be called a character time slot CTS.

The relationship between the timing signals described above and the character time slot is shown by the waveforms of FIG. 4. Remembering that the 591.352 KHZ pulses and the 2.365411 MHZ clock pulses applied to the phase counter are combined therein to produce four phases of the master clock, ϕA, ϕB, ϕC, and ϕD, and that the phase counter is made synchronous with either external or internal timing by means of a 2.365411 MHZ clock, these phase counter outputs enable circuit operation at the beginning, middle or end of each bit. The timing relationship is such that the time span from ϕA to ϕD is equal to one bit time which is approximately 1.69 microseconds.

The ϕD output is used within the timing circuit as a clock input to bit counter 91 which consists of three flip-flops in a divide by seven network, thereby producing seven outputs, CTS, (CTS + 1), (CTS + 2), (CTS + 3), (CTS + 4), (CTS + 5), and (CTS + 6), shown in FIG. 4 as waveforms *i*, *j*, *k*, *l*, *m*, *n*, and *o*, respectively. Character time slot CTS occurs as the first bit of a character and is the intercharacter time, or in a system in which editing is used may provide timing for editing purposes. The character time slot plus one, (CTS + 1), shown in FIG. 4*j* occurs in coincidence with the least significant bit LSB of the six data bits of the character. The (CTS + 1) timing pulse may be used to gate additional data into the delay line memory. The (CTS + 2) through (CTS + 5) pulses are character intervals occurring in coincidence with data bits 2 through 5 and are used as timing pulses for gating data into the delay line memory and to perform logical operations coincident with the corresponding time slots. The (CTS + 6) pulse occurs in coincidence with the most significant bit MSB of the six data bits of a character, and is used to perform operations in coincidence with the (CTS + 6) time slot. The time span from CTS time to the next CTS time is 11.83 microseconds, which is equivalent to one character time.

The bit counter 91 is synchronized to the (CTS + 3) count each time by either internal or external sync received by flip-flop 92 which causes bit counter 91 to start counting at a binary 0 during (CTS + 3) by means of a clear bit counter pulse shown in FIG. 4*p* and syncs the bit counter at (CTS + 3) during character 46 line 23 phase A to a binary count of zero. Once the bit counter is synchronized, the flip-flops therein continuously cycle through the seven count sequence.

As previously mentioned, the sync pulses shown in FIG. 4*p* are used to develop the horizontal and vertical drive signals. The horizontal drive pulse is used to indicate the time required for the cathode ray tube scan to retrace from the end of one line to the beginning of the next line, which is 82.81 microseconds or seven character times.

The horizontal drive circuit 93 consists of a flip-flop and two input gates which generate the 82.81-microsecond gate signal shown in FIG. 3*c*. The leading edge of this pulse occurs at character count 46 in the ϕD portion of the (CTS + 6) time slot as is apparent from FIG. 3*c*. This gate pulse is followed by a 532-microsecond interval which represents the horizontal line trace time required to enter 45 characters into the memory. Thus, it takes 615 microseconds for the combination of horizontal retrace and trace of a single line to occur. At ϕA of the (CTS + 5) time slot of character 0 on line 1, the horizontal retrace is synchronized clear and appears on the trailing edge of ϕD of the (CTS + 6) time slot during character counts 46 and 1 of each line. The output of the same flip-flop that provides the horizontal retrace is inverted and also provides the vertical drive signal.

The vertical drive pulse is used to indicate the time required for the cathode ray tube scan to move from the last horizontal line up to the first horizontal line which is equivalent to 52 characters or 615 microseconds. When a gate detects a vertical drive pulse along with the sync pulse of FIG. 4*p*, the vertical drive pulse shown in FIGS. 2*d* and 3*d* is developed in a flip-flop in the vertical drive circuit 93 (the inversion of the horizontal output). The leading edge of ϕB during the (CTS + 2) time slot character count 46 line 23 (the last line) presents the vertical drive generation flip-flop which is cleared by the leading edge of the positive horizontal drive signal pulse which occurs at the leading edge of ϕB in the (CTS + 1) time slot of character 46 line 0. The vertical retrace time is a pulse approximately 611 microseconds wide, which is approximately equal to the horizontal line time. The gates are

separated by the frame time, 14.78 milliseconds, which is the time necessary to generate 23 horizontal lines plus the vertical retrace time. The refresh rate is 67 Hertz.

The delta pulse shown in FIGS. 2*f* and 3*f* is developed in logic circuitry **94**, which consists of two flip-flops and associated decode gates (not shown). This pulse is used throughout the display logic to initiate various display functions. It corresponds to the first word of each line and is reset during (CTS + 1) phase B of the next character.

Other control signals are developed in their respective time slots by various flip-flops and decode gates similar to those described above and these signals produce various timing pulses throughout the logic circuitry.

The 1.18 MHZ square wave generator **95** supplies a square wave which is applied to the vertical expansion generator **34** which feeds the Y deflection amplifier **25** and also to the high-frequency auxiliary vertical deflection coil **13** on the neck of the cathode ray tube. The 1.18 MHZ square wave is connected to a sine wave in the monoscope deflection amplifier.

The square wave signal is 180° out of phase on alternate cathode ray tube scans and is used to modulate the horizontal deflection voltage to increase the line height on the cathode ray tube screen to approximately 0.17 inch in the present embodiment. However, any suitable line height may be obtained by varying the excursion of the generated square wave. The phase reversal effectively doubles the frequency to produce a sharper horizontal line. In the Y amplifier, the minor vertical sweep signal causes the monoscope beam to paint the character being scanned as described with reference to FIG. 1, the phase reversal effectively doubling the number of times the character is painted, thereby providing a more accurate video output signal defining the character being scanned, and also locks the starting phase so that character sweeps always start during the same phase. In summary, the 1.18 MHZ square wave signal develops the minor vertical sweep signal used to produce the high resolution alphanumeric symbol character display on the cathode ray tube screen. Square wave generator **95** is clocked by the 2.365411 MHZ clock and by the negative (inverted) pulses in the vertical drive signal and comprises a flip-flop plus a series of logic gates which generate the 1.18 MHZ signal and which provide the frequency interlacing described above. FIGS. 2*e* and 3*e* illustrate this phase change in the 1.18 MHZ square wave.

Many additional modifications of this system are possible. For example, two delay line sections may be used in series with a signal reforming circuit interposed between the two sections instead of a single delay line. A further modification in which the total desired delay may be increased may be increased many comprise the recirculation of the output of the delay line as alternate bits of information back to the input so that each bit of information goes through the delay line twice.

What is claimed is:

1. A visual display system comprising:
- a cathode ray tube having a visual display area upon which characters are displayed in a raster pattern;
- character generation means for generating characters on the cathode ray tube;
- a central memory wherein character information is stored in the form of character address codes;
- a refresh memory loop including a delay line for providing a constant refresh of visual characters displayed on the cathode ray tube, the rate of refresh corresponding to the complete scan cycle of the cathode ray tube and the amount of character data in said refresh memory loop corresponding to one raster pattern;
- first transfer means for transferring character information from the central memory to the refresh memory loop; and
- second transfer means for transferring all of said character information from the refresh memory loop to the character generation means during each complete raster pattern.

2. A visual display system comprising:
- a cathode ray tube upon which characters are displayed in a raster pattern;
- character generation means for generating characters on the cathode ray tube;
- a refresh memory loop including a delay line for providing a constant refresh of visual characters displayed on the cathode ray tube, the rate of refresh corresponding to the complete scan cycle of the cathode ray tube and a number of characters recirculated in said refresh memory loop corresponding to one complete raster pattern;
- character code input means;
- first transfer means for transferring character codes from the character code generation means to the refresh memory loop; and
- second transfer means for transferring all of said character codes from the refresh memory loop to the character generation means during each complete raster pattern.

3. A visual display system in accordance with claim 2, wherein the delay line provides a delay time approximately equal to the time required for the cathode ray tube scan to move from a character position on the screen through a complete scan cycle and back to the original position.

4. A visual display system in accordance with claim 2, wherein the character code input means includes an input register.

5. A visual display system in accordance with claim 4, wherein the character code is a digital code.

6. A visual display system in accordance with claim 5, wherein the first transfer means comprises a shift register and the second transfer means comprises a storage register.

7. A visual display system in accordance with claim 6, wherein the first transfer means serially shifts the digital character code transferred to said first transfer means into the delay line and parallel transfers the character code into the second transfer means.

8. A visual display system in accordance with claim 7, wherein the digital character code transfers to the delay line and to the second transfer means occur only after a complete character code is present in the first transfer means.

9. A visual display system in accordance with claim 8, wherein the character generation means includes a target matrix which is scanned by an electron gun to produce an output video signal which is coupled to the cathode ray tube to produce the character display.

10. A visual display system in accordance with claim 9, wherein the character generation means further includes a digital-to-analog converter and a deflection amplifier whereby the digital character code transferred to the character generation means is converted to analog voltages which are applied to the deflection amplifier for positioning the output of the electron gun.

11. A visual display system in accordance with claim 1, wherein the delay line provides a delay time equal to the time required for the cathode ray tube scan to move from a character position on the screen through a complete scan cycle and back to the original position.

12. A visual display system in accordance with claim 1, wherein the character code is a digital code.

13. A visual display system in accordance with claim 1, wherein the first transfer means comprises a shift register and the second transfer means comprises a storage register.

14. A visual display system in accordance with claim 13, wherein the digital character code is serially shifted into the first transfer means.

15. A visual display system in accordance with claim 14, wherein the contents of the first transfer means is serially shifted into the delay line and parallel transferred into the second transfer means.

16. A visual display system in accordance with claim 15, wherein the digital character code transfers to the delay line and to the second transfer means occur only after a complete character code is present in the first transfer means.

17. A visual display system in accordance with claim 12, wherein the character generation means includes a target matrix which is scanned by an electron gun to produce an output video signal which is coupled to the cathode ray tube to produce the character display.

18. A visual display system in accordance with claim 17, wherein the character generation means further includes a digital-to-analog converter and a deflection amplifier whereby the digital character code transferred to the character generation means is converted to analog voltages which are applied to the deflection amplifier for positioning the output of the electron gun.

19. A visual display system comprising:

a cathode ray tube upon which characters are displayed in a raster pattern;

character generation means for generating characters on the cathode ray tube from character code information;

a recirculating delay line for providing a constant refresh of visual characters displayed on the cathode ray tube wherein the delay is equal to the time required for the cathode ray tube scan to move from a character position on the screen through a complete scan cycle and back to the original position and wherein the amount of character data recirculated in said recirculating delay line is equal to the number of characters included when said scan of said cathode ray tube moves from one of said character positions on the screen through said complete scan cycle and back to the original position;

first transfer means to which character code information is serially transferred from the delay line; and

second transfer means to which character code information is parallel transferred from the first transfer means, and from which character code information is transferred to the character generation means.

20. A visual display system in accordance with claim 19, wherein the character storage capacity of the delay line is greater than the possible number of characters displayable on the display area.

21. A visual display system in accordance with claim 20, wherein the delay line is a mechanical delay line.

22. A visual display system in accordance with claim 21, wherein the delay line is an ultrasonic delay line.

23. A visual display system in accordance with claim 2, wherein a mechanical delay line provides a delay time approximately equal to the time required for the cathode ray tube scan to move from a character position on the screen through a complete scan cycle and back to the original position.

24. A visual display system in accordance with claim 1, wherein a mechanical delay line provides a delay time equal to the time required for the cathode ray tube scan to move from a character position on the screen through a complete scan cycle and back to the original position.

25. A visual display system in accordance with claim 19, wherein the delay line is an ultrasonic delay line.

26. A visual display system in accordance with claim 2, wherein an ultrasonic delay line provides a delay approximately equal to the time required for the cathode ray tube scan to move from a character position on the screen through a complete scan cycle and back to the original position.

27. A visual display system in accordance with claim 1, wherein an ultrasonic delay line provides a delay time equal to the time required for the cathode ray tube scan to move from a character position on the screen through a complete scan cycle and back to the original position.

28. A visual display system in accordance with claim 19, wherein the delay line is a magnetostrictive delay line.

29. A visual display system in accordance with claim 2, wherein the delay line is a magnetostrictive delay line.

30. A visual display system in accordance with claim 1, wherein the delay line is a magnetostrictive delay line.

31. A visual display system comprising:

a cathode ray tube including means for scanning vertically and horizontally;

a monoscope with a target from which signals are derived for display on said cathode ray tube including means for scanning a region of the target of said monoscope containing a character to be presented on said cathode ray tube substantially linearly in one direction and substantially sinusoidally in another direction; and

means for synchronizing said sinusoidal scan to begin in a predetermined phase relationship with previous scans of said region.

32. A visual display system in accordance with claim 31, wherein said last mentioned means additionally modulates and synchronizes the cathode ray tube deflection voltage.

33. A visual display system in accordance with claim 32, wherein the signal supplied by the modulating means is phase shifted on alternative cathode ray tube

scans whereby the cathode ray tube line presentation is sharpened and the signal output from the monoscope target contains increased character information.

34. A visual display system including:

a visual display area for displaying character information;

local storage means for storing the addresses of all of the characters to be displayed on said visual display area; and

character generation means for generating a complete raster of characters on said display area in response to all of said character addresses from said local storage means such that each character on said visual display area is sequentially generated.

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