(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
26 May 2005 (26.05.2005)

PCT

(10) International Publication Number
WO 2005/048321 A1

(51) International Patent Classification[7]: H01L 21/00

(21) International Application Number:
PCT/US2004/033633

(22) International Filing Date: 12 October 2004 (12.10.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/705,499 10 November 2003 (10.11.2003) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

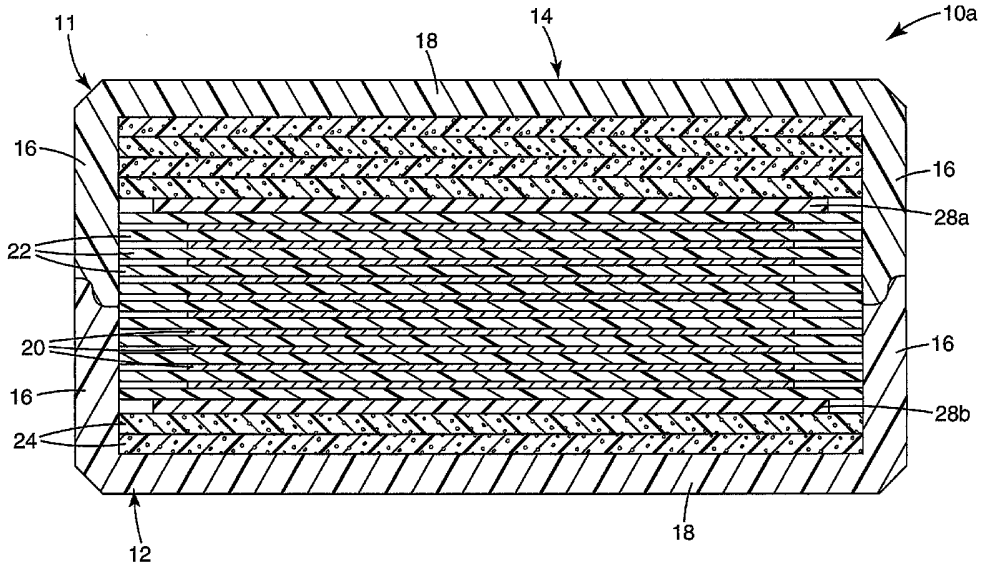
(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for the following designations AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS,*

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(54) Title: A CONTAINER FOR CONTAINING SEMICONDUCTOR WAFERS



(57) Abstract: A container for containing semiconductor wafers. A preferred embodiment of the invention provides a container for containing semiconductor wafers that includes a first container body including a base and a wall connected to the base, a first wafer support plate located inside the first container body; and at least one semiconductor wafer between the base of the first container body and the first wafer support plate, wherein the semiconductor wafer is stabilized between the first wafer support plate and the first container body.

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JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW, ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG)

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii)) for all designations*

Published:

— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

A CONTAINER FOR CONTAINING SEMICONDUCTOR WAFERS

TECHNICAL FIELD

The present invention relates to a container for containing semiconductor wafers. The present invention relates more particularly to a container for containing semiconductor wafers that includes a first container body including a base and a wall connected to the base, a first wafer support plate located inside the first container body; and at least one semiconductor wafer between the base of the first container body and the first wafer support plate, wherein the semiconductor wafer is stabilized between the first wafer support plate and the first container body.

BACKGROUND OF THE INVENTION

In the semiconductor industry, many types of semiconductor wafer containers have been utilized. These containers typically are supposed to protect the brittle wafers, minimize contamination from particulates, and minimize static electricity buildup. Some examples of such containers or systems maybe found in the following references: U.S. Pat. No. 4,787,508, U.S. Pat. No. 5,366,079, U.S. Pat. No. 5,553,711, U.S. Pat. No. 5,699,916, U.S. Pat. No. 6,119,865, U.S. Pat. No. 6,193,090, U.S. Pat. No. 6,193,068, U.S. Pat. No. 6,286,684, and PCT Publication WO 01/92135 A1.

In addition, various companies offer various containers for transporting semiconductor wafers between different locations, for example between raw wafer processing locations and finished wafer processing locations. As one example, Entegris, Inc. based in Chaska, Minnesota, offers wafer shipper systems for shipping various sized wafers ranging from 125 mm to 300 mm (4.92 in to 11.81 in.) in diameter, where the wafers are either stacked horizontally or vertically in a carrier. As another example, SPI/Semicon based in Ogden, Utah offers wafer storage and shipping systems for shipping various sized wafers ranging from 3 inches to 8 inches (76.2 mm to 203.2 mm) in diameter, where the wafers are typically stacked horizontally in a wafer jar and lid, including foam liners, foam cushion discs, and wafer interleaf discs between the wafers. As another example, Central Corporation based in Yamanashi, Japan offers horizontal

wafer shippers, where the wafers are stacked horizontally in a container including polyurethane cushions and spacers between the wafers. As another example, Malaster Company, Inc. based in Sunnyvale, CA offers horizontal wafer shippers, where the wafers are stacked horizontally in a container that has an internal cushion of foam along the outside of the wafers. As another example, 3M Company based in St. Paul, Minnesota offers reusable semiconductor wafer transport systems and services where the wafers are stacked horizontally in a container with foam-cushioning and wafer separators between the wafers. Typically, the 3M containers are inserted into an air cushioning packaging and then placed in a box for shipping.

SUMMARY OF THE INVENTION

One aspect of the present invention provides a container for containing semiconductor wafers. The container for containing semiconductor wafers comprises: a first container body including a base and a wall connected to the base; a first wafer support plate located inside the first container body; and at least one semiconductor wafer between the base of the first container body and the first wafer support plate, where the semiconductor wafer is stabilized between the first wafer support plate and the first container body.

In one preferred embodiment of the above container further comprises: a second wafer support plate located inside the first container body, where the second wafer support plate is between the base of the first container body and the semiconductor wafer, and where the semiconductor wafer is stabilized between the first wafer support plate and the second wafer support plate. In another preferred embodiment of the above container, the container further comprises: a second container body opposite the first container body, where the second container body includes a base and a wall connected to the base, and where the first container body is operatively connected to the first container body. In another aspect of this embodiment, the container further comprises: an internal cushioning member between the base of the second container body and the base of the first container body. In another aspect of this embodiment, the internal cushioning member is a foam-cushioning member. In another aspect of this embodiment, the internal cushioning member is an air-cushioning member.

In another preferred embodiment of the above container, the semiconductor wafer has a first major surface and a second major surface opposite the first major surface, where the first major surface has a first surface area, the first wafer support plate has a first major surface and a second major surface opposite the first major surface, the second major surface has a second surface area, the first major surface of the semiconductor wafer is opposite the second major surface of the first wafer support plate, and the first surface area of the semiconductor wafer is less than the second surface area of the first wafer support plate. In another aspect of this embodiment, the first surface area of the semiconductor wafer is at least 10% less than the second surface area of the first wafer support plate. In another aspect of this embodiment, the first surface area of the semiconductor wafer is at least 25% less than the second surface area of the first wafer support plate.

In another preferred embodiment of the above container, the container further comprises a plurality of semiconductor wafers inside the first container body. In another aspect of this embodiment, the container further comprises a plurality of wafer separator sheets, where a wafer separator sheet is between adjacent semiconductor wafers. In another preferred embodiment of the above container, when the container is dropped, the semiconductor wafer does not contact the wall of the first container body.

Another aspect of the present invention provides an alternative container for containing semiconductor wafers. This container for containing semiconductor wafers, comprises: a first container body including a base and a wall connected to the base; at least one semiconductor wafer where the semiconductor wafer has a first major surface and a second major surface opposite the first major surface, where the first major surface has a first surface area; a first wafer support plate located inside the first container body, where the first wafer support plate has a first major surface and a second major surface opposite the first major surface, where the second major surface has a second surface area; and where the semiconductor wafer is between the base of the first container body and second major surface of the first wafer support plate, where the first surface area of the semiconductor wafer is at least 10% less than the second surface area of the first wafer support plate, and where the semiconductor wafer is stabilized between the first wafer support plate and the first container body.

In one preferred embodiment of the above container, the container further comprises: a second wafer support plate located inside the first container body, where the

second wafer support plate is between the base of the first container body and the semiconductor wafer, and where the semiconductor wafer is stabilized between the first wafer support plate and the second wafer support plate. In another aspect of this embodiment, the first surface area of the semiconductor wafer is at least 25% less than the second surface area of the first wafer support plate. In another aspect of this embodiment, the container further comprises: a second container body opposite the first container body, where the second container body includes a base and a wall connected to the base, and where the first container body is operatively connected to the first container body. In another aspect of this embodiment, the container further comprises: an internal cushioning member between the base of the second container body and the base of the first container body. In another aspect of this embodiment, the internal cushioning member is a foam-cushioning member. In another aspect of this embodiment, the internal cushioning member is an air-cushioning member.

In one preferred embodiment of the above container, the container of further comprises a plurality of semiconductor wafers inside the first container body. In another aspect of this embodiment, the container further comprising a plurality of wafer separator sheets, where a wafer separator sheet is between adjacent semiconductor wafers. In another aspect of this embodiment, when the container is dropped, the semiconductor wafer does not contact the wall of the first container body.

Another aspect of the present invention provides yet another alternative container for containing semiconductor wafers. This container for containing semiconductor wafers, comprises: a first container body including a base and a wall connected to the base; a plurality of semiconductor wafer, where each semiconductor wafer has a first major surface and a second major surface opposite the first major surface, where the first major surface has a first surface area; a first wafer support plate located inside the first container body, where the first wafer support plate has a first major surface and a second major surface opposite the first major surface, where the second major surface has a second surface area; and where the plurality semiconductor wafers is between the base of the first container body and second major surface of the first wafer support plate, and where the first surface area of the semiconductor wafers is at least 10% less than the second surface area of the first wafer support plate; a second wafer support plate located inside the first container body, where the second wafer support plate has a first major surface and a

second major surface opposite the first major surface, where the plurality semiconductor wafer is between the second major surface of the first wafer support and first major surface of the second wafer support plate, where the first major surface of the second wafer support plate has a first surface area, where the first surface area of the semiconductor wafers is at least 10% less than the first surface area of the second wafer support plate, and where the semiconductor wafer is stabilized between the first wafer support plate and the second wafer support plate; a second container body opposite the first container body, where the second container body includes a base and a wall connected to the base, and where the first container body is operatively connected to the first container body; and an internal cushioning member between the base of the second container body and the base of the first container body, where the internal cushioning member is a foam-cushioning member; and a plurality of wafer separator sheets, where a separator sheet is between adjacent semiconductor wafers.

Another aspect of the present invention provides a method of safely shipping semiconductor wafers. This method comprises the steps of: a) providing a container for containing semiconductor wafers, where the container comprises: a first container body including a base and a wall connected to the base; a second container body including a base and a wall connected to the base; a first wafer support plate located inside the first container body; b) providing a plurality of semiconductor wafers; c) stacking the plurality of semiconductor wafers in a stack and placing the stack of semiconductor wafers inside the first container body; d) placing the first wafer support plate on the stack of semiconductor wafers inside the first container body; e) operatively connecting the first container body with the second container body so as to enclose the wafer support plate and stack of semiconductor wafers inside the container and to stabilize the stack of semiconductor wafers between the base of the first container body and the first wafer support plate.

In another aspect of this method, the container further comprises a second wafer support plate, step c) further comprises placing the second wafer support plate inside the first container body and placing the stack of semiconductor wafers on the second wafer support body inside the first container body, and the stack of semiconductor wafers is stabilized between the first wafer support plate and the second wafer support plate. In another aspect of the above method, the semiconductor wafers have a first major surface

and a second major surface opposite the first major surface, where the first major surface has a first surface area, where the first wafer support plate has a first major surface and a second major surface opposite the first major surface, where the second major surface has a second surface area, and where the first surface area of the semiconductor wafer is at least 10% less than the second surface area of the first wafer support plate. In another aspect of the above method, the first surface area of the semiconductor wafer is at least 25% less than the second surface area of the first wafer support plate. In another aspect of the above method, when the container is dropped, the semiconductor wafers do not contact the wall of the first container body.

In yet another aspect of the above method, step b) further comprises providing a plurality of wafer separator sheets, where a wafer separator sheet is between adjacent semiconductor wafers, step c) further comprising stacking the plurality of semiconductor wafers and the plurality of wafer separator sheets in a stack, a wafer separator sheet is between two adjacent semiconductor wafers, and placing the stack of semiconductor wafers and separator sheets inside the first container body. In another aspect of the above method, the method, further includes the steps of: f) transporting the container and stack of semiconductor wafers to a new location; g) separating the second container body from the first container body to remove the stack of semiconductor wafers from the container; h) inspecting the stack of semiconductor wafers and observing that the stack of semiconductor wafers are not damaged or broken.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be further explained with reference to the appended Figures, wherein like structure is referred to by like numerals throughout the several views, and wherein:

Figure 1 illustrates a cross-sectional view of prior art system for containing and transporting semiconductor wafers;

Figure 2a illustrates an expanded, cross sectional view of one preferred embodiment of the wafer transport system for containing and transporting semiconductor wafers of the present invention;

Figure 2b illustrates a cross sectional view of the wafer transport system of Figure 2a with the semiconductor wafers and other supporting materials enclosed within the container;

Figure 3 illustrates a cross sectional view of another preferred embodiment of the wafer transport system for containing and transporting semiconductor wafers of the present invention;

Figure 4 illustrates a cross sectional view of another alternative, preferred embodiment of the wafer transport system for containing and transporting semiconductor wafers of the present invention; and

Figure 5 illustrates a cross sectional view of yet another alternative, preferred embodiment of the wafer transport system for containing and transporting semiconductor wafers of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Integrated circuits are manufactured from semiconductor wafers that are typically round in shape and made of highly brittle silicon. Such wafers are subjected to a variety of processing steps in transforming the semiconductor wafers into integrated circuit components. When semiconductor wafers are manufactured, they are typically transported between different locations where different fabrication steps are performed. For example, a semiconductor wafer may be transported from a raw wafer manufacturing location to a semi-finished processing fabrication location, where the front side of the wafer is fabricated, and then to an assembly site where the wafer is diced into chips and packaged. These different processing locations may be as close as different buildings in the same plant, or may be geographically remote from each other, such as located in different states or even in different countries.

As the semiconductor wafers are getting larger in scale, now up to 300 millimeters in diameter, the density of the components is getting significantly greater. Moreover, semiconductor wafers are also getting thinner, providing much thinner completed integrated circuit packages. This has been driven, at least in part, by the cellular phone industry. Accompanying the trend towards larger, more dense and thinner wafers, the

wafers are becoming more valuable, more brittle, and more easily damaged during shipment. Due to the fragility of the semiconductor wafer, care must be taken in transporting the wafers to avoid damaging or breaking the wafers, which can be very expensive.

Traditionally, during the processing, storage, and shipping of the semiconductor wafers, the wafers are supported vertically in containers and constrained at their edges to prevent any contact between the wafers and possible damage or contamination to the faces of the wafers having the circuits thereon. Typically, the wafers are held vertically in the carrier by their edges (as opposed to lying flat) separated from each other by guides. These types of transport systems are typically known as "vertical shippers." Most of these vertical shippers require additional cushioning on the outside of the container, such as air cushioning packaging or traditional foam packaging. Usually, the vertical shippers and its accompanying external cushioning materials are placed in another container, and shipped to its next location. One example of a vertical shipper system is offered by Entegris, Inc. based in Chaska, Minnesota, and is referenced in the Background section of this application.

Alternatively, semiconductor wafers may be transported horizontally and supported in what are traditionally known as "horizontal shippers." One example of a prior art, horizontal shipper system is illustrated in Figure 1. 3M Company based in St. Paul, Minnesota offers this horizontal shipper system as the 3M™ Wafer Transport System. The wafer transport system 5 includes a container 11 made from a first container body 12 and a second container body 14. The first container body 12 and second container body 14 are sized and shaped to fit together, and may be held together by cooperative latches (not shown). One example of a suitable container 11 is taught in U.S. Pat. No. 6,193,090, "Reusable Container," (Connors et al.), which is hereby incorporated by reference. Each container body 12, 14 includes a base 18 attached to a wall 16. Preferably, the base 18 and the wall 16 are both cylindrically shaped to closely fit the outer edges of the circular semiconductor wafers 20.

A plurality of semiconductor wafers 20 is stacked within the container 11, with each wafer 20 separated from the other by a separator sheet 22. The separator support sheets help protect the faces of the semiconductor wafers 20. Separator sheets may be

flexible and made of a film. An example of a suitable separate sheet is made of a spun-bonded olefin material sold under the trade name TYVEK commercially available from E.I. du Pont de Nemours and Company, located in Wilmington, Delaware. The container 11 further includes a plurality of circular-shaped, internal cushioning members 24 or spacing members 24 between the base 18 of the container bodies 12, 14 and the stack of semiconductor wafers 20 and separator sheets 22. Preferably, the internal cushioning members 24 are foam-cushioning pads made from polyurethane open cell foam or polyethylene closed cell foam.

Surrounding the container 11 is an external cushioning member 26. For the 3M™ Wafer Transport System, the external cushioning member 26 is an air inflatable cushioning member. Examples of suitable air inflatable cushioning members are taught in U.S. Pat. No. 4,872,558, "Bag-In-Bag Packaging System," U.S. Pat. No. 6,283,296, "Quilted Inflatable Packaging Device," and U.S. Pat. No. 6,464,079, "Suspension Air Packaging Device, all of which are hereby incorporated by reference. Typically, the container 11 (along with its contents of semiconductor wafers 20, separator sheets 22, and internal foam-cushioning members 24) is placed inside the air cushioning packaging 26 and then the air cushioning packaging is inflated around the container, to provide cushioning to the container 11 and its contents. Then, the inflated air cushioning packaging 26 and container 11 are placed in a corrugated cardboard box, and the box is shipped to its destination. The box may include additional packaging materials inside the box to provide further cushioning of the container 11. After the box arrives, a user may deflate the air cushioning packaging 26, withdraw the container 11 from the packaging 26, and open up the container 11 to remove the semiconductor wafers 20.

The prior art vertical shippers and horizontal shippers for transporting the semiconductor wafers all generally require some external cushioning, such as air cushioning or foam-cushioning, outside of the wafer shipping containers to ensure that the semiconductor wafers make it safely to their destinations without damaging or breaking the semiconductor wafers. Often this external packaging can be more than two inches thick, which adds the overall shipping volume of the shipping box that holds the shipping container and external packaging. As illustrated by the examples, the present invention provides a shipping container that does not require external packaging outside of the shipping container, but instead relies on the configuration inside of the inventive shipping

container to protect the semiconductor wafers from damage or breakage. By minimizing the amount of external cushioning or eliminating the need for external cushioning outside of the semiconductor wafer shipping container, additional packaging materials are eliminated and the overall package volume is reduced, which results in lower overall costs of shipping semiconductor wafers, in comparison to prior art shipping containers or wafer transport systems. The present inventive container allows semiconductor wafers to be shipped inside the container within a simple, inexpensive, padded envelope or small, corrugated box without the need for significant, additional external packaging.

In addition, most of the prior art wafer shippers are shaped similarly to the shape of the wafers they contain. For example, the vertical shipping containers are approximately the same height as the height of the semiconductor wafers when they are stood up on their edges inside the containers. As another example, the circumference of the horizontal shipping containers match closely to the circumference of the semiconductor wafers. In fact, the prior art wafer shippers, both vertical and horizontal, are sold according to what size of wafers is to be shipped inside of them. For example, the 200 mm Horizontal Wafer Shipper System sold by Entegris, Inc. based in Chaska, Minnesota and the 200 mm Wafer Transport System sold by 3M Company based in St. Paul, Minnesota are both designed for shipping 200 mm (8diameter semiconductor wafers. The configuration of these prior art vertical and horizontal shippers to generally match the shape and circumference of the semiconductor wafers help to distribute the stress of holding the wafers evenly along the outside circumference of the wafers. Since the edges of semiconductor wafer correspond to the circumference of the carrier, there is no concentration of stress at any particular point along the semiconductor wafer because of the close fit between the wafer and its carrier, which helps minimize damage to the semiconductor wafers, so long as the wafer containers are shipped in appropriate cushioning materials outside the containers

The inventors of this patent application have discovered that the damage to or breakage of the semiconductor wafers during shipping is frequently caused by the edge of the wafer contacting or impacting the edge of the carrier causing the edge of the wafer to become distorted, damaged, or crushed. Often when the semiconductor wafer contacts the edge of the carrier, it may cause a break along the edge of the wafer that may eventually propagate throughout the entire wafer, causing the wafer to break into pieces. The present

invention offers improved protection of the edges of the semiconductor wafers, thus avoiding damage to or breakage of the wafers during shipping.

Overall, the wafer transport system of present invention protects the semiconductor wafers from mechanical shock, damage, or breakage while the wafers are being shipped between various locations, thus avoiding unnecessary costs resulting from damaged wafers occurring during shipping. The inventive wafer transport system also helps reduce overall shipping volume for shipping the semiconductor wafers, which eliminates unnecessary associated packaging components and results in overall savings in the packaging and shipping of the semiconductor wafers.

One embodiment of the wafer transport system 10a of the present invention is illustrated in Figures 2a and 2b. Figure 2a illustrates an expanded view of the wafer transport system 10a and Figure 2b illustrates the semiconductors and other supporting materials enclosed within the container.

The wafer transport system 10a includes some of the same components as the prior art wafer transport system 5 illustrated in Figure 1. The system 10a includes the container 11 made from a first container body 12 and a second container body 14. The first container body 12 and second container body 14 are sized and shaped to fit together, and may be held together by cooperative latches (not shown). One example of a suitable container 11 is taught in U.S. Pat. No. 6,193,090, "Reusable Container," (Connors et al.), which is hereby incorporated by reference. Each container body 12, 14 includes a base 18 attached to a wall 16. Preferably, the container bodies 12, 14 are cylindrically shaped. For example, the base 18 is the shape of a circle and the wall 16 is in the shape of a cylinder. Preferably, the surface area of the bases 18 is larger than the surface area of the semiconductor wafers 20. Likewise, the inside circumference of the wall 16 is larger than the outer circumference of the semiconductor wafers 20. For example, the inside diameter of the base 18 may be 200 mm and the diameter of the semiconductor wafers may be 150 mm. Alternatively, the container bodies may be any shape or size. For instance, the container bodies may be octagonal shaped. However, it is preferred that the surface area of the base 18 is larger than the surface area of the semiconductor wafers 20. The container 11 may be injected molded or blow molded plastic material. Preferably, the

container 11 is designed for special cleanliness or reduced static discharge, for example by choosing materials, cleaning procedures, and process controls

A plurality of semiconductor wafers 20 is stacked within the container 11. Each semiconductor wafer 20 has a first major surface 21 and a second major surface 23 opposite the first major surface. Each semiconductor wafer 20 is separated from the other by a wafer separator sheet 22. An example of a suitable wafer separator sheet is made of a spun-bonded olefin material sold under the trade name TYVEK commercially available from E.I. du Pont de Nemours and Company, located in Wilmington, Delaware. The separator support sheets help protect the faces of the semiconductor wafers. Preferably, the surface area of the major surfaces of the separator sheets 22 is larger than the surface area of the major surfaces 21, 23 of the semiconductor wafers 20. The large separator sheets also help protect the edges of the semiconductor wafers 20. Preferably, the separator sheets are sized to fit the surface area inside the container bodies 12, 14. However, the separator sheets 22 may be of any size or shape, so long as they protect the faces of the semiconductor wafers 20.

The separator sheets 22 may be selected such that the material the sheets 22 are made of have a high coefficient of friction. This has the benefit of helping the semiconductor wafers 20 between the separator sheets 22 resist lateral movement, and helps to stabilize the stack of semiconductor wafers 20 and sheets 20 inside the container 11.

The container 11 further includes a plurality of internal cushioning members 24 between the bases 18 of the container bodies 12, 14 and the stack of semiconductor wafers 20 and separator sheets 22. Preferably, the internal cushioning members 24 are foam-cushioning pads made from polyurethane open cell foam. Preferably, the internal cushioning members 24 have a larger surface area than the surface area of the semiconductor wafers 20. Preferably, the internal cushioning members 24 are sized and shaped to fit closely inside the container bodies 12, 14. The system 10a may include any number of internal cushioning members 20. The internal cushioning members 24 function to help fill up volume inside the container 11 to assist in applying pressure between the bases 18 of the container bodies 12, 14 and the wafer support plates 28.

The wafer transport system 10a preferably includes at least one wafer support plate 28. However, the wafer transport system 10a may include any number of wafer support plates 28. The system 10a is illustrated as having a first wafer support plate 28a and a second wafer support plate 28b. The first wafer support plate 28a is between one end of the stack of semiconductor wafers 20 and separator sheets 22 and the base 18 of the second container body 14. The second wafer support plate 28b is between the opposite end of the stack of semiconductor wafer 20 and separator sheets 22 and the base 18 of the first container body 12. Each surface support plate includes a first major surface 30 and a second major surface 32 opposite the first major surface.

Preferably, the wafer support plates 28 are rigid and not easily bendable. A suitable wafer support plate 28 is made of steel, plywood, or a hard plastic. The wafer support plates 28 may be made of metal, ceramic, a hard plastic depending on the specific needs for rigidity, cleanliness, chemical compatibility and static dissipative characteristics. Examples of suitable plastic materials include polypropylene, polycarbonate, and an acetal resin plastic sold under the trade name DELRIN, which is commercially available from E.I. du Pont de Nemours and Company, located in Wilmington, Delaware. Preferably, the rigid support plates 28 are at least five times as thick as the semiconductor wafers 20. Preferably, the major surfaces 30, 32 of the rigid support plates 28 respectively have a surface area larger than the surface areas of the major surfaces 21, 23 respectively of the semiconductor wafers. For example, the rigid support plates 28 may have a diameter of 175 mm and the semiconductor wafers 20 may have a diameter of 150 mm. However, the rigid support plates 28 may be sized to fit closely inside the container bodies 12, 14. For example, the rigid support plates 28 may have a diameter of 298 mm and the inside diameter of the base 18 of the container bodies 12, 14 may have a diameter of 300 mm.

The rigid support plates 28 function to stabilize the stack of semiconductor wafers 20 within the container 11 to prevent damage to or breakage of the wafers 20 during shipping or transport of the container 11. When using the term "stabilized" as used in reference to the stack of semiconductor wafers, including the claims, it is meant that that stack of semiconductor wafers is resistant to change its relative position. The thicknesses of the foam internal cushioning members 24, the rigid support plates 28, and stack of semiconductor wafers 20 and wafer separator sheets 22 are all configured such that all of the components together tightly fit into the container 11 when the first container body 12

and second container body 14 are closed together. With this configuration, the first rigid support plate 28a presses down upon the stack of semiconductor wafers 20, pressing the stack of wafers against the base 18 of the first container body 12. At the same time, the second rigid support plate 28b presses against the stack of semiconductor wafers 20, pressing the stack of wafers against the base 18 of the second container body 14. Because the stack of semiconductor wafers 20 is tightly held between the first and second rigid plates 28a, 28b, this helps prevent the movement or rotation of the semiconductor wafers 20 within the container 11, even when the container is shaken or dropped. The forces applied to the semiconductor wafers 20 by the rigid plates 28 are in a direction that is at a 90° angle relative to the major surface of the semiconductor wafers, which helps prevent the semiconductor wafers from slipping in the direction of their major surface. The normal force on the support plates 28 and stack of wafers and separator sheets also helps keep the wafers 20 stabilized within the container 11. The first and second rigid plates 28a, 28b apply equal or substantially equal forces on the wafers, which helps keep the semiconductor wafers 20 rigid, so they will not flex. This feature is especially useful with protecting semiconductor wafers from damage or breaking because semiconductor wafers will often bend and commonly break because they are so thin. Lastly, the uniform or substantially uniform pressure applied to the stack of semiconductor wafers 20 by the rigid support plates 28a, 28b, helps prevent the relative position of the wafers from changing within the container 11, which assists in safely transporting them without damage to or breakage of the wafers.

Preferably, the surface area of the major surfaces 21, 23 of the semiconductors 20 is smaller than the diameter of the rigid support plates 28 to help protect the edges of the semiconductor wafers 20. As explained above, the inventors of this patent application have discovered that the damage or breakage of the semiconductor wafers during shipping is frequently caused by the edge of the wafer contacting or impacting the edge of the carrier causing the edge of the wafer to become distorted, damaged, or crushed. Often when the wafer contacts the edge of the carrier, it may cause a break along the edge of the wafer that may eventually propagate throughout the entire wafer, causing the wafer to break into pieces. By shipping the semiconductor wafers 20 with at least one rigid support plates 28 that have a larger surface area than the semiconductor wafers, this configuration helps prevent the wafers from contacting or impacting the walls 16 of the container bodies

12, 14, thus helping to prevent damage or breakage of the semiconductor wafers during shipping or transport.

Preferably, the surface area of the major surfaces 21, 23 of the semiconductor wafers 20 is smaller than the surface areas of the major surface 30, 32 of the rigid support plate 28. In addition, the surface area of the major surfaces 21, 23 of the semiconductor wafers 20 is smaller than the surface areas of the bases 18 of the container bodies 12, 14. More preferably, the area of the major surfaces 21, 23 of the semiconductor wafer 20 is at least 10% less than the area of the second surface 30, 32 of the wafer support plates 28a, 28b. More preferably, the area of the major surfaces 21, 23 of the semiconductor wafer 20 is at least 25% less than the area of the second surface 30, 32 of the wafer support plates 28a, 28b. For example, for shipping semiconductor wafers 20 with a 150 mm diameter, (which is an approximate surface area of 17671 mm^2), it is recommended that the diameter of the rigid support plate be at least 175 mm diameter (which is an approximate surface area of 24,053 mm^2), or at least 200 mm (which is an approximate surface area of 31416 mm^2). Preferably there should be about 10 mm or more of distance between the edge of the semiconductor wafers 20 and the walls 16 of the container bodies 12, 14 all the way around the semiconductor wafer 20. However, the major surfaces 30, 32 of the wafer support plates 28a, 28b may be any size or shape, so long as they have a larger surface area than the surface area of the semiconductor wafers 20 to adequately protect the edges of the wafers from contacting the side walls 16 of the container 11 to help prevent damage to or breakage of the wafers. Prior art shipping containers, such as those described above, typically are sized to be just slightly bigger than the diameter of the semiconductor wafers they are to receive, for instance just a few millimeters larger than the diameter of the wafer, so as to allow the wafers to fit inside of the container. However, this is in sharp contrast to the present invention, where the containers are purposefully designed to allow a certain amount of space between the edges of the semiconductor wafers 20 and the side walls 16 of the container to adequately protect the edges of the wafers from contacting the walls 16.

The rigid support plates 28 may be selected such that the material the sheets 28 are made of have a high coefficient of friction. This has the benefit of helping the stack of semiconductor wafers 20 between the support plates 28 resist lateral movement ,and helps to stabilize the stack of semiconductor wafers 20 and sheets 20 inside the container 11.

Figure 3 illustrates an alternative wafer transport system 10b for the storage and transport of semiconductor wafers safely without damage or breakage. The system 10b is very similar to the system 10a illustrated in Figures 2a and 2b and functions similarly. System 10b includes the same stack of semiconductor wafers 20 and separator sheets 22, and the same support plates 28 as system 10a. The container 11 of system 10b is made from container bodies 12, 14 similar to the system 10a. However, the system 10b differs from system 10a in that it does not include the internal cushioning members. Instead, the depth of the container 11 is configured to closely hold a stack of semiconductor wafers 20, separator sheets 22, and at least one rigid support plate 28a. The first container body 12 and second container body 14 both have latches to allow for a snap fit between the container bodies 12, 14. A user may insert a stack of semiconductor wafers 20 and separator sheets 22 inside the first container body 12, and then press fit the second container body 14 onto the first container body 12 until adequate pressure is applied by the rigid support plate 28a against the stack of semiconductor wafers. The first rigid support plate 28a applies a force to the stack of semiconductor wafers 20 and separator sheets 22, pinning the stack against the base 18 of the first container body 12, so as to stabilize the semiconductor wafers 20 and to prevent the movement of the semiconductor wafers 20 within the container 11, even when the container 11 is tilted or dropped, for example during transport or shipping. In addition, similar to the system 10a described above, the support plate 28a and separator sheets 22 are both preferably of larger surface area compared the surface area of the semiconductor wafers to protect the edges of the semiconductor wafers 20 from contacting the side walls 16 of the container 11. The surface area of the bases 18 of the container bodies 12, 14 are also larger than the surface area of the semiconductor wafers 20 to accommodate the support plates 28.

Alternatively, the system 10b may include a second rigid support plate 28b between the stack of semiconductor wafers 20 and the base 18 of the first container body 12. However, a second support plate 28b is not necessary. In addition, the support plates 28 may be separate from the container bodies 12, 14, or integrally molded as part of the container bodies 12, 14. Also, the wafer transport system 10b may optionally include any number of internal cushioning members.

Figure 4 illustrates an alternative wafer transport system 10c for the storage and transport of semiconductor wafers safely without damage or breakage. The system 10c is

very similar to the system 10a illustrated in Figures 2a and 2b and functions similarly. System 10c includes the same stack of semiconductor wafers 20 and separator sheets 22, the same support plates 28, and the same container 11 as system 10a. However, the wafer transport system 10c differs from wafer transport system 10a in that it does not include the internal cushioning members 24. Instead, the wafer transport system 10c includes an internal, inflatable air-cushioning member 36, which may be inflated after the first container body 12 and second container body 14 are closed together. The second container body 14 has a hole in its base 18 to accommodate the valve and air supply tube 38 to the internal air-cushioning member 36. The air-cushioning member 36 allows for the convenience of placing stacks of semiconductors 20 and separator sheets 22 of varying heights inside of the container 11 without the need for varying containers of different depths. Alternatively, the air-cushioning member 36 may be inflated to its proper size prior to placing it inside the container 11, and then attaching the second container body 14 to the first container body 12.

After the stack of semiconductors 20 and separate sheets 22 is placed inside the first body container 12, the first rigid support plate 28a is place on top of the stack and the deflated, the internal, air cushioning member 36 is placed on top of the rigid wafer support plate. The valve and air hose is pulled through the hole in the second container body 14 and the second container body 14 is attached to the first container body 12. Next, the internal, air cushioning member 36 is inflated until the member 36 is pressing sufficient force against the first rigid wafer support plate 28a, such that the semiconductor wafers 20 are stabilized between the support page 28a and the base 18 of the first container body. Preferably, enough air is pumped into the air cushioning packaging 36 to apply pressure against the first wafer support plate 28a and thus apply pressure against the stack of semiconductor wafers, so as to prevent the movement of the semiconductor wafers 20 within the container 11, even when the container is tilted or dropped, for example during shipping or transport of the container . In addition, similar the system 10a described above, the major surfaces of the support plate 28a and separator sheets 22 are all preferably of larger surface area compared the surface area of the major surfaces 21, 23 of the semiconductor wafers to protect the edges of the semiconductor wafers 20 from contacting the side walls 16 of the container 11. The surface area of the bases 18 of the

container bodies 12, 14 are also preferably larger than the surface area of the major surfaces 21, 23 of the semiconductor wafers 20 to accommodate the support plates 28.

Alternatively, the system 10c may include a second rigid support plate 28b between the stack of semiconductor wafers 20 and the base 18 of the first container body 12. However, a second support plate is not necessary. In addition, the second support plate 28b may be separate from the first container bodies 12 or integrally molded as part of the first container bodies 12.

Figure 5 illustrates an alternative wafer transport system 10d for the storage and transport of semiconductor wafers safely without damage or breakage. The system 10d is very similar to the system 10c illustrated in Figure 4 and functions similarly. System 10d includes the same stack of semiconductor wafers 20 and separator sheets 22, and the same support plates 28 as system 10a. The container 11 of system 10d is made from the first container body 12 similar to the system 10c. However, the system 10d differs from system 10c in that the air cushioning member 40 completely surrounds the container 11 and the air cushioning member 40 and container 11 are enclosed inside another container, such as a box 42. A user may insert a stack of semiconductor wafers 20 and separator sheets 22 inside the first container body 12 and then place the first wafer support plated 28a on top of the stack. The container 11 is then placed inside an uninflated air-cushioning member 40. Next, the air cushioning packaging member 40 is inflated until the first rigid support plate 28a applies a force to the stack of semiconductor wafers 20 and separator sheets 22, pinning the stack against the base 18 of the first container body 12, so as to stabilize the semiconductor wafers 20 and to prevent the movement of the semiconductor wafers 20 within the container 11, even when the container 11 is tilted or dropped, for example during transport or shipping. In addition, similar the system 10c described above, the support plate 28a and separator sheets 22 are both preferably of larger surface area compared the surface area of the semiconductor wafers to protect the edges of the semiconductor wafers 20 from contacting the side walls 16 of the container 11. The surface area of the bases 18 of the container bodies 12, 14 are also larger than the surface area of the semiconductor wafers 20 to accommodate the support plates 28. Lastly, the air cushioning member 40 and container 11 may be placed inside another container 42 and shipped to its destination.

Alternatively, the system 10d may include a second rigid support plate 28b between the stack of semiconductor wafers 20 and the base 18 of the first container body 12. However, a second support plate 28b is not necessary. In addition, the first support plate 28b may be separate from the first container body 12 or integrally molded as part of the container body 12.

The wafer transport systems 10a-10d are all illustrated as horizontal type shippers, where the semiconductor wafers are stacked horizontally. However, the wafer transport systems 10a-10d may just as easily carry the semiconductor wafers vertically by turning the systems 90°.

All of the wafer transport systems 10a, 10b, 10c, 10d are designed to not require external air cushioning or foam packaging outside of the containers 11, such as illustrated in Figure 1, to protect the semiconductor wafers. Instead it is recommended that the systems 10, 10b, 10c, 10d may be used with a simple padded envelope or corrugated box to ship semiconductor wafers safely without damage or breakage.

The system 10 of the present invention has been described above as being particularly useful for shipping semiconductor wafers. However, the system may be used for shipping a variety of objects, such as records, CDs, DVDs, or any flat, fragile items made of glass, ceramic, or other similar materials..

The operation of the present invention will be further described with regard to the following detailed examples. These examples are offered to further illustrate the various specific and preferred embodiments and techniques. It should be understood, however, that many variations and modifications may be made while remaining within the scope of the present invention.

Test Methods

Free Fall Drop Test

One embodiment of the container for semiconductor wafers of the present invention was prepared. The embodiment of the container was similar to the containers described above. The outside of the container was in the shape of an octagon, while the inside of the container (the base and the walls) was in the shape of a circle. The container was prepared as described below having semiconductor wafers stored therein, and was placed inside a bubble mailer, which was commercially available under the

Jiffylite brand from Sealed Air Corporation located in Saddle Brook, New Jersey, and evaluated as described in ASTM D 5276-98, "Standard Test Method for Drop Test of Loaded Containers by Free Fall." The impact surface was steel. One of two different procedures was employed. The first procedure used the "Six Flat Drop Cycle" wherein the article to be tested was dropped six times from a height of 48 inches (122 centimeters (cm)), such that it landed one time on each face surface of the article, which included the two major surfaces of the mailer and the four edges of the mailer. Two test sets were run. After completion of this test, the container for semiconductor wafers was opened and the semiconductor wafers inspected for damage to or breakage of the wafers. Undamaged semiconductor wafers from the first test set were employed in the second test set.

The second procedure used the "Ten Drop Cycle," where the same container from the Six Flat Drop Cycle and semiconductor wafers were placed inside a corrugated box and then were dropped a total of ten times from a height of 30 inches (76 cm): once so it landed on a corner, three times on each edge forming that corner, and once on each of the six different face surfaces of the container. .

Controlled Shock Test

A sample of the rigid support plates of the container for semiconductor wafers of the present invention having semiconductor wafers stored therein was evaluated as described in ASTM D 3332-99, "Standard Test Method for Mechanical-Shock Fragility of Products, Using Shock Machines." Specifically, "Test Method A – Critical Velocity Change Shock Test" of ASTMD 3332-99 was employed using a shock machine (Model 846 MTS Shock Machine commercially available from MTS Systems Corp, located in Eden Prairie, Minnesota). The carriage was aluminum. The wafers were held between rigid plates on the shock testing machine, in either a horizontal or vertical orientation and tested at equivalent free fall drop heights of from 18 inches (45.72 cm.) to 66 (167.64 cm.) inches in increments of 6 inches (15.2 cm).

Examples

Comparative Examples 1-2 and Examples 1-5

One embodiment of the container for semiconductor wafers of the present invention was used in Examples 1-7. This container was similar to the container illustrated in Figures 2a and 2b. The outside of the container was in the shape of an octagon, while the inside of the container (the base and the walls) was in the shape of a circle. The rigid plates were also in the shape of a circle The first container body and second container body were joined together, having a wafer holding area therein, with 150 mm diameter semiconductor wafers stored inside and prepared as follows. The following materials were placed in a horizontal position, ordered from bottom to top, in the wafer holding area of the first container body:

1. 0.25 inch (6.35 millimeters (mm)) thick, circular shaped polyurethane open cell foam cushion pads;
2. (where employed) a flat 0.125 inch (3.18 mm) thick, circular shaped, plastic support plate made from acetal resin material sold under the trade name DELRIN, commercially available from E.I. du Pont de Nemours and Company, located in Wilmington, Delaware;
3. a stack of 0.006 inch (152 micrometers) thick, circular shaped separator sheets made of a spun-bonded olefin material sold under the trade name TYVEK commercially available from E.I. du Pont de Nemours and Company, located in Wilmington, Delaware) and 0.0177 inch (450 μm) thick semiconductor wafers, arranged such that 12 wafers were separated from each other and covered by 13 separator sheets;
4. (where employed) a second support plate as described above in #2; and
5. additional foam pads as described above in #1.

The second container body of the container was then securely fastened to the first container body using cooperative latches attached to the first and second container bodies, such that sufficient pressure was applied to the contents, so that the lateral movement of the items was minimized. The container was then placed inside a bubble mailer, which was commercially available under the Jiffylite brand from Sealed Air Corporation located in Saddle Brook, New Jersey. Then, the container and bubble mailer was evaluated using

the "Six Flat Drop Cycle" test as described in the test method "Free Fall Drop Test" above. The results are shown in Table 1 below.

Table 1

Ex.	Wafer Holding Area Diameter (mm)	Wafer Diameter (mm)	No. of Wafer Support Plates and Plate Diameter (mm)	No. of Foam Pads and Pad Diameter (mm)	Separator Sheet Diameter (mm)	Test Set 1 (No. of Broken Wafers out of 12)	Test Set 2 (No. of Broken Wafers out of 12)
CE 1	150	150	None	7 @ 150	150	4	2
1	150	150	2 @ 150	6 @ 150	150	2	2
2	200	150	2 @ 175	6 @ 200	200	0	0
3	200	150	1 @ 175	6 @ 200	200	0	0
4	200	150	2 @ 200	6 @ 200	200	0	0
5	200	150	1 @ 200	6 @ 200	200	0	0
CE 2	200	150	None	7 @ 200	200	0	3

Example 1-5 and comparative examples 1-2 above help illustrate some unexpected benefits of the present invention. First, when either one or two of the rigid wafer support plates were included in the semiconductor wafer container, the number of broken semiconductor wafers was reduced by half in Test Set 1 (from 4 broken wafers to 2 broken wafers in comparison to the Comparative Example 1) and no semiconductor wafers were broken in Examples 2-5, Test Sets 1 and 2. . Second, when either one or two of the rigid wafer support plates having diameters larger than diameters of the semiconductor wafer (and thus greater surface area) were included in the semiconductor wafer container, the number of broken semiconductor wafers dropped to zero in all of the test sets for Examples 2-5. In contrast, when the container did not include any rigid support plates, the wafers were broken in all of the Comparative Examples, except for Test Set 1 of Comparative Example 2. .

Comparative Example 3-4 and Examples 6-10

Examples 1-5 were repeated with the following modification to perform Examples 6-10, with the modification that the thickness of the semiconductor wafers was 0.008 inches (200 micrometers). The results are shown in Table 2 below.

Table 2

Ex.	Wafer Holding Area Diameter (mm)	Wafer Diameter (mm)	No. of Wafer Support Plates and Plate Diameter (mm)	No. of Foam Pads and Pad Diameter (mm)	Separator Sheet Diameter (mm)	Test Set 1 (No. of Broken Wafers out of 12)	Test Set 2 (No. of Broken Wafers out of 12)
CE3	150	150	None	7 @ 150	150	4	8
6	150	150	2 @ 150	6 @ 150	150	9	10
7	200	150	2 @ 175	6 @ 200	200	0	0
8	200	150	1 @ 175	6 @ 200	200	0	0
9	200	150	2 @ 200	6 @ 200	200	0	0
10	200	150	1 @ 200	6 @ 200	200	0	0
CE4	200	150	None	7 @ 200	200	0	1

Examples 6-10 above help illustrate some unexpected benefits of the present invention. First, when at least one or two rigid wafer support plates were included in the container, the number of broken semiconductor wafers was reduced to zero in all of the Examples, except for Example 6. Second, when the diameter of the rigid wafer support plate was larger than the diameter of the semiconductor wafers (and thus, had a larger surface area), the number of broken semiconductor wafers was reduced to zero in Examples 7-10. In contrast, when no rigid wafer support plates were included in the container, at least one of the wafers was broken in all of the Comparative Examples 3 and 4, except Test Set 1 of Comparative Example 4.

Example 11

A sample of another embodiment of the container for semiconductor wafers of the present invention was used for Example 11. This container was similar to the container illustrated in Figure 5. The outside of the container was in the shape of a circle, and the inside of the container (the base and the walls) was also in the shape of a circle. The rigid plates were also in the shape of a circle. The container was formed from a first container

body having a wafer holding area therein and a flat, circular-shaped rigid wafer support plate on top. The wafer support plate was prepared from plywood having a thickness of 0.50 inches (1.3 centimeters). A container containing semiconductor wafers was prepared as follows. The following materials were placed in a horizontal position, ordered from bottom to top, in the wafer holding area of the container body:

1. a 0.25 inch (6.35 millimeters (mm)) thick, circular shaped polyurethane open cell foam cushion pad;
2. an stack of 0.006 inch (152 micrometers) thick, circular shaped separator sheets made of a spun-bonded olefin material sold under the trade name TYVEK commercially available from E.I. du Pont de Nemours and Company, located in Wilmington, Delaware and 0.0177 inch (450 micrometers) thick semiconductor wafers, 150 mm diameter, arranged such that 3 wafers were separated from each other and covered by 4 separator sheets; and
3. a 0.25 inch (6.35 millimeters (mm)) thick, circular shaped polyurethane open cell foam cushion pad; and
4. the 0.50 inches (1.3 cm) thick plywood wafer support plate.

The base of the wafer holding area in the container body and the wafer support plate both had a diameter of 200 millimeters. Next, the assembly of the container and its components therein was placed inside a 3M™ Air Cushion Packaging system (available from 3M Company, St. Paul, MN) having a un-inflated size of 16 inches x 16 inches (40.6 centimeters x 40.6 centimeters). The air packaging cushioning member was inflated to 1.25 psi and as a result, the wafer support plate of the wafer transport system was held in place by the pressure of the inflated air-cushioning member surrounding the wafer transport system. Next, wafer transport system and inflated air cushioning member was placed inside a closely fitting, corrugated cardboard box, having inside dimensions of 14 inches by 12 inches by 9 inches (35.6 cm by 30.5 cm by 22.9 cm). This entire article was then evaluated using the "Ten Drop Cycle" test as described in the test method "Free Fall Drop Test"" above. The results are shown in Table 3 below.

Table 3

Ex.	Wafer Holding Area Diameter (mm)	Wafer Diameter (mm)	No. of Wafer Support Plates and Plate Diameter (mm)	No. of Foam Pads and Pad Diameter (mm)	Separator Sheet Diameter (mm)	Test Set 1 (No. of Broken or Damaged Wafers out of 3)	Test Set 2 (No. of Damaged or Broken Wafers out of 3)
11	200	150	1 @ 200	2 @ 200	4 @ 200	0	0

Example 11 above helps illustrate that the semiconductor wafers did not break and were not damaged when they were held between two rigid, wafer support plates that had a larger surface area than the surface area of the semiconductor wafers.

Examples 12-20

A portion of the wafer transport system described above was assembled, fixed in both a vertical and horizontal manner, and tested for drop shock sensitivity. More specifically, the following materials were assembled, ordered from bottom to top, as follows:

1. a 0.50 inch (1.25 cm) thick, 8 inch (20.3 cm) diameter aluminum plate;
2. a stack of 0.006 inch (152 micrometers) thick, 200 millimeter diameter, circular shaped separator sheets of TYVEK (a spun-bonded olefin material available from E.I. du Pont de Nemours and Company, Wilmington, DE) and semiconductor wafers having a diameter of 200 mm and a thickness of 280 micrometers, arranged such that 2 wafers were separated and covered by 3 separator sheets; and
3. a 0.50 inch (1.25 cm) thick, 8 inch (20.3 cm) diameter aluminum plate.

The assembly described above was then tightly joined together with C-clamps and locked on the shock testing machine in either a vertical or horizontal orientation and evaluated for drop shock sensitivity as described in the test method "Controlled Shock Test" above. Then, the semiconductor wafers were inspected for damage to or breakage of the wafers. The results are shown in Table 4 below.

Table 4

Ex.	Drop No.	Equivalent Free Fall Drop Height (inches)	Velocity Change (in./sec.)	Peak Acceleration (G-sec.)	Pulse Duration (milli-seconds)	Damage to or Breakage of Wafers in Horizontal mode	Damage to or Breakage of Wafers in Vertical mode
12	1	18	116.6	255.7	1.58	None	None
13	2	24	135.4	316.2	1.89	None	None
14	3	30	155.4	384.6	1.89	None	None
15	4	36	167.6	423.9	1.93	None	None
16	5	42	182.8	474.6	1.62	None	None
17	6	48	191.4	514.2	1.54	None	None
18	7	54	206.3	548.7	1.62	None	None
19	8	60	215.8	578.7	1.58	None	None
20	9	66	225.5	621.5	1.54	None	None

The same two semiconductor wafers were used for all the tests run. The maximum shock level of the machine was reached without any damage to the wafers being observed.

The tests and test results described above are intended solely to be illustrative, rather than predictive, and variations in the testing procedure can be expected to yield different results.

The present invention has now been described with reference to several embodiments thereof. The foregoing detailed description and examples have been given for clarity of understanding only. No unnecessary limitations are to be understood therefrom. All patents and patent applications cited herein are hereby incorporated by reference. It will be apparent to those skilled in the art that many changes can be made in the embodiments described without departing from the scope of the invention. Thus, the scope of the present invention should not be limited to the exact details and structures described herein, but rather by the structures described by the language of the claims, and the equivalents of those structures.

WHAT IS CLAIMED IS:

1. A container for containing semiconductor wafers, comprising:

a first container body including a base and a wall connected to the base;

a first wafer support plate located inside the first container body; and

at least one semiconductor wafer between the base of the first container body and the first wafer support plate, wherein the semiconductor wafer is stabilized between the first wafer support plate and the first container body.

2. The container of claim 1 further comprising:

a second wafer support plate located inside the first container body, wherein the second wafer support plate is between the base of the first container body and the semiconductor wafer, and wherein the semiconductor wafer is stabilized between the first wafer support plate and the second wafer support plate.

3. The container of claim 1 further comprising:

a second container body opposite the first container body, wherein the second container body includes a base and a wall connected to the base, and wherein the first container body is operatively connected to the first container body.

4. The container of claim 3 further comprising:

an internal cushioning member between the base of the second container body and the base of the first container body.

5. The container of claim 4, wherein the internal cushioning member is a foam-cushioning member.

6. The container of claim 4, wherein the internal cushioning member is an air-cushioning member.

7. The container of claim 1, wherein the semiconductor wafer has a first major surface and a second major surface opposite the first major surface, wherein the first major surface has a first surface area, wherein the first wafer support plate has a first major surface and a second major surface opposite the first major surface, wherein the second major surface has a second surface area, wherein the first major surface of the semiconductor wafer is opposite the second major surface of the first wafer support plate, and wherein the first surface area of the semiconductor wafer is less than the second surface area of the first wafer support plate.

8. The container of claim 7, wherein the first surface area of the semiconductor wafer is at least 10% less than the second surface area of the first wafer support plate.

9. The container of claim 8, wherein the first surface area of the semiconductor wafer is at least 25% less than the second surface area of the first wafer support plate.

10. The container of claim 1 further comprising a plurality of semiconductor wafers inside the first container body.

11. The container of claim 10, further comprising a plurality of wafer separator sheets, wherein a wafer separator sheet is between adjacent semiconductor wafers.

12. The container of claim 2, wherein when the container is dropped, the semiconductor wafer does not contact the wall of the first container body.

13. A container for containing semiconductor wafers, comprising:

a first container body including a base and a wall connected to the base;

at least one semiconductor wafer wherein the semiconductor wafer has a first major surface and a second major surface opposite the first major surface, wherein the first major surface has a first surface area;

a first wafer support plate located inside the first container body, wherein the first wafer support plate has a first major surface and a second major surface opposite the first major surface, wherein the second major surface has a second surface area; and

wherein the semiconductor wafer is between the base of the first container body and second major surface of the first wafer support plate, wherein the first surface area of the semiconductor wafer is at least 10% less than the second surface area of the first wafer support plate, and wherein the semiconductor wafer is stabilized between the first wafer support plate and the first container body.

14. The container of claim 10 further comprising:

a second wafer support plate located inside the first container body, wherein the second wafer support plate is between the base of the first container body and the semiconductor wafer, and wherein the semiconductor wafer is stabilized between the first wafer support plate and the second wafer support plate.

15. The container of claim 13, wherein the first surface area of the semiconductor wafer is at least 25% less than the second surface area of the first wafer support plate.

16. The container of claim 13 further comprising:

a second container body opposite the first container body, wherein the second container body includes a base and a wall connected to the base, and wherein the first container body is operatively connected to the first container body.

17. The container of claim 16 further comprising:

an internal cushioning member between the base of the second container body and the base of the first container body.

18. The container of claim 17, wherein the internal cushioning member is a foam-cushioning member.

19. The container of claim 17, wherein the internal cushioning member is an air-cushioning member.

20. The container of claim 10 further comprising a plurality of semiconductor wafers inside the first container body.

21. The container of claim 20, further comprising a plurality of wafer separator sheets, wherein a wafer separator sheet is between adjacent semiconductor wafers.

22. The container of claim 14, wherein when the container is dropped, the semiconductor wafer does not contact the wall of the first container body.

23. A container for containing semiconductor wafers, comprising:

a first container body including a base and a wall connected to the base;

a plurality of semiconductor wafer, wherein each semiconductor wafer has a first major surface and a second major surface opposite the first major surface, wherein the first major surface has a first surface area;

a first wafer support plate located inside the first container body, wherein the first wafer support plate has a first major surface and a second major surface opposite the first major surface, wherein the second major surface has a second surface area; and wherein the plurality semiconductor wafers is between the base of the first container body and second major surface of the first wafer support plate, and wherein the first surface area of the semiconductor wafers is at least 10% less than the second surface area of the first wafer support plate;

a second wafer support plate located inside the first container body, wherein the second wafer support plate has a first major surface and a second major surface opposite the first major surface, wherein the plurality semiconductor wafer is between the second major surface of the first wafer support and first major surface of the second wafer support plate, wherein the first major surface of the second wafer support plate has a first surface area, wherein the first surface area of the semiconductor wafers is at least 10% less than the first surface area of the second wafer support plate, and wherein the semiconductor wafer is stabilized between the first wafer support plate and the second wafer support plate;

a second container body opposite the first container body, wherein the second container body includes a base and a wall connected to the base, and wherein the first container body is operatively connected to the first container body; and

an internal cushioning member between the base of the second container body and the base of the first container body, wherein the internal cushioning member is a foam-cushioning member; and a plurality of wafer separator sheets, wherein a separator sheet is between adjacent semiconductor wafers.

24. A method of safely shipping semiconductor wafers, comprising the steps of:

a) providing a container for containing semiconductor wafers, wherein the container comprises:

a first container body including a base and a wall connected to the base;

a second container body including a base and a wall connected to the base;

a first wafer support plate located inside the first container body;

b) providing a plurality of semiconductor wafers;

c) stacking the plurality of semiconductor wafers in a stack and placing the stack of semiconductor wafers inside the first container body;

d) placing the first wafer support plate on the stack of semiconductor wafers inside the first container body;

e) operatively connecting the first container body with the second container body so as to enclose the wafer support plate and stack of semiconductor wafers inside the container and to stabilize the stack of semiconductor wafers between the base of the first container body and the first wafer support plate.

25. The method of claim 24, wherein the container further comprises a second wafer support plate, wherein step c) further comprises placing the second wafer support plate inside the first container body and placing the stack of semiconductor wafers on the second wafer support body inside the first container body, and wherein the stack of semiconductor wafers is stabilized between the first wafer support plate and the second wafer support plate.

26. The method of claim 24, wherein the semiconductor wafers have a first major surface and a second major surface opposite the first major surface, wherein the first major surface has a first surface area, wherein the first wafer support plate has a first major surface and a second major surface opposite the first major surface, wherein the second major surface

has a second surface area, and wherein the first surface area of the semiconductor wafer is at least 10% less than the second surface area of the first wafer support plate.

27. The method of claim 26, wherein the first surface area of the semiconductor wafer is at least 25% less than the second surface area of the first wafer support plate.

28. The method of claim 26, wherein when the container is dropped, the semiconductor wafers do not contact the wall of the first container body.

29. The method of claim 24, wherein step b) further comprises providing a plurality of wafer separator sheets, wherein a wafer separator sheet is between adjacent semiconductor wafers, wherein step c) further comprising stacking the plurality of semiconductor wafers and the plurality of wafer separator sheets in a stack, wherein a wafer separator sheet is between two adjacent semiconductor wafers, and placing the stack of semiconductor wafers and separator sheets inside the first container body.

30. The method of claim 24, further including the steps of:

f) transporting the container and stack of semiconductor wafers to a new location;

g) separating the second container body from the first container body to remove the stack of semiconductor wafers from the container;

h) inspecting the stack of semiconductor wafers and observing that the stack of semiconductor wafers are not damaged or broken.

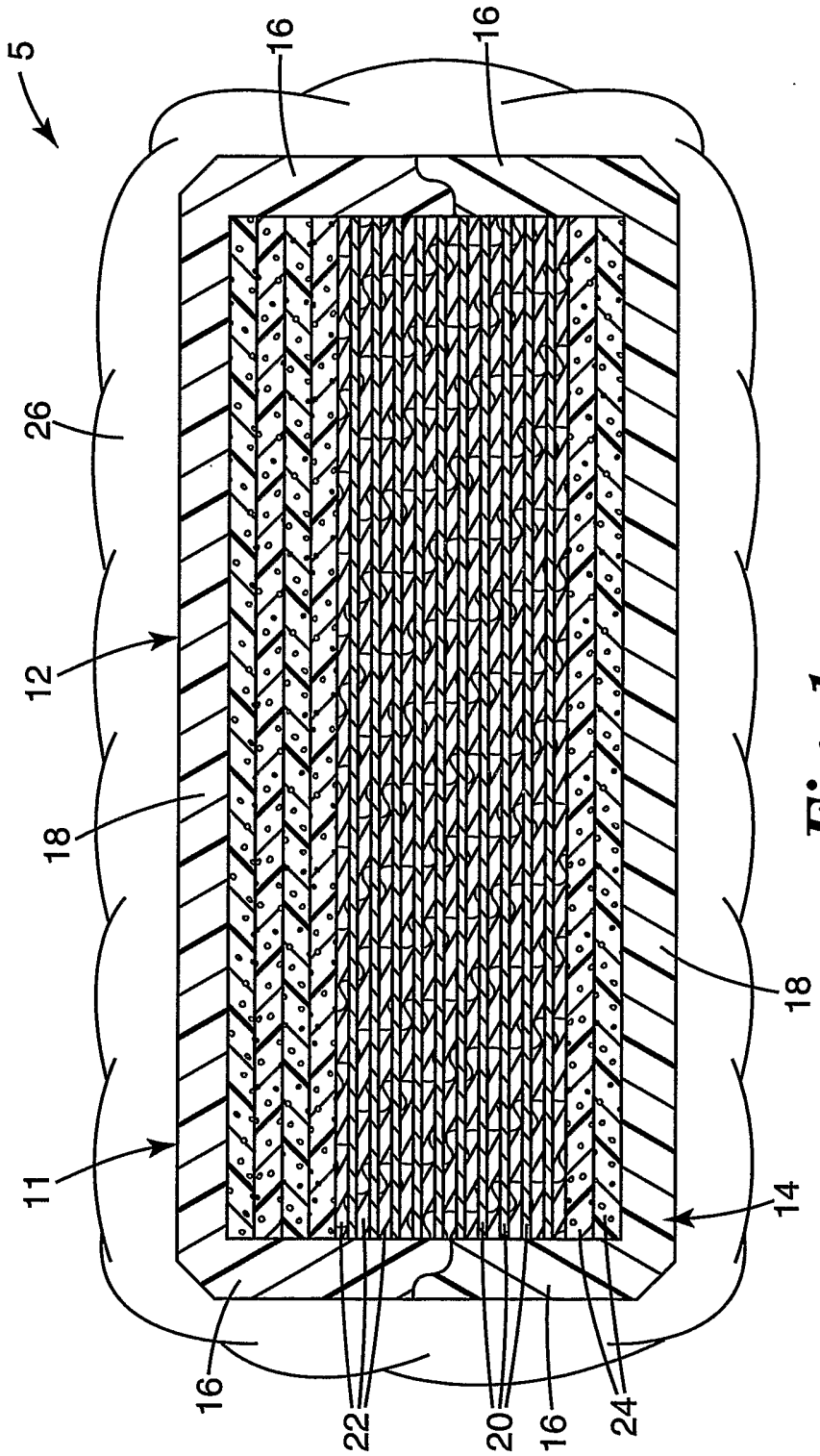


Fig. 1
PRIOR ART

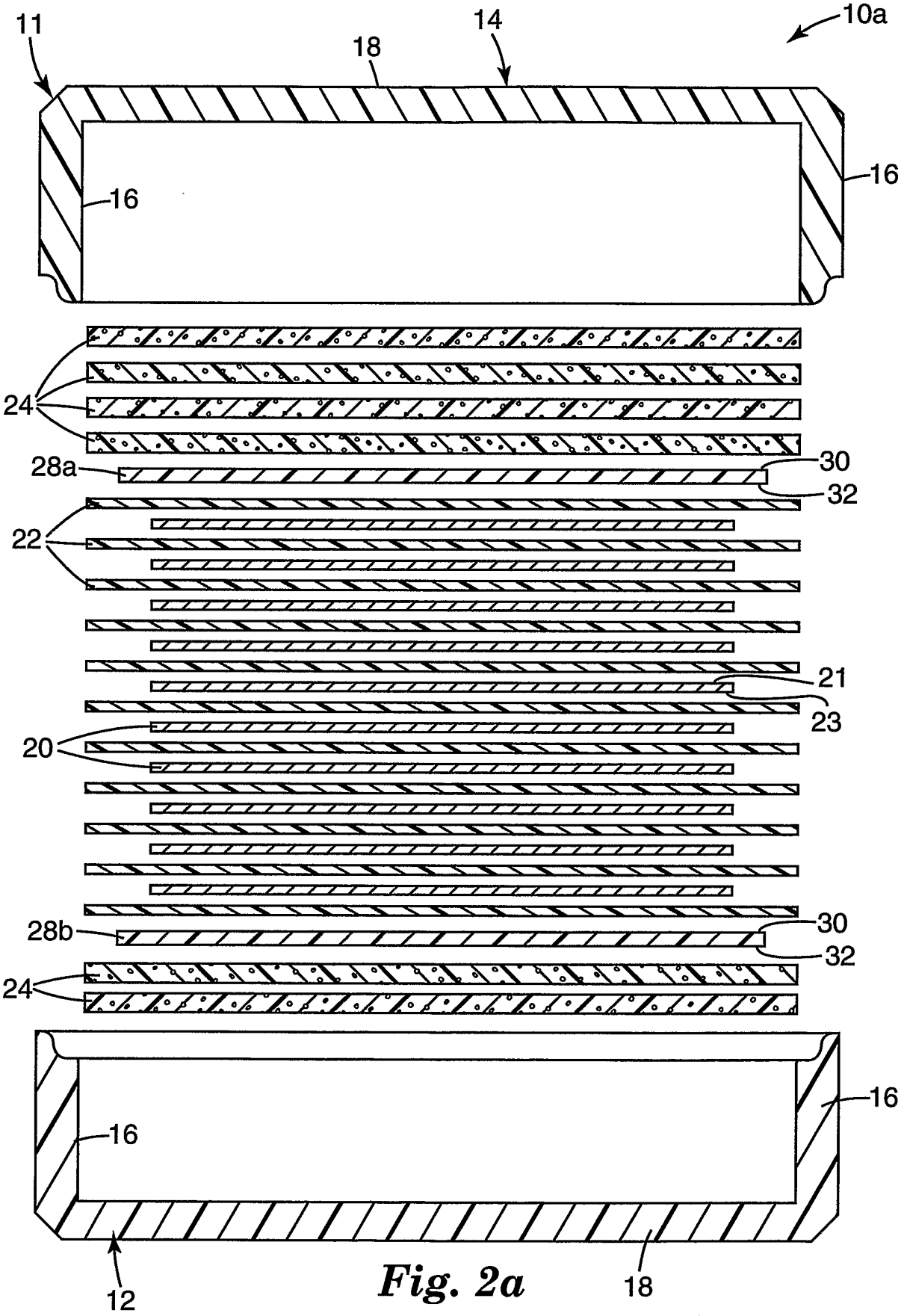


Fig. 2a

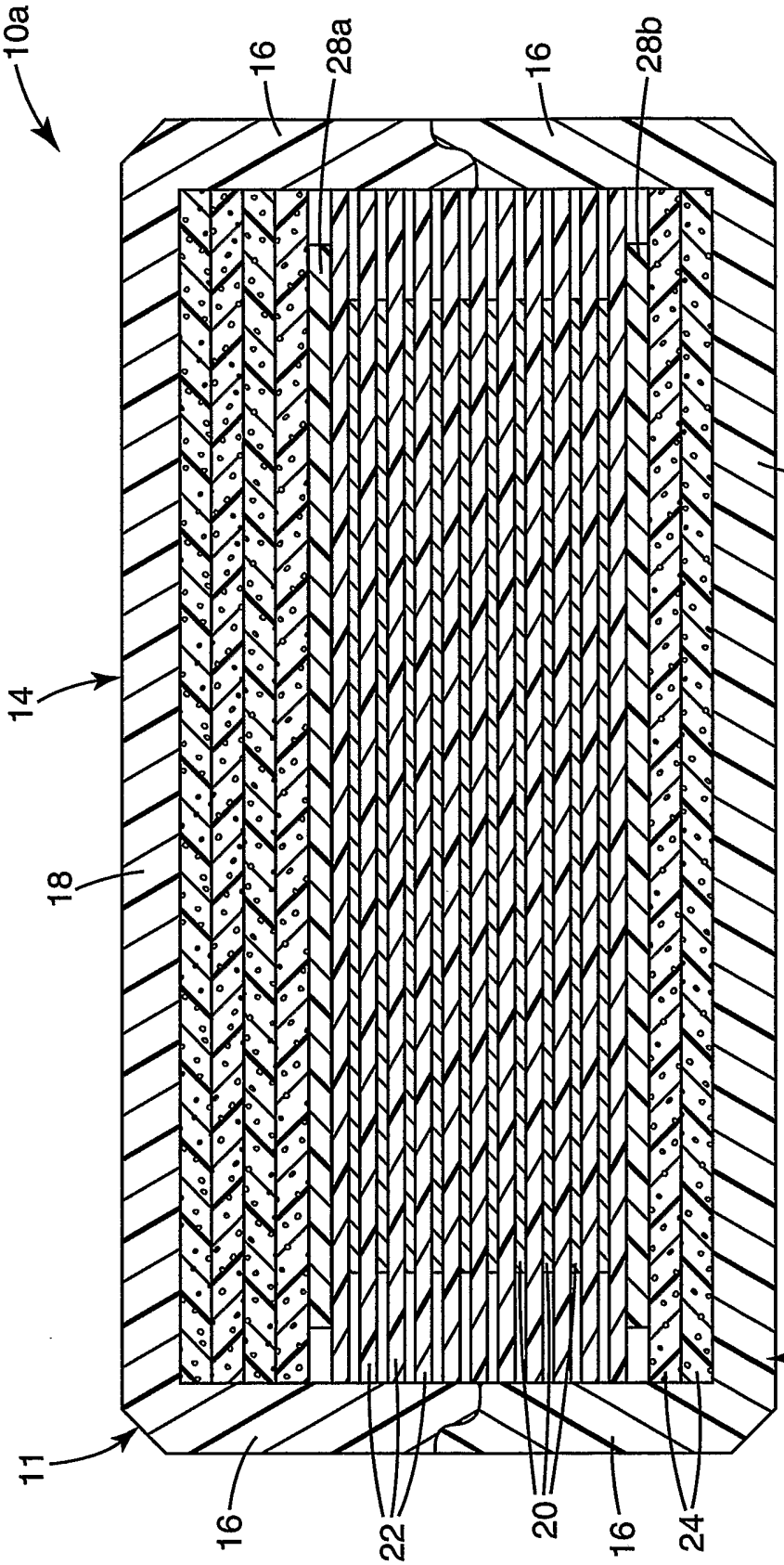


Fig. 2b

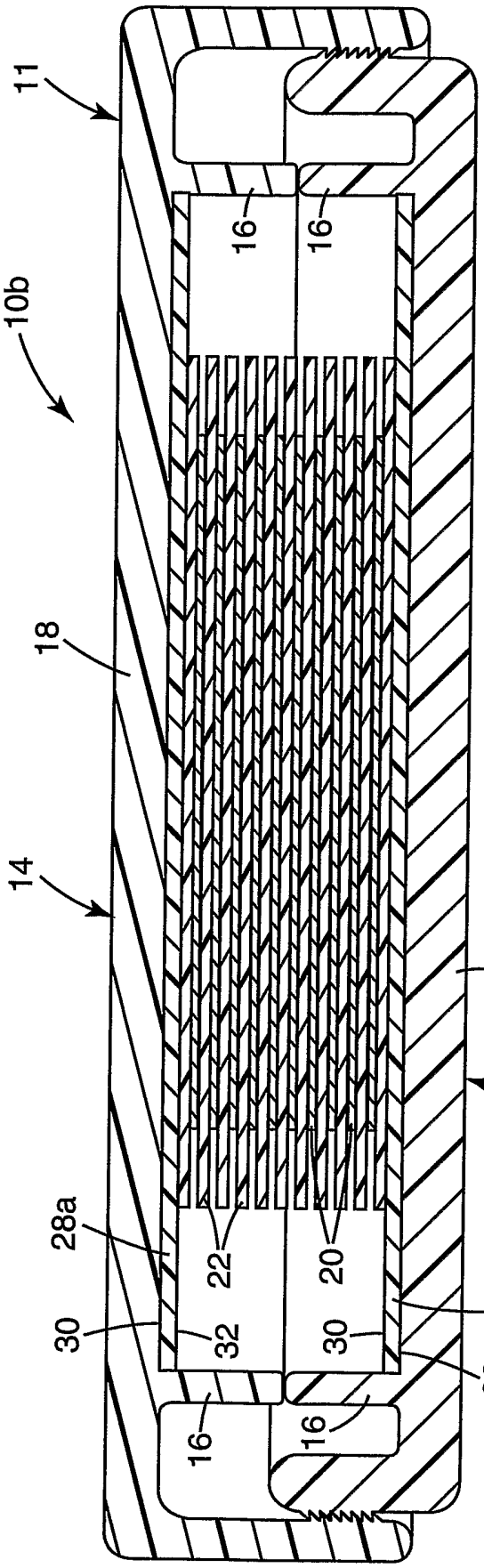


Fig. 3

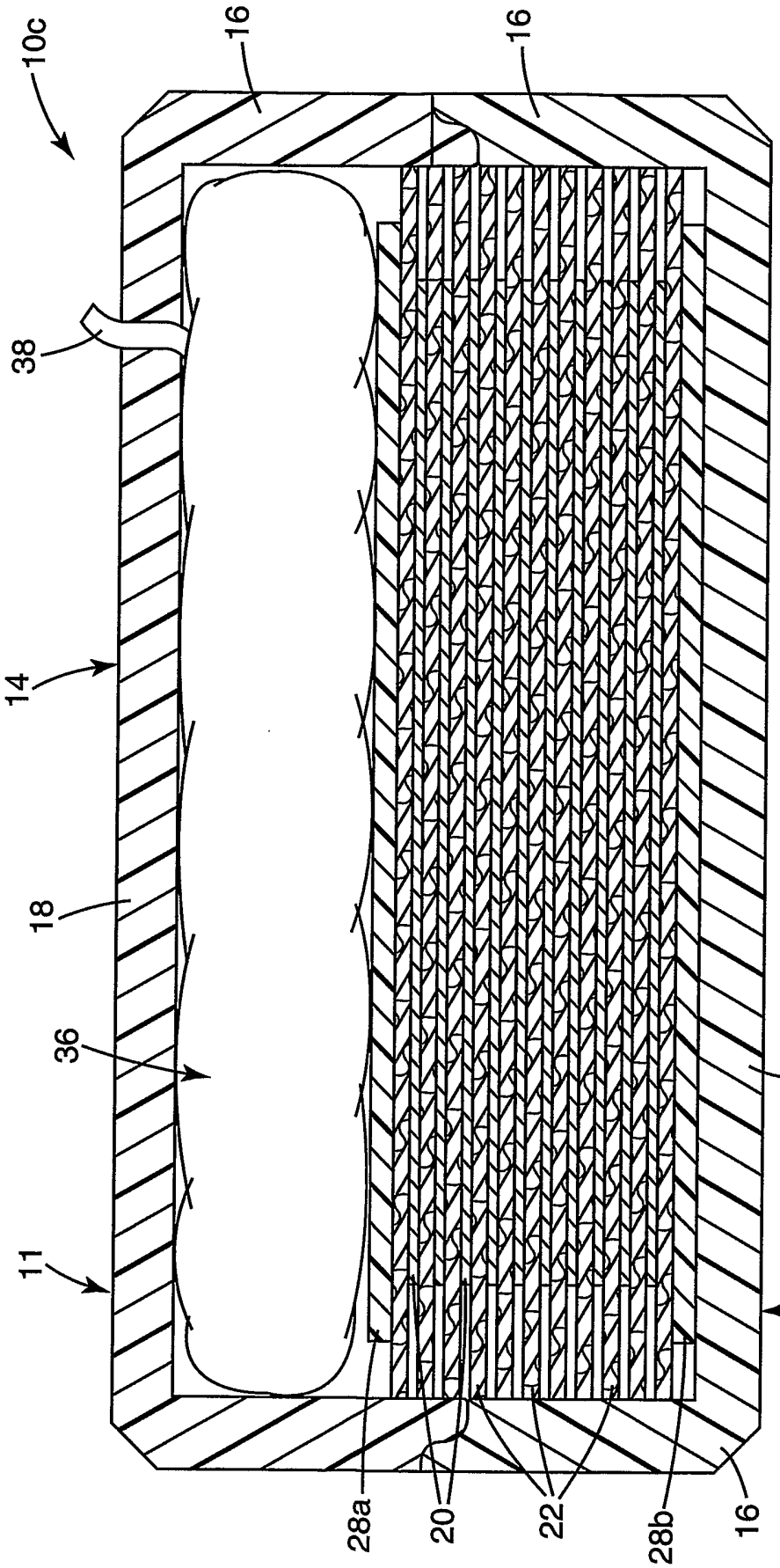


Fig. 4

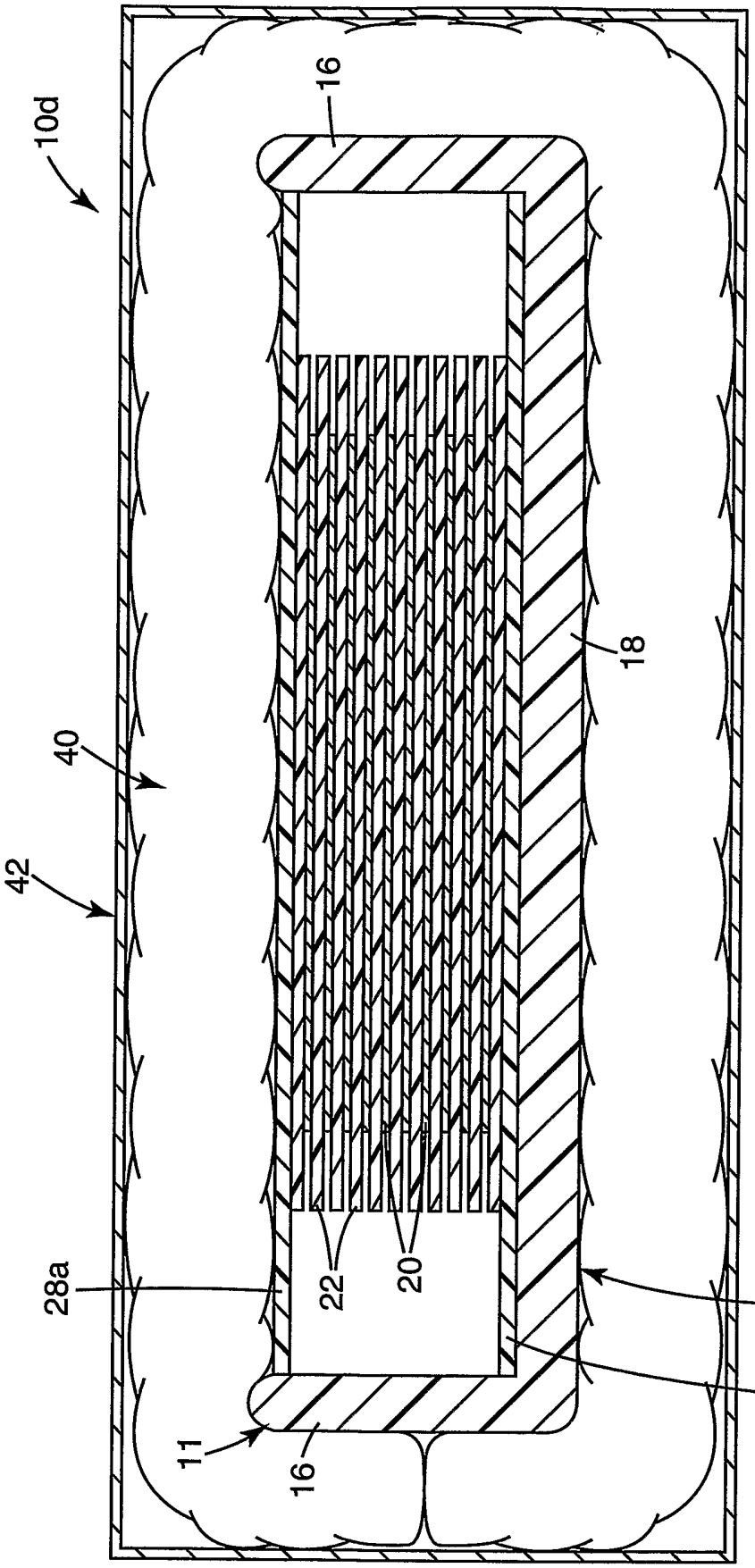


Fig. 5

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US2004/033633

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 789 393 A (ACHILLES CORPORATION) 13 August 1997 (1997-08-13) abstract; figures 4,5	1-5,24, 25,29,30
Y		14,23
X	PATENT ABSTRACTS OF JAPAN vol. 2003, no. 04, 2 April 2003 (2003-04-02) -& JP 2002 362736 A (NITTO DENKO CORP), 18 December 2002 (2002-12-18) abstract	1,7-13, 15-18, 20-22, 24,26-30
Y		14,23
X	US 6 119 865 A (KAWADA) 19 September 2000 (2000-09-19) cited in the application abstract; figure 2	1,24

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
25 January 2005	01/02/2005

Name and mailing address of the ISA	Authorized officer
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INTERNATIONAL SEARCH REPORT

International Application No
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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