May 30, 1933. E. GREEN 1,912,191

STABILIZED AMPLIFIER CIRCUITS

Filed April 6, 1931 2 Sheets-Sheet 1

Fig. 1

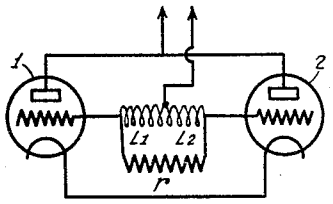


Fig. 2

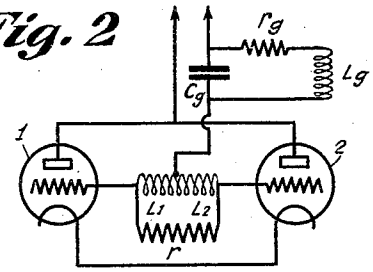


Fig. 3

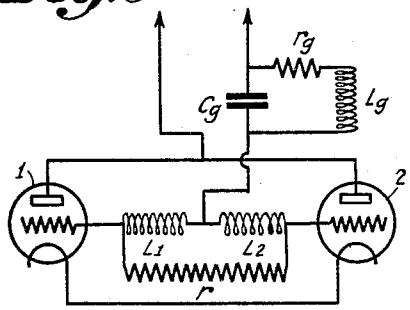


Fig. 4

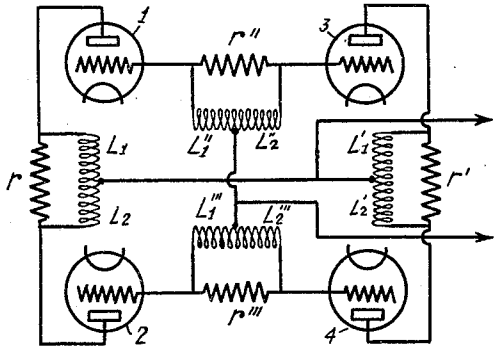
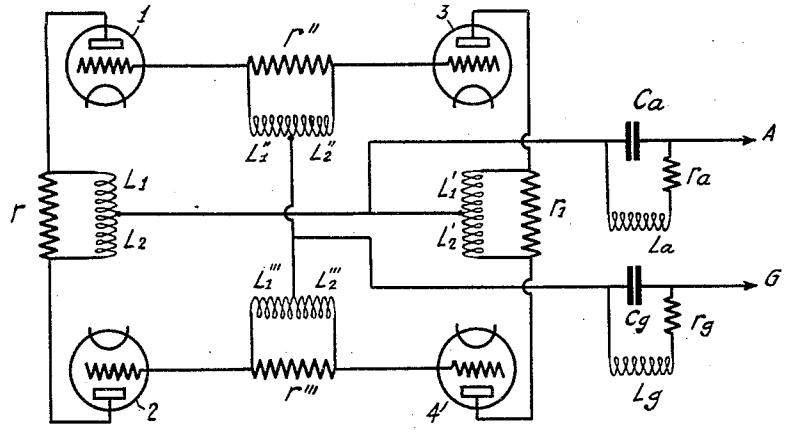


Fig. 5



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Filed April 6, 1931 2 Sheets-Sheet 2

Fig. 6

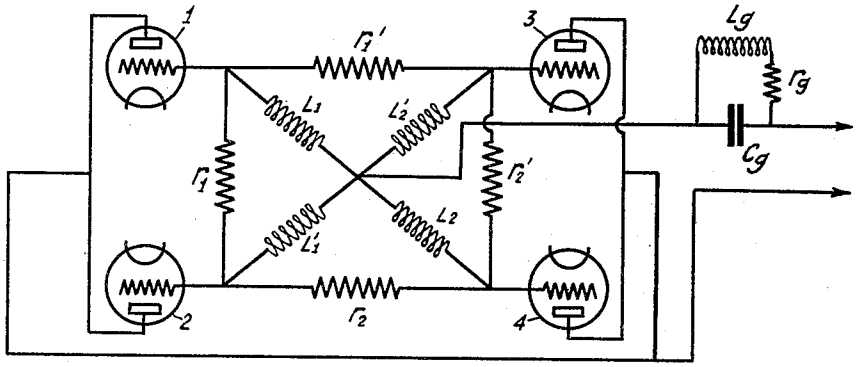


Fig. 7

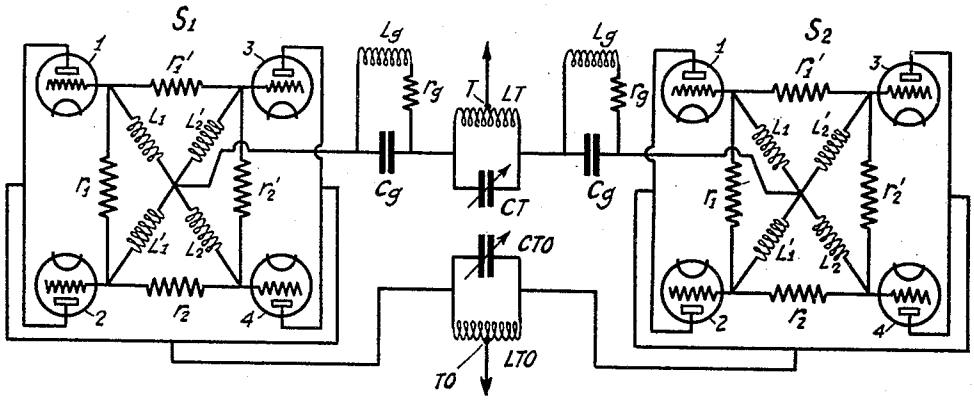
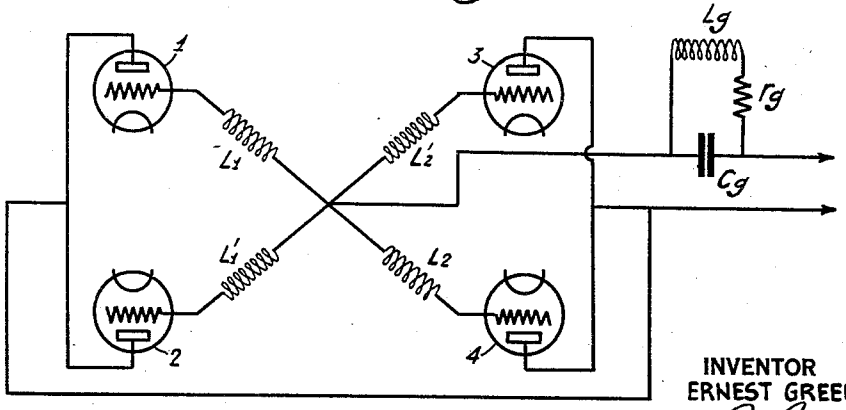


Fig. 8



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STABILIZED AMPLIFIER CIRCUITS

Application filed April 6, 1931, Serial No. 527,917, and in Great Britain May 23, 1930.

This invention relates to thermionic valve circuits, and more particularly to oscillating or amplifying circuits for use on high frequencies.

It is well known that when thermionic valves are connected in parallel in oscillating, or amplifying, circuits there is a tendency for parasitic oscillations to occur due to the transfer of energy through the grid-anode self-capacities of the valves. For example, in a simple arrangement in which two triodes are connected in parallel, i. e., in which the filament grid and anode of one valve are connected respectively to the filament grid and anode of the other, there is a tendency for parasitic oscillations to occur in a circuit passing from the grid of one valve to the anode thereof, to the anode of the other valve and thence to the grid of the said first valve. Obviously the frequency of such parasitic oscillations will be very high.

Where the main circuit is tuned to a relatively low frequency several methods have been proposed for preventing the occurrence of such parasitic oscillations. One such known method consists in inserting damping resistances in the leads which connect plate to plate and grid to grid. Another method consists in inserting inductances in the leads to the two grids while keeping the inductances in the anode leads as low as possible. A further method, which is a modification of the last mentioned method, consists in shunting each of the inductances by a resistance, a third resistance being connected direct from grid to grid. Yet another method which can be regarded as a development of the method last described consists in dispensing with the third resistance and coupling the inductances together so as to reduce the resultant inductance for oscillations of the main frequency whilst increasing it for the undesired high frequency parasitic oscillations.

These methods, while reasonably satisfactory where the frequency of the main circuit is relatively low as compared to that of the parasitic oscillations, are not sufficient when the main oscillation frequency is high enough to be comparable with the parasitic oscillation frequency.

It has been found that in such cases either or both of two important defects exist with these known methods. One of these defects is that the resistances inserted to suppress parasitic oscillations have a more or less serious damping effect on the main oscillation, and the other is that where inductances are inserted to by-pass the main oscillations the reactance offered by such inductances to the said oscillations becomes undesirably large.

According to this invention these defects are avoided by providing a low reactance path for the main oscillation whilst maintaining a high reactance path for the parasitic oscillations which path is shunted by a damping resistance (where such are employed) connected only between points which are at the same potential as regards the main oscillation whilst being at different potentials as regards the parasitic oscillation. The low reactance path for the main oscillation may be provided either by suitably arranging the inductances to offer a small reactance to the main oscillation or providing means for compensating either wholly or in part for such reactance. In carrying out the invention these methods may be employed singly or in combination.

Various arrangements in accordance with the present invention are illustrated in Figures 1, 2, 3, 4, 5, 6, 7 and 8 of the accompanying drawings.

In the arrangement illustrated in Fig. 1 two triodes 1, 2 are connected in parallel the anodes of the triodes being connected together as shown and also the cathodes. The grids of the triodes are connected together through a pair of inductances L_1 L_2 which are coupled together as closely as possible the junction of the said inductances forming the point of connection for the common grid input. The inductances L_1 L_2 are shunted by a resistance r. In the extreme cases, i. e. in very high frequency circuits, the inductances of the leads to the valves are appreciable and in such cases the inductances L_1 L_2 may be constituted by such connections to the valves, the resistance r being connected directly to

the valve terminals. Similar remarks apply to the other arrangements described in the specification when intended for use in very high frequency circuits.

In a modification shown in Fig. 2 a capacity C_g shunted by a suitable inductance L_g and resistance r_g in series is inserted in the common grid lead so as to compensate for the residual inductance effect of the inductances L_1 L_2 at the main oscillation frequency.

Fig. 3 shows a slightly modified arrangement in which the inductances L_1 L_2 are not coupled at all and the inserted circuit $C_g L_g r_g$ is relied upon to compensate for the whole of the inductance effect of the inductances L_1 and L_2 at the main oscillation frequency.

In the arrangement shown in Figs. 1, 2 and 3, the parasitic oscillation suppressing devices are illustrated as inserted in the input circuits of the valves but obviously similar devices may be connected in the output circuits in addition or in place of those in the input circuits.

Fig. 4 shows an arrangement in accordance with this invention in which four triodes 1, 2, 3, 4, are connected in parallel. As will be seen the anode of the valve 1 is connected to that of the valve 2 through close coupled inductances L_1 L_2 shunted by the resistance r. The anodes of the valves 3, 4 are similarly connected through an inductive and resistive circuit L_1' L_2' r'. Similar inductive and resistive circuits L_1'' L_2'' r'' and L_1''' L_2''' r''' are employed to connect the grid of the valve 1 with that of the valve 3 and the grid of the valve 2 with that of the valve 4. The common grid input lead for the four valves is shown at G and the common anode output lead is shown at A.

The arrangement shown in Fig. 5 is precisely similar to that shown in Fig. 4 except that a condenser C_g shunted by an inductance L_g and a resistance r_g in series is inserted in the common grid input lead a similar circuit $C_a L_a r_a$ being inserted in the common anode lead. The inserted circuits serve to compensate for the reactances of the inductances L_1 L_2 L_1' L_2' L_1'' L_2'' L_1''' L_2''' at the working frequency.

Fig. 6 illustrates the arrangement shown in Fig. 3 as applied to four valves 1, 2, 3, 4. In this arrangement the grids of the valves 1 and 4 are connected together through inductances L_1 L_2 and the grids of the valves 2 and 3 are connected together through inductances L_1' L_2' the shunt resistances are shown at r_1 r_2 r_1' r_2'. As before G is the common grid input lead and A the common grid output lead. The inductances L_1 L_2 L_1' L_2' are entirely uncoupled and their reactive effect is compensated for by a circuit consisting of a condenser C_g shunted by an inductance L_g and a resistance r_g in series inserted in the common grid input lead.

Fig. 7 is a modification of the arrangement shown in Fig. 6 in which two sets of four valves in parallel are arranged in push-pull. The sets are generally designated S_1 S_2. Voltage input is applied to the sets in push-pull relation by means of the usual tuned circuit L_T C_T having the customary midpoint tapping T upon the inductance L_T the tuned output circuit is shown at L_{TO} and C_{TO} anode potential being applied viz the customary midpoint tapping TO upon the induction L_{TO}. It will be seen that the arrangement shown in Fig. 7 consists in effect of a duplicate of the arrangement shown in Fig. 6 each set of four valves with the associated parasitic oscillation suppressing devices being equivalent to one of the valves in the ordinary well known push-pull circuit. The circuit shown in Fig. 7 is one which is very advantageous for use on very short waves and will normally be employed therefor.

In some cases the damping resistances may be dispensed with entirely the inductance of the anode connections being kept as low as possible and the inductance in the grid connections being increased to a value sufficient to prevent parasitic oscillations the reactive effect of these inductances being compensated for at the frequency of the main oscillation. An arrangement of this kind is shown in Fig. 8 in which L_1 L_2 L_1' L_2' are the inductances inserted in the grid circuit and the circuit consisting of the condenser C_g inductance L_g and resistance r_g is the circuit which compensates for the reactive effect of the inductances L_1 L_1' L_2 L_2' at the working frequency.

Although the modifications above described specifically are concerned with pairs of valves or with arrangements of four valves in parallel the invention is obviously not limited to such numbers of valves, but is applicable generally to parallel thermionic valve arrangements.

Having now particularly described and ascertained the nature of my said invention and in what manner the same is to be performed, I declare that what I claim is:

1. A thermionic valve circuit comprising a pair of valves in parallel, the anodes of said valves being connected together, the cathodes of said valves being connected together, and the grids of said valves being connected together through a pair of uncoupled inductances, the junction point of said inductances forming the common input point for the valves, the lead to said common grid input point including means for compensating for the reactance of the inductances at the main operating frequency of said circuit.

2. An arrangement as claimed in claim 1, and in which the grids are also connected together through a damping resistance.

3. An arrangement as claimed in claim 1, and in which the compensation means include

a capacity inserted in the lead to the common grid input point and an inductance and a resistance in series with one another, and in shunt across said capacity, substantially as described.

4. An amplifier circuit comprising a pair of tubes having their anodes connected together, a path including lumped inductance connecting the grids of the tubes, a path connected to the midpoint of the inductance providing a common input point for the tubes, and a network, including a condenser shunted by an inductance and resistor in said second path for compensating for the reactance of said lumped inductance at the amplifier operating frequency whereby said lumped inductance path provides a high reactance path for parasitic oscillations of the order of said operating frequency but a low reactance path for the latter.

5. An amplifier circuit comprising a pair of tubes having their anodes connected together, a path including lumped inductance connecting the grids of the tubes, a path connected to the midpoint of the inductance providing a common input point for the tubes, and a network, including a condenser shunted by an inductance and resistor, in said second path for compensating for the reactance of said lumped inductance at the amplifier operating frequency whereby said lumped inductance path provides a high reactance path for parasitic oscillations of the order of said operating frequency but a low reactance path for the latter, and a damping resistor shunted across said lumped inductance.

6. In combination, in a short wave amplifier, a pair of tubes connected in parallel, a second pair of tubes connected in parallel, an inductance connecting the grid of each tube to a common input point, a common output conductor connected to the anodes of said tubes, a common input conductor connected to said input point, a damping resistor connecting the grids of each pair of tubes, a second group of two pairs of tubes having each pair of tubes connected in parallel and inductances connecting the grid of each tube to a common input point, damping resistors connecting the grids of each pair of tubes of the second group, said common input conductor being connected to the input point of the second group, said common output conductor being connected to the anodes of said second group, a tunable oscillation circuit connected to each of the input and output conductors, and a network, in series between the oscillation circuit in the common input circuit and the common input point of each group of tubes, arranged to maintain parasitic oscillations of a frequency of the order of the operating frequency of the amplifier at a minimum.

7. In combination, in a short wave amplifier, a pair of tubes connected in parallel, a second pair of tubes connected in parallel, an inductance connecting the grid of each tube to a common input point, a common input conductor connected to said input point, a common output conductor connected to the anodes of said tubes, and a network connected to the common input conductor, said network being designed to compensate for the reactance of the inductances at the operating frequency of the amplifier whereby parasitic oscillations of a frequency of the order of said operating frequency are substantially suppressed.

8. In combination, in a short wave amplifier, a pair of tubes connected in parallel, a second pair of tubes connected in parallel, an inductance connecting the grid of each tube to a common input point, a common input conductor connected to said input point, a common output conductor connected to the anodes of said tubes, a network connected to the common input conductor, said network being designed to compensate for the reactance of the inductances at the operating frequency of the amplifier whereby parasitic oscillations of a frequency of the order of said operating frequency are substantially suppressed and a network connected to said common output conductor, and a compensating network, similar to said first network, connected to said common output conductor.

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