



US00RE48879E

(19) **United States**
(12) **Reissued Patent**
Torok et al.

(10) **Patent Number:** **US RE48,879 E**
(45) **Date of Reissued Patent:** **Jan. 4, 2022**

(54) **SPINRAM**

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Berkeley, CA (US)

(21) Appl. No.: **16/447,777**

(22) Filed: **Jun. 20, 2019**

Related U.S. Patent Documents

Reissue of:

(64) Patent No.: **9,741,923**
Issued: **Aug. 22, 2017**
Appl. No.: **15/272,228**
Filed: **Sep. 21, 2016**

U.S. Applications:

(60) Provisional application No. 62/232,977, filed on Sep.
25, 2015.

(51) **Int. Cl.**

H01L 43/02 (2006.01)
H01L 23/528 (2006.01)
H01L 27/00 (2006.01)
G11C 11/16 (2006.01)
H01L 43/08 (2006.01)
H01L 27/22 (2006.01)
H01L 43/10 (2006.01)

(52) **U.S. Cl.**

CPC **H01L 43/02** (2013.01); **G11C 11/161**
(2013.01); **H01L 23/528** (2013.01); **H01L**
27/222 (2013.01); **H01L 43/08** (2013.01);
H01L 43/10 (2013.01)

(58) **Field of Classification Search**

CPC ... **H01L 23/528**; **H01L 23/481**; **H01L 23/147**;

H01L 27/222; H01L 27/226; H01L
27/115; H01L 27/112; H01L 43/02; H01L
43/10; H01L 43/08; H01L 45/085; H01L
45/1233; G11C 11/161; G11C 11/11;
G11C 11/15; G11C 11/1675

See application file for complete search history.

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Primary Examiner — Tuan H Nguyen

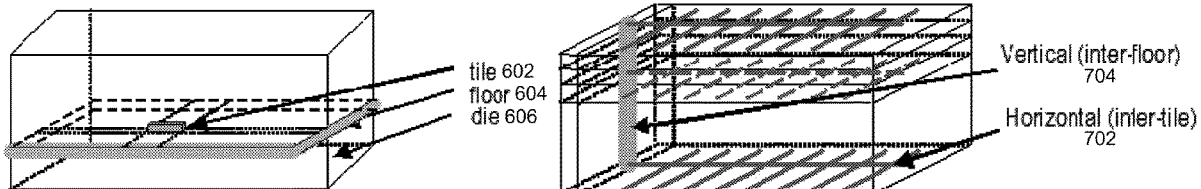
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ABSTRACT

Magnetic random-access memory (RAM) cells and arrays
are described based on magnetoresistive thin-film structures.

18 Claims, 14 Drawing Sheets



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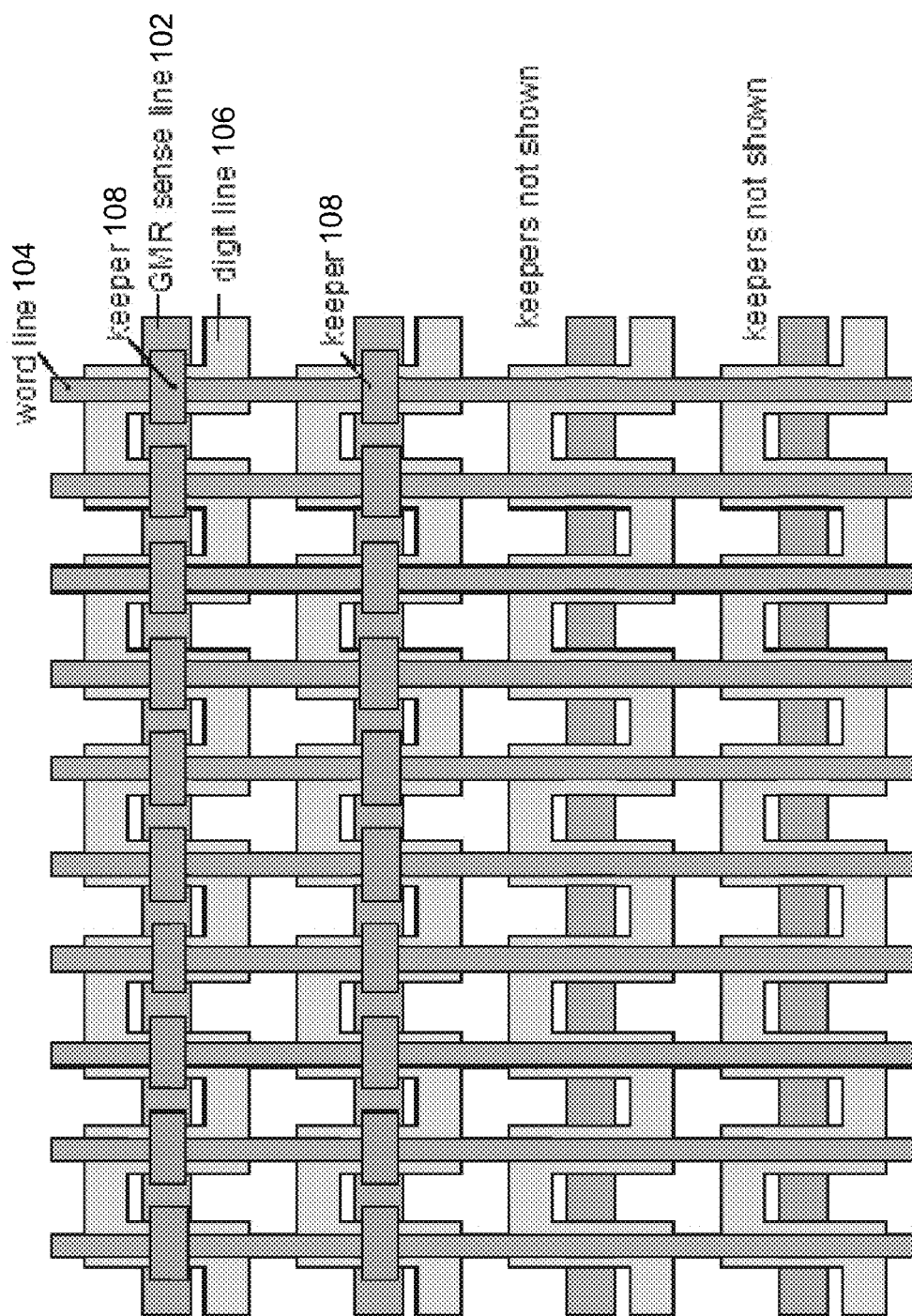


FIG. 1

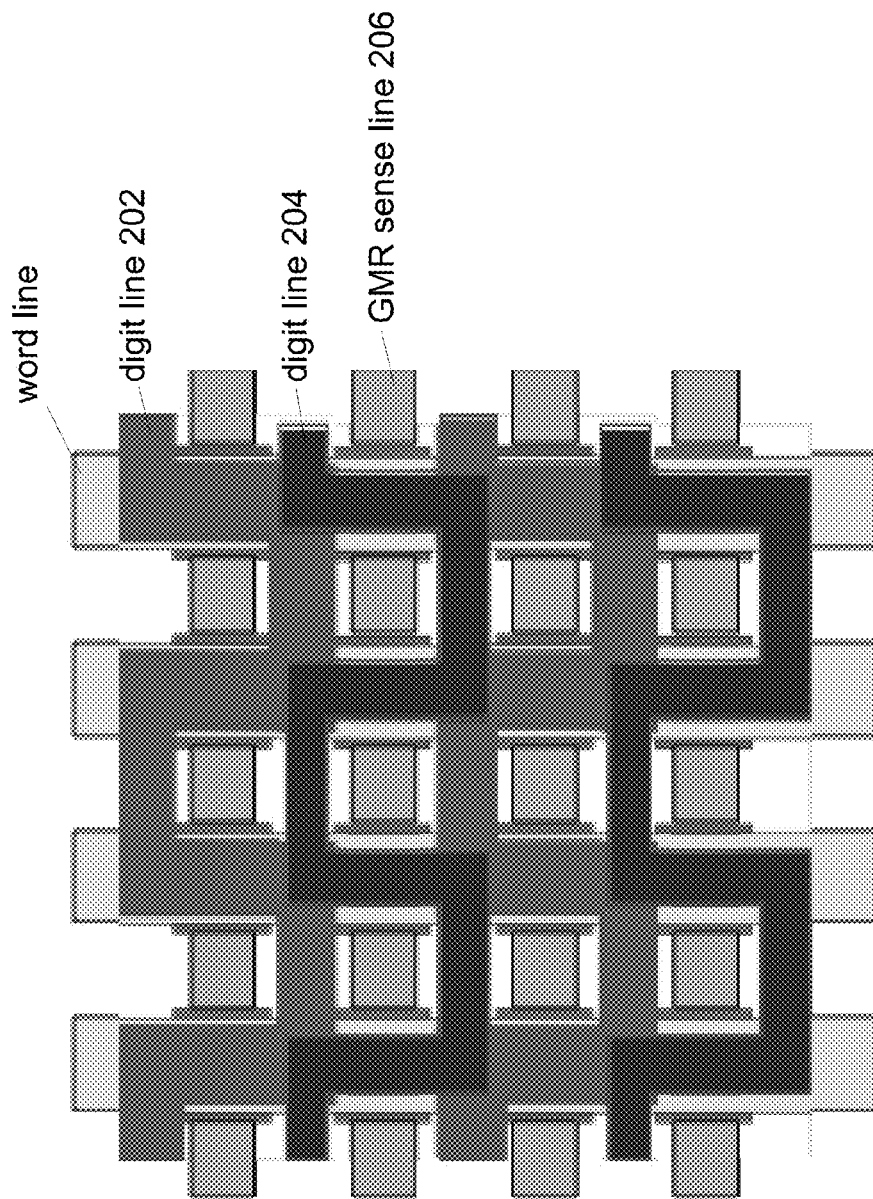


FIG. 2

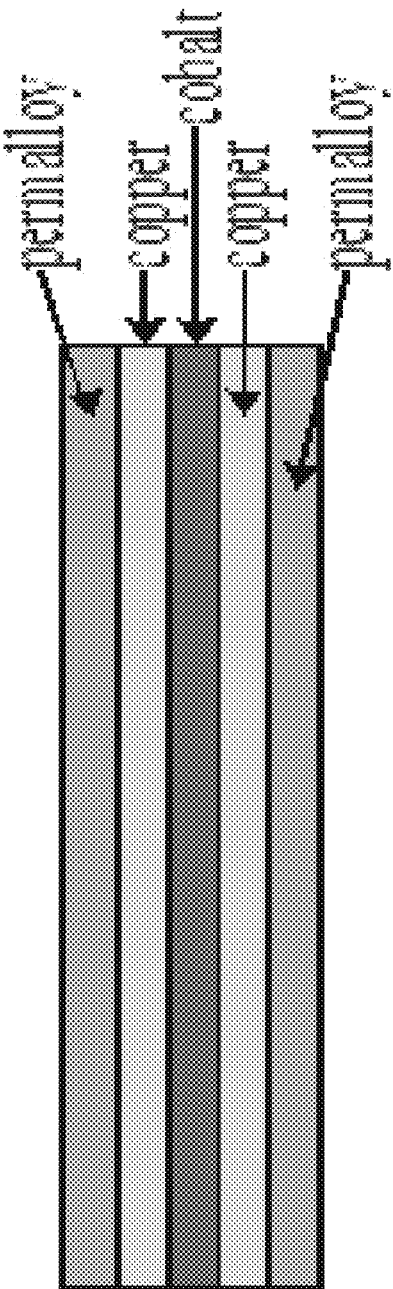


FIG. 3

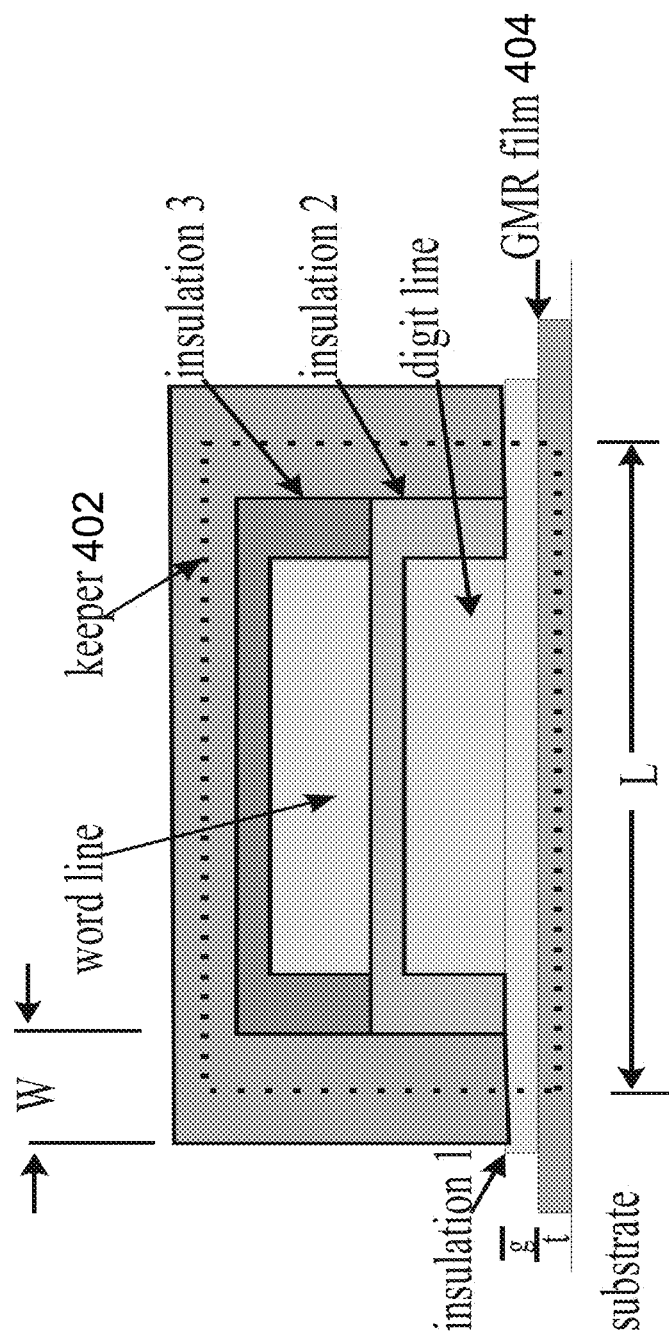


FIG. 4

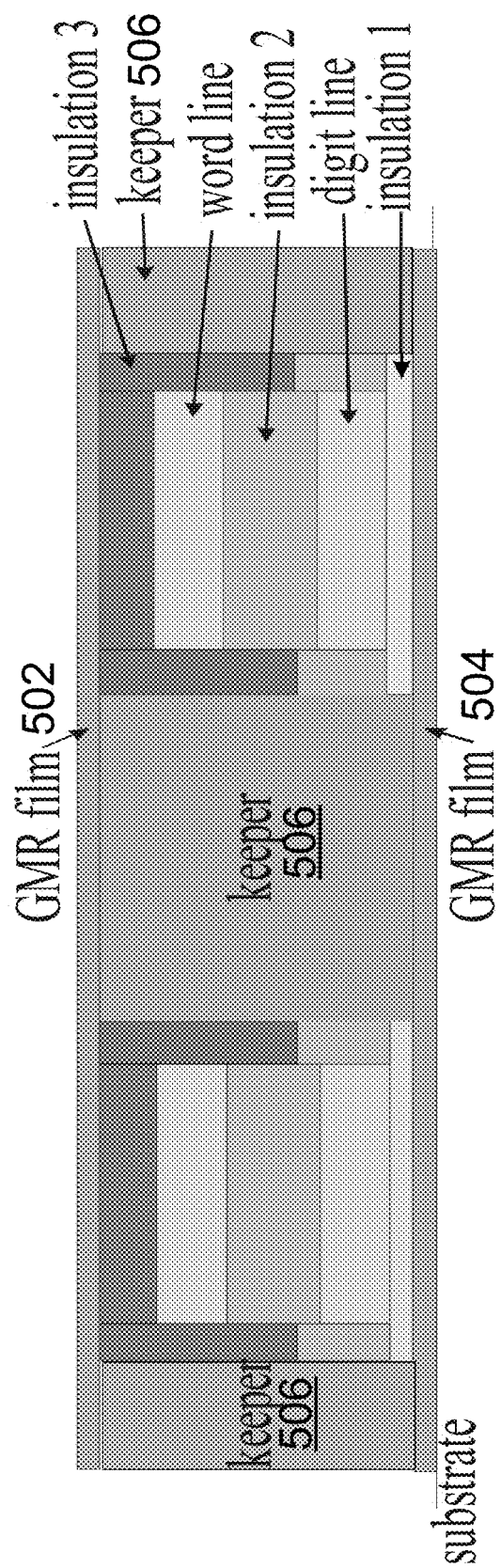


FIG. 5

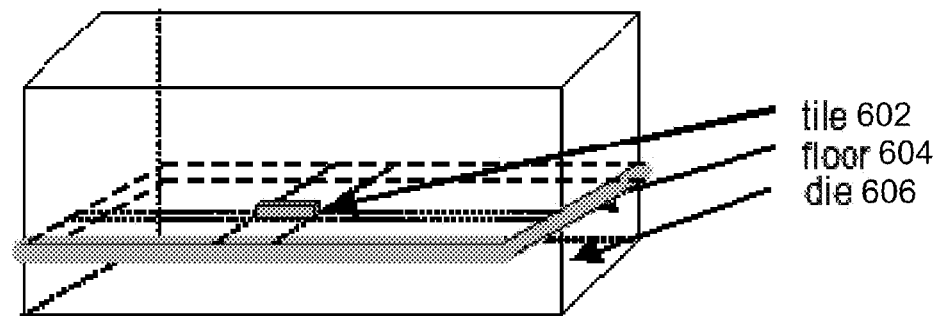


FIG. 6

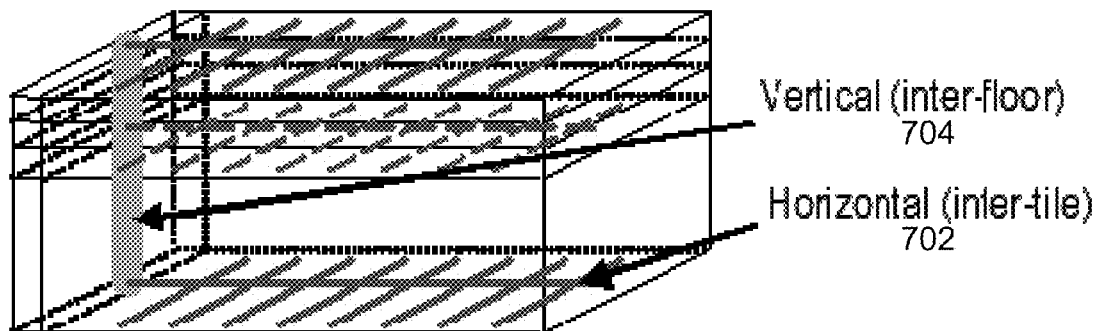


FIG. 7

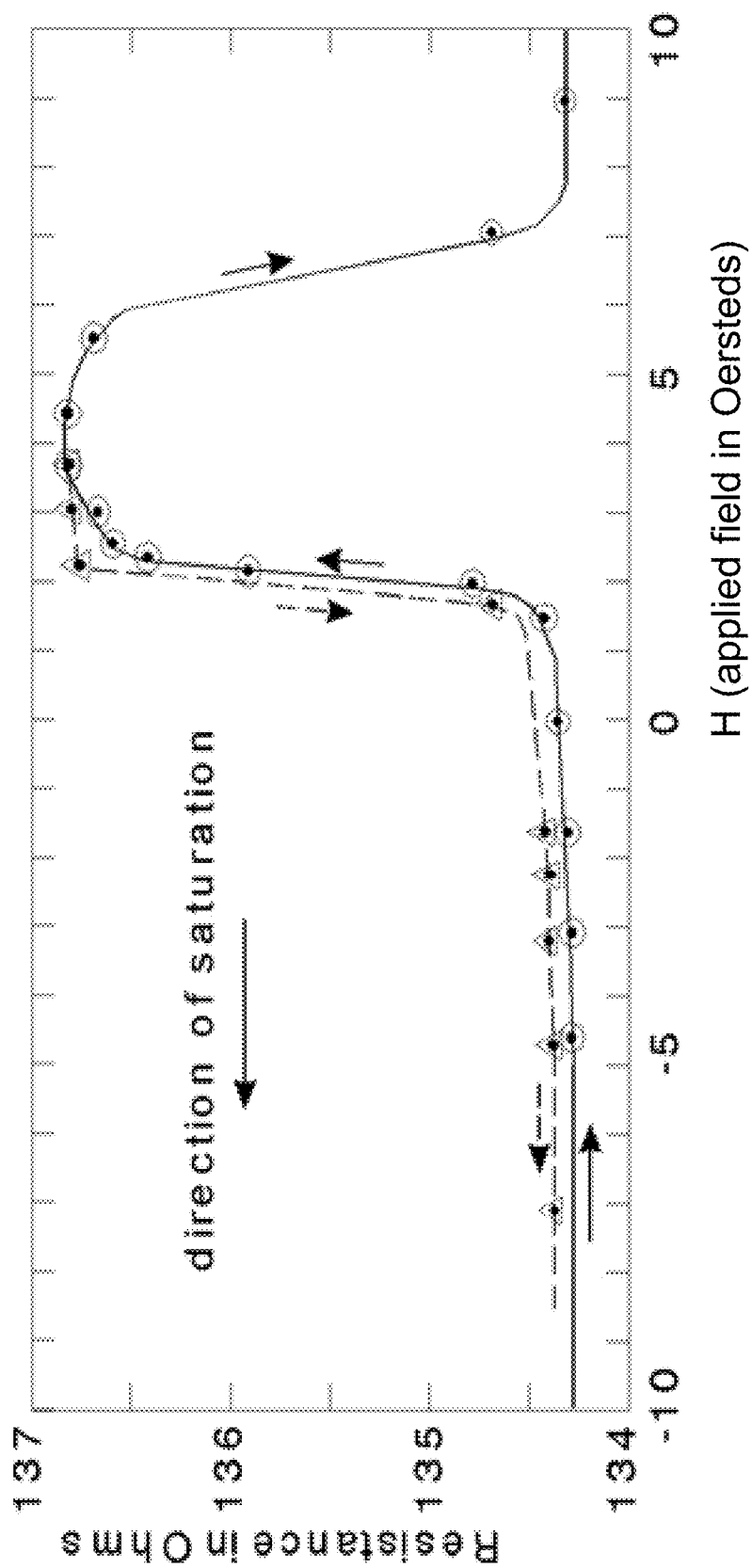


FIG. 8

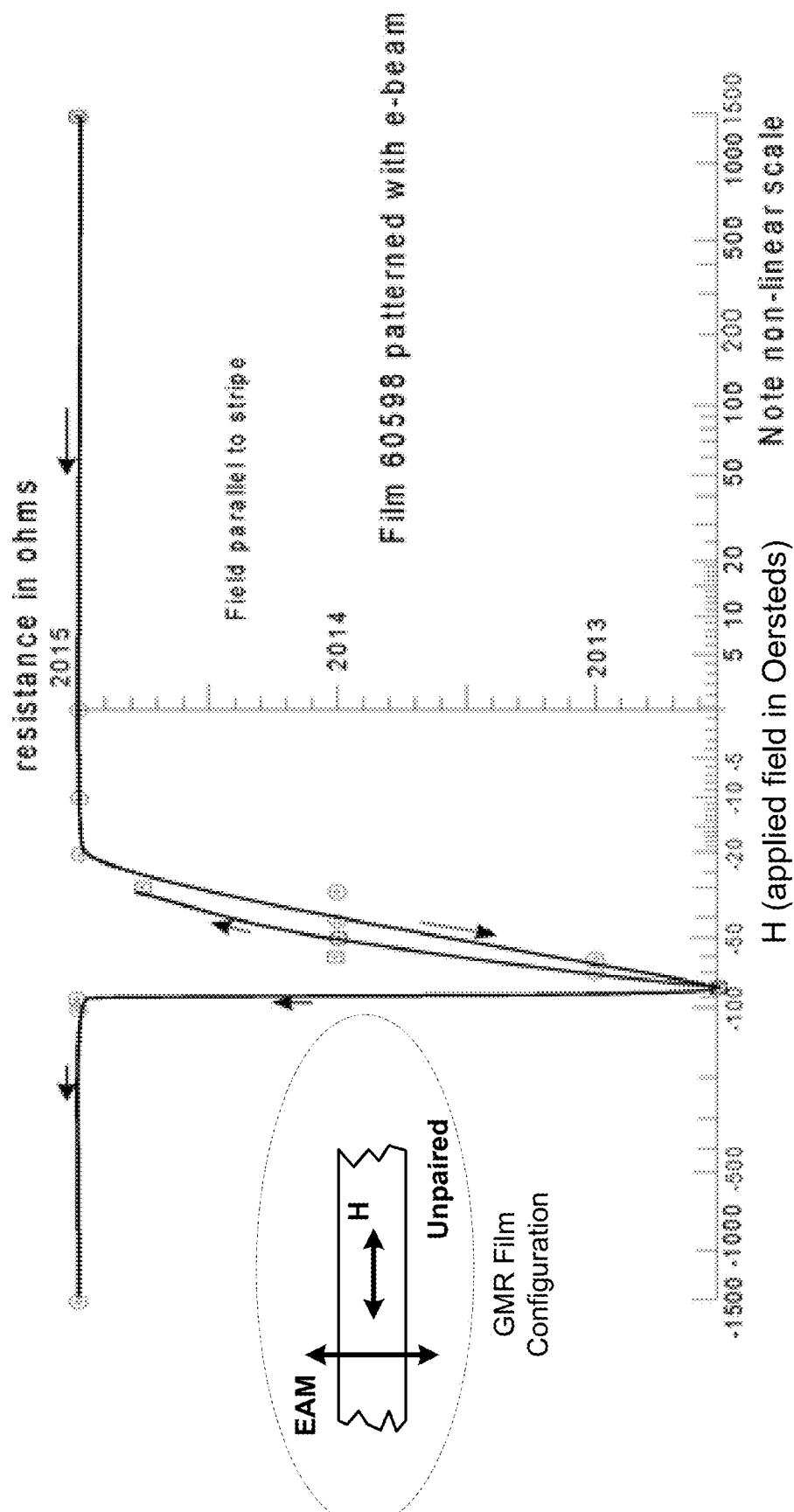


FIG. 9

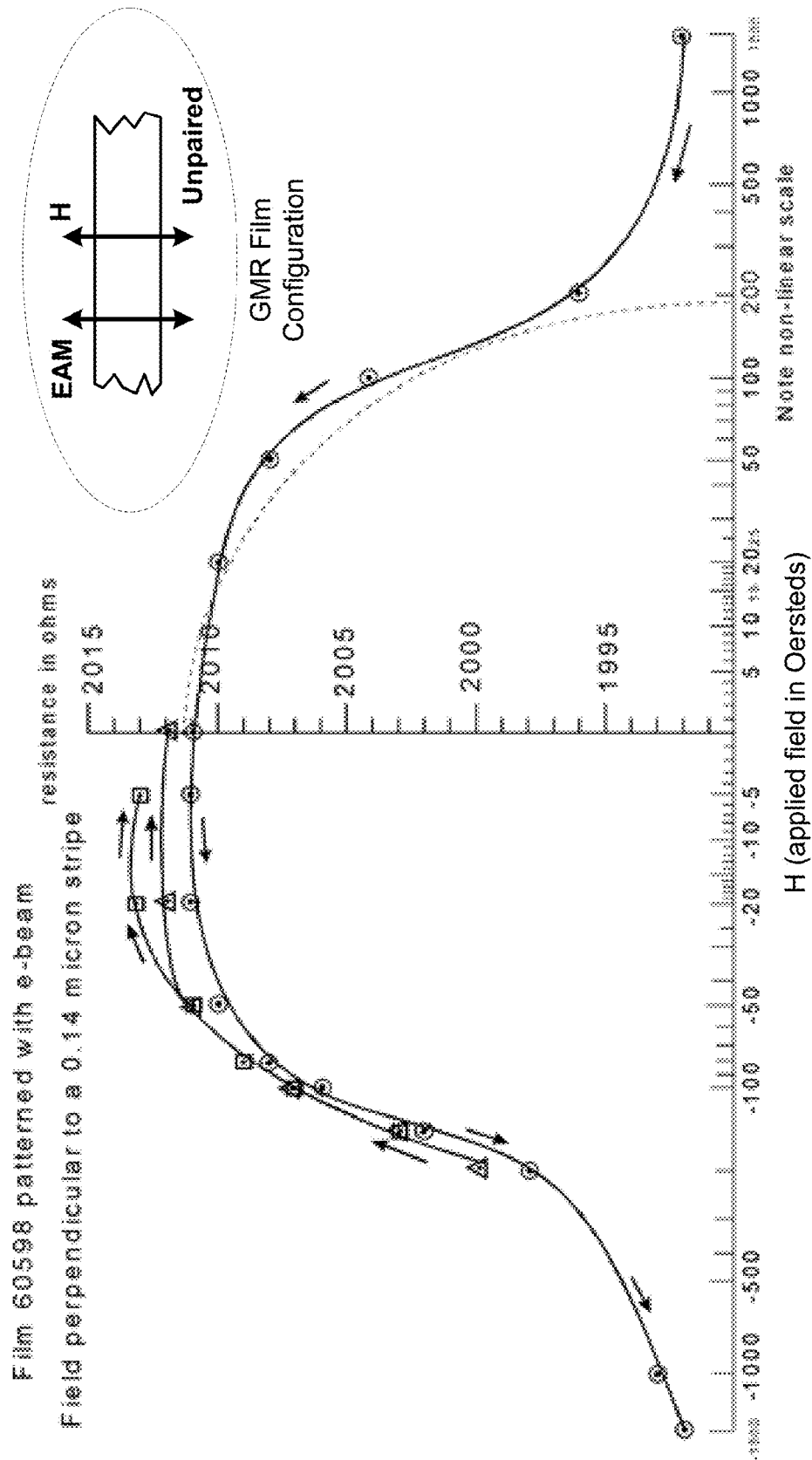


FIG. 10

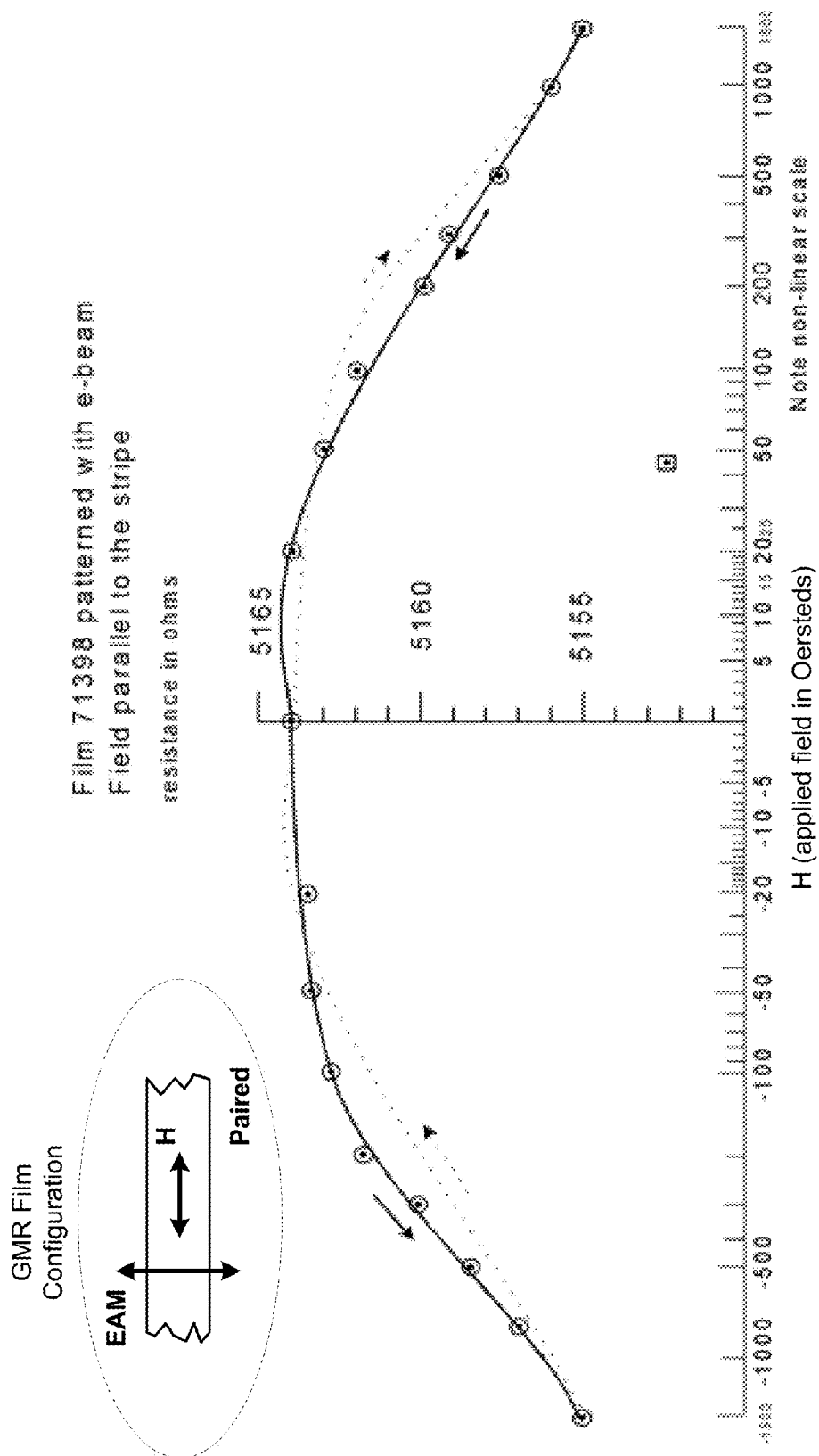


FIG. 11

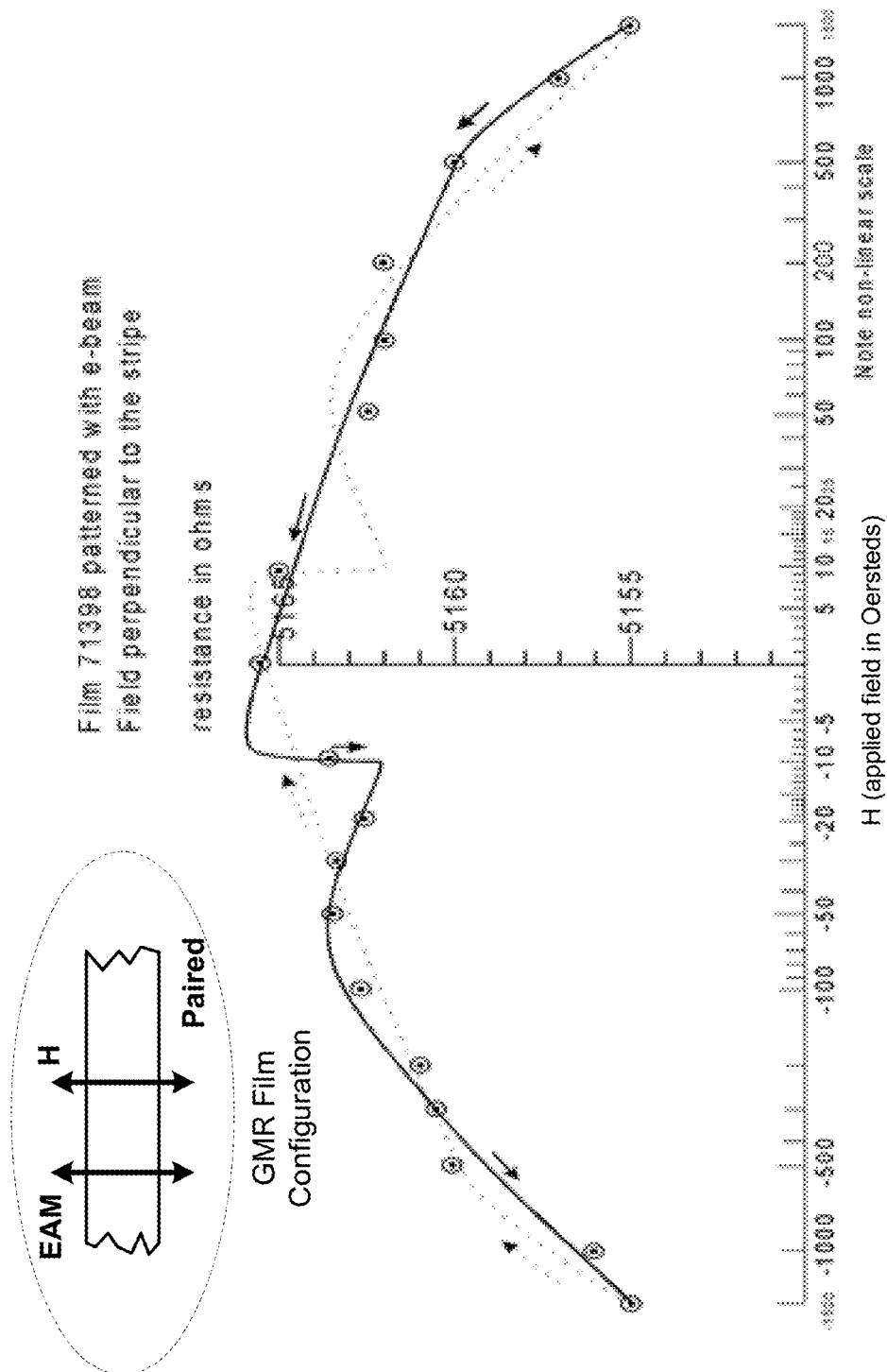


FIG. 12

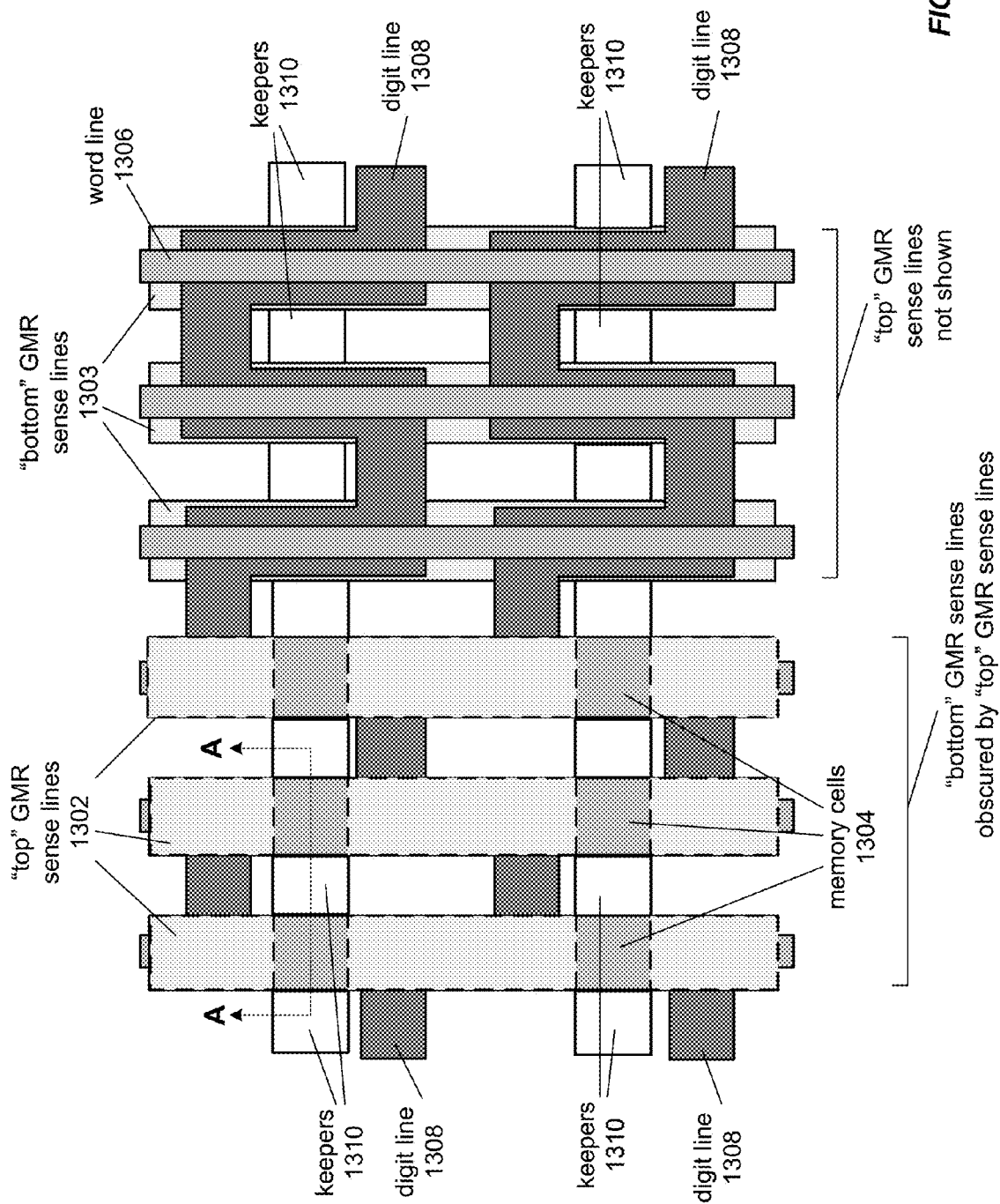


FIG. 13

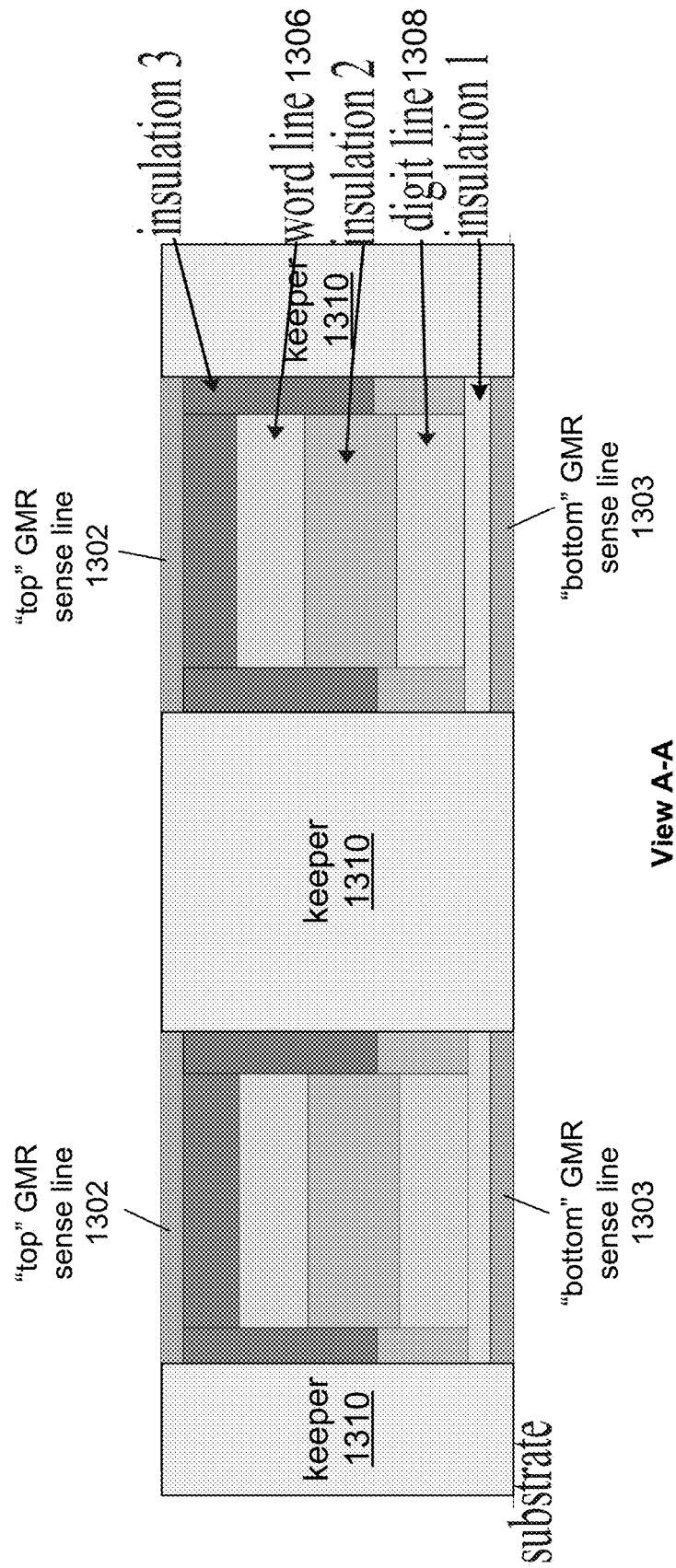


FIG. 14

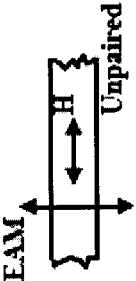
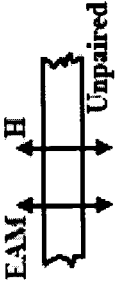
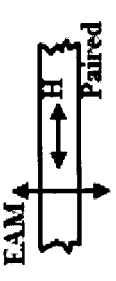
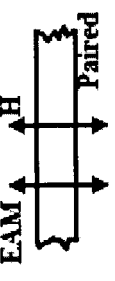
Figure	Key parameters	Width	GMR observed	Switching field (sf)
9	 EAM ↑ H → Unpaired	600 nm	No	10 x bulk sf
10	 EAM ↑ H → Unpaired	140 nm	No	100 x bulk sf
11	 EAM ↑ H → Paired	600 nm	No	150 x bulk sf
12	 EAM ↑ H → Paired	140 nm	Yes	2 x bulk sf

Table 1

FIG. 15

SPINRAM

Matter enclosed in heavy brackets [] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue; a claim printed with strikethrough indicates that the claim was canceled, disclaimed, or held invalid by a prior post-patent action or proceeding.

RELATED APPLICATION DATA

The present application is a reissue of U.S. patent application Ser. No. 15/272,228, now U.S. Pat. No. 9,741,923, which claims priority under 35 U.S.C. 119(e) to U.S. Provisional Patent Application No. 62/232,977 entitled SpinRAM filed on Sep. 25, 2015, the entire disclosure of which is incorporated herein by reference for all purposes.

BACKGROUND

In order to realize the full potential of magnetic random access memory (RAM), whether based on tunnel magnetoresistance (TMR) or giant magnetoresistance (GMR), fundamental challenges at the basic cell design need to be addressed. Such challenges include (1) scalability (e.g., decreasing drive currents and stable error rates with decreasing feature size); (2) endurance (e.g., the number of read/write cycles before cell breakdown); and (3) thermal stability of stored information (e.g., stability against errors due to thermally-induced transitions between two states that represent different bit values, an effect that increases with decreasing element volume and comes into play at deep nanoscale feature sizes).

Cell design features that we have conceived to enable scalability, increased endurance, and thermal stability include (1) a closed-flux cell structure, (2) parallel drive lines at the memory cell, and (3) increased film thickness. Each of these design features is described in more detail below.

An issue that transcends the individual cell design is the compatibility of magnetic RAM fabrication technology with CMOS processing. Some success with regard to this issue has already been demonstrated by commercial magnetic RAM. Another higher level issue is capacity (e.g., sufficient write and read margins for large arrays). We found that the issues attendant to scalability and capacity can be treated as distinct.

The issue of thermal stability has been resolved conceptually. See, for example, U.S. Pat. No. 7,911,830 entitled Scalable Nonvolatile Memory issued Mar. 22, 2011, the entire disclosure of which is incorporated herein by reference for all purposes.

We determined that a critical factor for scalability is control of the demagnetizing field H_d , i.e., the field produced by the magnetization M according to: $V \cdot H_d = -4\pi V \cdot M$. The presence of H_d in a magnetic RAM (e.g., due to incomplete flux closure in its memory cells) causes multiple problems. Inside the memory cell the write current needs to overcome H_d to impress a given magnetization on the material, i.e., the write current must increase to write the bit value. Additionally, H_d from one cell can disturb the magnetization (i.e., change the bit values) of neighboring cells, causing errors. Increasing cell footprint can mitigate increase in error rates, but this sacrifices cell density. H_d also causes “shearing,” a decrease in the slope of the intrinsic hysteresis loop of a cell, that produces skewed minor loop operation and a resulting

decrease in the signal strength of the cell’s read signal. Moreover, in a cell without fully-closed flux, H_d increases strongly as feature size decreases into nanoscale.

These problems—increasing drive currents, increasing error rates, increasing cell footprint, and decreasing signal strength—are exacerbated by increasing demagnetizing fields that accompany decreasing feature size. These problems are further exacerbated by the interplay between thermal fluctuations and H_d in that the two can reinforce each other in specific configurations. To address these problems, we designed a memory cell that has a fully closed-flux and which is characterized by decisive advantages in power consumption, error rates, and memory density over designs with incomplete flux closure.

We also developed a measurement protocol to separate out the effects of demagnetizing fields from possible thermal effects in a magnetic RAM (based on either GMR or TMR) and to determine the magnitude of both. See R. Spitzer and E. Wuori, Demagnetizing Fields in Magnetic RAM, Intermag 2009, Session ET-06, the entire disclosure of which is incorporated herein by reference for all purposes.

Capacity is linked to the signal strength provided by the film (GMR or TMR) used in the memory cell. We chose GMR films for our cell design, despite the smaller signal of presently available GMR structures than that of TMR, for three reasons: (i) simplicity of cell design—the GMR cell size is about one-half that of the TMR cell size, and requires fewer than one-half the number of masking steps; (ii) the method for addressing thermal stability at deep nanoscale lends itself much more readily to GMR than to TMR structures; (iii) the functional memory components of our magnetic RAM—the memory array without support electronics—may be constructed with metals and insulators alone (no semiconductors). This provides the potential for monolithic 3D structures (vertically replicated 2D arrays). The storage density of such a 3D SpinRAM with 4 levels of 2D arrays can exceed that of a hard disk at 30 nm feature size and, for many mainstream applications (e.g., ones that depend on a specific number of input/output operations per second) it will likely be strongly economically competitive with hard disks. Additional information and examples are provided in U.S. Pat. No. 6,992,919 entitled All-Metal Three-Dimensional Circuits and Memories issued Jan. 31, 2006, the entire disclosure of which is incorporated herein by reference for all purposes.

To realize the strong sense signal needed for high capacity, we developed a ferromagnetically-coupled GMR superlattice with low drive fields and potential for significantly higher useful GMR values than currently available, well upwards of 50%. Examples of such a superlattice structure are described in U.S. Pat. No. 8,619,467 entitled High GMR Structure With Low Drive Fields issued Dec. 31, 2013, the entire disclosure of which is incorporated herein by reference for all purposes.

The issue of cell endurance is addressed by our crosspoint magnetic RAM with a coincident-current architecture and tied to the configuration of the drive lines in the memory array as described, for example, in U.S. Pat. No. 7,911,830 incorporated herein by reference above.

Despite these successes in the advancement of magnetic RAM design, further improvement continues to be our goal.

SUMMARY

According to a particular class of implementations, a memory includes a plurality of first signal lines, a plurality of second signal lines, and a plurality of first thin-film

structures exhibiting magnetoresistance. The first signal lines, the second signal lines, and the first thin-film structures form an array of memory cells. Each memory cell includes (i) a portion of a corresponding one of the first thin-film structures; (ii) a portion of a corresponding one of the first signal lines coinciding with the portion of the corresponding first thin-film structure and electrically isolated therefrom; (iii) a portion of a corresponding one of the second signal lines coinciding with the portion of the corresponding first signal line and the portion of the corresponding first thin-film structure, the portion of the corresponding second signal line being electrically isolated from the corresponding first signal line and the corresponding first thin-film structure; and (iv) one or more keeper elements in direct contact with the portion of the corresponding first thin-film structure such that the portion of the corresponding first thin-film structure and the one or more keeper elements form at least part of a fully-closed-flux structure of the memory cell. For each memory cell, the portion of the corresponding first thin-film structure has an easy axis of magnetization perpendicular to a longitudinal axis of the portion of the corresponding first thin-film structure. The first and second signal lines are configured to generate magnetizing fields at each memory cell that are perpendicular to the longitudinal axis of the portion of the corresponding first thin-film structure.

According to a specific implementation, the memory includes a plurality of second thin-film structures exhibiting magnetoresistance, and each memory cell includes a portion of a corresponding one of the second thin-film structures. The portion of the corresponding second thin-film structure for each memory cell coincides with and is electrically isolated from the corresponding first signal line, the corresponding second signal line, and the corresponding first thin-film structure. For each memory cell, the portion of the corresponding second thin-film structure forms part of the fully-closed flux structure.

According to a specific implementation, the first and second signal lines are configured such that, for each memory cell, a primary direction of current flow in the portion of the corresponding first signal line is parallel to a primary direction of current flow in the portion of the corresponding second signal line.

According to a specific implementation, at each memory cell, the portion of the corresponding first thin-film structure and the portions of the corresponding first and second signals lines are co-linear. According to a more specific implementation, each of the first thin-film structures includes sections of non-magnetic conductors between adjacent memory cells.

According to a specific implementation, the first thin-film structure includes at least one high-coercivity magnetic layer and at least one low-coercivity magnetic layer. According to a more specific implementation, the first thin-film structure includes a pair of low-coercivity magnetic layers. According to another more specific implementation, the first thin-film structure comprises a ferromagnetically-coupled superlattice having multiple periods of the high and low-coercivity layers.

According to a specific implementation, each memory cell is characterized by an aspect ratio of approximately 1 to 1.2.

According to another class of implementations, a memory cell includes (i) a portion of a first thin-film structure; (ii) a first signal line coinciding with the portion of the first thin-film structure and electrically isolated therefrom; (iii) a second signal line coinciding with the first signal line and the

portion of the first thin-film structure, the second signal line being electrically isolated from the first signal line and the first thin-film structure; and (iv) one or more keeper elements in direct contact with the portion of the first thin-film structure such that the portion of the first thin-film structure and the one or more keeper elements form at least part of a fully-closed-flux structure of the memory cell. The portion of the first thin-film structure has an easy axis of magnetization perpendicular to a longitudinal axis of the first thin-film structure. The first and second signal lines are configured to generate magnetizing fields that are perpendicular to the longitudinal axis of the first thin-film structure.

According to a specific implementation, the memory cell includes a portion of a second thin-film structure coinciding with and electrically isolated from the first signal line, the second signal line, and the first thin-film structure. The portion of the second thin-film structure forms part of the fully-closed flux structure.

According to a specific implementation, the first and second signal lines are configured such that a primary direction of current flow in the first signal line at the memory cells is parallel to a primary direction of current flow in the second signal line at the memory cell.

According to a specific implementation, the portion of the first thin-film structure and the first and second signals lines are co-linear at the memory cell. According to a more specific implementation, the first thin-film structure includes sections of non-magnetic conductors on either side of the memory cell.

According to a specific implementation, the portion of the first thin-film structure includes at least one high-coercivity magnetic layer and at least one low-coercivity magnetic layer. According to a more specific implementation, the portion of the first thin-film structure includes a pair of low-coercivity magnetic layers. According to another more specific implementation, the portion of the first thin-film structure comprises a ferromagnetically-coupled superlattice having multiple periods of the high and low-coercivity layers.

According to another class of implementations, a memory cell includes (i) a portion of a first thin-film structure exhibiting giant magnetoresistance, the first thin film structure including a high-coercivity magnetic layer and a corresponding pair of low-coercivity magnetic layers; (ii) a first signal line coinciding with the portion of the first thin-film structure and electrically isolated therefrom; (iii) a second signal line coinciding with the first signal line and the portion of the first thin-film structure, the second signal line being electrically isolated from the first signal line and the first thin-film structure; (iv) a portion of a second thin-film structure coinciding with and electrically isolated from the first signal line, the second signal line, and the first thin-film structure, the second thin-film structure exhibiting giant magnetoresistance and including a high-coercivity magnetic layer and a corresponding pair of low-coercivity magnetic layers; and (v) one or more keeper elements in direct contact with the portion of the first thin-film structure and the portion of the second thin-film structure such that the portion of the first thin-film structure, the portion of the second thin-film structure, and the one or more keeper elements form a fully-closed-flux structure of the memory cell. The portion of the first thin-film structure has an easy axis of magnetization perpendicular to a longitudinal axis of the first thin-film structure. The portion of the second thin-film structure has an easy axis of magnetization perpendicular to a longitudinal axis of the second thin-film structure. The first and second signal lines are configured to generate magne-

tizing fields that are perpendicular to the longitudinal axes of both the first and second thin-film structures.

A further understanding of the nature and advantages of various implementations may be realized by reference to the remaining portions of the specification and the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a simplified representation of the layout of a SpinRAM array.

FIG. 2 shows a simplified representation of the layout of another SpinRAM array.

FIG. 3 shows an example of a structure of a GMR film for use with SpinRAM arrays.

FIG. 4 shows a cross-section of a SpinRAM memory cell.

FIG. 5 shows a cross-section of another SpinRAM memory cell.

FIG. 6 shows the physical organization of 3D SpinRAM array.

FIG. 7 illustrates chip-scale interconnectivity for a 3D SpinRAM array.

FIG. 8 shows the R-H curve of a bulk GMR material.

FIGS. 9-12 show the R-H curves for patterned GMR films having different characteristics.

FIG. 13 shows a simplified representation of the layout of another SpinRAM array.

FIG. 14 shows a cross-section of another SpinRAM memory cell.

FIG. 15 includes Table 1 which provides a summary of results for GMR-film and drive-line characteristics in FIGS. 9-12, with no keepers.

DETAILED DESCRIPTION

Reference will now be made in detail to specific implementations. Examples of these implementations are illustrated in the accompanying drawings. It should be noted that these examples are described for illustrative purposes and are not intended to limit the scope of this disclosure. Rather, alternatives, modifications, and equivalents of the described implementations are included within the scope of this disclosure as defined by the appended claims. In addition, specific details may be provided in order to promote a thorough understanding of the described implementations. Some implementations within the scope of this disclosure may be practiced without some or all of these details. Further, well known features may not have been described in detail for the sake of clarity.

The present application describes various implementations of memory cells and memory architectures collectively referred to as SpinRAM. As will be discussed, particular implementations are projected to enable SpinRAM arrays with feature sizes decreasing into deep nanoscale.

According to a particular class of implementations, SpinRAM is implemented as a coincident-current architecture. An example of the physical layout of a SpinRAM array is shown in the plan view of FIG. 1. The dimensions shown are not to scale. The memory cells include portions of the GMR sense lines 102. The cells are thus in series, though they are not necessarily structurally distinct entities in the GMR film. That is, the GMR film portions of the cells may be part of one continuous structure. In the depicted implementation, the physical locations of the cells—the active parts of the GMR line—are determined by the portions of the GMR film that coincide with the overlay of the straight word lines 104 and serpentine digit lines 106 where these drive lines are

co-linear. The co-linearity of the drive lines ensures that the drive fields at the cell location are co-linear.

This design choice—co-linear word and digit lines at the storage location—was implemented to improve cell endurance. That is, there is a cumulative disturb mechanism—magnetization creep—that limits endurance in cell configurations based on architectures with a geometry in which easy-axis and hard-axis drive fields act concurrently. It can cause a film to become demagnetized and lose its information content. This form of disturb, which is distinct from that caused by demagnetizing fields, generally arises for perpendicular drive lines. The problem is avoided, or at least mitigated, with co-linear word and digit lines at the memory cell. This design choice also allows the ends of the keepers 108 to be positioned closely to or in contact with the GMR film, which improves flux closure. Each keeper is constructed from one or more magnetic materials used to help close the flux of the corresponding cell. Magnetization creep is described in Magnetization Creep in Nickel-Iron Films via the Lever Mechanism, A. L. Olson and E. J. Torok, J. Appl. Phys. 37, 1297 (1966), and Magnetization Creep of Cross-Tie Walls, E. J. Torok et al., J. Appl. Phys. 40, 1222 (1969), the entire disclosures of both of which are incorporated herein by reference for all purposes.

The bit value of each cell is stored in the hard layer of the GMR film (a higher coercivity layer that switches at relatively higher field strengths; e.g. cobalt) as a magnetization direction of the cell. The soft layer (a lower coercivity layer that switches at relatively lower field strengths; e.g. permalloy) is used for readout. See further discussion of the operation below.

The size of the cell in the example array of FIG. 1 is $8F^2$, where F is the feature size. Cell size can be reduced to $4F^2$, the theoretical limit for a single-bit cell in a crosspoint memory, by fabricating alternating digit lines in two separate deposition and patterning steps and introducing additional GMR lines in between the GMR lines in the layout of FIG. 1. In such a design, the two sets of serpentine digit lines are insulated from, and partly overlap, each other. In the depicted implementation, there is no GMR film under the overlap of the digit lines, so no memory cell that could be affected by the field they produce. A simplified schematic of such a $4F^2$ structure is shown in FIG. 2.

FIG. 2 shows a $4F^2$ cell structure with two separately deposited and patterned sets of serpentine digit lines 202 and 204. The two sets of digit lines are insulated from—and partly overlap—each other. As shown, GMR sense line 206 does not coincide with the overlap of sense lines 202 and 204, so no memory cell are affected by the field they produce. The keeper layers are not shown. Again, the dimensions shown are not to scale.

Yet denser structures can be realized by making cells containing more than one bit. We have fabricated dibit SpinRAM cells by deposition of additional layers in the GMR films. This is a natural extension of the single-bit cell structure, in that GMR films are already 3D constructs. We also have designs for a quadbit structure, which will result in an effective $1F^2$ area per bit.

It takes eight masks to produce the $8F^2$ SpinRAM structure and, if CMOS support circuitry is used, an additional two masking layers to connect it to this circuitry. There are two additional masking steps in going from $8F^2$ to $4F^2$; one additional step from 1 bit per cell to dibit; and three additional steps from dibit to quadbit. Additional information and examples of multibit cells are provided in U.S. Pat. No. 6,594,175 entitled High Density Giant Magnetoresistive

Memory Cell issued Jul. 15, 2003, the entire disclosure of which is incorporated herein by reference for all purposes.

Functional components of a SpinRAM memory cell are based on structured magnetic films. A generic feature of a SpinRAM array is that it is made entirely of metals and insulators—no semiconductors. This enables unique SpinRAM capabilities. For example, it can be fabricated on top of an underlying semiconductor IC such as, for example, a CMOS processor. It also enables fabrication of 3D monolithic memories by incorporating replicated 2D arrays into a vertically integrated process in the same production line as the 2D structures. The combination of scalable SpinRAM with 3D capability enables a nonvolatile memory with a density greater than that of hard disk. And because of its all-metal construction, SpinRAM is inherently radiation hard.

SpinRAM operation involves a dynamic role for both the hard layer(s) and the soft layer(s) of the multilayer thin-film structure. The bit value is stored as a magnetization direction in the hard layer which may be constructed from, for example, cobalt. A write operation is achieved by coincident half-select currents in word and digit lines that combine into the full-select current required to impress a specific magnetization on the memory cell where the two lines coincide.

The soft layer (which may be constructed from, for example, permalloy) is used to effect a read operation by applying a current pulse that switches the soft layer of all cells in the selected word line. The resistance of the GMR element is relatively low for parallel orientations of the magnetization directions in the soft and hard layers, and relatively high for antiparallel orientations. This difference in resistance is used to determine the direction of the hard-layer magnetization, and therefore the bit value of the cell. Several methods may be used. The following methods are simply provided as examples.

One method is to apply a full-select bipolar word-current pulse. The cell to be read is selected by the sense line that intersects the word line at this cell. In the nondestructive-readout variant, a sample-and-hold circuit stores the sense signal for one magnetization orientation of the soft layer; this signal is then compared to that for the opposite soft-layer magnetization. The comparison yields the orientation of the hard layer. In a destructive-readout variant, the sense line is connected to the input of an amplifier with autonull capability. The amplifier is then autonulled (i.e., an automatic bias current causes the amplifier output to be adjusted to zero during the time the sense line is connected). The data bit is next written to '0' using the write-current circuit. If the bit value was already '0', no change in amplifier output occurs and a '0' is stored in the output latch. If the bit value was a '1', the state of the sense line changes, the amplifier produces a nonzero output, and a '1' is stored in the output latch. The original datum is then rewritten from value stored by the latch.

An alternative method is to store one bit in two cells located on neighboring sense lines, configured so that the soft and hard layers are parallel in one cell and antiparallel in the other. A differential amplifier will see a signed signal that will establish the magnetization of the hard layer. This is a nondestructive readout and is expected to be faster than using a bipolar pulse, but it halves the storage density.

A readout-related issue in this architecture is that the number of cells that can be placed on a line is limited by noise and the GMR value. The signal-to-noise ratio of the sense-line output in this architecture is proportional to GMR and inversely proportional to the square root of both the bandwidth and the number of cells/line. It therefore affects

both the read speed and memory capacity. GMR values in conventional films are too low to meet the capacity requirements of commercial memories. As mentioned above, we have developed a GMR film structure that raises the useful GMR value so as to enable high-capacity memories. Examples of this type of structure are described in U.S. Pat. No. 8,619,467 incorporated herein by reference above.

According to some implementations, the GMR films in the SpinRAM cells are double pseudo spin valve structures with one or more periods including layers permalloy/copper/cobalt/copper/permalloy as shown in FIG. 3. According to a particular implementation, the permalloy is dusted with cobalt to inhibit diffusion, and the cobalt contains 10% iron to minimize magnetostriction. In a bulk (unpatterned) film the cobalt switches at a field of about 10 Oe; the permalloy, at about 2 Oe.

SpinRAM cells with partially-closed flux (e.g., see FIG. 4) have been fabricated and tested at 5 μm , 500 nm, 100 nm feature sizes. The metallic keeper 402 is separated from the GMR film 404 in this design by the thin insulation layer labeled "insulation 1" in FIG. 4 in order not to short the signal in the GMR film. The gap created by insulation 1 results in a magnetic discontinuity in the magnetic circuit between the keeper and the storage element (the GMR film).

Test results showed that, though the cell shown in FIG. 4 could be successfully operated, the drive currents exceeded twice those expected of a cell with closed flux. Analysis of the results showed that the source of the problem was the gap, which causes significantly increased demagnetizing fields H_d as feature size approaches the gap size. This presents an obstacle to scalability unless gap thickness is correspondingly reduced. It was found that, below a feature size of about 90 nm, the gap would have to be made so thin as to short the signal in the GMR film. Increasing H_d , in turn, increases drive currents and error rates.

Alternative approaches to magnetic RAM (e.g., magnetic tunneling junction (MTJ) MRAM) have large and increasing drive currents and increasing error rates with decreasing feature size F. Both of these factors indicate the presence of large H_d in MTJ MRAMs; likely caused by gaps in their cell designs.

An example of an implementation of SpinRAM cells with fully-closed flux is shown in FIG. 5. In the depicted implementation, each of the two adjacent cells includes sections of two GMR films 502 and 504 (i.e., "paired" GMR films) as opposed to the single GMR film 404 (i.e., an "unpaired" GMR film) shown in FIG. 4. The cell cross sections in FIG. 5 are perpendicular to the plane of the array in FIG. 1 with the horizontal direction of the GMR films 502 and 504 corresponding to the horizontal direction of the GMR film strips 102 in the plane of FIG. 1. The drive line currents are perpendicular to the plane of the cell cross sections (i.e., into and out of the page). These currents produce either clockwise or counterclockwise-circulating magnetic fields around the drive lines parallel to the plane of the cross sections. These magnetic fields are contained by the fully-closed flux structures formed by GMR films 502 and 504, and non-conductive magnetic keeper elements 506.

We determined that, in order to avoid large demagnetizing fields, (1) each cell preferably has fully-closed flux (e.g., as shown in FIG. 5); (2) the GMR films preferably have paired magnetic layers (e.g., the two permalloy layers in FIG. 3); and (3) the cell preferably has paired GMR films (e.g., films 502 and 504 of FIG. 5). Provided these design features are met, SpinRAM drive currents and power consumption are projected to decrease with feature size into deep nanoscale, with error rates remaining stable. In some implementations,

the cells depicted in FIG. 5 may incorporate ferromagnetically coupled GMR superlattices as operating elements in the cell structure. In addition, such cells may be implemented without semiconductor elements, thereby enabling 3D monolithic capability.

That is, implementing a SpinRAM cell without semiconductors obviates a major obstacle that characterizes the fabrication of 3D semiconductor circuits. It allows SpinRAM structures to be stacked vertically and electrically connected, as needed, by interconnecting layers. The vertical disposition of SpinRAM structures modifies the physical deployment of the system building blocks without affecting the logical and electronic functionality of the system.

Vertical manufacturing technology enables building non-volatile memory structures with the all-metal support electronics—sense amplifiers, decode circuitry, bit and word drivers, data buffers—physically deployed above, beneath, or alongside the memory cell array. This significantly reduces the overall physical area of the memory component. Examples of all-metal support electronics are described in U.S. Pat. No. 5,929,636 entitled All-Metal, Giant Magnetoresistive, Solid-State Component issued Jul. 27, 1999, the entire disclosure of which is incorporated herein by reference.

Vertical manufacturing capability creates the potential for 3D SpinRAM to exceed the density of mechanical-magnetic storage (hard disk drives). In addition, SpinRAM consumes little power because only accessed lines and associated support electronics are powered, so that, unlike hard-disk storage in data centers, power density remains substantially constant with increasing capacity. Furthermore, a 3D structure may significantly reduce the cost of electronic components as the cost of an IC is more nearly proportional to its area rather than its volume. A simplified schematic of such a structure is shown in FIG. 6.

Physically, the development of such a 3D structure may involve a highly modular construction. The basic module, referred to herein as a “tile” **602**, is a self-contained memory block, i.e., a memory cell array and associated circuitry. Multiple tiles are physically organized into a 2D construction referred to herein as a “floor” **604**. Multiple floors are stacked to form the 3D “die” **606**. Each tile **602** has a three-level structure: 1) the memory cell array; 2) connections to support electronics (address logic, sense amplifiers) at the periphery; and 3) connection stratum (for intra-die connectivity). The advantage of such a three-level tile structure is that the overhead and connections do not increase the footprint appreciably (i.e., nearly 100% cell-array efficiency). A simplified schematic of intra-die interconnectivity is shown in FIG. 7.

Logically, the 3D structure appears linear as the tiles are contiguously connected in a linear address space. Floors are transparent to the selection logic. Intra-tile and inter-tile (horizontal) connectivity is achieved via a dedicated connection stratum **702**. Inter-floor (vertical) connectivity **704** is achieved via a dedicated area at the floor edges which increases floor area by about 2%-5%. The tiles are connected to an internal bus. The number of data and control lines does not increase with component capacity. The number of address lines increases slightly. Such a 3D structure differs fundamentally from the packaging of multiple wafers in a single module. Additional information and examples are provided in U.S. Pat. No. 6,992,919 incorporated herein by reference above.

To analyze the extent of flux closure needed for scalability into deep subnanoscale, we implemented a partially-closed flux cell design with a gap as shown in and described above

with reference to FIG. 4. We fabricated and tested this design at feature sizes F ranging from 5 μm down to 100 nm. We found that drive currents and error rates increased with decreasing F , and that drive currents at fixed cell-feature size depend on gap thickness.

We simulated performance of the cell design of FIG. 4 into nanoscale. We found that write currents increase rapidly as feature size shrinks below a micron. We believe this to be due to the sharp rise in the demagnetizing field H_d at nanoscale dimensions. We also found that to reduce H_d to an acceptable level, gap thickness has to be decreased correspondingly so as not to exceed strip width. At feature size below about 90 nm, the gap would have to be made so thin as to short the signal in the GMR film. The requirement that the gap layer must remain thick enough to be reliably short free prevents miniaturization of the cell design of FIG. 4 into deep nanoscale.

To analyze the optimal GMR film structure, we analyzed restrictions on the structure of GMR films needed to minimize demagnetizing fields. Our theoretical results showed that narrow GMR film strips with either unpaired magnetic layers or paired magnetic layers of wide separation have large demagnetizing fields H_d . At micronscale, H_d is significantly lower for paired magnetic layers than it is for a stand-alone film strip, indicating that the large demagnetizing fields in unpaired films can be well controlled at this feature size by pairing the magnetic layers, provided the spacer thickness between them is kept small. This pairing of magnetic layers was incorporated into the GMR film and is illustrated in FIG. 3 and has been used in our SpinRAM cell designs. We also fabricated GMR films at micronscale with and without the paired layers. We found that H_d in films with paired layers was more than an order of magnitude lower than in the unpaired-layer films, confirming the theoretical results.

We also analyzed demagnetizing fields of GMR films with paired layers at nanoscale feature sizes. We found that the demagnetizing field, even of paired magnetic layers, increases greatly from micronscale to nanoscale. We found that we can compensate for this increase by using paired GMR films and magnetic keepers to form a closed-flux memory cell structure as shown, for example, in FIG. 5.

We also analyzed the restrictions on the choices of geometric cell parameters imposed by the requirements of stability of the magnetized state and maintaining low switching fields. We found that the aspect ratio of the cell (i.e., length-to-width) was best kept between 1.2 and 1. We also found that the aspect ratio, the separation of the magnetic layers, and the layer thicknesses should not be varied independently in that changes in one parameter typically required compensation by changes in the other two in order to maintain both stability and low switching field.

To determine the relative orientation of patterned GMR films and the drive field required for a viable SpinRAM cell, we fabricated a set of GMR films with paired layers of composition (the symbol “Pe” is used for permalloy)/Pe 6 nm/Cu 2 nm/Co 6 nm/Cu 2 nm/Pe 4 nm/. The R-H curve of a bulk film (i.e., not cut into strips) is shown in FIG. 8. The depicted curve is the desired behavior for GMR film strips patterned to nanoscale.

In the four configurations of patterned GMR films discussed below, the thin strips are cut perpendicular to the easy axis defined by the direction of the magnetic field present during film deposition (EAM). We used e-beam lithography at the Cornell Nanotechnology Facility to pattern films with paired layers into strips of widths ranging from 5 μm down to 100 nm. The results varied depending on whether the

11

GMR films in the cell are paired or unpaired, on feature size, and on the relative orientations of the GMR strip and the drive fields.

Measurements on an unpaired GMR film showed no GMR effect for either of the two configurations of the in-plane drive field relative to the EAM (i.e., the easy axis defined by the magnetic field impressed during deposition). The switching field for a 600 nm-wide strip with the applied field H perpendicular to the EAM (see the R-H curve of FIG. 9) was an order of magnitude higher than that for a wide strip. The switching field for a 140 nm-wide strip with the drive field parallel to the EAM (see the R-H curve of FIG. 10) was two orders of magnitude higher than that for a wide strip.

In both FIGS. 9 and 10, the EAM is perpendicular to the strip, but the shape-anisotropy easy axis is in the direction of the strip. Theoretical analysis indicates that narrow strips of either unpaired films or paired films of very wide separation have large demagnetizing fields, and that permalloy and cobalt switch together rather than separately because the differences in anisotropy and coercivity of permalloy and cobalt are overwhelmed by the shape anisotropy and stray field of the strips in an unpaired GMR film. Each of the R-H curve loops has the shape and low resistance change typical of anisotropic magnetoresistance (AMR) rather than that of GMR.

For paired films at feature sizes corresponding to those of the unpaired films, there is still no GMR effect for the configuration with the drive field in the direction along the strip (see the R-H curve of FIG. 11). By contrast, the configuration with the in-plane drive field perpendicular to the GMR strip (see the R-H curve of FIG. 12) does show the GMR effect, and the switch takes place at a value on the order of, though larger than, that of the wide strip. The use of paired GMR films thus substantially cancels the demagnetizing field and greatly lowers the switching threshold of nanoscale memory elements. Note that in this configuration, the GMR strip is parallel and co-linear with the word line rather than perpendicular as shown in FIGS. 1 and 2.

We redesigned the memory cell so as to eliminate the gap entirely resulting in a cell design with a fully-closed flux as shown in FIG. 5. We simulated performance of this cell design down to deep nanoscale. We found that drive currents decrease and error rates remain low with decreasing feature size.

The orientation of the GMR strip (co-linear with the word line) allows for a similar increase in density as described above with reference to the array of FIG. 2 without the need for adding GMR strips relative to the array shown in FIG. 1. This is because the overlapping, serpentine digit lines now intersect with the vertical GMR strips at more locations to create memory cells.

When the GMR strip is co-linear with the word line, the resulting area of the memory element (overlap of the two drive lines and the GMR line) is now $1F \times 3F$, i.e., three squares in a vertical line with one another; where a square can be thought of as the area of the intersection of a horizontal and vertical line. This aspect ratio may be undesirably far from unity. Therefore, according to some implementations, configurations are contemplated that reduce this area closer to $1F \times 1F$. According to one such implementation, the parts of the GMR line that correspond to the two outer squares in the overlap region of the GMR line are replaced by non-magnetic conductors. This reduces the area of the memory cell to $1F \times 1F$ with the non-magnetic conductor portions of the GMR line being between adjacent memory cells that share that line. It also avoids having two

12

adjacent digit lines interacting with the same portion of the GMR line (e.g., where the digit lines overlap as shown in FIG. 2).

The results represented by the R-H curves of FIGS. 9-12 for patterned films are summarized in Table 1. Note that the low value of the switching field for the observed GMR is obtained without the use of keepers, an important element of the memory cell that are expected to lower the switching field further. "EAM" is the easy axis defined by the magnetic field impressed during deposition. "Paired" and "Unpaired" refers to the GMR films (rather than the layers of the GMR films).

As described herein, SpinRAM feature size can be decreased into deep nanoscale, provided the cell geometry and parameters are designed appropriately. These may include, for example, that (1) the GMR films have paired magnetic layers (e.g., as shown in FIG. 3); (2) the GMR films in the memory cell are paired (e.g., as shown in FIG. 5); (3) magnetic flux is closed in the memory cell (e.g., as in the cell of FIG. 5); (4) the easy axis defined by the direction of the magnetic field present during film deposition (EAM) is perpendicular to the strip length; and/or (5) the cell aspect ratio is approximately 1. In addition, the design with fully-closed flux has decisive advantages in power consumption, error rates, and memory density over designs with incomplete flux closure.

FIG. 13 shows a plan view of a portion of a SpinRAM array in which the GMR films have paired magnetic layers, the GMR films at each memory cell are paired, each memory cell has a fully-closed flux structure, the EAM is perpendicular to the longitudinal axis of the GMR strips, and the GMR strips are co-linear with the word lines. FIG. 14 shows a cross-section of two adjacent memory cells represented by cross-section line A-A in FIG. 13.

The left-hand half of the array includes the "top" GMR strips (i.e., sense lines) 1302 that obscure the corresponding "bottom" GMR strips 1303 from the depicted perspective. The right-hand half of the array is shown without the "top" GMR strips 1302 so that the underlying structures (i.e., word lines 1306, digit lines 1308, and "bottom" GMR strips 1303) may be more clearly illustrated. Insulators are not shown in FIG. 13 for clarity. It should be understood that the terms "top" and "bottom" are relative terms used for illustrative purposes and may or may not correspond to how those terms relate to a local gravitational field. It should also be noted that the depicted structures are not shown to scale.

Each memory cell 1304 is located at the coincidence of a top GMR sense line 1302, a bottom GMR sense line 1303, a word line 1306, and a digit line 1308. In contrast with the array of FIG. 1, GMR sense lines 1302 and 1303 are co-linear with word lines 1306. That is, the longitudinal axes of GMR sense lines 1302 and 1303 are perpendicular to the view of FIG. 14 (i.e., extending into and out of the page). Similar to the array of FIG. 1, digit lines 1308 are serpentine structures so that the drive fields generated by currents in digit lines 1308 and word lines 1306 are aligned with each other along the same axis; in this case perpendicular to the longitudinal axes of GMR sense lines 1302 and 1303. And because the EAM of paired GMR sense lines 1302 and 1303 is also perpendicular to the longitudinal axes of these sense lines, the cell configuration corresponds to the configuration discussed above with reference to FIG. 12. Non-conductive magnetic keepers 1310, along with top and bottom GMR sense lines 1302 and 1303 form a fully-closed flux structure at each memory cell 1304.

Because keepers 1310 are in parallel with memory cells 1304, keepers 1310 are constructed (at least in part) from a

13

non-conductive magnetic material to avoid providing a shorting path for the sense current in GMR sense lines **1302** and **1303**. According to various implementations, keepers **1310** may be constructed using, for example, a magnetically soft ferrite. "Soft" in this context refers to material having high permeability & low coercivity. In some cases, the keepers may be constructed entirely from such a material. In other cases, the keepers may be constructed using more than one type of material as long as shorting of GMR sense lines **1302** and **1303** is avoided.

According to a particular implementation, GMR sense lines **1302** and **1303** are constructed with alternating sections of GMR film (at each memory cell) and non-magnetic conductors (between memory cells) as represented by the dashed lines on GMR sense lines **1302**. As will be appreciated, these intervening non-magnetic segments of the GMR sense lines allow for greater density in that the digit lines may be moved closer together or even overlap as discussed above with reference to FIG. 2. They also allow for memory cell aspect ratios in the more desirable range of approximately 1 to 1.2.

It will be understood by those skilled in the art that changes in the form and details of the implementations described herein may be made without departing from the scope of this disclosure. In addition, although various advantages, aspects, and objects have been described with reference to various implementations, the scope of this disclosure should not be limited by reference to such advantages, aspects, and objects. Rather, the scope of this disclosure should be determined with reference to the appended claims.

What is claimed is:

1. A memory, comprising:

a plurality of first signal lines;

a plurality of second signal lines; and

a plurality of first thin-film structures exhibiting magnetoresistance, *each of the first thin-film structures having a longitudinal axis;*

a plurality of second thin-film structures exhibiting magnetoresistance, each of the second thin-film structures having a longitudinal axis;

wherein the first signal lines, the second signal lines, [and] the first thin-film structures, *and the second thin-film structures* form an array of memory cells, each memory cell comprising:

a portion of a corresponding one of the first thin-film structures;

a portion of a corresponding one of the second thin-film structures;

a portion of a corresponding one of the first signal lines coinciding with the portion of the corresponding *one of the first thin-film [structure] structures and the portion of the corresponding one of the second thin-film structures* and electrically isolated therefrom;

a portion of a corresponding one of the second signal lines coinciding with the portion of the corresponding *one of the first signal [line and] lines, the portion of the corresponding one of the first thin-film [structure] structures, and the portion of the corresponding one of the second thin-film structures, the portion of the corresponding one of the second signal [line] lines* being electrically isolated from the corresponding *one of the first signal [line and] lines, the corresponding one of the first thin-film [structure] structures, and the corresponding one of the second thin-film structures;* and

14

[one or more] *a plurality of* keeper elements in direct contact with the portion of the corresponding *one of the first thin-film [structure] structures and the portion of the corresponding one of the second thin-film structures* such that the portion of the corresponding *one of the first thin-film [structure] structures, the portion of the corresponding one of the second thin-film structures, and the [one or more] keeper elements* form at least part of a fully-closed-flux structure of the memory cell; and

wherein, for each memory cell, the portion of the corresponding *one of the first thin-film structure* has an easy axis of magnetization perpendicular to [a] *the longitudinal axis of the corresponding one of the first thin-film structures and in a plane of the portion of the corresponding one of the first thin-film [structure] structures, and the portion of the corresponding one of the second thin-film structures has an easy axis of magnetization perpendicular to the longitudinal axis of the corresponding one of the second thin-film structures and in a plane of the portion of the corresponding one of the second thin-film structures, and wherein the first and second signal lines are configured to generate magnetizing fields at each memory cell that have components in the planes of the corresponding portions of the corresponding one of the first thin-film structures and the corresponding one of the second thin-film structures that are perpendicular to the longitudinal [axis of the portion] axes of the corresponding one of the first thin-film structures and the corresponding one of the second thin-film [structure] structures.*

[2. The memory of claim 1, further comprising a plurality of second thin-film structures exhibiting magnetoresistance, each memory cell further comprising a portion of a corresponding one of the second thin-film structures, the portion of the corresponding second thin-film structure for each memory cell coinciding with and being electrically isolated from the corresponding first signal line, the corresponding second signal line, and the corresponding first thin-film structure, and wherein, for each memory cell, the portion of the corresponding second thin-film structure forms part of the fully-closed flux structure.]

3. The memory of claim 1, wherein the first and second signal lines are configured such that, for each memory cell, a primary direction of current flow in the portion of the corresponding *one of the first signal [line] lines* is parallel to a primary direction of current flow in the portion of the corresponding *one of the second signal [line] lines.*

4. The memory of claim 1, wherein at each memory cell, the portion of the corresponding *one of the first thin-film [structure] structures* and the portions of the corresponding *one of the first signal lines and the corresponding one of the second signals lines* are co-linear.

5. The memory of claim 4, wherein each of the first thin-film structures includes sections of non-magnetic conductors between adjacent memory cells.

6. The memory of claim 1, wherein *each of the first thin-film [structure] structures* includes at least one high-coercivity magnetic layer and at least one low-coercivity magnetic layer.

7. The memory of claim 6, wherein *each of the first thin-film [structure] structures* includes a pair of low-coercivity magnetic layers.

8. The memory of claim 7, wherein *each of the first thin-film [structure] structures* includes a first permalloy layer, a first copper layer, a cobalt layer, a second copper layer, and a second permalloy layer.

15

9. The memory of claim 6, wherein *each of* the first thin-film [structure] *structures* comprises a ferromagnetically-coupled superlattice having multiple periods of the high and low-coercivity layers.

10. The memory of claim 1, wherein each memory cell is characterized by an aspect ratio of approximately 1 to 1.2.

11. A memory cell comprising:

a portion of a first thin-film structure, *the first thin-film structure having a longitudinal axis;*

a portion of a second thin-film structure, *the second thin-film structure having a longitudinal axis;*

a first signal line coinciding with the portion of the first thin-film structure and *the portion of the second thin-film structure, the first signal line being electrically isolated therefrom;*

a second signal line coinciding with the first signal line [and], the portion of the first thin-film structure, and *the portion of the second thin-film structure, the second signal line being electrically isolated from the first signal line and the first thin-film structure; and*

[one or more] *a plurality of keeper elements in direct contact with the portion of the first thin-film structure and the portion of the second-thin film structure such that the portion of the first thin-film structure, the portion of the second thin-film structure, and the [one or more] keeper elements form at least part of a fully-closed-flux structure of the memory cell; and*

wherein, the portion of the first thin-film structure has an easy axis of magnetization perpendicular to [a] *the longitudinal axis of the first thin-film structure and in a plane of the first thin-film structure, wherein the second thin-film structure has an easy axis of magnetization perpendicular to the longitudinal axis of the second thin-film structure and in a plane of the second thin-film structure, and wherein the first and second signal lines are configured to generate magnetizing fields having components in the planes of the first and second thin-film structures that are perpendicular to the longitudinal [axis] axes of the first and second thin-film [structure] structures.*

[12. The memory cell of claim 11, further comprising a portion of a second thin-film structure coinciding with and electrically isolated from the first signal line, the second signal line, and the first thin-film structure, wherein the portion of the second thin-film structure forms part of the fully-closed flux structure.]

13. The memory cell of claim 11, wherein the first and second signal lines are configured such that a primary direction of current flow in the first signal line at the memory cells is parallel to a primary direction of current flow in the second signal line at the memory cell.

14. The memory cell of claim 11, wherein the portion of the first thin-film structure and the first and second signals lines are co-linear at the memory cell.

15. The memory cell of claim 14, wherein the first thin-film structure includes sections of non-magnetic conductors on either side of the memory cell.

16

16. The memory cell of claim 11, wherein the portion of the first thin-film structure includes at least one high-coercivity magnetic layer and at least one low-coercivity magnetic layer.

17. The memory cell of claim 16, wherein the portion of the first thin-film structure includes a pair of low-coercivity magnetic layers.

18. The memory cell of claim 17, wherein the portion of the first thin-film structure includes a first permalloy layer, a first copper layer, a cobalt layer, a second copper layer, and a second permalloy layer.

19. The memory cell of claim 16, wherein the portion of the first thin-film structure comprises a ferromagnetically-coupled superlattice having multiple periods of the high and low-coercivity layers.

20. A memory cell comprising:

a portion of a first thin-film structure exhibiting giant magnetoresistance, the first thin film structure including a high-coercivity magnetic layer and a corresponding pair of low-coercivity magnetic layers, *the first thin-film structure having a longitudinal axis;*

a first signal line coinciding with the portion of the first thin-film structure and electrically isolated therefrom;

a second signal line coinciding with the first signal line and the portion of the first thin-film structure, the second signal line being electrically isolated from the first signal line and the first thin-film structure;

a portion of a second thin-film structure coinciding with and electrically isolated from the first signal line, the second signal line, and the first thin-film structure, the second thin-film structure exhibiting giant magnetoresistance and including a high-coercivity magnetic layer and a corresponding pair of low-coercivity magnetic layers, *the second thin-film structure having a longitudinal axis oriented in parallel with the longitudinal axis of the first thin-film structure; and*

[one or more] *a plurality of keeper elements in direct contact with the portion of the first thin-film structure and the portion of the second thin-film structure such that the portion of the first thin-film structure, the portion of the second thin-film structure, and the [one or more] keeper elements form a fully-closed-flux structure of the memory cell; and*

wherein, the portion of the first thin-film structure has an easy axis of magnetization perpendicular to [a] *the longitudinal axis of the first thin-film structure and in a plane of the first thin-film structure, the portion of the second thin-film structure has an easy axis of magnetization perpendicular to [a] the longitudinal axis of the second thin-film structure and in a plane of the second thin-film structure, and wherein the first and second signal lines are configured to conduct currents having a primary direction of current flow parallel to the longitudinal axes of the first and second thin-film structures and to thereby generate magnetizing fields having components in the planes of the first and second thin-film structures that are perpendicular to the longitudinal axes of both the first and second thin-film structures.*

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