

[54] CHARACTER DISPLAY SYSTEM

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[22] Filed: **July 24, 1972**

[21] Appl. No.: **274,742**

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[30] Foreign Application Priority Data

July 27, 1971 Japan 46-56618
Aug. 6, 1971 Japan 46-59692
Aug. 31, 1971 Japan 46-67232
Aug. 31, 1971 Japan 46-67235
Sept. 7, 1971 Japan 46-69421
Sept. 7, 1971 Japan 46-69424
Oct. 15, 1971 Japan 46-81994

[52] U.S. Cl. 340/324 AD, 315/22

[51] Int. Cl. G06f 3/14

[58] Field of Search.... 340/324 AD, 324 A; 315/18, 315/19, 22

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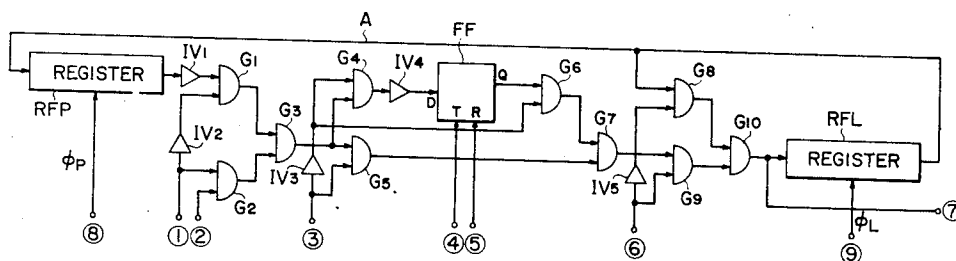
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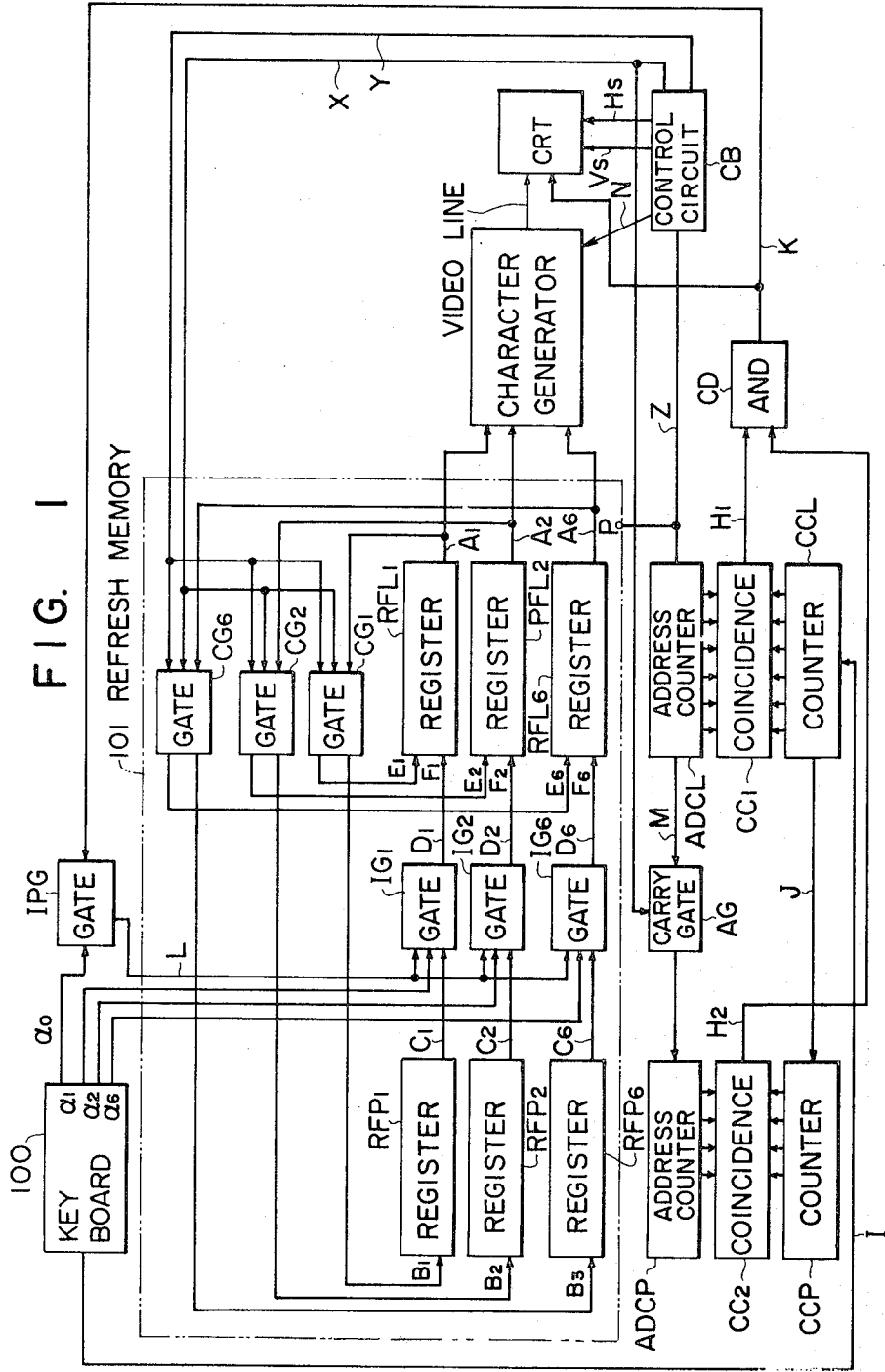
[57]

ABSTRACT

A character display system of multi-rows and multi-columns comprising a first and a second memory for achieving repeated reading in the character display process, and means for inserting or erasing a character or characters in the information transfer between the first and the second memory or in editing the information in the first memory. Said means includes a shift register which can be inserted and disconnected from the recirculation loop of the data. The character display system has a function of arbitrary deletion or insertion of a character or characters in the display image plane.

9 Claims, 25 Drawing Figures





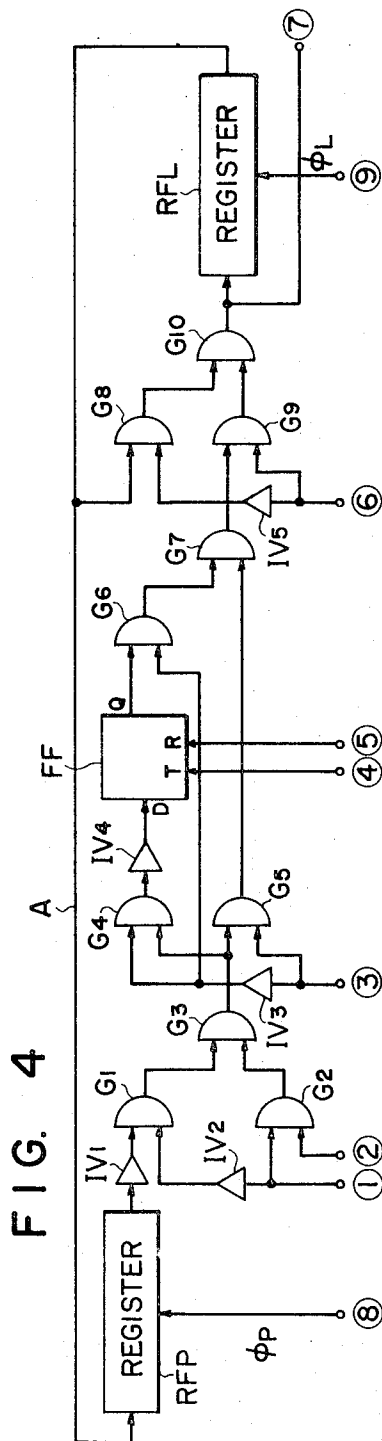
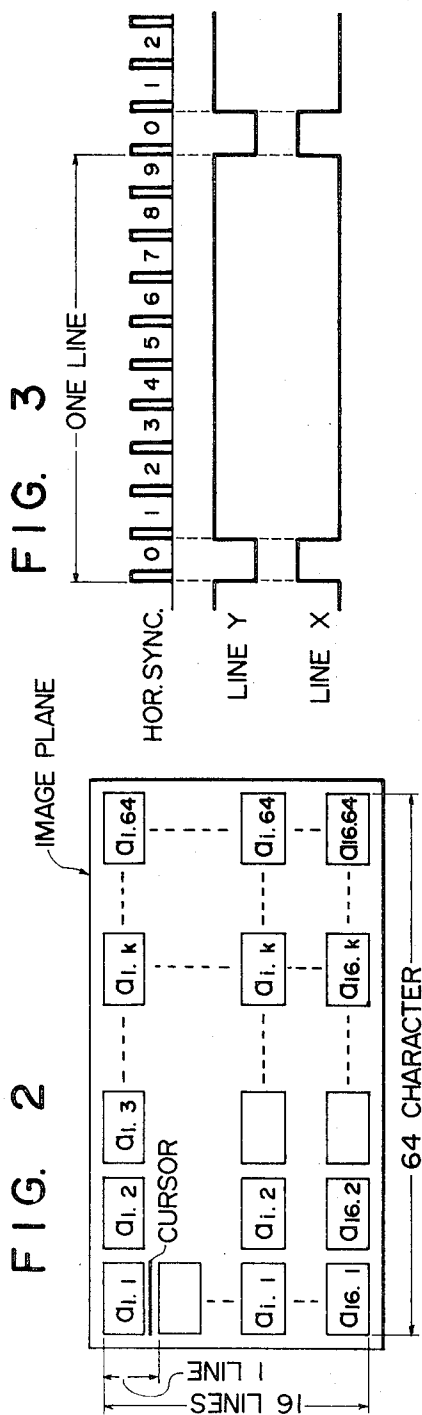


FIG. 5

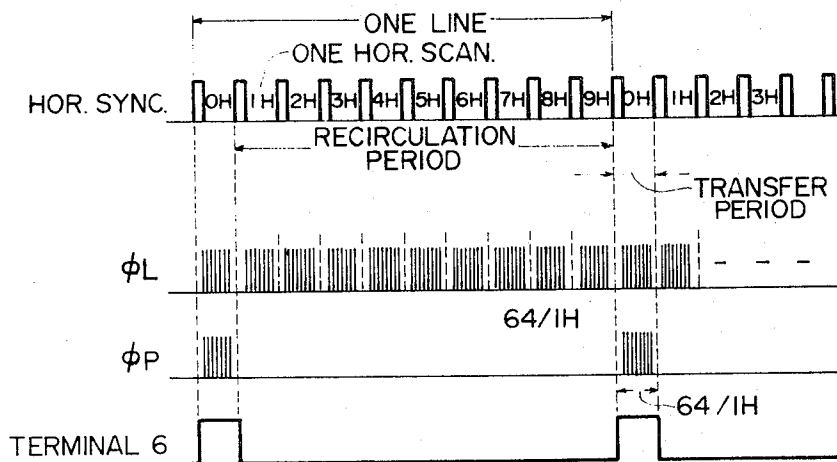


FIG. 6a

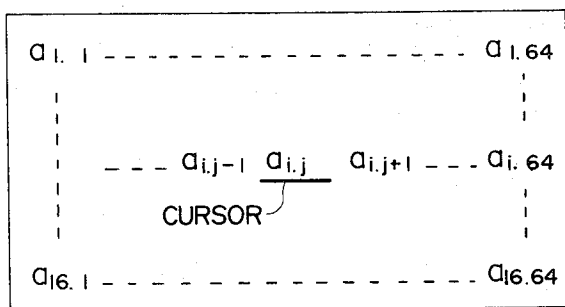


FIG. 6b

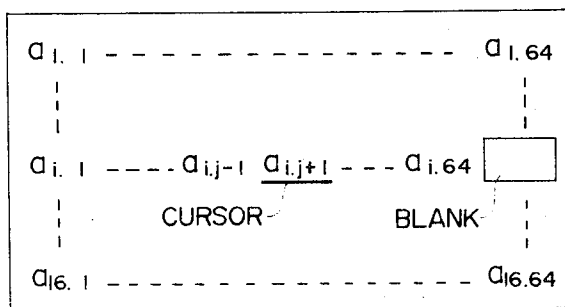


FIG. 7

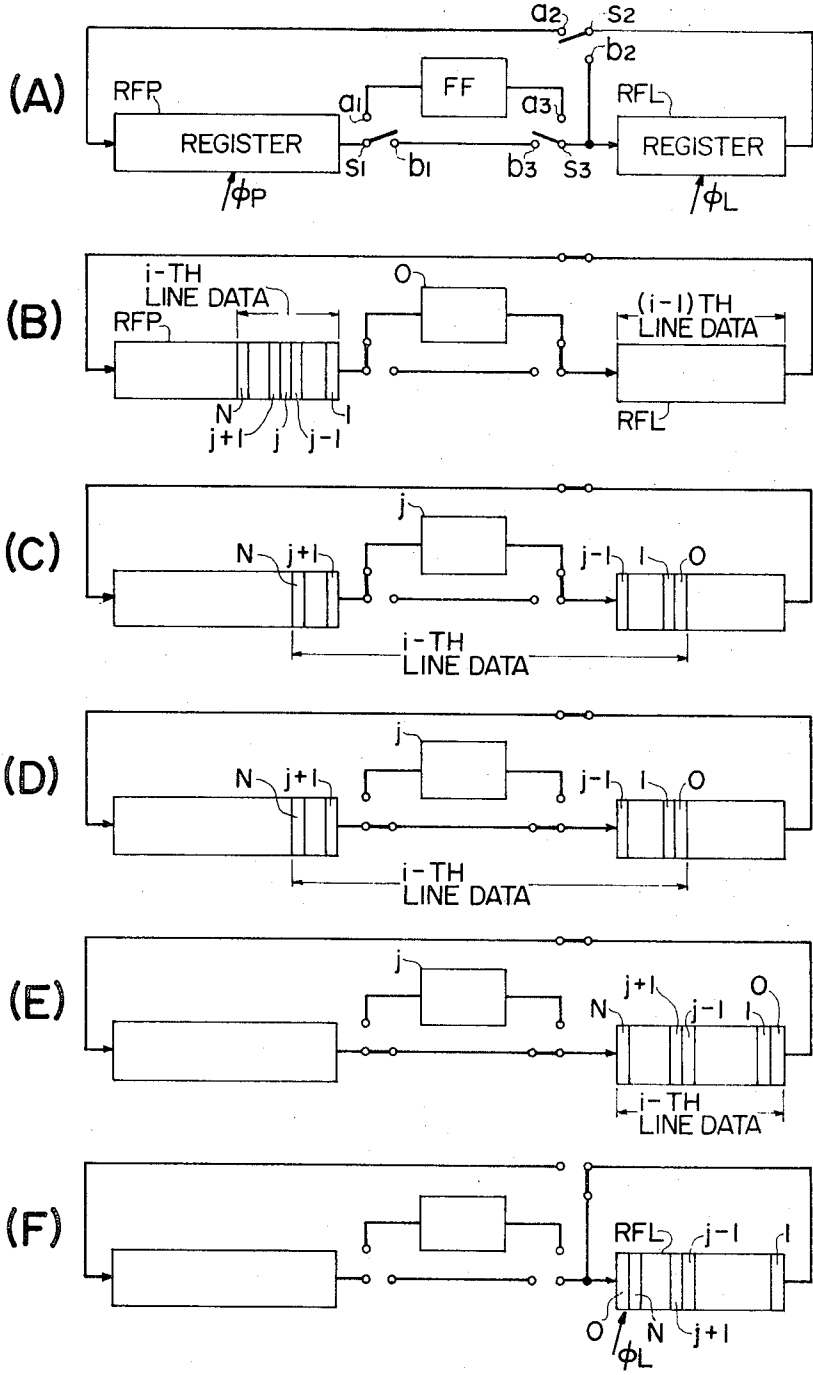


FIG. 8a

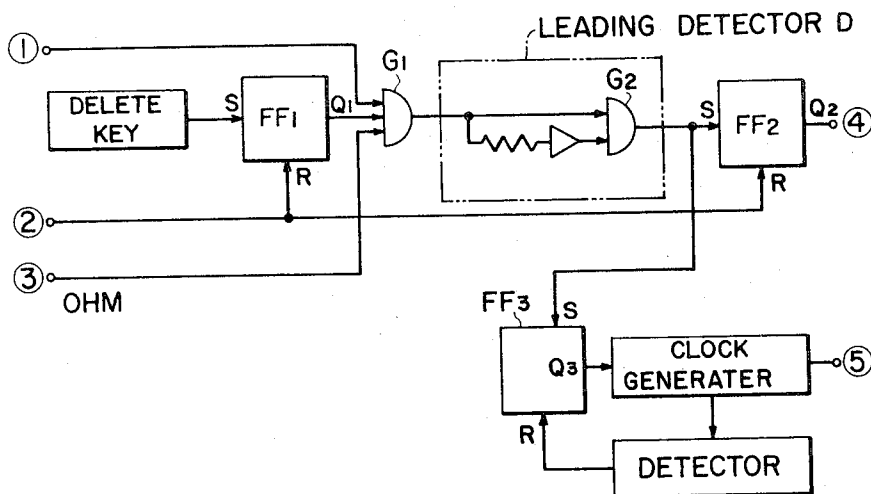


FIG. 8b

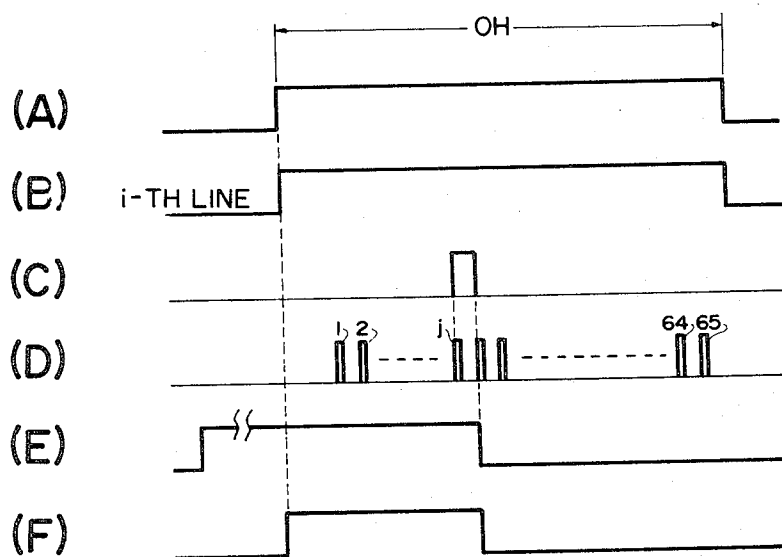


FIG. 9a

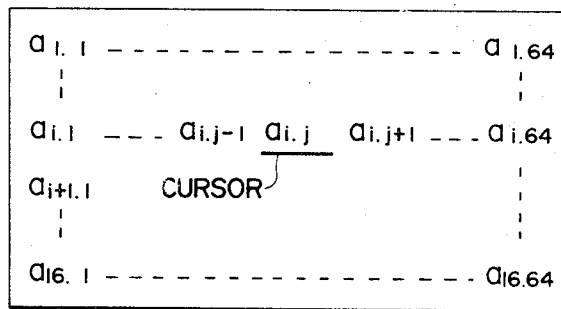


FIG. 9b

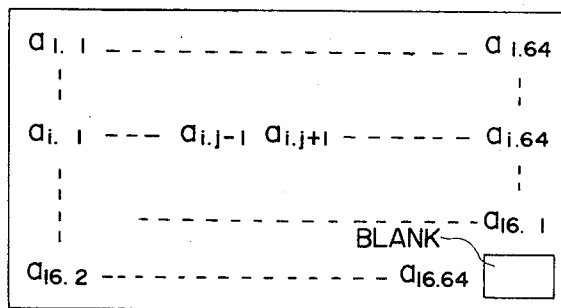


FIG. 10

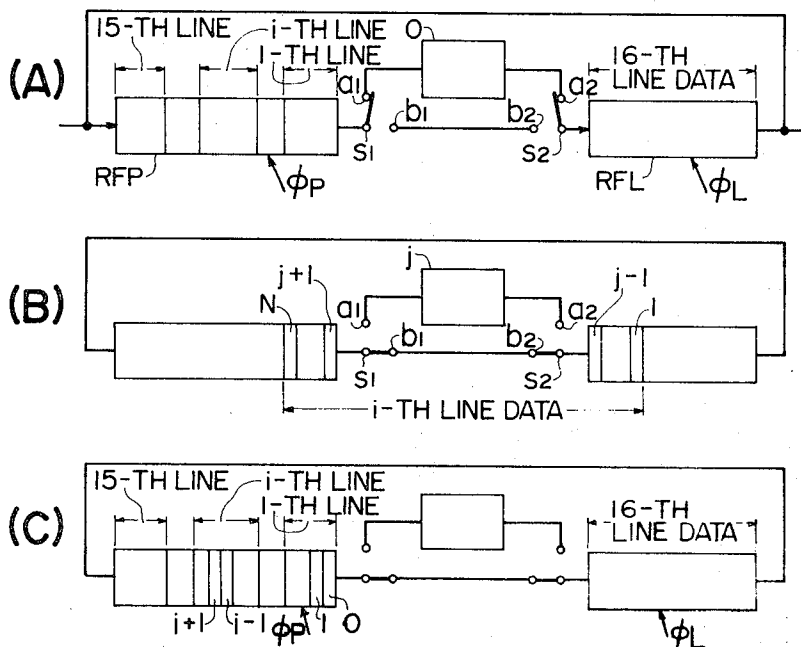


FIG. 13

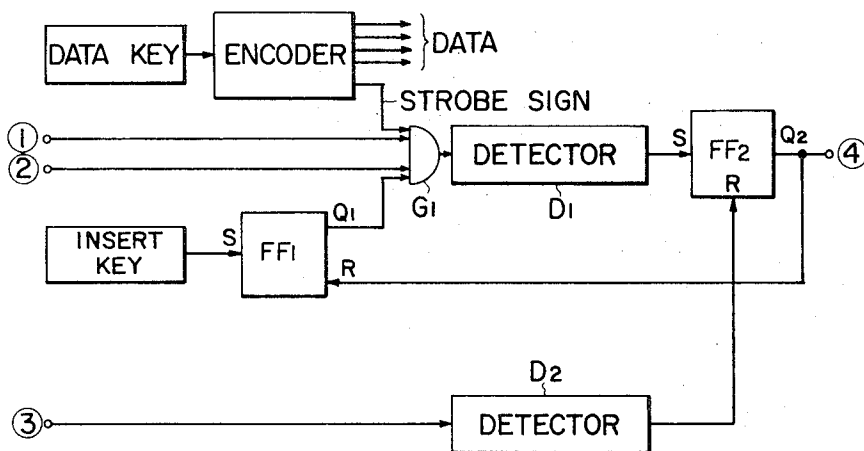


FIG. 14

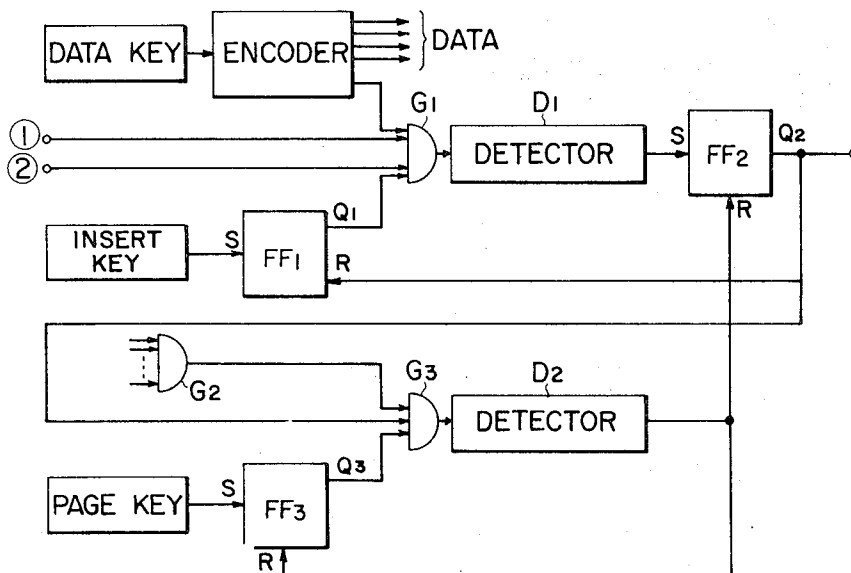


FIG. 15

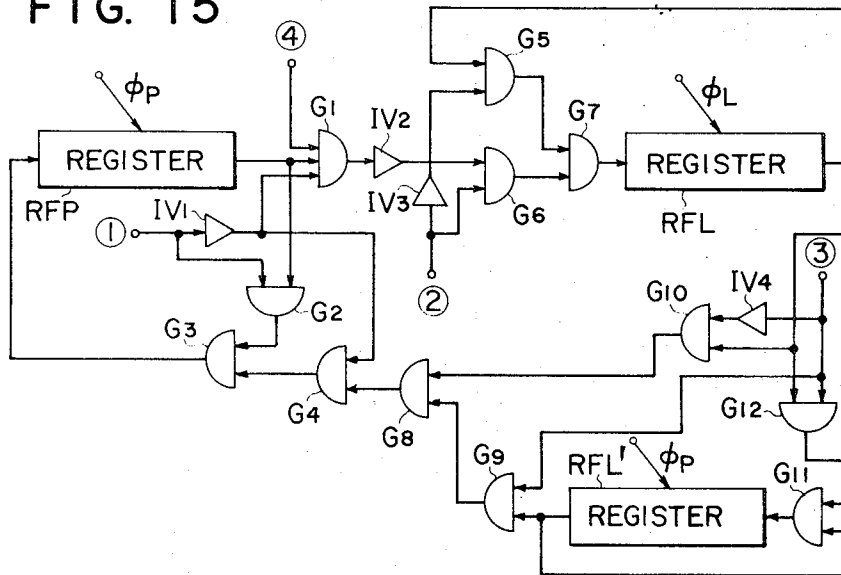


FIG. 16a

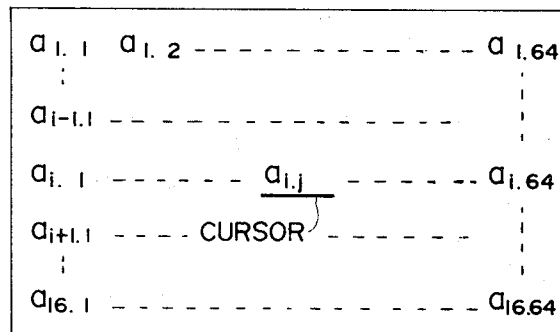


FIG. 16b

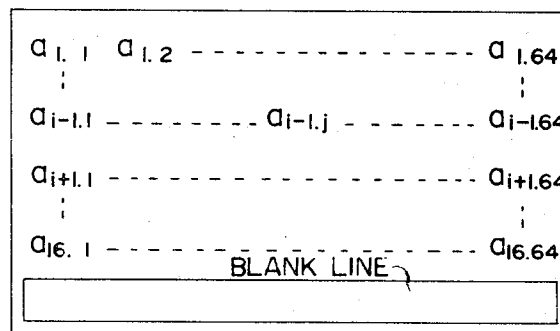


FIG. 17

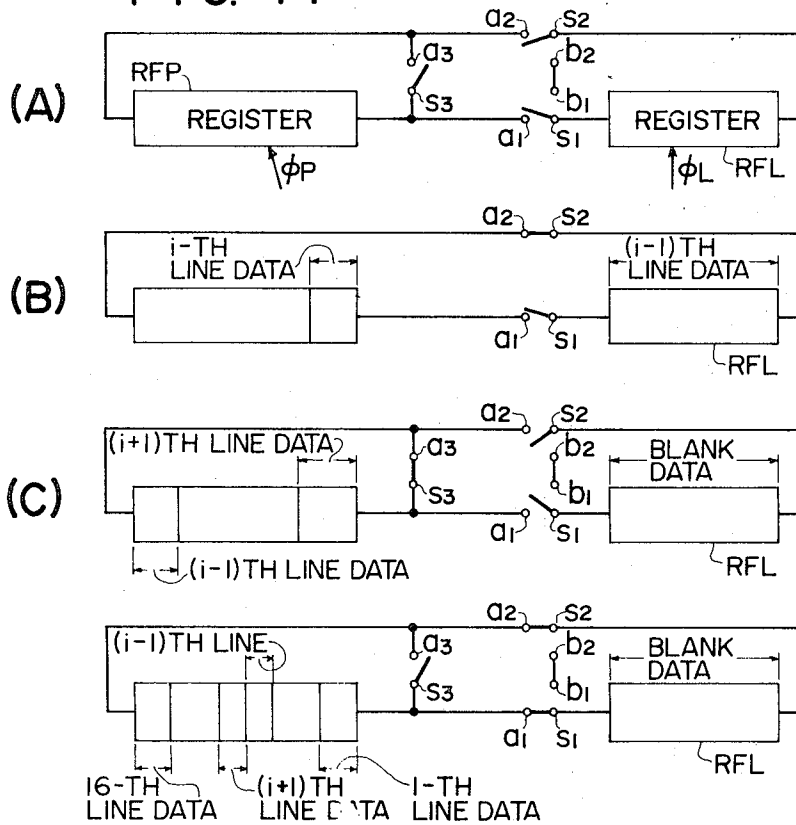


FIG. 18

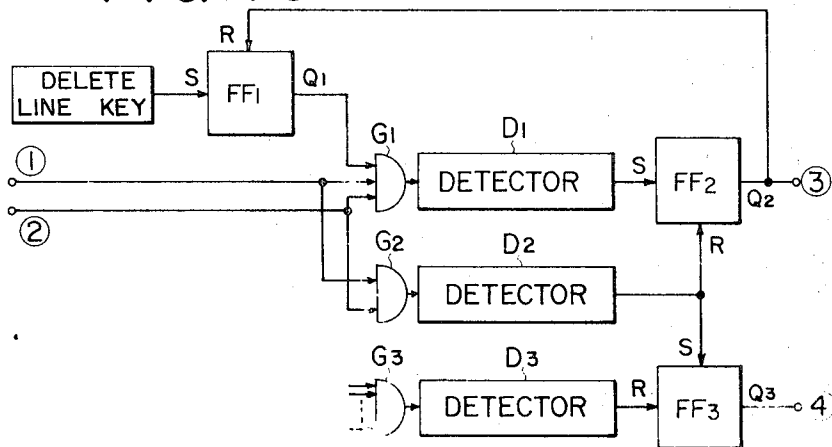
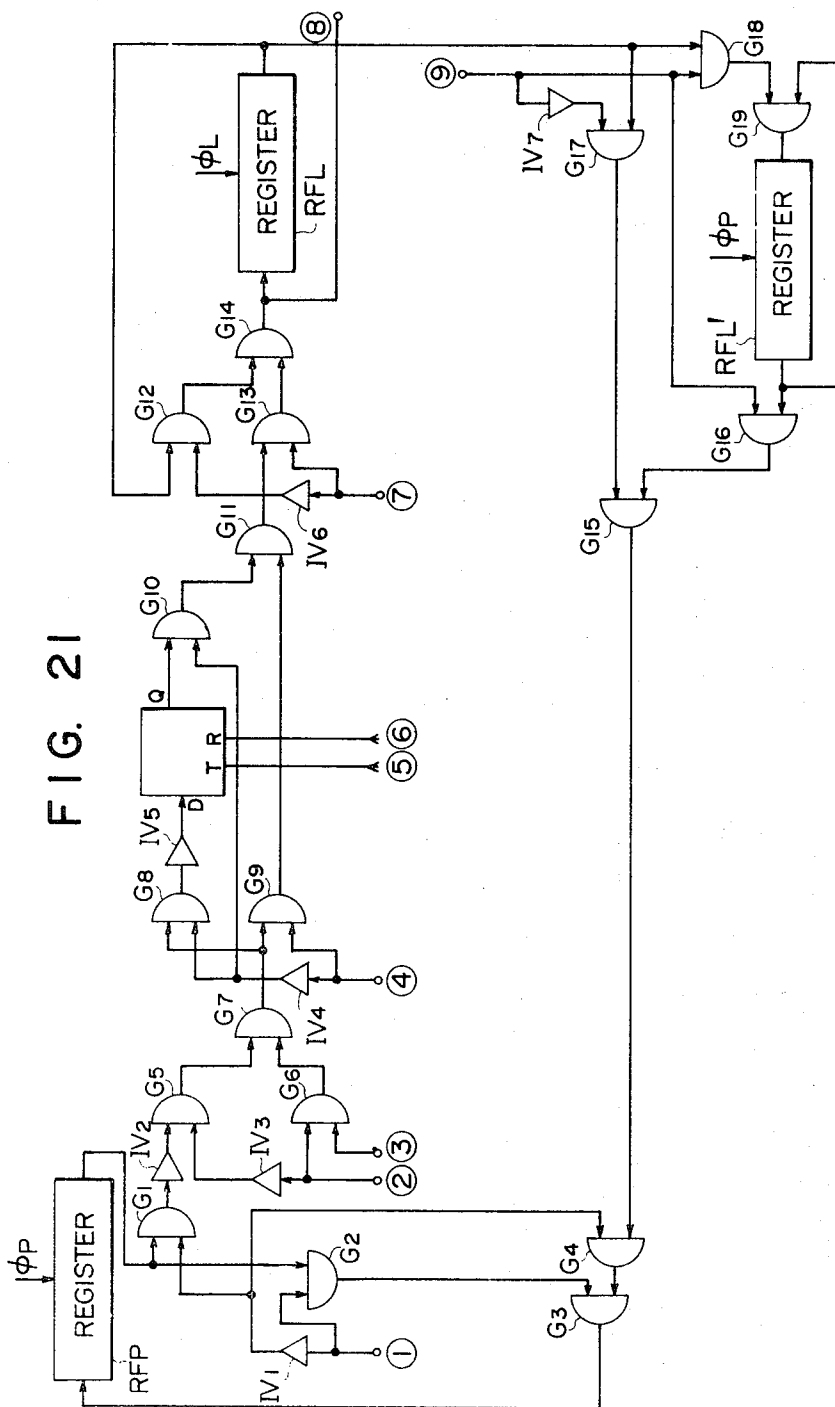


FIG. 21



CHARACTER DISPLAY SYSTEM

This invention relates to a character display system and more particularly to a character display system capable of arbitrarily changing the arrangement of the displayed characters.

In a character display unit, characters are displayed in the image plane of a cathode ray tube. It is desired that displayed characters can be erased or amended according to necessity through a key board, etc. In systems for displaying characters in a display unit employing raster scanning such as a usual commercial television receiver on the basis of data supplied in the form of digital signals, it is also desired to arbitrarily change the arrangement of displayed characters.

An object of this invention is to provide a character display system for displaying $M \times N$ characters in a display surface comprising: a first memory for storing $(M - 1) \times N$ characters including a plurality of refreshing memories each of which has at least $(M - 1) \times N$ bits; a second memory for storing N characters including a plurality of refreshing memories each of which has at least N bits; a circuit for repeatedly reading out the memory stored in said second memory for a predetermined number of times; a display unit for displaying said read-out information as characters; and means for connecting said first and said second memory and transferring the stored character information in a predetermined order, thereby displaying $M \times N$ characters in the form of M rows and N columns in the display surface of said display unit.

According to an embodiment of this invention, there is provided a character display system capable of deleting an arbitrary character in the display surface designated by an operator and forming a corresponding blank at the end of the line including the deleted character.

According to another embodiment of this invention, there is provided a character display system capable of deleting an arbitrary character in the display surface designated by an operator and forming a corresponding blank at the end of the page including the deleted character.

According to another embodiment of this invention, there is provided a character display system capable of inserting a character at an arbitrary character position in the display surface designated by an operator and forming an additional character position at the end of the row including said character position.

According to another embodiment of this invention, there is provided a character display system capable of inserting a character at an arbitrary character position in the display surface designated by an operator and forming an additional character position at the end of the page including said character position.

According to another embodiment of this invention, there is provided a character display system capable of deleting the characters of an arbitrary row in the display surface designated by an operator and forming a corresponding blank line in the lowest row of the page including the deleted row.

According to another embodiment of this invention, there is provided a character display system capable of inserting character positions of one row in an arbitrary row in the display surface designated by an operator and deleting the forced-out lowest row from the display surface.

Description will now be made on the preferred embodiments in connection with the accompanying drawings in which:

FIG. 1 is a block diagram of a basic character display unit;

FIG. 2 illustrates an example of character display in a display unit;

FIG. 3 shows the relation among the signals on lines X and Y and the horizontal synchronizing signal in the circuit of FIG. 1;

FIG. 4 shows an embodiment of a refreshing memory according to the invention;

FIG. 5 shows signal waveforms at various points of the memory of FIG. 4;

FIGS. 6a and 6b illustrate the process of character deletion on the display surface;

FIG. 7 illustrates the process of said character deletion in the circuit structure;

FIGS. 8a and 8b are a circuit diagram for generating control signal and the timing chart of various signals for achieving the character deletion according to this invention;

FIGS. 9a and 9b illustrates the movement of a blank generated by a character deletion on a display surface;

FIG. 10 illustrates in circuit structure how the movement of a blank as shown in FIG. 9 can be achieved;

FIG. 11 is a block diagram of a control signal generating circuit for achieving the character deletion as shown in FIGS. 9a and 9b;

FIG. 12 shows in electrical circuit how a character is inserted;

FIG. 13 is a block diagram of a control signal generating circuit for achieving the operation shown in FIG. 12 according to this invention;

FIG. 14 is a block diagram of a control signal generating circuit for achieving the function of disposing the excess character forced out by a character insertion at the end of the page according to this invention;

FIG. 15 is a block diagram of an embodiment of a refreshing memory circuit according to this invention;

FIGS. 16a and 16b illustrate how a row is deleted in a display surface;

FIG. 17 illustrates in block circuit diagram how the function illustrated in FIG. 16 can be achieved;

FIG. 18 is a block diagram of a control signal generating circuit for achieving the function of FIG. 17 according to this invention;

FIG. 19 illustrates in block circuit diagram how a row of characters can be inserted;

FIG. 20 is a block diagram of a control signal generating circuit for achieving the function of FIG. 19 according to the invention; and

FIG. 21 is a block diagram of an embodiment of a refreshing memory according to this invention.

A basic character display system is shown in FIG. 1 in which a character is expressed in digital signals of six bits and supplied parallelly. These digital signals are once stored in a refreshing memory and recirculated in a certain relation with the synchronizing signal for scanning a display device in which raster scanning is carried out, so as to give refreshing effect. Character signals corresponding to these digital signals can be generated by applying these data to a character generator and display is carried out in a cathode ray tube (CRT) at such a scanning speed that a displayed character does not flicker. In a typical raster system, 64

characters are contained in one line (or row) and 16 lines are displayed in a image plane (or plate), as is shown in FIG. 2.

When a key top in a key board 100 is depressed, coded signals of six bits corresponding to a character designated by the depressed key top are generated at terminals $\alpha_1, \alpha_2, \dots, \alpha_6$. A portion circled in a dotted line is a refreshing memory 101 in which six unit refreshing memories are parallelly disposed corresponding to said six bits coded system. The contents of these six refreshing memories recirculate in synchronism with a clock pulse applied at a terminal P. This refreshing memory will be described in more detail. It is assumed here that in a raster scanned display device, seven horizontal scanning lines are used for achieving a character display of one line (row), one scan is used for the interval between the characters and the cursor, and one is used for the interval between the cursor and the next line, thereby ten horizontal scanning lines being used to display one display line or row. For the display of the first line in FIG. 2 ($a_{1,1}, a_{1,2}, \dots, a_{1,64}$), the coded signals for this line should at least synchronously recirculate with the horizontal scanning signal for at least seven horizontal scanning periods. In FIG. 1, refresh memories RFL 1 to RFL 6 are of said kind of refresh memories and should have a memory capacity of 64 bits for each to express 64 characters in one line as is the case with the display shown in FIG. 2. On the completion of the display of the first line, the data contents of the first line stored in RFL 1 to RFL 6 are sent and stored in RFP 1 to RFP 6, and the data for the second line are transferred from RFP 1 to RFP 6 to RFL 1 to RFL 6, respectively. The above procedure is repeated for each time. As is clear from the above, the refreshing memories RFP 1 to RFP 6 should have a memory capacity of $64 \times (16 - 1) = 960$ bits for each and the combination of refresh memories RFP i and RFL i should have a bit capacity of $64 \times 16 = 1024$ bits equal to the number of characters in one image plane (page). In the following description, it is assumed that the data transfer from RFP 1 to RFP 6 to RFL 1 to RFL 6 is done in such horizontal scanning period that precedes the first horizontal scanning period for displaying characters, i.e., the period before that of the uppermost scanning signal for displaying characters, (which is expressed as the 0-th scanning period). Gate circuits CG 1 to CG 6 change the data transfer loop in said refreshing memories. In the series of RFP 1 and RFL 1, during the first to the ninth horizontal scanning periods of one line display the data in RFP 1 are held stationary and the data in RFL 1 are recirculated in the loop formed by RFL 1 - terminal A1 - CG 1 - RFL 1. In the 0-th horizontal scanning period, the data transfer path becomes RFL 1 - terminal A1 - CG 1 - RFP 1 - IG 1 - RFL 1. Thus, the data of 64 bits in RFL 1 are transferred to RFP 1 and another data of 64 bits for the next line are transferred from RFP 1 to RFL 1. Signals on lines X and Y control the change of this data transfer path. The signal on the line X has a value in 0-th horizontal scanning period and changes the data transfer path into RFL 1 - CG 1 - RFP 1 - RFL 1, whereas the signal on the line Y has a value in the first to the ninth horizontal scanning period and changes the data transfer path into RFL 1 - CG 1 - RFL 1. The relation of these signals is illustrated in FIG. 3. Input gates IG 1 to IG 6 are used only when the output of the key board 100 is to be written in the refreshing memory and otherwise only trans-

mit the signals on points C1 to C6 to points D1 to D6, respectively. An address counter ADCL counts the clock pulses supplied to the terminal P of the refreshing memory and thus counts the number of characters displayed in a line. This counting is done in perfect synchronism with the recirculation of the data in the refreshing memories RFL 1 to RFL 6. Thereby, the content of the counter ADCL at an arbitrary moment designates the address of the data supplied from the refreshing memory RFL 1 to RFL 6 at that moment and the position of the character displayed in the image plane. The counter ADCL is formed of six flip-flops, etc. ($2^6 = 64$ bits), while six-bit outputs are supplied to a coincidence detector CC 1 and a carry signal is supplied to a line M. This carry signal is generated once per one horizontal scanning period. Another address counter ADCP counts the number of displayed lines in the image plane (cf. FIG. 2). A carry control gate AG transmits a carry signal from ADCL only when a signal exists on the line X. Namely, the carry pulse from ADCL can be transmitted to ADCP only when data are transferred from RFL to RFP. The address counter ADCP is formed of four flip-flops ($2^4 = 16$ bits), while its four-bit outputs are supplied to a coincidence detector CC 2. The content of ADCP at an arbitrary moment designates the line position in the image plane of the data in the refreshing memory RFL at that moment. Thus, the position of the displayed data in the display surface at an arbitrary moment can be designated by the contents of ADCL and ADCP.

Cursor counters CCL and CCP are supplied inputs from the key board 100 through a line J, where an arbitrary signal is supplied from the key board by an operator. A carry signal from CCL is transmitted to CCP through a line J. The cursor counters CCL and CCP have the same capacity as ADCL and ADCP, respectively. The coincidence detector CC 1 compares the contents of counters ADCL and CCL and generates an output on a line H1 when the two contents coincide each other. Another coincidence detector CC 2 compares the contents of the counters ADCP and CCP and supplies an output on the line H2 when the two coincide each other. An AND gate CD detects the AND-condition of the signals on the lines H1 and H2 and generates an output signal on line K when the AND-condition is satisfied. This signal is applied to CRT in the ninth horizontal scanning period of each line display and displayed as a cursor as shown in FIG. 2. Namely, this signal is supplied when the data in the address designated by cursor counters CCL and CCP are supplied from RFL 1 to RFL 6. Due to this signal, particular data in the refreshing memory can be selectively treated. Further, the signal on a line K is applied to an input pulse generator IPG together with a strobe signal and generates a control signal on a line L for the input gates IG 1 to IG 6 when new data is to be supplied from the key board, etc., to the position designated by a cursor.

A control block CB is formed of control circuits for relatedly functioning the various parts of the system. The control block CB generates a clock signal for driving said refreshing memory and said address counter ADCL through a line Z in a certain relation with the vertical and horizontal synchronizing signals generated on lines V_s and H_s . Further, the block CB generates said signals for changing the data transfer path in the refreshing memory on the lines X and Y in a certain re-

lation with signals on the lines V_s and H_s as is shown in FIG. 3. Through a line N , a signal for selecting the display line is supplied to the character generator.

The character generator receives the coded signal stored in the refreshing memory and generates corresponding character signals on a video line. When such character signals are applied to a cathode ray tube CRT together with the synchronizing signals, characters are displayed in CRT as is shown in FIGS. 2a and 2b.

In the foregoing, description is made on one system for displaying characters in a display unit of raster scanning type. Now, the details of this invention will be described on the basis of the structure of FIG. 1. For the simplicity of description, description will be made on one-bit system of, for example, RFP 1 - IG 1 - RFL 1 - CG 1 - RFP 1 in the refreshing memory and on the case where shift registers are used as the recirculating memories RFP 1 and RFL 1.

FIG. 4 shows an embodiment of a refreshing memory circuit for achieving the arbitrary deletion or insertion of a character. A register RFP is a shift register of 960 bits and another register RFL is a shift register of 64 bits. They are supplied with clock pulses ϕ_p and ϕ_L at terminals 8 and 9. These clock pulses are in a predetermined relation with the horizontal scanning signal as is shown in FIG. 5. Namely, ϕ_L is composed of 64 pulses for each horizontal scanning period and is generated in every horizontal scanning period, whereas ϕ_p is composed of 64 pulses for one horizontal scanning period and is generated only in the 0-th horizontal scanning period of each line display period. In the 0-th horizontal scanning period, the data for one line stored in RFL is sent to and stored in RFP and the data for the next line is sent from RFP to RFL. In the figure, IV 1 to IV 5 are signal inversion circuits, $G_1, G_2, G_4, G_5, G_6, G_8$ and G_9 are NAND gates, G_3, G_7 and G_{10} are NOR gates, and FF is a flip-flop of D-type.

In FIG. 6, deletion of a character is illustrated in the image plane of CRT, in which FIG. 6a shows a display before deletion, characters $a_{1,1}$ to $a_{16,64}$ express the display position and a character a_{ij} to be deleted is designated by a cursor. FIG. 6b shows the display after the deletion of the character a_{ij} , and the blank due to the deletion of a_{ij} is generated at the end of the i -th line. FIG. 7 schematically illustrates the operation of the refreshing memory of FIG. 4. In the figure, S_1, S_2 , and S_3 represent switching circuits. In the normal operation, the refreshing memories RFP and RFL act as follows. In the first to the ninth horizontal scanning periods (1H to 9H in FIG. 5) the data in RFL is recirculated once for one horizontal scanning period in the loop of RFL - S_2 - b_2 - RFL. In these periods, no clock pulse is applied to RFP as can be seen from FIG. 5 and the content of RFP is not moved. In the 0-th horizontal scanning period (0H in FIG. 5), the data in RFP and RFL are shifted by one line (64 bits) in the loop of RFP - S_1 - b_1 - b_3 - S_3 - RFL - S_2 - a_2 - RFP. In stages B to E of FIG. 7, the deletion of a character a_{ij} in the position of the i -th line and j -th column (i, j) will be described. Here, the flip-flop FF works for the insertion or deletion of a character. Stage B of FIG. 7 shows the state in which the data of the ($i-1$)-th line have been displayed and the data of the i -th line is to be transferred from RFP to RFL. It is assumed here that the character in the i -th line and j -th column is to be deleted. Just before the transfer of the data of the i -th line from RFP to RFL, the flip-flop FF is inserted in the data transfer

loop by changing the switches. The timing of this switching can be easily detected by the leading edge of the signal on line H_2 (cf. FIG. 1) (when the content of the cursor counter CCP is set i). At this moment, the content of FF is set 0. Stage C of FIG. 7 shows the state at such moment when the data transfer of the i -th line has started and the j -th data has entered FF. At this moment, the data transfer loop from RFP to RFL is changed from that of stage C of FIG. 7 to that of stage D of FIG. 7 and the flip-flop FF is separated from the loop. The timing of this switching is obtained by the signal on the line K (FIG. 1) (when the content of the cursor counter CCL is set j). Continuing the data transfer of the i -th line from RFP to RFL, when the 64-th clock pulse has been supplied, the content 0 which was set in FF at the initial moment is now set at the head of the i -th line and the data of the i -th line except the j -th column element are succeedingly set in RFL as is shown in stage E of FIG. 7. To see this process in the image plane of FIG. 6b, a blank is formed at the place of a_{i1} and the characters a_{i1} to a_{i64} succeed. When the transfer loop is switched to that of stage F of FIG. 7 and one more clock pulse (i.e., the 65th clock pulse from the start of the data transfer of the i -th line) is applied to RFL but not to ADCL, the content 0 at the head of the shift register RFL is sent now to the end of the register as shown in stage F of FIG. 7. In the image plane, the blank is formed at the place of $a_{i,64}$ as shown in FIG. 6b. The above procedure will be described in more detail referring to FIGS. 4 and 8. In FIG. 4, a signal of 0 level is usually applied to a terminal 1, a gate G_1 is in on state and a gate G_2 is in off state. On a terminal 6, a signal as shown in waveform D of FIG. 5 is applied to control the data transfer between RFP and RFL as is described above. The signal applied to a terminal 3 and the signal ϕ_L applied to RFL work to achieve the deletion of a desired character. FIGS. 8a and 8b show a circuit diagram for generating the control signal to be applied to the terminal 3 and the waveforms and timing relation of the signals at the various points of the memory circuit. In FIG. 8a, a delete key shown in a block is one of the function keys provided on the key board. First, a cursor is set at a character position a_{ij} which is to be deleted by an operator (cf. FIG. 6a) and the delete key is depressed. Then, this information is sent to and stored in a flip-flop FF 1 and the output terminal Q_1 of FF 1 becomes high as shown by the waveform E of FIG. 8b. To a terminal 1, a signal representing that the address counter ADCP (FIG. 1) designates the i -th line is applied from the line H_2 (as shown by the waveform B of FIG. 8b). To a terminal 3, a signal representing that the content of the address counter ADCL designates the 0-th horizontal scanning period 0H is applied from the line H_1 (as shown by the waveform A of FIG. 8b). The AND condition of these signals is detected in the gate circuit G_1 . A leading edge detector indicated by D detects the leading edge of the output signal of the gate G_1 and thereby sets the flip-flop FF2. The coincidence signal representing that the content of the address counter ADCP is i and that of the address counter ADCL is j is supplied from the line K (FIG. 1) to a terminal 2 (waveform C of FIG. 8b), and resets the flip-flops FF 1 and FF 2. Thus, a signal (waveform F of FIG. 8b) which takes high level at the starting point of the i -th line and then takes low level by the i -th line and j -th column clock pulse can be provided at a terminal 4 of FIG. 8a. This signal is applied to the terminal 3 of

FIG. 4 and the data transfer path is changed as is described in connection with FIG. 7. In FIG. 8a, a flip-flop FF 3 detects the initiation of the line to be deleted (the 0-th scanning period of the line) and controls the clock generator by its output to generate 65 clock pulses only in such a line. These 65 clock pulses are applied only to RFL but in this normal condition 64 clock pulses are applied to the address counter (in FIG. 4, ADCL, ADCP).

Then the positioning of the blank generated by the deletion of a character will be described. FIGS. 9a and 9b show how the blank due to the deletion of a character is positioned at the end of a page; in which FIG. 9a shows a display example before the deletion and FIG. 9b shows the display after a character a_{ij} is deleted. In FIG. 9b, the blank due to the deletion of a_{ij} is formed at the end of the page and the characters $a_{i,j+1}$ to $a_{16,64}$ are shifted by one character position respectively. This can be achieved by the switching operation as shown in FIG. 10. Stage A of FIG. 10 shows the state when the data of the 16-th line has been displayed on the image plane and the data transfer between RFP and RFL is to begin. In this state, if no deletion is carried out, the data are transferred through the loop of RFP - S_1 - b_1 - b_2 - S_2 - RFL - RFP. In the case of carrying out a deletion operation, a flip-flop is inserted in the transfer path just before the data of the first line are transferred from RFP to RFL as is shown in stage A of FIG. 10. This timing is detected by the content of the address counters shown in FIG. 1. The flip-flop takes the state 0 at the initial state. Data transfer is continued till the data of the i -th line and j -th column enter the flip-flop. When the data of the i -th line and j -th column have entered the flip-flop, said flip-flop is separated from the transfer path as is shown in stage B of FIG. 10. This timing can be detected in a similar manner as described in connection with FIG. 7. After one recirculation of the data in RFP and RFL, the data arrangement as shown in stage C of FIG. 10 can be achieved. In the display image plane of FIGS. 9a and 9b, a blank is formed at the position of $a_{1,1}$, the characters $a_{1,1}$ to $a_{i,j-1}$ are shifted backward by one character position, and the characters $a_{i,j+1}$ to $a_{16,64}$ occupy the original position. Thus, after the data of the 16-th line are transferred from RFP to RFL and if one more clock pulse (i.e., the 65-th clock pulse in the data transfer of the 16-th line) is added to ϕ_L and ϕ_R , the data in the shift registers RFP and RFL are shifted to the right side by one bit position, and thereby the blank 0 is placed at the end of the 16-th line. Thus, a display as shown in FIG. 9b can be achieved in which the blank due to the deletion of a character is placed at the end of the page.

FIG. 11 shows a circuit structure for generating the control signals for the above use. In FIG. 11, a page key and a delete key indicated in blocks are control keys on a keyboard (they may be replaced by other means according to the terminal devices). The page key is provided so as to distinguish the structure from that of FIG. 8a and may be dispensed with. Flip-flops FF 1 and FF 2 memorize the depression of said keys. A gate G_1 decodes the content of the address counter shown in FIG. 1 and generates an output when the address counter indicates the first line. A gate G_2 detects and AND condition of said three signals and generate an output designating the first line of the page in which the deletion of a character is desired. A leading edge detector D_1 is similar to D of FIG. 8a. Thus, a flip-flop FF 3

connected to D_1 is set at the beginning of the page. The signal of the i -th line and j -th column is supplied through a terminal 1 similar to the terminal 2 of FIG. 8a and resets FF 3. Thus, the flip-flop FF 3 generates a switching signal for the data transfer path on a terminal 3 which takes the high level at the beginning of the page and becomes of the low level at a_{ij} . This signal is applied to the terminal 3 of the circuit of FIG. 4. A gate G_3 decodes the content of the address counter and detects the last (16-th) line of the page. A detector D_2 has a similar structure as the detector D_1 , detects the trailing edge of the input signal, and resets FF 1, FF 2 and FF 4. The flip-flop FF 4 is set at the beginning of the page and reset at the end of the page, and stores the deletion order in this duration. The gate G_4 examines the AND condition of the output of FF 4, the output of G_3 representing the 16-th line and the 0-th horizontal scanning period supplied from the terminal 2, then sets FF 5, and controls the clock pulse generator to generate 65 pulses only in this occasion. In this way, the deletion of an arbitrary character and the disposal of the corresponding blank at the end of the page can be achieved.

Now, the insertion of an arbitrary character in an arbitrary position will be described. In the image plane, a character a_X is to be inserted at the position of $a_{i,j}$ from the key board, etc., characters $a_{i,j}$ to $a_{i,63}$ are to be shifted rightward by one character position, and the last character $a_{i,64}$ is to be forced out from the image plane. Circuit operation for achieving this function is schematically shown in FIG. 12. First, the character to be inserted is preliminarily set in the flip-flop between RFP and RFL. This character is expressed as X in FIG. 12. Data transfer from RFP to RFL is carried out normally until the data of the i -th line and j -th column at which X is to be inserted appears at the output terminal of RFP. On the appearance of the i -th line and j -th column data at the output terminal of RFP, the data transfer path is changed from the normal one shown in stage A of FIG. 12 into one shown in stage B of FIG. 12 so that said flip-flop (1 bit shift register) is inserted in the transfer path. In this manner, the data X follows the $(j-1)$ -th data and the j -th data follows thereafter. When the 64-th data has entered the flip-flop (at the 64-th clock pulse from the beginning of the i -th line transfer),

The transfer path is returned to the original one as shown in stage C of FIG. 12 to achieve the aforementioned operation. An embodiment of a signal generating circuit for achieving the operation shown in FIG. 12 is shown in FIG. 13. In FIG. 13, when a data key is depressed, the required data are encoded in an encoder and given at the output terminals. If an insert key is preliminarily depressed, these data are stored in the flip-flop shown in FIG. 4. To a terminal 1, the signal designating the i -th line and j -th column is applied from the line K of FIG. 1. To a terminal 2, the 0-th horizontal scanning signal is applied. The insert key is a control key provided on the key board. When this insert key is depressed, the flip-flop FF 1 is set to hold the inserting state. When a strobe signal from the encoder and said three signals are applied to a gate G_1 of FIG. 13 to satisfy the AND condition, an output is generated from G_1 . A leading edge detector D_1 similar to D of FIG. 8a generates an output on the entrance of an input and sets a flip-flop FF 2. When the output Q_2 of the flip-flop FF 2 becomes high, the flip-flop FF 1 is reset. From a terminal 3, a signal on the line H_2 of FIG. 1 designating

the i -th line is supplied. A trailing edge detector D_2 detects the trailing edge of the input signal and resets the flip-flop FF 2 by its output. Thus, such a signal is generated at an output terminal 4 which is set by the clock pulse of the i -th line and j -th column to become high and reset by the trailing edge of the i -th line to become low as is described in connection with FIG. 12. This signal is applied to the terminal 3 of FIG. 4 to achieve said operation.

Now, another embodiment will be described in which a character is inserted in an arbitrary position and an excess character due to this insertion is disposed at the end of the page. This process can be achieved in a similar manner to that of the foregoing embodiment. Namely, this can be achieved by inserting a flip-flop into the transfer path from RFP to RFL at the character position a_{ij} and disconnecting this flip-flop at the end of the page. A control signal generating circuit for achieving the above operation is shown in FIG. 14. In FIG. 14, similar signals as those applied to the terminals 1 and 2 of FIG. 13 are applied to terminals 1 and 2. A data key, an insert key, a gate G_1 , a detector D_1 , flip-flops FF 1 and FF 2 are also similar to those of FIG. 13. Here, only the reset signal for FF 2 differs from that of FIG. 13. A gate circuit G_2 decodes the content of the address counter and detects the 16-th line. A page key is a control key in the key board similar to the insert key. A flip-flop FF 3 memorizes the depression of the page key and is reset after the required process has finished. A gate G_3 examines the AND condition of the signal applied to the terminal 3 and said two signals and supplies an output to a trailing edge detector D_2 . Namely, in the 16-th line, when the page key is depressed, in the 0-th horizontal scanning period, and when editing process is under way, an output is generated from the gate G_3 . The trailing edge detector D_2 detects the trailing edge of the input pulse, i.e., detects the moment when the data of the last line of the page have been sent from RFP, and generates an output pulse to FF 2 and FF 3 to reset the same. Thus, such a signal is generated at the output terminal of FF 2 that becomes of high level at the position of a_{ij} and returns to low level at the end of the page. This signal is supplied to the terminal 3 of the refreshing memory of FIG. 4 to achieve the aforementioned operation.

Another embodiment in which one line is arbitrarily deleted or inserted will be described in connection with FIG. 15. FIG. 15 schematically shows the composition of a refreshing memory for achieving the above operation. This operation seen in the image plane is illustrated in FIGS. 16a and 16b. Namely, if a cursor is set under a character position a_{ij} and the deletion of one line is ordered, the i -th line is deleted from the image plane, the $(i + 1)$ -th to the last lines are shifted upward by one row and a blank line due to the deletion of the i -th line is formed in the lowest line of the page.

A circuit operation for achieving the above operation is illustrated in FIG. 17. Stage A of FIG. 17 represents the circuit of FIG. 15 except the loop of RFL'. In the usual display state as that of FIG. 16a, the contents of RFP and RFL are recirculated in the 0-th horizontal scanning period of each line display in the loop path of RFP - a_1 - S_1 - RFL - S_2 - a_2 - RFP. In the case of deleting the i -th line when the data of the i -th line have appeared at the output terminal of RFP (this timing can be detected by the leading edge of the signal on the line H_2 of FIG. 1), a switch S_1 is opened to disconnect the

connection between a_1 and S_1 . Holding this stage, the data of the i -th line are sent from RFP. In this operation, blank data (either of all 1 and all 0) are written in RFL and the data of the $(i - 1)$ -th line are transferred to RFP. When all of the data of the i -th line have been sent from RFP, a memory state as shown in stage C of FIG. 17 is realized. When the data of the i -th line have been sent out of RFP (this timing can be detected by the trailing edge of the signal on the line H_2 of FIG. 1), the switch of S_3 - a_3 is closed and that of S_1 - a_2 is opened to form the transfer path shown in stage C of FIG. 17. In this state, data transfer is carried out until the first datum of the data of the first line appears at the output terminal of RFP. On the appearance of the first line data at the output terminal of RFP (this timing is obtained by detecting the first line of the address counter in FIG. 1), the switch S_3 - a_3 is opened and the switches S_2 - a_2 and S_1 - a_1 are closed to realize the circuit of stage D of FIG. 17. As is apparent from the contents of RFP and RFL, the data of the i -th line are deleted and blank line data are formed at the last line of the page. A practical circuit for achieving the above operation is shown in FIG. 18. In FIG. 18, a delete line key is a control key provided in the key board and the depression of this key temporarily stores the order of line deletion in FF 1. A signal designating the i -th line is supplied from the line H_2 of FIG. 1 to a terminal 1, whereas the signal of the 0-th scanning period is applied from the line X of FIG. 1 to a terminal 2. AND gates G_1 and G_2 examine the AND condition of the respective inputs. Detectors D_1 and D_3 detect the leading edge of the respective inputs and a detector D_2 detects the trailing edge of the input pulse. Thus, the output of D_1 represents the leading edge of the i -th line and the output of D_2 represents the trailing edge of the i -th line. A gate G_3 decodes the content of the address counter of FIG. 1 and detects the first line. Thus, the output of the leading edge detector D_3 represents the initiation of a page. By set-reset controlling the flip-flops FF 2 and FF 3 with these signals, that signal is provided at the terminal 3 which becomes of high level at the leading edge of the i -th line and becomes of low level at the trailing edge of the i -th line, whereas that signal is provided at the terminal 4 which becomes of high level at the trailing edge of the i -th line and becomes of low level at the beginning of the page. This signal on the terminal 3 is reversed in polarity and applied to the terminal 4 of FIG. 15 and the signal on the terminal 4 of FIG. 18 is applied to the terminal 1 of FIG. 15 to achieve the aforementioned operation. This system is featured by the fact that no modulation is made on the clock signals for RFP and RFL.

Now, another embodiment in which a line can be arbitrarily inserted and then a forced out line (the last line in the page) is deleted from the image plane will be described. Here, it is assumed that in an image plane as that of FIG. 16a a blank line is to be inserted at the position of the i -th line, the lines succeeding the i -th line are to be shifted downward by one line for each and the lowest, 16-th line is to be deleted from the image plane.

This function can be achieved by the circuit operation shown in FIG. 19. In FIG. 19, shift registers RFL and RFL' have the same bit number and are applied with a clock signal ϕ_p . In the normal display state, the data in the refreshing memory are transferred in the 0-th horizontal scanning period through the path of RFP

- $a_1 - S_1 - RFL - S_2 - a_2 - a_3 - S_3 - RFP$. A blank line data (all 1 or all 0) are preliminarily set in RFL' . After the data of the i -th line have been transferred from RFP to RFL , switches $S_2 - b_2$ and $S_3 - b_3$ are closed to insert RFL' in the data transfer path. This timing can be detected by the trailing edge of the signal on the line H_2 . This state is shown in stage B of FIG. 19. When the first line data have entered RFL and the 16-th line data have entered RFL' , switches $S_2 - a_2$ and $S_3 - a_3$ are closed to disconnect RFL' from the transfer path, as is shown in stage C of FIG. 19. Thus, the timing of this switching is obtained by the trailing edge of the first line from the address counter.

A practical circuit arrangement for achieving the above operation is shown in FIG. 20. An insert key is a control key on the key board and the depression of this key temporarily stores the order of line insertion in FF 1. A signal designating the i -th line is supplied from the line H_2 of FIG. 1 through a terminal 1, and the signal of the 0-th horizontal scanning period in each line display is supplied through the terminal 2 from the line X of FIG. 1. A gate circuit G_1 examines the AND condition of these signals and supplies an output when the AND condition is satisfied. A detector D_1 detects the trailing edge of the input pulse. Thus, a flip-flop FF 2 generates that output signal which is set and becomes of high level when the data of the i -th line have been transferred from RFP to RFL . A gate G_3 decodes the content of the address counter and detects the first line. A gate G_2 examines the AND condition of this signal and the signal of the 0-th horizontal scanning period. A detector D_2 detects the trailing edge of the output pulse of the gate G_2 and resets FF 2. Namely, D_2 resets FF 2 at the moment when the first line data have been transferred to RFL , as is shown in stage C of FIG. 19. Thus, a signal as described in connection with FIG. 19 can be obtained at the terminal 3. This signal is applied to the terminal 3 of FIG. 15 to provide the desired operation.

When the memory arrangements of FIG. 4 and FIG. 15 are combined, there is provided a memory arrangement as shown in FIG. 21 which can achieve all the functions as described hereinbefore.

What we claim is:

1. In a character display system having a scanning cathode ray tube display for displaying $M \times N$ characters and a plurality of storage units coupled with said cathode ray tube display for storing characters to be displayed, the improvement including an editing apparatus for inserting and removing characters to and from said storage units, comprising: first memory means for storing $(M - 1) \times N$ bits of information; second memory means for storing N bits of information; a first data transfer path coupling said first and second

memory means together; third memory means for storing a single bit of information; first switching means for switching said third memory means into and out of said first data transfer path in a predetermined manner; fourth memory means for storing N bits of information; second switching means for switching said fourth memory means into and out of said first data transfer path in a predetermined manner; a second, recirculation, data transfer path for transferring data from the output of said first memory means to the input of said first memory means; third switch-

ing means for switching the output of said first memory means between said first and second data transfer paths in a predetermined manner; means generating an external clock signal having a predetermined timing relationship with a scan control signal of said scanning cathode ray tube display; means coupling said clock signal generating means to said first, second and third switching means, respectively, to control the circulation of information stored in said memories in synchronization with said external clock signal; an address counter coupled to said external clock signal generating means during a normal character display for monitoring the address of $M \times N$ bits of information; means for detecting the first and last information bits in a given data display row and the first and last information bits in a given data display page in accordance with the content of said address counter, the output of said detecting means being coupled to at least one of said switching means to switch at least one of said memory means between said first and second data transfer paths; a cursor counter having the same capacity as said address counter and including means coupled to said address counter to arbitrarily set the contents of said address counter by an external control signal; and control means applying an additional clock signal to at least a portion of said memories to control insertion and deletion of information stored in said memories.

2. A character display system according to claim 1 capable of deleting a character, further comprising:

means for inserting said third memory in the transfer path between said first and said second memory before the transfer of the information of that row from said first to said second memory which includes a character to be deleted; and means for detecting the entry of the character information to be deleted into said third memory, then disconnecting said third memory from the transfer path between said first and second memories, and directly connecting said first and said second memories.

3. A character display system according to claim 2, wherein said control means comprises: means for applying to said second memory only one more clock pulse than those of a regular number after the complete character information of that row in which a desired character is deleted has been transferred to said second memory, whereby the blank generated by the deletion of a character is disposed at the end of said row.

4. A character display system according to claim 2, wherein said control means comprises: means for applying one more clock pulse than those of a regular number to said first and said second memories after the complete character information of the M th row of a display image in which a desired character is deleted has been transferred to said second memory, whereby the blank generated by the deletion of a character is disposed at the end of the image plane.

5. A character display system according to claim 1, capable of inserting a character at an arbitrary position, further comprising: means supplying the character information to be inserted to said third memory for storing the supplied information of one character bit; and wherein said first switching means includes means for inserting said third memory in the first data transfer path from the first to the second memory during the time that information of that line which includes the

portion for insertion is transferred and immediately before the character information at said insertion position is transferred.

6. A character display system according to claim 5, capable of deleting the character at the end of the line in which a character is inserted, further comprising:

means for disconnecting said third memory from said first transfer path after all bits but one of the character information of said line have been transferred out of said first memory.

7. A character display system according to claim 5, further comprising: means for disconnecting said third memory from said transfer path after all bits but one of the character information of the last row of a display image have been transferred out of said first memory, thereby the system being capable of deleting the last character of said display image.

8. A character display system according to claim 1, further comprising:

means for serially connecting said first and said second memories;

means coupled to said third switching means for switching said first memory from said first to said second data transfer path at the moment the character information of the row to be deleted is transferred to said second memory;

means for writing blank information into said second memory to erase the character information of the row to be deleted stored therein; and

means switching said first memory from said second back to said first data transfer path just before the character information of the next row after the deleted row is transferred from said first memory.

9. A character display system according to claim 1, said second switching means further comprising:

means for inserting said fourth memory in the data transfer path from said second to said first memory after the character information of a row in which a new line of character information is to be inserted is transferred from said first to said second memory; and

means for disconnecting said fourth memory from the transfer path from said second to said first memory at the moment when the character information of the first row is transferred to said second memory.

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