(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
21 September 2017 (21.09.2017)

WIPO | PCT

(10) International Publication Number
WO 2017/160235 A1

(51) International Patent Classification:
H01L 21/56 (2006.01) *H01L 25/00* (2006.01)
H01L 23/31 (2006.01) *H01L 23/538* (2006.01)

(21) International Application Number:
PCT/SG2017/050130

(22) International Filing Date:
16 March 2017 (16.03.2017)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10201602014P 16 March 2016 (16.03.2016) SG

(71) Applicant: **AGENCY FOR SCIENCE, TECHNOLOGY AND RESEARCH** [SG/SG]; 1 Fusionopolis Way, #20-10 Connexis North Tower, Singapore 138632 (SG).

(72) Inventors: **HO, David**; c/o Industry Development, Institute of Microelectronics, 2 Fusionopolis Way, #08-02 Innovis Tower, Singapore 138634 (SG). **RAO, Vempati Srinivasa**; c/o Industry Development, Institute of Microelectronics, 2 Fusionopolis Way, #08-02 Innovis Tower, Singapore 138634 (SG). **CHAI, Tai Chong**; c/o Industry Development, Institute of Microelectronics, 2 Fusionopolis Way, #08-02 Innovis Tower, Singapore 138634 (SG). **BHATTACHARYA, Surya**; c/o Industry Development, Institute of Microelectronics, 2 Fusionopolis Way, #08-02 Innovis Tower, Singapore 138634 (SG).

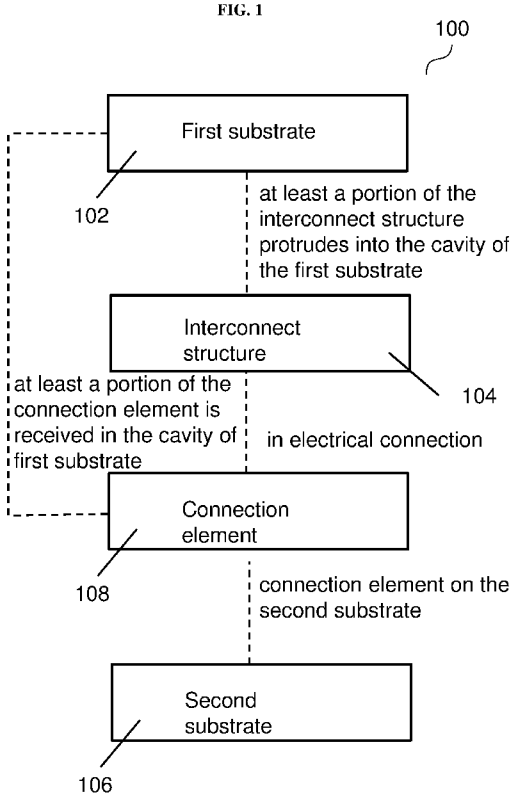
(74) Agent: **VIERING, JENTSCHURA & PARTNER LLP**; P.O. Box 1088, Rochor Post Office, Rochor Road, Singapore 911833 (SG).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

[Continued on next page]

(54) Title: ELECTRICAL CONNECTION STRUCTURE, SEMICONDUCTOR PACKAGE AND METHOD OF FORMING THE SAME

FIG. 1



(57) Abstract: Various embodiments may provide an electrical connection structure. The electrical connection structure may include a first substrate having a first surface defining a cavity, and an inner wall defining a via extending from the cavity. The electrical connection structure may also include an interconnect structure provided in the via so that at least a portion of the interconnect structure protrudes into the cavity. The electrical connection structure may further include a second substrate having a second surface facing the first surface. The electrical connection structure may additionally include a connection element on the second surface. At least a portion of the connection element may be received in the cavity so that the connection element is in electrical connection with the interconnect structure.

WO 2017/160235 A1

(84) **Designated States** *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

ELECTRICAL CONNECTION STRUCTURE, SEMICONDUCTOR PACKAGE AND METHOD OF FORMING THE SAME

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims the benefit of priority of Singapore application No. 10201602014P filed on March 16, 2016, the contents of it being hereby incorporated by reference in its entirety for all purposes.

TECHNICAL FIELD

[0002] Various aspects of this disclosure relate to electrical connection structures and/or methods of form electrical connection structures. Various aspects of this disclosure relate to semiconductor packages and/or methods of forming semiconductor packages.

BACKGROUND

[0003] Fan-out wafer level packaging is becoming more popular in recent years, due to low cost, good reliability and ease of multi-chips integration. Fan-out packages are widely adopted in mobile applications due to the low package profile because such packages do not involve the use of a ball grid array (BGA) substrate. First generation fan-out wafer level packages involve laterally connecting embedded chips using re-distribution layer (RDL) layers on the surrounding mold compound. Second generation and third generation of fan-out wafer level packages include vertical interconnects in the mold area for package on package (PoP) stacking application.

[0004] For mobile applications, the desirable package height should be lower than 1 mm. However, conventional PoP stacks are very high due to BGA substrate and thick solder balls used to connect top and bottom package. Fan-out wafer level packages have been effective in reducing the package height, but considerable efforts are required to further reduce the stacked package height.

SUMMARY

[0005] Various embodiments may provide an electrical connection structure. The electrical connection structure may include a first substrate having a first surface defining a cavity, and an inner wall defining a via extending from the cavity. The electrical connection

structure may also include an interconnect structure provided in the via so that at least a portion of the interconnect structure protrudes into the cavity. The electrical connection structure may further include a second substrate having a second surface facing the first surface. The electrical connection structure may additionally include a connection element on the second surface. At least a portion of the connection element may be received in the cavity so that the connection element is in electrical connection with the interconnect structure.

[0006] Various embodiments may provide a method of forming an electrical connection structure. The method may include providing a first substrate having a first surface. The method may also include forming a cavity on the first surface. The method may further include forming an inner wall defining a via extending from the cavity. The method may additionally include forming an interconnect structure in the via so that at least a portion of the interconnect structure protrudes into the cavity. The method may further include providing a second substrate having a second surface facing the first surface. The method may also include forming a connection element on the second surface. At least a portion of the connection element may be received in the cavity so that the connection element is in electrical connection with the interconnect structure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] The invention will be better understood with reference to the detailed description when considered in conjunction with the non-limiting examples and the accompanying drawings, in which:

FIG. 1 is a general illustration of an electrical connection structure according to various embodiments.

FIG. 2 shows a schematic of a method of forming an electrical connection structure according to various embodiments.

FIG. 3A is a cross-sectional schematic of a semiconductor package according to various embodiments.

FIG. 3B shows the electrical connection structure according to various embodiments.

FIG. 3C shows the electrical connection structure according to various other embodiments.

FIG. 3D shows the electrical connection structure including an interconnect finishing layer on the portion of the interconnect structure protruding into the cavity according to various embodiments.

FIG. 3E shows the electrical connection structure including a cavity finishing layer on at least a portion of the first surface defining the cavity according to various other embodiments.

FIG. 4 is a cross-sectional schematic of a solder joint connection of a conventional package on package (PoP) structure.

FIG. 5A is a cross-sectional schematic of an electrical connection structure according to various embodiments.

FIG. 5B is a cross-sectional schematic of an electrical connection structure according to various other embodiments.

FIG. 6A shows forming a sacrificial layer on or over a carrier according to various embodiments.

FIG. 6B shows forming of a first redistribution layer on or over the sacrificial layer according to various embodiments.

FIG. 6C shows forming one or more interconnect structures according to various embodiments.

FIG. 6D shows providing one or more semiconductor dice over the first redistribution layer 614 according to various embodiments.

FIG. 6E shows forming the first mold encapsulation structure according to various embodiments.

FIG. 6F shows forming cavities on the mold encapsulation structure according to various embodiments.

FIG. 6G shows removal of the carrier according to various embodiments.

FIG. 6H shows forming of a plurality of solder balls and the singulation of the molded structure according to various embodiments.

FIG. 6I shows forming a semiconductor package according to various embodiments.

DETAILED DESCRIPTION

[0008] The following detailed description refers to the accompanying drawings that show, by way of illustration, specific details and embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, and logical changes may be made without departing from the scope of the invention. The various

embodiments are not necessarily mutually exclusive, as some embodiments can be combined with one or more other embodiments to form new embodiments.

[0009] Embodiments described in the context of one of the methods or structures/packages are analogously valid for the other methods or structures/packages. Similarly, embodiments described in the context of a method are analogously valid for a structure/package, and vice versa.

[0010] Features that are described in the context of an embodiment may correspondingly be applicable to the same or similar features in the other embodiments. Features that are described in the context of an embodiment may correspondingly be applicable to the other embodiments, even if not explicitly described in these other embodiments. Furthermore, additions and/or combinations and/or alternatives as described for a feature in the context of an embodiment may correspondingly be applicable to the same or similar feature in the other embodiments.

[0011] The word "over" used with regards to a deposited material formed “over” a side or surface, may be used herein to mean that the deposited material may be formed "directly on”, e.g. in direct contact with, the implied side or surface. The word "over" used with regards to a deposited material formed “over” a side or surface, may also be used herein to mean that the deposited material may be formed "indirectly on” the implied side or surface with one or more additional layers being arranged between the implied side or surface and the deposited material. In other words, a first layer “over” a second layer may refer to the first layer directly on the second layer, or that the first layer and the second layer are separated by one or more intervening layers.

[0012] The structure/package as described herein may be operable in various orientations, and thus it should be understood that the terms “top”, “bottom”, etc., when used in the following description are used for convenience and to aid understanding of relative positions or directions, and not intended to limit the orientation of the structure/package.

[0013] In the context of various embodiments, the articles “a”, “an” and “the” as used with regard to a feature or element include a reference to one or more of the features or elements.

[0014] In the context of various embodiments, the term “about” or “approximately” as applied to a numeric value encompasses the exact value and a reasonable variance.

[0015] As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

[0016] For the sake of clarity and to avoid clutter, not all features in some of the figures have been labelled. Features which are similar to features that have already been labelled may not be labelled to improve clarity and to avoid clutter.

[0017] One area of improvement is to reduce solder ball interconnect height between the package top and the bottom package.

[0018] FIG. 1 is a general illustration of an electrical connection structure 100 according to various embodiments. The electrical connection structure 100 may include a first substrate 102 having a first surface defining a cavity, and an inner wall defining a via extending from the cavity. The electrical connection structure 100 may also include an interconnect structure 104 provided in the via so that at least a portion of the interconnect structure 104 protrudes into the cavity. The electrical connection structure 100 may further include a second substrate 106 having a second surface facing the first surface. The electrical connection structure 100 may additionally include a connection element 108 on the second surface. At least a portion of the connection element 108 may be received in the cavity so that the connection element 108 is in electrical connection with the interconnect structure 104.

[0019] In other words, the electrical connection structure 100 may include a first substrate 102 having a cavity containing an end portion of the interconnect structure 104, and a second substrate 106 with a connection element 108, which is received by the cavity of the first substrate 102 and which connects with the interconnect structure 104.

[0020] Various embodiments may mitigate or address the abovementioned problems. Various embodiments may reduce solder ball interconnect height between the package top and the bottom package.

[0021] In various embodiments, the cavity may be a hemispherical cavity. The hemispherical cavity may be of a perfect hemisphere or may not be of a perfect hemisphere. For instance, the depth of the hemispherical cavity may be slightly greater or slightly smaller than a lateral radius of the hemispherical cavity. The imperfect hemispherical shape may arise due to the fabrication process. In various embodiments, the cavity may be of any other suitable shape.

[0022] The first surface may include a substantially planar first portion, and a second portion defining the cavity. The second portion may adjoin the first portion, and the first

portion and the second portion to define a continuous surface, i.e. the first surface. The second portion may be concave to define the hemispherical cavity.

[0023] The first substrate 102 may include or may be a mold encapsulation structure. The cavity and the via may be defined in the mold encapsulation structure.

[0024] In various embodiments, the interconnect structure 104 may extend vertically into the cavity. The interconnect structure 104 may be electrically conductive. The interconnect structure 104 may be a pillar or a wire. The interconnect structure 104 may include an electrically conductive material, for instance a metal such as copper.

[0025] The connection element 108 may include or be solder.

[0026] In various embodiments, the electrical connection structure 100 may further include an interconnect finishing layer on or over the portion of the interconnect structure 104 protruding into the cavity. The interconnect finishing layer may include one or more elements selected from a group consisting of copper, nickel, gold and palladium. The one or more elements may be deposited onto the portion of the interconnect structure protruding into the cavity via electroless plating and/or immersion plating. For instance, gold and/or palladium may be plated by immersion plating, while nickel and/or palladium may be deposited by electroless plating. The interconnect finishing layer may be an electroless nickel immersion gold (ENIG) plating or an electroless nickel immersion palladium immersion gold (ENIPIG) plating.

[0027] In various embodiments, the electrical connection structure 100 may further include a cavity finishing layer on at least a portion of the first surface defining the cavity. The cavity finishing layer may also extend to on or over the portion of the interconnect structure 104 protruding into the cavity. The cavity finishing layer may include one or more elements selected from a group consisting of copper, nickel, palladium and gold. The cavity finishing layer may include a seed layer in contact with the first substrate 102 (and the portion of the interconnect structure 104 protruding into the cavity) and an under bump metallization (UBM) on the seed layer.

[0028] The via may extend from the cavity to a further surface of the first substrate opposite the first surface. The via may be a through mold via. The interconnect structure 104 may also extend from within the cavity to at least the further surface.

[0029] The second substrate 106 may include a mold encapsulation structure. The second substrate 106 may also include a redistribution layer defining the second surface of the

second substrate 106. The redistribution layer may include an under bump metallization in contact with the connection element 108.

[0030] Various embodiments may provide a semiconductor package including the electrical connection structure 100 as described herein. The electrical connection structure 100 may include a first substrate 102 having a first surface defining a cavity, and an inner wall defining a via extending from the cavity. The electrical connection structure 100 may also include an interconnect structure 104 provided in the via so that at least a portion of the interconnect structure 104 protrudes into the cavity. The electrical connection structure 100 may further include a second substrate 106 having a second surface facing the first surface. The electrical connection structure 100 may additionally include a connection element 108 on the second surface. At least a portion of the connection element 108 may be received in the cavity so that the connection element 108 is in electrical connection with the interconnect structure 104.

[0031] The first substrate 102 may include a first semiconductor die. The first substrate 102 may further include a first redistribution layer in electrical connection with the first semiconductor die. The first substrate 102 may also include a first mold encapsulation structure on or over the first redistribution layer, the first mold encapsulation structure encapsulating the first semiconductor die. The first substrate 102 may further include a plurality of solder bumps in electrical connection with the first redistribution layer. The plurality of solder bumps and the first mold encapsulation structure may be on opposite sides of the first redistribution layer.

[0032] In the present context, a mold encapsulation structure encapsulating a semiconductor die may refer to the mold encapsulation structure in contact or covering the semiconductor die. In various embodiments, the mold encapsulating structure may partially, substantially, or completely cover or surround the semiconductor die.

[0033] The second substrate 106 may include a second semiconductor die. The second substrate 106 may further include a second redistribution layer in electrical connection with the second semiconductor die. The second substrate 106 may also include a second mold encapsulation structure on the second redistribution layer, the second mold encapsulation structure encapsulating the second semiconductor die.

[0034] In various embodiments, the first surface may be defined on the first mold encapsulation structure of the first substrate 102. The second surface may be defined on the second redistribution layer of the second substrate 106.

[0035] In various embodiments, the first redistribution layer may include one or more conductive elements. The interconnect structure 104 may be in electrical connection with the one or more conductive elements in the first redistribution layer. The interconnect structure 104 may extend from the first redistribution layer through the first mold encapsulation structure to the connection element 108. The connection element 108 may be in electrical connection with the second redistribution layer.

[0036] The semiconductor package may be a package on package (PoP) structure.

[0037] FIG. 2 shows a schematic 200 of a method of forming an electrical connection structure according to various embodiments. The method may include, in 202, providing a first substrate having a first surface. The method may also include, in 204, forming a cavity on the first surface. The method may further include, in 206, forming an inner wall defining a via extending from the cavity. The method may additionally include, in 208, forming an interconnect structure in the via so that at least a portion of the interconnect structure protrudes into the cavity. The method may further include, in 210, providing a second substrate having a second surface facing the first surface. The method may also include, in 212, forming a connection element on the second surface. At least a portion of the connection element may be received in the cavity so that the connection element is in electrical connection with the interconnect structure.

[0038] In other words, the method may include forming an electrical connection structure as described herein. The method may include creating a cavity in a first substrate, forming an interconnect structure in the first substrate so that the interconnect structure protrudes into the cavity. The method may also include forming a connection element on a second substrate, so that the cavity receives the connection element, and the connection element is in electrical connection with the interconnect structure.

[0039] The steps shown in FIG. 2 may not be in sequence. For instance, the cavity may be formed after forming the interconnect structure.

[0040] The cavity may be formed by laser machining. The cavity may be hemispherical.

[0041] The method may also include bringing the first substrate and the second substrate together so that at least the portion of the connection element is received in the cavity.

[0042] The method may further include forming an interconnect finishing layer on the portion of the interconnect structure protruding into the cavity by using one of electroless plating and immersion plating.

[0043] The method may additionally or alternatively include forming a cavity finishing layer on at least a portion of the first surface defining the cavity by using at least one of sputtering and plating (e.g. electroplating). In various embodiments, the method may include disposition or forming of a seed layer within the cavity and on the first surface, i.e. the second portion of the first surface defining the cavity. The method may further include forming of an underbump metallization (UBM) layer on the seed layer by electroplating.

[0044] Various embodiments may provide forming a semiconductor package as described herein. The semiconductor package may be a PoP structure.

[0045] The method may include forming a first redistribution layer (e.g. on or over a carrier). The method may include providing or forming a first semiconductor die on or over the first redistribution layer so that the first redistribution layer is in electrical connection with the first semiconductor die. The method may also include forming an interconnect structure so that the interconnect structure is in electrical connection with the first redistribution layer. The method may include forming a first mold encapsulation structure on or over the first redistribution layer, the first mold encapsulation structure encapsulating the first semiconductor die. The first mold encapsulation structure may further encapsulate or cover the first interconnect structure. The method may additionally include forming a cavity on the first substrate so that at least a portion of the first interconnect structure protrudes into the cavity. The method may also include separating a molded structure or wafer (including the first redistribution layer, the first semiconductor die, the first interconnect structure and the first mold encapsulation structure) from the carrier. The first redistribution layer, the first semiconductor die, and the first mold encapsulation structure may form or be comprised in the first substrate. The interconnect structure may be provided in a via defined in an inner wall of the first substrate, and a portion of the interconnect structure may protrude into the cavity.

[0046] The method may include forming a second redistribution layer (e.g. on or over another carrier). The method may include providing or forming a second semiconductor die on or over the second redistribution layer so that the second redistribution layer is in electrical connection with the second semiconductor die. The method may include forming a second

mold encapsulation structure on or over the second redistribution layer, the second mold encapsulation structure encapsulating the second semiconductor die. The method may also include separating a further molded structure or wafer (including the second redistribution layer, the second semiconductor die, and the second mold encapsulation structure) from the carrier. The method may additionally include forming the connection element, e.g. a solder ball, on the second redistribution structure. The connection element and the mold encapsulation structure may be on opposite sides of the redistribution layer. The connection element may be in electrical connection with the second redistribution structure. The second redistribution layer, the second semiconductor die, and the second mold encapsulation structure may be formed or may be comprised in the second substrate. The connection element may be on a surface of the second substrate.

[0047] The method may additionally include bringing the first substrate and the second substrate together so that at least a portion of the connection element is received in the cavity and the connection element is in electrical connection with the interconnect structure.

[0048] FIG. 3A is a cross-sectional schematic of a semiconductor package 310 according to various embodiments. The semiconductor 310 may be a package on package (PoP) structure, and may include a bottom package, and a top package over the bottom package. The semiconductor package 310 may be attached to a printed circuit board (PCB) 312.

[0049] The bottom package may include a first substrate 302. The first substrate 302 may include a first redistribution layer (RDL) 314, a first semiconductor die 316 (which may be referred to as integrated circuit (IC) chip), and the first mold encapsulation structure 318 (which may be referred to as mold). The first mold encapsulation structure 318 may include mold epoxy.

[0050] The fist redistribution layer 314 may include one or more metallizations, and one or more dielectric layers embedding or covering the one or more metallizations. The first semiconductor die 316 may be electrically connected to the first redistribution layer 314, i.e. the one or more metallization, via one or more one or more contact structures such as solder bumps 320. Solder bumps 322 may be formed on the redistribution layer 314. The solder bumps 322 may be attached to the PCB 312 and may provide electrical connection between the PCB 312 and the bottom package. Only two of the solder bumps 320 and three of the solder bumps 322 are labelled in FIG. 3A to avoid clutter and improve clarity. The first mold encapsulation structure 318 may encapsulate or surround the first semiconductor die 316 and

one or more interconnect structures 304, which may be referred to as through mold interconnects (TMIs).

[0051] The top package may be or may include a second substrate 306. The second substrate 306 may include the second redistribution layer (RDL) 324, the second semiconductor die 326 (which may be referred to as integrated circuit (IC) chip), and the second mold encapsulation structure 328 (which may be referred to as mold). The second mold encapsulation structure 328 may include mold epoxy.

[0052] Similar to the first redistribution layer 314, the second redistribution layer 324 may include one or more metallizations, and one or more dielectric layers embedding or covering the one or more metallizations. The second semiconductor die 326 may be electrically connected to the second redistribution layer 324, i.e. the one or more metallization, via one or more one or more contact structures such as solder bumps 330. Only two of the solder bumps 330 have been labelled in FIG. 3A to avoid clutter and improve clarity. The second mold encapsulation structure 328 may encapsulate or surround the second semiconductor die 326.

[0053] Connection elements 308 such as solder bumps may be formed on the second redistribution layer 324, and may be electrically connected to the second redistribution layer 324, i.e. the metallizations of the second redistribution layer 324. The connection elements 308 may be received in the cavities of the first substrate 302 or the bottom package, and may be in electrical connection with the one or more interconnect structures 304.

[0054] The first semiconductor chip 316, the second semiconductor chip 326, and the PCB 312 may be in electrical connection with one another via solder bumps 308, 320, 330, 322, metallizations in RDLs 314, 324, and the one or more interconnect structures 304.

[0055] The dashed box shown in FIG. 3A indicates an electrical connection structure 300 according to various embodiments.

[0056] FIG. 3B shows the electrical connection structure 300 according to various embodiments. FIG. 3C shows the electrical connection structure 300 according to various other embodiments. As shown in FIGS. 3B and 3C, the second redistribution layer 324 may include an under bump metallization (UBM) 324a, and the solder bump 308 may be on the under bump metallization 324a. The under bump metallization 324a may be on a dielectric layer 324b, but may be in electrical connection with other metallizations present in the second redistribution layer 324.

[0057] The solder bump 308 may be received in a hemispherical cavity defined by an inner wall of the first mold encapsulation structure 318. The first mold encapsulation structure 318 may be on the first redistribution layer 314, which may include metallization 314a and dielectric layer 314b.

[0058] FIG. 3B shows that the connection structure 304 may be a conductive pillar such as a copper pillar or a copper electro-plated pillar, while FIG. 3C shows that the connection structure 304 may be a conductive wire or wire-bond, such as a copper wire. The connection structure 304 may be in electrical connection with metallization 314a. As shown in FIGS. 3B, 3C, at least a portion of the connection structure 304 may protrude into the cavity. The connection structure 304 may form a metallic joint or intermetallic joint with the solder bump 308. The solder bump 308 may form the intermetallic joint with the exposed metal comprised in the connection structure 304 during assembly reflow process.

[0059] The conductive wire 304 shown in FIG. 3C may be metallically bonded on a wire-bondable surface such as a conductive pad 332a (e.g. aluminum pad with or without gold finish, or copper pad with or without gold finish) using wire ball bonding material 332a, with one end of the conductive wire 332a standing on the conductive pad 332a so that the conductive wire 304 is in a vertical position.

[0060] The solder bump 308 may fill in the hemispherical cavity and may reduce the package gap between the top package and the bottom package, hence decreasing the stacked package height. The hemispherical cavity may also prevent solder bridging of adjacent solder balls. Further, since the hemispherical cavity encloses the solder bump 308, the reliability of the joint between the solder bump 308 and the interconnect structure 304 may be improved. During thermal cycling, a solder crack that forms may be diverted to the protruding potion of the vertical interconnect 304 and may be impeded by the vertical interconnects. The interconnect structure 304 may include a material such as copper (Cu) that is harder than solder, which allows the interconnect structure 304 to impede the propagation of the crack.

[0061] In addition, as the embedded vertical interconnect structure 304 does not need to extend over the entire thickness of the mold epoxy, the process of fabricating the vertical interconnect 304 may also be less demanding.

[0062] FIG. 3D shows the electrical connection structure 300 including an interconnect finishing layer 334 on the portion of the interconnect structure 304 protruding into the cavity according to various embodiments. Nickel (Ni) and/or palladium (Pd) may be deposited over

the portion of the interconnect structure 304 by electroless plating, while palladium (Pd) and/or gold (Au) may be deposited over the portion of the interconnect structure 304 by immersion plating. The Pd metal and/or the Ni metal may act as a diffusion barrier to improve the solder joint reliability, while the Au metal may act as an oxidation protective layer to help improve solder wetting in assembly reflow process.

[0063] FIG. 3E shows the electrical connection structure 300 including a cavity finishing layer 336 on at least a portion of the first surface defining the cavity according to various other embodiments. A seed layer including nickel, palladium and/or gold may be sputtered onto the sidewall defining the cavity as well as onto the portion of the interconnect structure 304 protruding into the cavity. An under bump metallization (UBM) layer may also be formed on the seed layer and over the sidewall as well as the portion of the interconnect 304. The UBM layer may include copper, nickel, palladium, and/or gold. The cavity finishing layer 336 may include the seed layer and the UBM layer. The cavity finishing layer 336 may improve the solder joint reliability as the layer may remove or reduce gaps along the interfaces. There may be few or no gaps along the interface between the first mold encapsulation structure 318 and the UBM or the interface between the UBM and the solder bump 308 after reflow. The gap-less hemispherical solder interface may behave like an underfill encapsulation.

[0064] FIG. 4 is a cross-sectional schematic of a solder joint connection 400 of a conventional package on package (PoP) structure. The PoP structure may include a bottom package 402 including a vertical interconnect 404, and a top package 406 with solder bump 408. The bottom package 402 may also include a mold encapsulation structure 412a covering the vertical interconnect 404, and an under bump metallization 410a in electrical connection with the vertical interconnect 404. The top package 406 may include may also include a mold encapsulation structure 412b and an under bump metallization 410b.

[0065] There may be intermetallic compound (IMC) layers 414a, 414b formed between the solder bump 408 and the under bump metallizations 410a, 410b. Cracks may start at the brittle IMC layers 414a, 414b, and may propagate along the IMC layers 414a, 414b until the entire solder joint connection 400 breaks off or fails.

[0066] FIG. 5A is a cross-sectional schematic of an electrical connection structure 500 according to various embodiments. The electrical connection structure 500 may include a first substrate 502 or bottom package having a first surface defining a hemispherical cavity,

and an inner wall defining a via extending from the cavity. The cavity and via may be defined in a first mold encapsulation structure 518. The electrical connection structure 500 may also include an interconnect structure 504 provided in the via so that at least a portion of the interconnect structure 504 protrudes into the cavity. The electrical connection structure may further include an interconnect finishing layer 534 on the portion of the interconnect structure 504 protruding into the cavity.

[0067] The electrical connection structure 500 may further include a second substrate 506 having a second surface facing the first surface. The top package may be or may include the second substrate 506 The electrical connection structure 500 may additionally include a connection element 508 on the second surface. The second substrate 506 may include a under bump metallization 524a, and the second surface may be a surface of the under bump metallization 524a . The second substrate 506 may also include a dielectric layer 524b.

[0068] At least a portion of the connection element 508 may be received in the cavity so that the connection element 508 is in electrical connection with the interconnect structure 504. The interconnect finishing layer 534 may be electrically conductive.

[0069] A first intermetallic compound (IMC) layer 538a may be formed along an interface between the interconnect finishing layer 534 and the connection element 508. The layer 538a may be formed from materials comprised in the connection element 508, the interconnect finishing layer 534 and/or the interconnect structure 504. A second intermetallic compound (IMC) layer 538b may be formed along an interface between the under bump metallization 524a and the connection element 508. The layer 538b may be formed from materials comprised in the connection element 508 and the under bump metallization 524a.

[0070] Stress may be concentrated at the edge of the first IMC layer 538a and the crack path may start at the edge of layer 538 where the stress concentration may be the highest. The crack path may be stopped by the protruding portion of the interconnect structure 504.

[0071] The interconnect structure 504 may include copper (Cu) which is harder than solder or the IMC material, and may stop the crack from propagating through the solder joint, thus increasing solder joint reliability.

[0072] FIG. 5B is a cross-sectional schematic of an electrical connection structure 500 according to various other embodiments. Instead of the interconnect finishing layer 534, the electrical connection structure 500 may include a cavity finishing layer 536 on at least a portion of the first surface defining the cavity. The cavity finishing layer 536 may include an

under bump metallization (UBM). The cavity finishing layer 536 may also extend onto the protruding portion of the interconnect structure 504. The first intermetallic compound (IMC) layer 538a may be formed along an interface between the connection element 508 and the protruding portion of the interconnect structure 504 as well as the portion of the first surface defining the cavity. The IMC layer 538a may be formed from the connection layer 508, the cavity finishing layer 536, and/or the interconnect structure 504.

[0073] The crack may start at the edge of the first intermetallic compound (IMC) layer 538a where the stress concentration is the highest. The crack may propagate along the IMC layer 538a along the hemispherical cavity, and may be stopped by the interconnect structure 504. The cavity finishing layer 536 may include a diffusion barrier which retards the growth of the IMC layer 538a, which may further improve reliability.

[0074] FIGS. 6A-I show a method of forming a semiconductor package according to various embodiments. Hemispherical through mold interconnects may be formed in a fan-out wafer level package.

[0075] FIG. 6A shows forming a sacrificial layer 642 on or over a carrier 640 according to various embodiments. FIG. 6B shows forming of a first redistribution layer 614 on or over the sacrificial layer 642 according to various embodiments. Underbump (UBM) metallization may be formed on the sacrificial layer 642 using a semi-additive process. The remaining of the first redistribution layer 614 may be formed on or over the underbump metallization. The first redistribution layer 614 may include one or more layers of metallizations. The first redistribution layer 614 may further include one or more dielectric layers including a suitable dielectric material. The one or more layers of metallizations may be embedded or covered by the one or more dielectric layers.

[0076] FIG. 6C shows forming one or more interconnect structures 604 according to various embodiments. The one or more interconnect structures 604 may be formed on or over the first redistribution layer 614 so that the one or more interconnect structures 604 may extend vertically. The one or more interconnect structures 604 may be in electrical connection with the one or more layers of metallizations in the first redistribution layer 614. The one or more interconnects 604 may be copper (Cu) wires or copper pillars. The one or more interconnects 604 may connect a portion of the top UBM metallization of the first redistribution layer 614.

[0077] FIG. 6D shows providing one or more semiconductor dice 616 over the first redistribution layer 614 according to various embodiments. The one or more semiconductor dice 616 (e.g. integrated circuit (IC) chips) may be in electrically connected to the first redistribution layer 614, i.e. to the metallization layers of the first redistribution layer 614 via one or more solder bumps 620. The one or more solder bumps 620 may be reflowed to attach the one or more semiconductor dice 616 to the first redistribution layer 614.

[0078] FIG. 6E shows forming the first mold encapsulation structure 618 according to various embodiments. The first mold encapsulation structure 618 may cover or encapsulate the one or more semiconductor dice 616. The first mold encapsulation structure 618 may further cover or encapsulate the one or more interconnect structures 604. Forming the first mold encapsulation structure 618 may including depositing a mold epoxy compound on or over the first redistribution layer 614 in a wafer level molding process.

[0079] FIG. 6F shows forming cavities on the mold encapsulation structure 618 according to various embodiments. The cavities may be formed on the exposed surface of the mold encapsulation structure 618 by a suitable method such as laser machining, and may be hemispherical. Further, the formation of the cavities may expose the one or more interconnect structures 604 such that a portion of each of the one or more interconnect structures 604 protrudes into a respective cavity. In various embodiments, an interconnect finishing layer may be formed on the portion of the interconnect structure 604 protruding into the cavity, or/and a cavity finishing layer on at least a portion of the first surface, i.e. exposed surface, defining the cavity.

[0080] FIG. 6G shows removal of the carrier 640 according to various embodiments. The carrier 640 may be separated from a molded structure or reconstituted wafer including the first redistribution layer, 614, the one or more semiconductor dice 616 with the one or more solder bumps 620, the encapsulation structure 618, and the one or more interconnect structures 604. The carrier 640 may be separated from the molded structure by debonding of the sacrificial layer 642.

[0081] FIG. 6H shows forming of a plurality of solder balls 622 and the singulation of the molded structure according to various embodiments. The plurality of solder balls 622 may be attached to the UBMs of the redistribution layer 614 such that the solder balls 622 and the chips 616 are on opposing sides of the redistribution layer 614. The molded structure or the reconstituted wafer may be dice to form single packages 602.

[0082] FIG. 6I shows forming a semiconductor package 610 according to various embodiments. A singulated fan-out package 602 shown in FIG. 6H may be assembled onto a printed circuit board (PCB) 612 by reflowing the solder balls 622 to PCB pads. A top package 606 such as another fan-out wafer level package may be stacked above the singulated fan-out package 602. The one or more connection elements or solder balls 608 may be reflowed to the hemispherical cavities of the package 602. The one or more solder balls 608 may form intermetallic joints with the one or more interconnect structures 604 and/or the interconnect finishing layer and/or the cavity finishing layer. The top package 606 may include a second redistribution layer 624, a further semiconductor die 626 connected to the second redistribution layer 624 using one or more solder bumps 630. The further semiconductor die 626 may be encapsulated by a further encapsulation structure 628.

[0083] The semiconductor package 610 may be traced using surface electron microscopy (SEM) or cross-sectional electron microscopy.

[0084] Various embodiments may have improved ease of integration of vertical interconnects due to lower height of vertical interconnect (Cu pillar or Cu wire) fabrication. The vertical interconnects may be smaller than the thickness of the mold encapsulation structure. Various embodiments involving wire bonding and/or copper pillar process may have less stringent requirements and greater ease of scaling down.

[0085] Various embodiments may possess enhanced solder joint reliability due to cavity structure and protruding vertical interconnects. The solder crack path may be diverted to and may be impeded by the protruding vertical interconnect. The vertical interconnect may be Cu material which is mechanically harder than solder and may effectively stop the crack path.

[0086] Various embodiments may have a lower package-on-package (PoP) stack height, as the solder balls sit in the cavity. Various embodiments may seek to provide a PoP package including a through mold interconnect (TMI) based structure having a reduced stand-off height. In various embodiments, the gap between the top package and the bottom package may be reduced die to the accommodation of the solder balls of the top package into the hemispherical cavities of the bottom package. In various embodiments, the cavity housing may prevent or reduce solder bump bridging for finer bump pitch.

[0087] Various embodiments may not require additional fabrication of through silicon vias and /or embedding of PCB bars.

[0088] While the invention has been particularly shown and described with reference to specific embodiments, it should be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention as defined by the appended claims. The scope of the invention is thus indicated by the appended claims and all changes which come within the meaning and range of equivalency of the claims are therefore intended to be embraced.

CLAIMS

1. An electrical connection structure comprising:

a first substrate having a first surface defining a cavity, and an inner wall defining a via extending from the cavity;

an interconnect structure provided in the via so that at least a portion of the interconnect structure protrudes into the cavity;

a second substrate having a second surface facing the first surface; and

a connection element on the second surface;

wherein at least a portion of the connection element is received in the cavity so that the connection element is in electrical connection with the interconnect structure.

2. The electrical connection structure according to claim 1,

wherein the cavity is a hemispherical cavity.

3. The electrical connection structure according to claim 1,

wherein the first surface comprises a substantially planar first portion, and a second portion defining the cavity.

4. The electrical connection structure according to claim 1,

wherein the first substrate comprises a mold encapsulation structure; and

wherein the cavity and the via are defined in the mold encapsulation structure.

5. The electrical connection structure according to claim 1,

wherein the interconnect structure extends vertically into the cavity.

6. The electrical connection structure according to claim 1,

wherein the connection element comprises solder.

7. The electrical connection structure according to claim 1, further comprising:

an interconnect finishing layer on the portion of the interconnect structure protruding into the cavity.

8. The electrical connection structure according to claim 7,

wherein the interconnect finishing layer comprises one or more elements selected from a group consisting of copper, nickel, gold and palladium.

9. The electrical connection structure according to claim 1, further comprising:

a cavity finishing layer on at least a portion of the first surface defining the cavity.

10. The electrical connection structure according to claim 9,

wherein the cavity finishing layer comprises one or more elements selected from a group consisting of copper, nickel, palladium and gold.

11. The electrical connection structure according to claim 1,

wherein the via extends from the cavity to a further surface of the first substrate opposite the first surface.

12. The electrical connection structure according to claim 1,

wherein the second substrate comprises a redistribution layer defining the second surface.

13. The electrical connection structure according to claim 12,

wherein the second substrate comprises a mold encapsulation structure; and

wherein the redistribution layer is on the mold encapsulation structure.

14. A semiconductor package comprising an electrical connection structure, the electrical connection structure comprising:

a first substrate having a first surface defining a cavity, and an inner wall defining a via extending from the cavity;

an interconnect structure provided in the via so that at least a portion of the interconnect structure protrudes into the cavity;

a second substrate having a second surface facing the first surface; and

a connection element on the second surface;

wherein at least a portion of the connection element is received in the cavity so that the connection element is in electrical connection with the interconnect structure.

15. The semiconductor package according to claim 14,

wherein the first substrate comprises:

a first semiconductor die;

a first redistribution layer in electrical connection with the first semiconductor die; and

a first mold encapsulation structure on the first redistribution layer, the first mold encapsulation structure encapsulating the first semiconductor die; and

wherein the second substrate comprises:

a second semiconductor die;

a second redistribution layer in electrical connection with the second semiconductor die; and

a second mold encapsulation structure on the second redistribution layer, the second mold encapsulation structure encapsulating the second semiconductor die;

wherein the first surface is defined on the first mold encapsulation structure; and

wherein the second surface is defined on the second redistribution layer.

16. The semiconductor package according to claim 15,

wherein the first redistribution layer comprises one or more conductive elements;

wherein the interconnect structure is in electrical connection with the one or more conductive elements in the first redistribution layer;

wherein the interconnect structure extends from the first redistribution layer through the first mold encapsulation structure to the connection element; and

wherein the connection element is in electrical connection with the second redistribution layer.

17. A method of forming an electrical connection structure, the method comprising:

providing a first substrate having a first surface;

forming a cavity on the first surface;

forming an inner wall defining a via extending from the cavity;

forming an interconnect structure in the via so that at least a portion of the interconnect structure protrudes into the cavity;

providing a second substrate having a second surface facing the first surface; and

forming a connection element on the second surface;

wherein at least a portion of the connection element is received in the cavity so that the connection element is in electrical connection with the interconnect structure.

18. The method according to claim 17,

wherein the cavity is formed after forming the interconnect structure.

19. The method according to claim 17, further comprising:

forming an interconnect finishing layer on the portion of the interconnect structure protruding into the cavity by using one of electroless plating and immersion plating.

20. The method according to claim 17, further comprising:

forming a cavity finishing layer on at least a portion of the first surface defining the cavity by using at least one of sputtering and plating.

FIG. 1

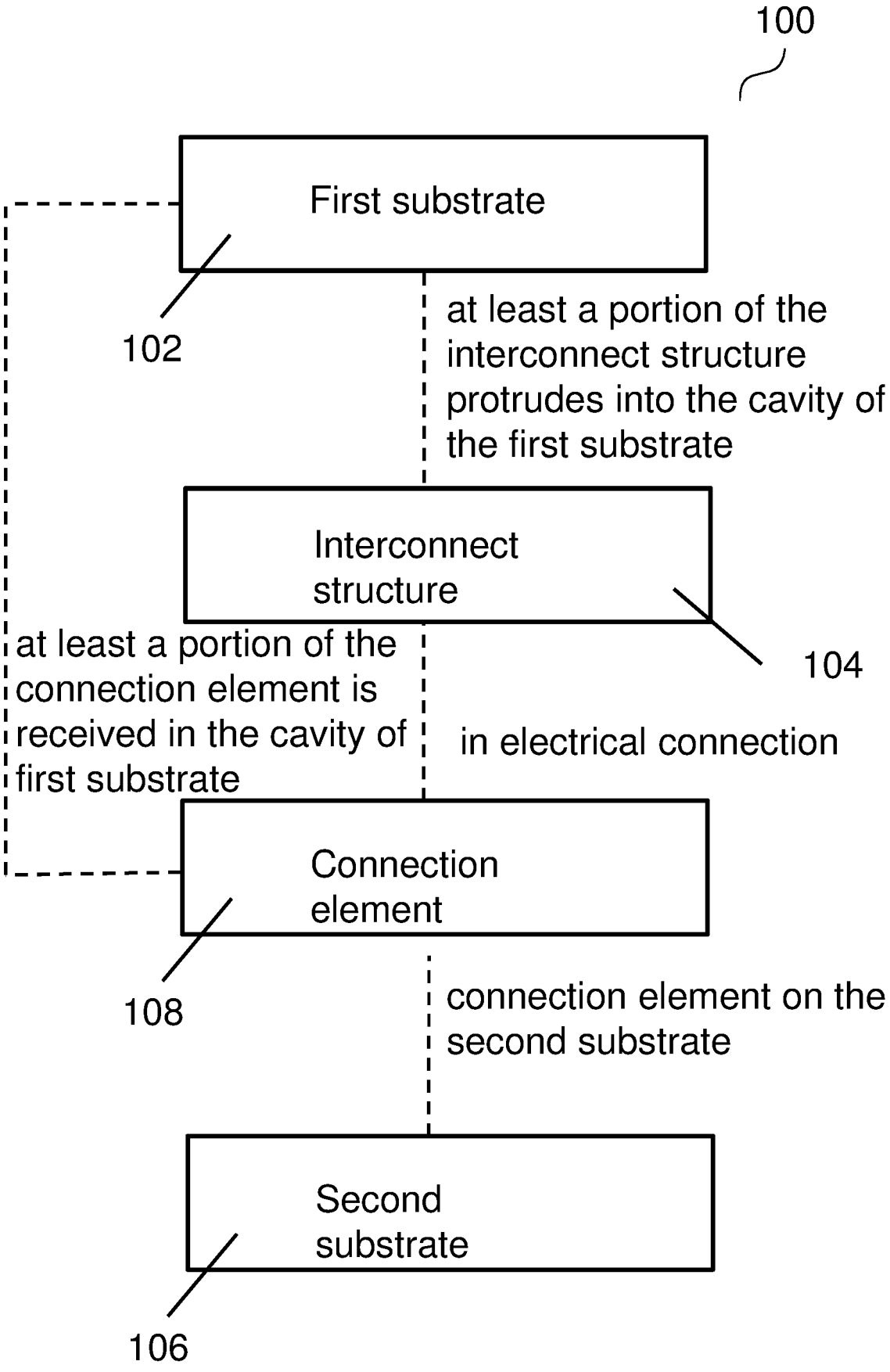
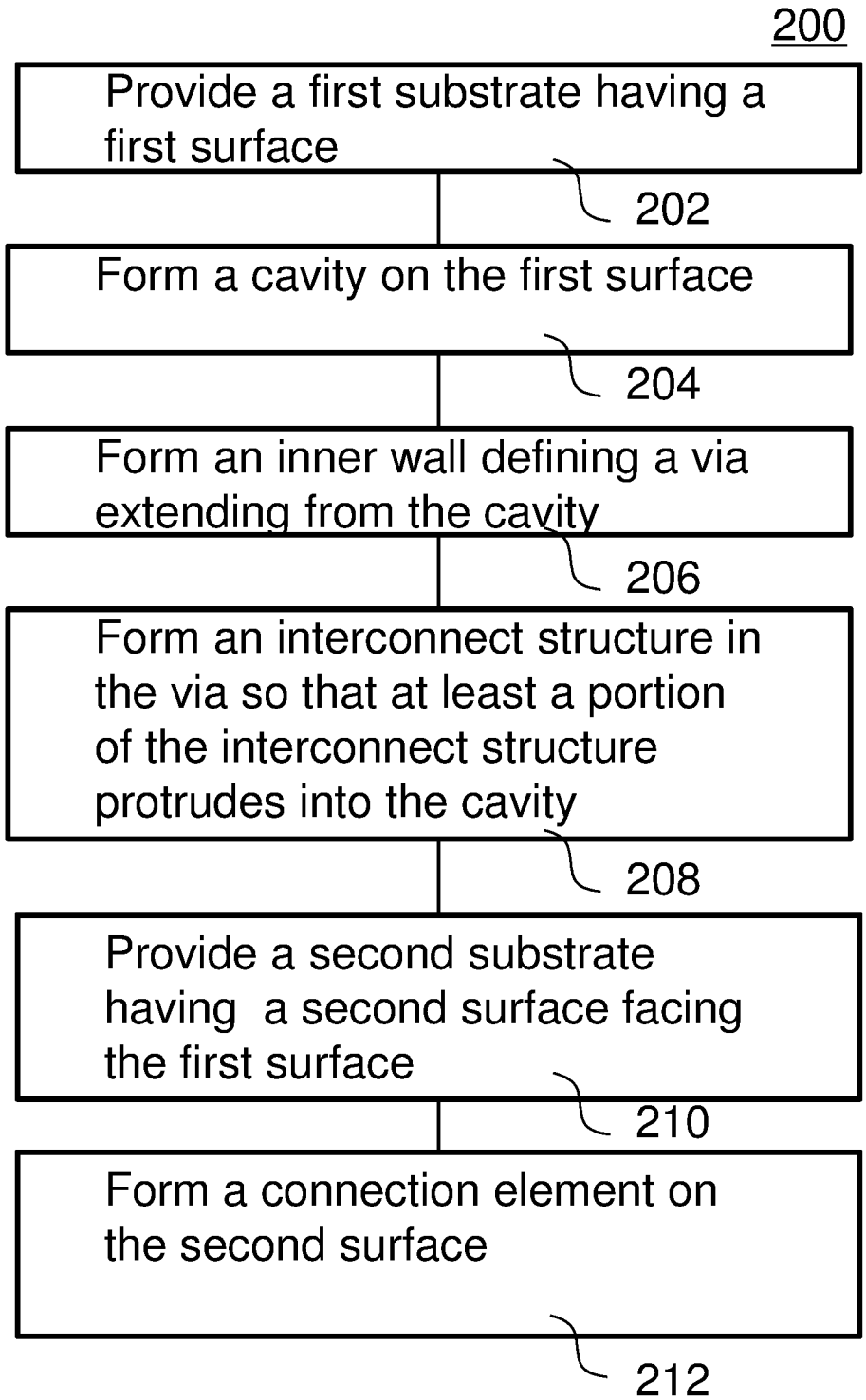

100
First substrate
102
at least a portion of the interconnect structure protrudes into the cavity of the first substrate
Interconnect structure
104
at least a portion of the connection element is received in the cavity of first substrate
in electrical connection
Connection element
108
connection element on the second substrate
Second substrate
106

FIG. 2


200
Provide a first substrate having a first surface
202
Form a cavity on the first surface
204
Form an inner wall defining a via extending from the cavity
206
Form an interconnect structure in the via so that at least a portion of the interconnect structure protrudes into the cavity
208
Provide a second substrate having a second surface facing the first surface
210
Form a connection element on the second surface
212

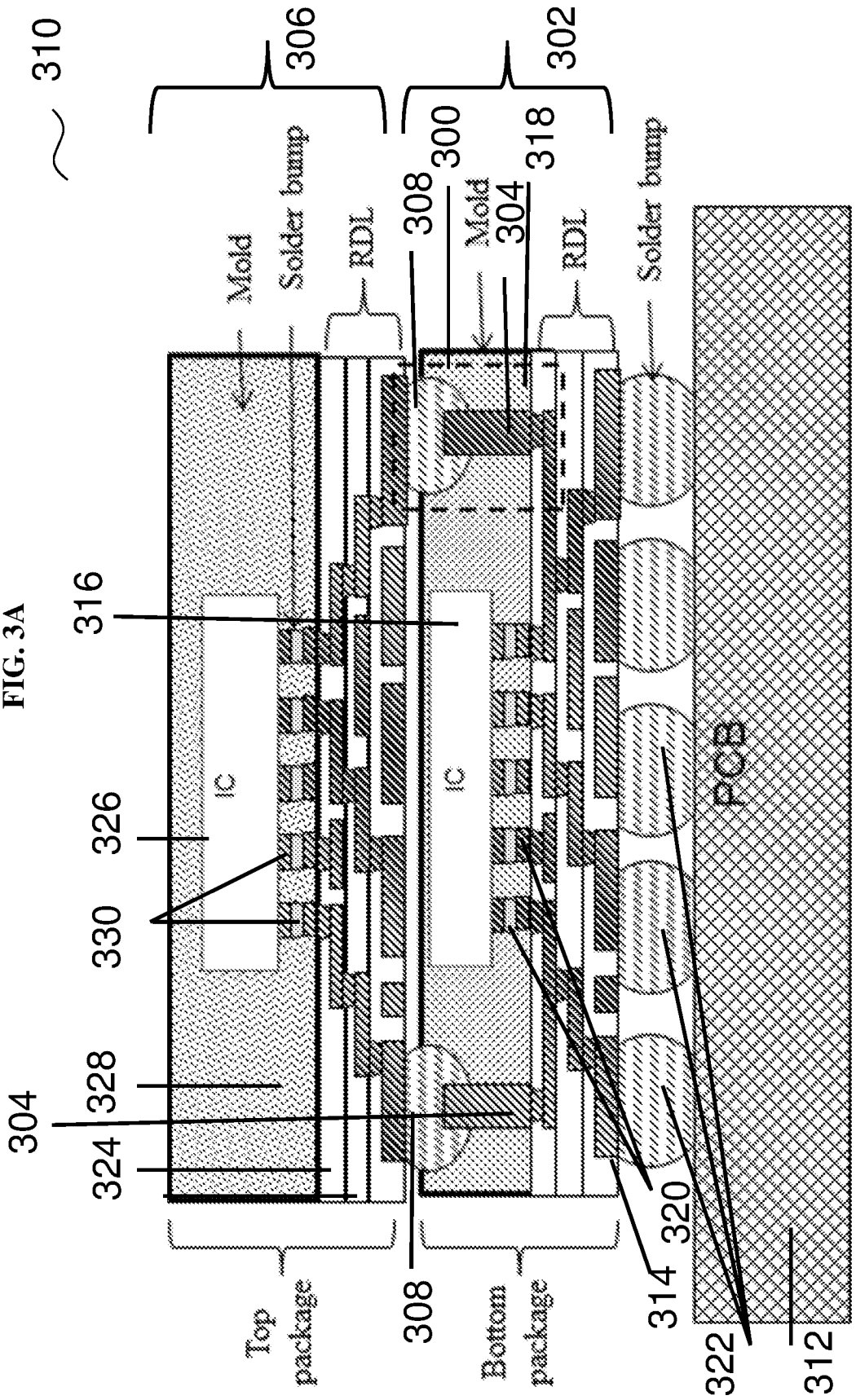

310
306
302
Mold
Solder bump
RDL
308
300
Mold
304
318
RDL
Solder bump
316
326
330
328
304
324
IC
IC
PCB
Top package
308
Bottom package
314
320
322
312

FIG. 3A

FIG. 3B

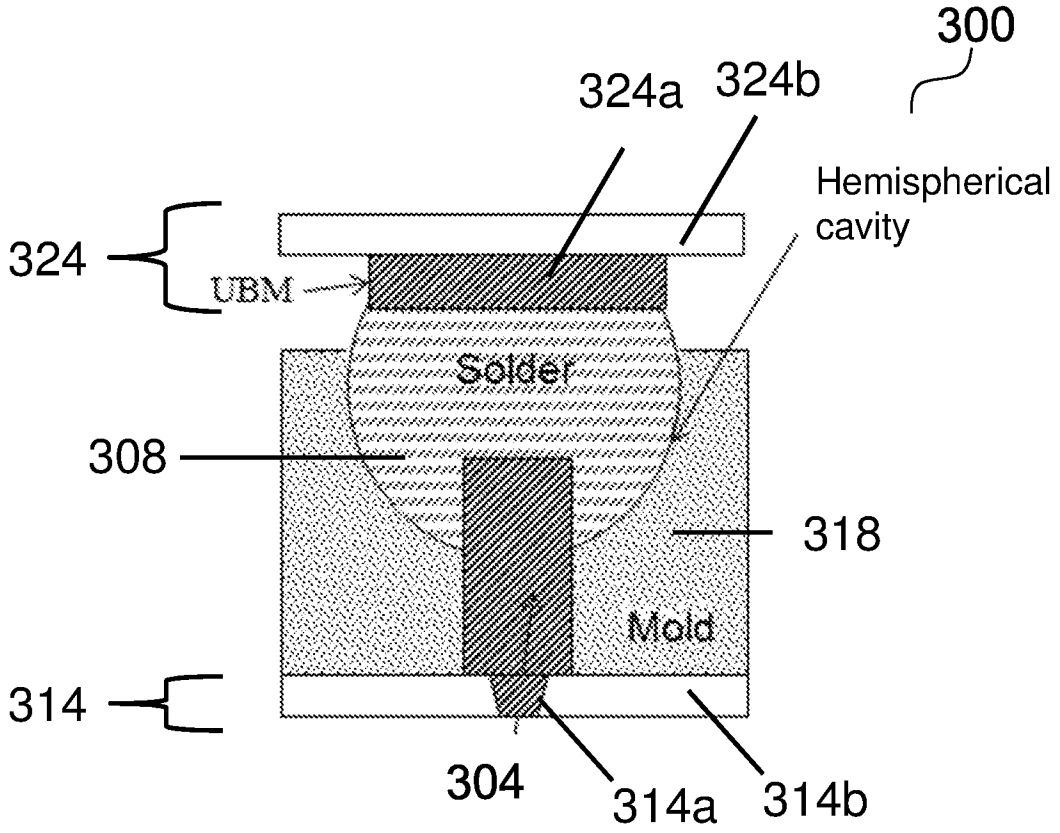

300
324a
324b
Hemispherical cavity
324
UBM
Solder
308
318
Mold
314
304
314a
314b

FIG. 3C

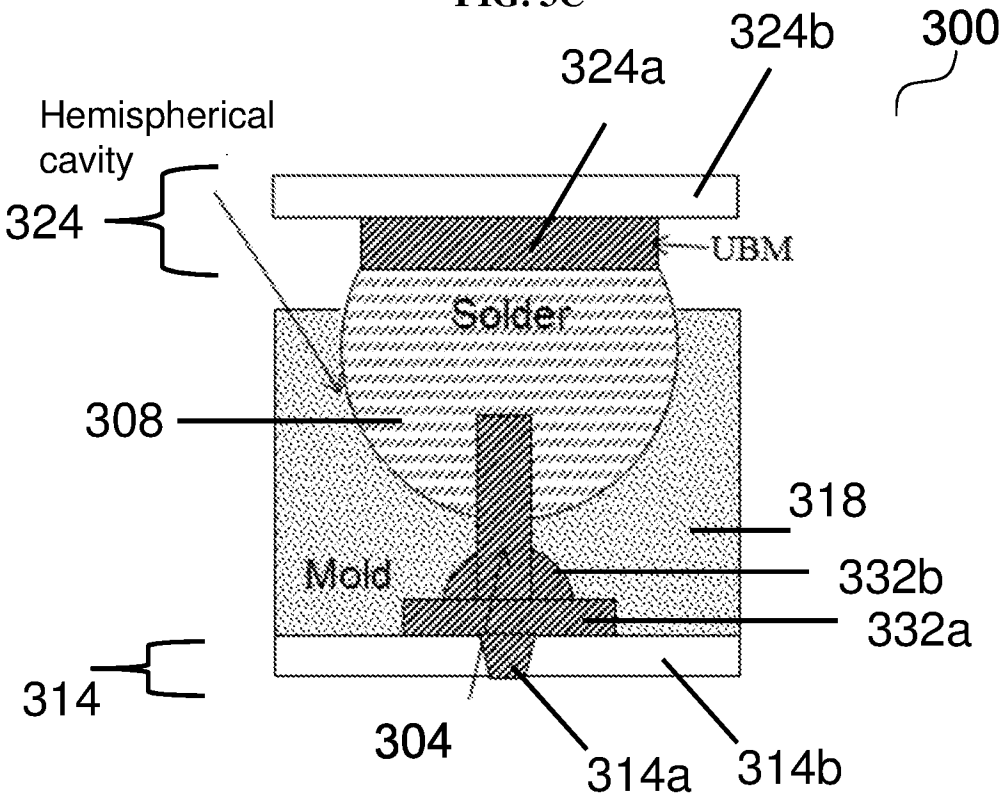

300
324b
324a
Hemispherical cavity
324
UBM
Solder
308
318
Mold
332b
332a
314
304
314a
314b

FIG. 3D

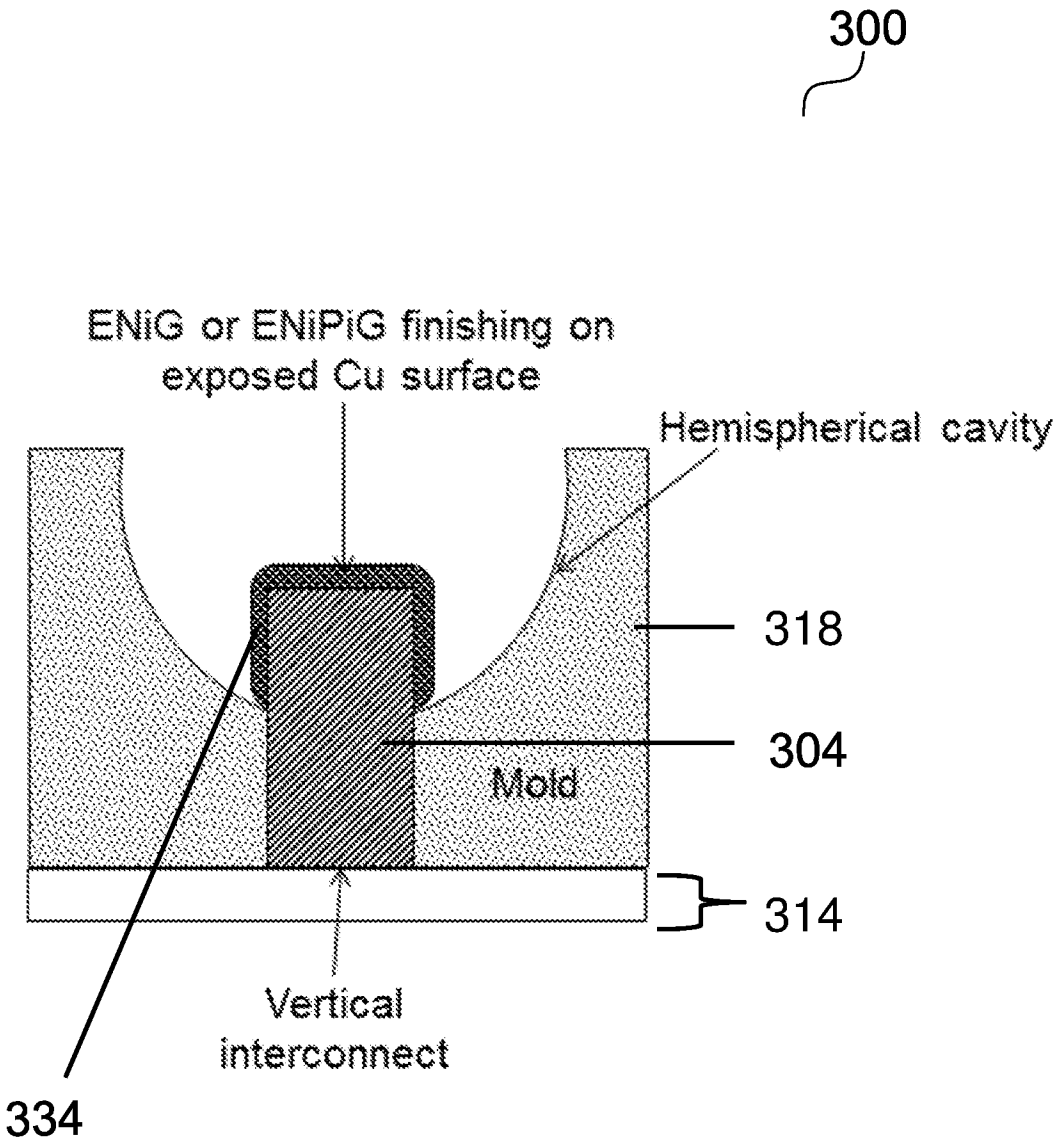

300
ENiG or ENiPiG finishing on exposed Cu surface
Hemispherical cavity
318
304
Mold
314
Vertical interconnect
334

FIG. 3E

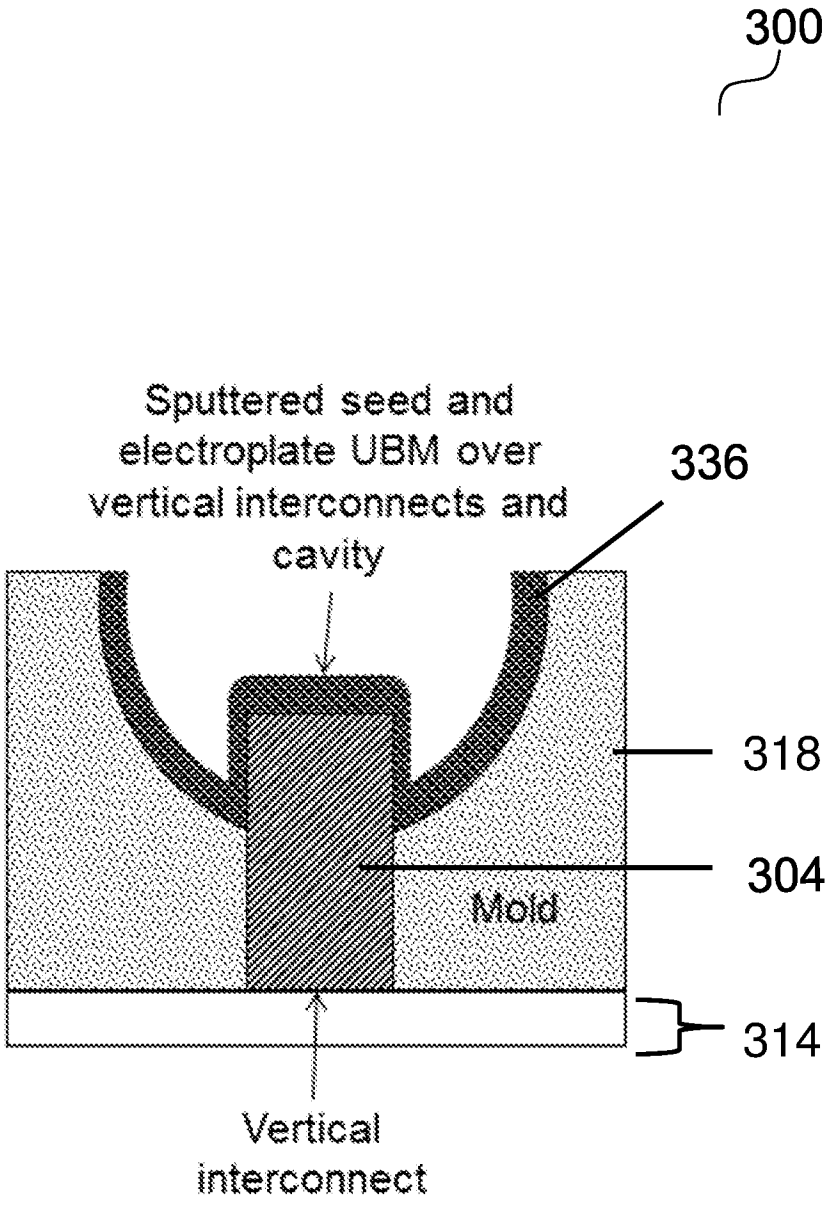

300
Sputtered seed and electroplate UBM over vertical interconnects and cavity
336
318
304
Mold
314
Vertical interconnect

FIG. 4

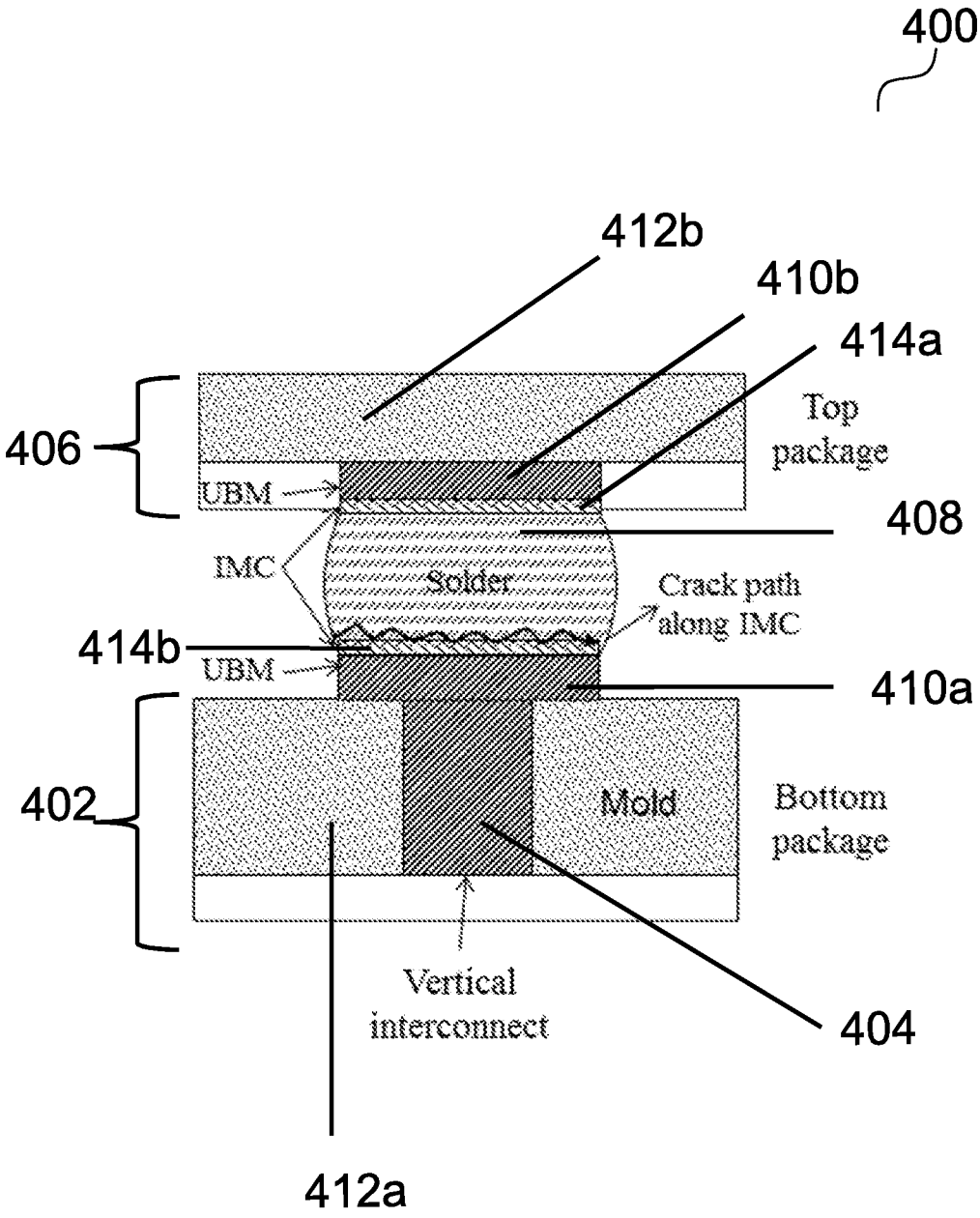

400
412b
410b
414a
406
Top package
UBM
408
IMC
Solder
Crack path along IMC
414b
UBM
410a
402
Mold
Bottom package
Vertical interconnect
404
412a

FIG. 5A

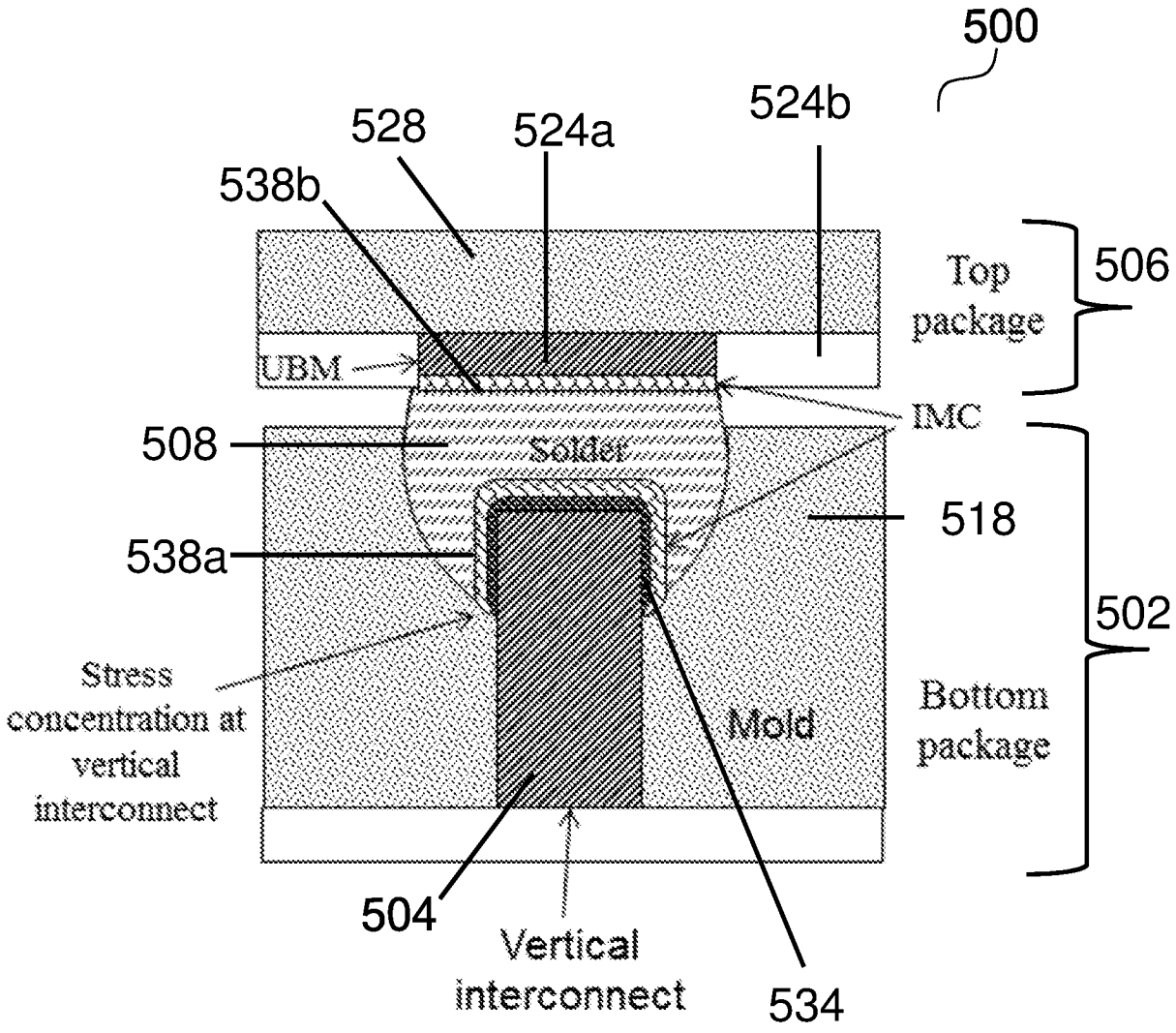

500
528
524a
524b
538b
Top package
506
UBM
IMC
508
Solder
518
538a
502
Stress concentration at vertical interconnect
Mold
Bottom package
504
Vertical interconnect
534

FIG. 5B

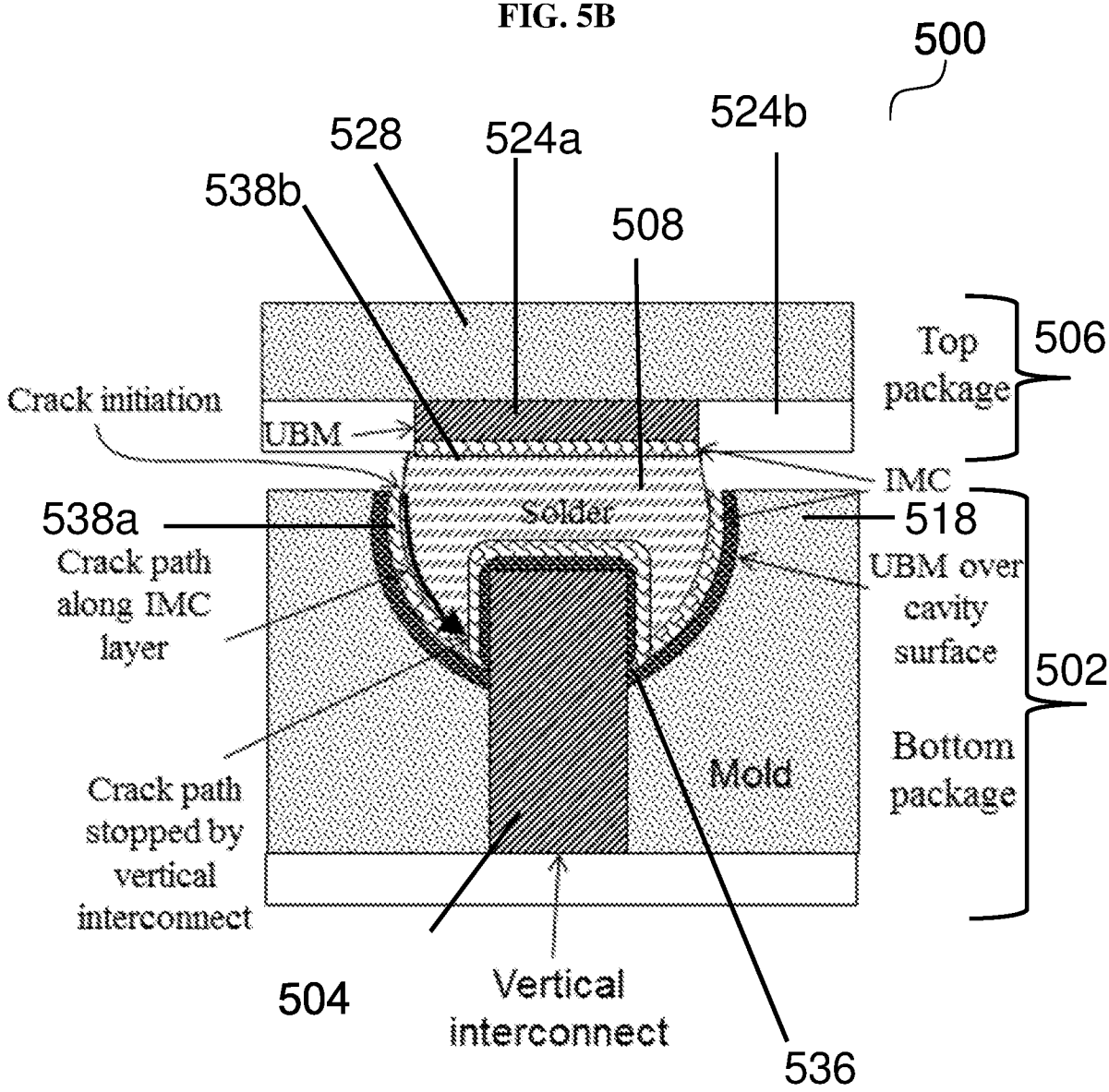

500
528
524a
524b
538b
508
Top package
506
Crack initiation
UBM
IMC
Solder
538a
Crack path along IMC layer
518
UBM over cavity surface
502
Bottom package
Mold
Crack path stopped by vertical interconnect
504
Vertical interconnect
536

FIG. 6A

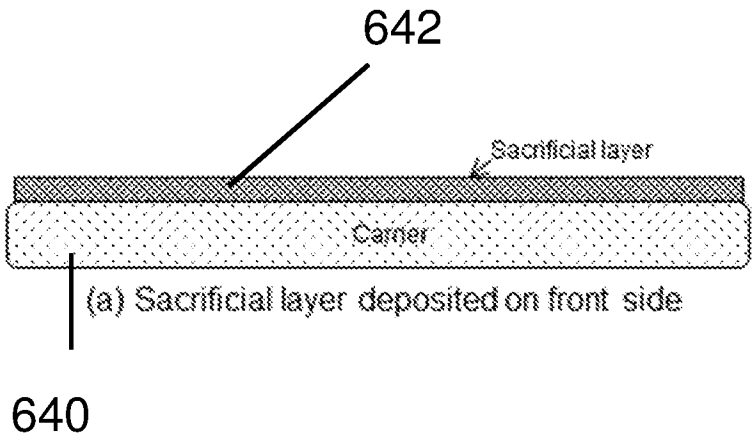

642
Sacrificial layer
Carrier
(a) Sacrificial layer deposited on front side
640

FIG. 6B

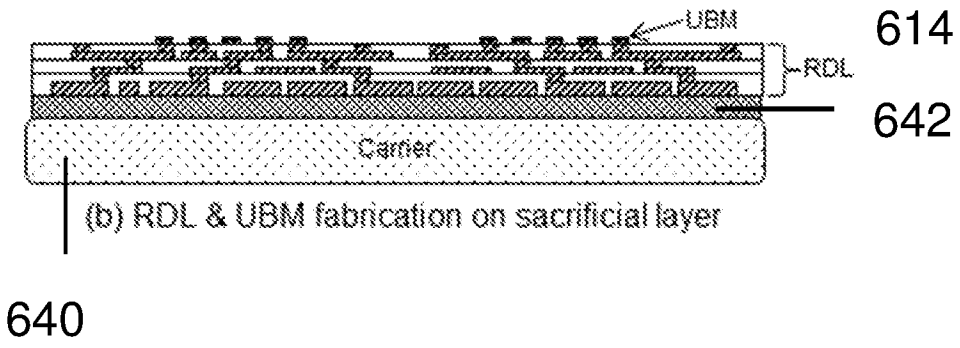
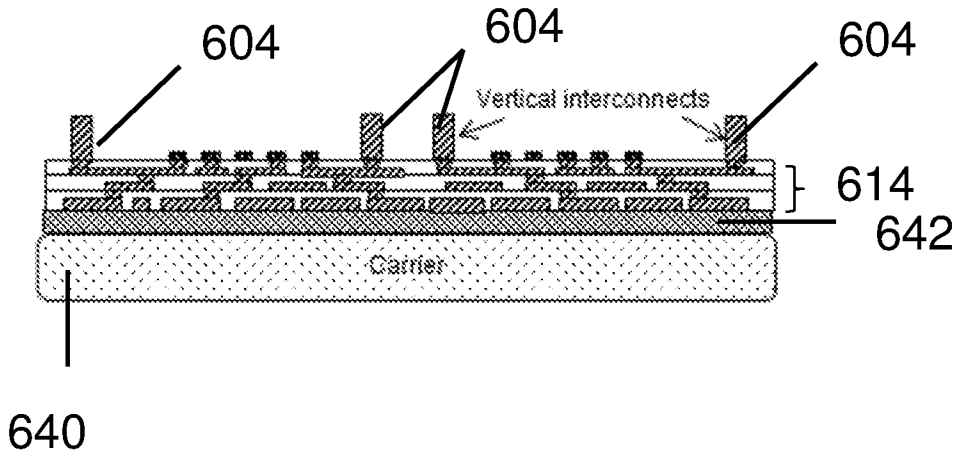
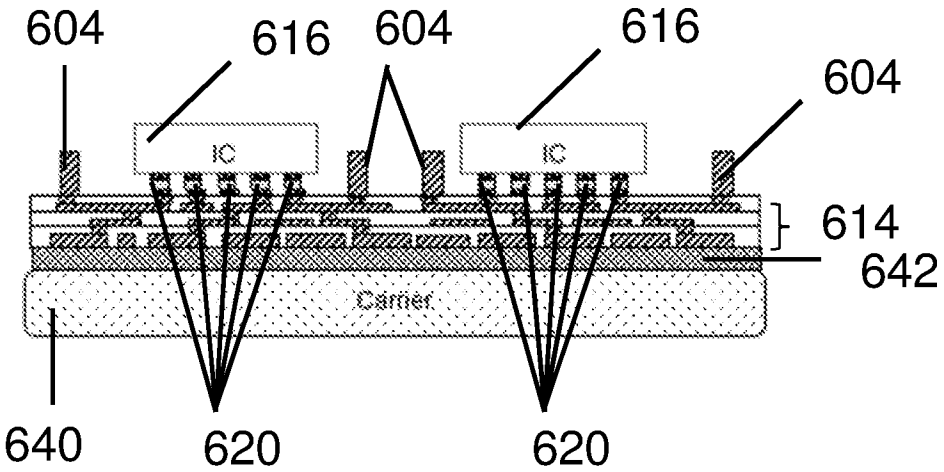

UBM
614
RDL
642
Carrier
(b) RDL & UBM fabrication on sacrificial layer
640

FIG. 6C



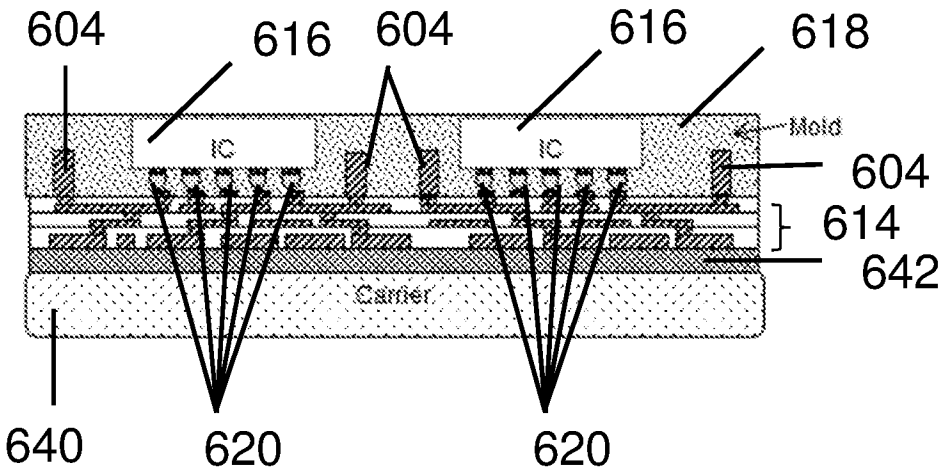
(c) Vertical interconnect formation (Cu wire or pillar)

FIG. 6D



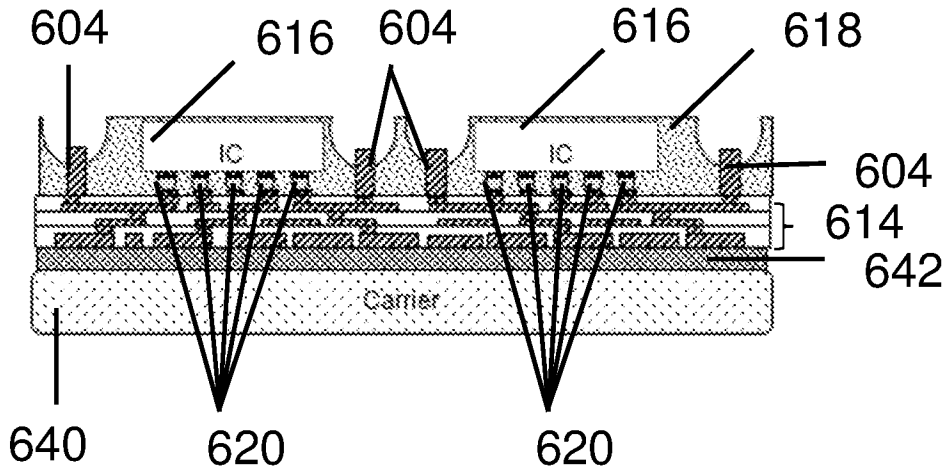
(d) Chip 2 wafer assembly

FIG. 6E



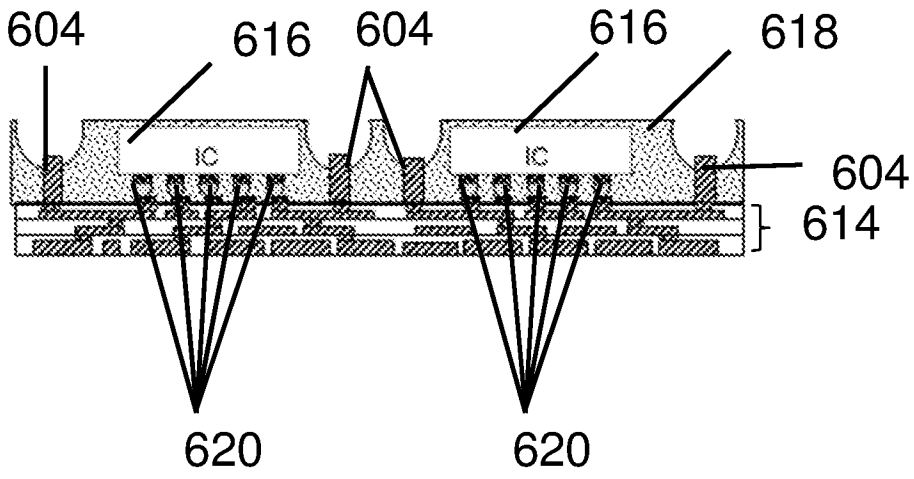
(e) Wafer level compression molding

FIG. 6F



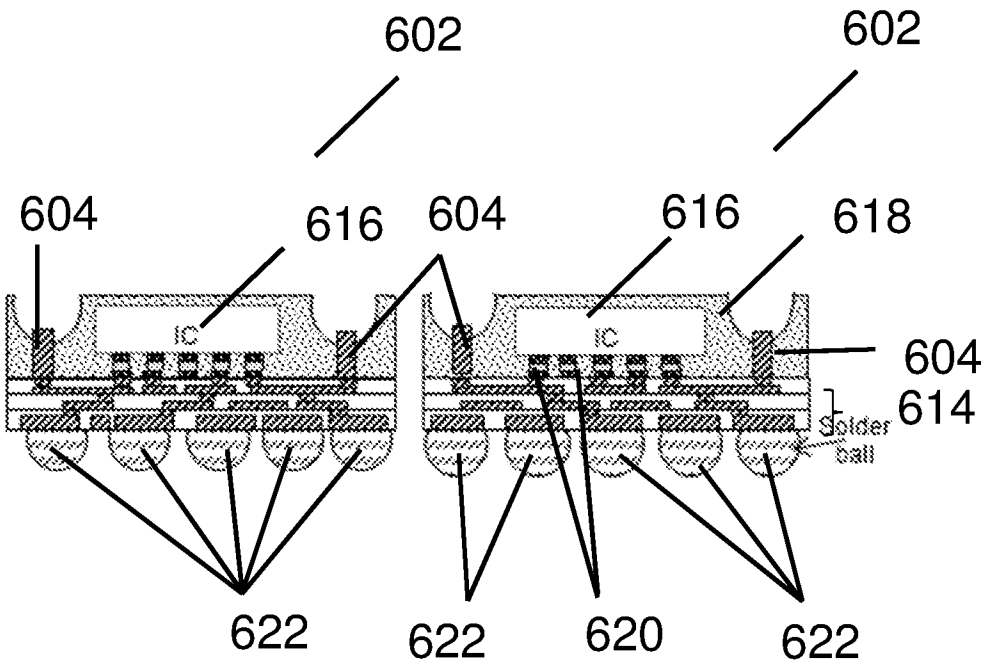
(f) Formation of hemispherical cavity on top of vertical interconnect & optional surface finishing

FIG. 6G



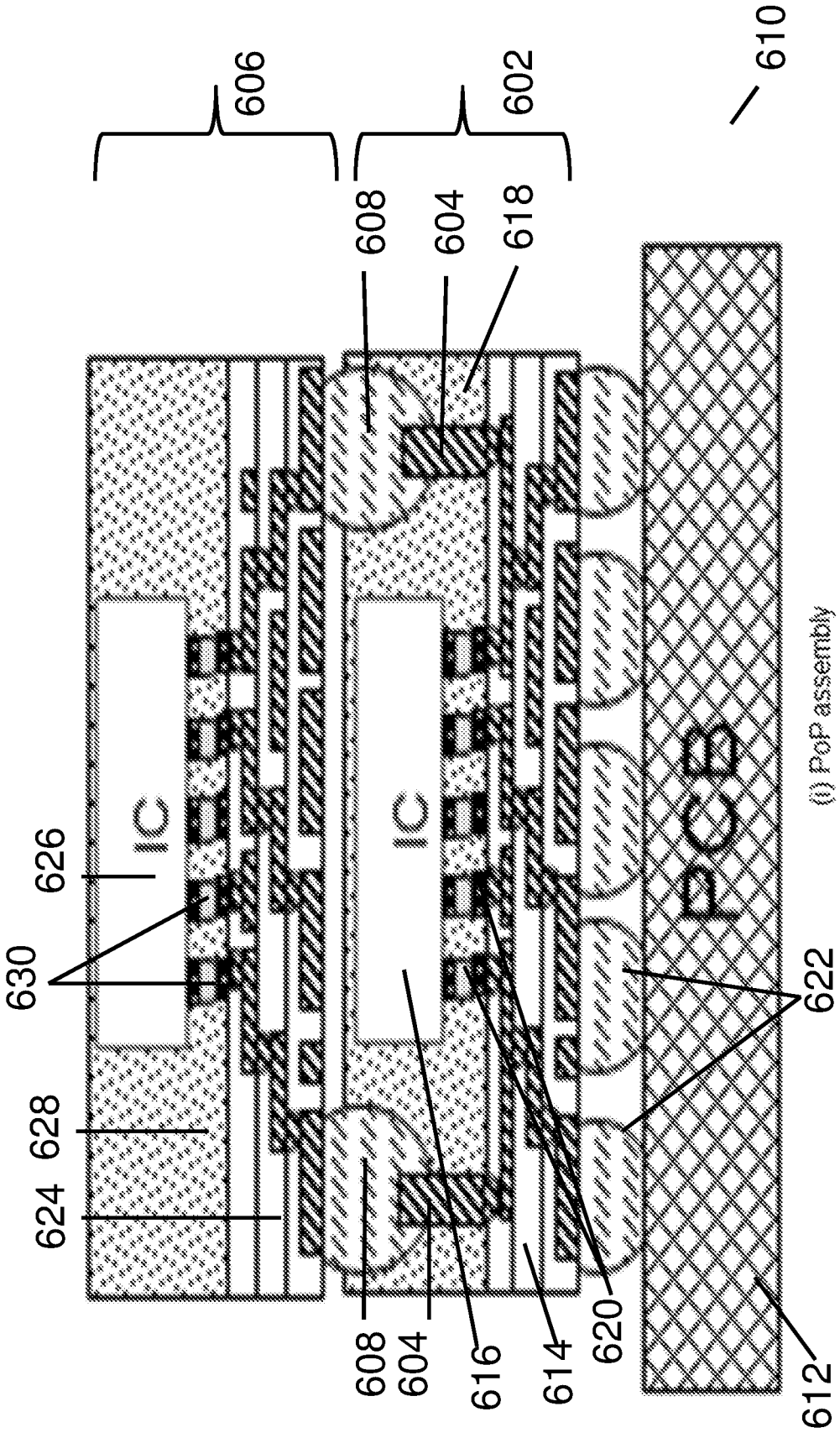
(g) Wafer de-bond from glass wafer

FIG. 6H



(h) Singulation & solder balls drop

FIG. 6I


606
602
610
608
604
618
IC
IC
626
630
628
624
PCB
(i) PoP assembly
622
608
604
616
614
620
612

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SG2017/050130

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/56 (2006.01) ***H01L 23/31 (2006.01)*** *H01L 25/00 (2006.01)* *H01L 23/538 (2006.01)*

According to International Patent Classification (IPC)

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

FAMPAT, Scopus: cavity, recess, hole, through mold via, through mold interconnect, stacked die, solder, fan out wafer level packaging, 空腔, 模腔, 通孔, 扇出晶片级封装, 堆叠封装 and other related terms

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	KR 10-2015-0098936 A (AMKOR TECHNOLOGY KOREA, INC.) 31 August 2015 paragraphs [0036], [0037], [0041], figures 2a, 2b, 2d, 2e of the machine translation	1-6, 11-18 7-10, 19, 20
Y	US 2013/0037929 A1 (ESSIG, K. S. ET AL.) 14 February 2013 paragraphs [0021], [0028], 0029], [0034], [0042], figures 2B and 4F	7-10, 19, 20
A	US 8779601 B2 (GAN, K. W. ET AL.) 15 July 2014 abstract, figure 4	-
P,X	US 2017/0053898 A1 (YEH, Y.-H. ET AL.) 23 February 2017 paragraph [0040] and figure 6	1-6, 12-18

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

*Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
05/06/2017 *(day/month/year)*	13/06/2017 *(day/month/year)*

Name and mailing address of the ISA/SG

IPOS INTELLECTUAL PROPERTY OFFICE OF SINGAPORE

Intellectual Property Office of Singapore
51 Bras Basah Road
#01-01 Manulife Centre
Singapore 189554

Email: pct@ipos.gov.sg

Authorized officer

Lee Yi Chau

IPOS Customer Service Tel. No.: (+65) 6339 8616

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/SG2017/050130

Note: This Annex lists known patent family members relating to the patent documents cited in this International Search Report. This Authority is in no way liable for these particulars which are merely given for the purpose of information.

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
KR 10-2015-0098936 A	31/08/2015	NONE	
US 2013/0037929 A1	14/02/2013	CN 102324418 A	18/01/2012
		TW 201308538 A	16/02/2013
		TW I445144 B	11/07/2014
US 8779601 B2	15/07/2014	US 2013/0105973 A1	02/05/2013
		US 2013/0105991 A1	02/05/2013
		US 8916481 B2	23/12/2014
US 2017/0053898 A1	23/02/2017	TW I559419 B	21/11/2016