



US 20050272272A1

(19) **United States**(12) **Patent Application Publication****Yeo et al.**(10) **Pub. No.: US 2005/0272272 A1**(43) **Pub. Date: Dec. 8, 2005**(54) **SEMICONDUCTOR DEVICE AND METHOD  
FOR MANUFACTURING THE SAME**(75) Inventors: **Jae-Hyun Yeo**, Seoul (KR); **Sung-Tae Kim**, Seoul (KR); **Young-Sun Kim**, Suwon-city (KR); **In-Sung Park**, Seoul-city (KR); **Seok-Jun Won**, Seoul (KR); **Yun-Jung Lee**, Seoul (KR); **Ki-Vin Im**, Suwon-city (KR); **Ki-Yeon Park**, Seoul-city (KR)

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**PORTLAND, OR 97204 (US)**(73) Assignee: **Samsung Electronics Co., Ltd.**, Suwon-si (KR)(21) Appl. No.: **11/198,541**(22) Filed: **Aug. 5, 2005****Related U.S. Application Data**

(62) Division of application No. 10/452,979, filed on Jun. 2, 2003, now Pat. No. 6,946,342.

(30) **Foreign Application Priority Data**

Aug. 16, 2002 (KR) ..... 2002-48404

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H01L 29/94; H01L 31/119;  
H01L 21/31; H01L 21/469(52) **U.S. Cl.** ..... **438/785**(57) **ABSTRACT**

A semiconductor device and a method for forming the same. A dielectric layer is formed on a semiconductor substrate or on a lower electrode of a capacitor. Vacuum annealing is performed on the dielectric layer. Thus, impurities remaining in the dielectric layer can be effectively removed, and the dielectric layer can be densified. As a result, the electrical characteristics of the semiconductor device are improved. For example, the leakage current characteristics of the dielectric layer are improved and capacitance is increased.

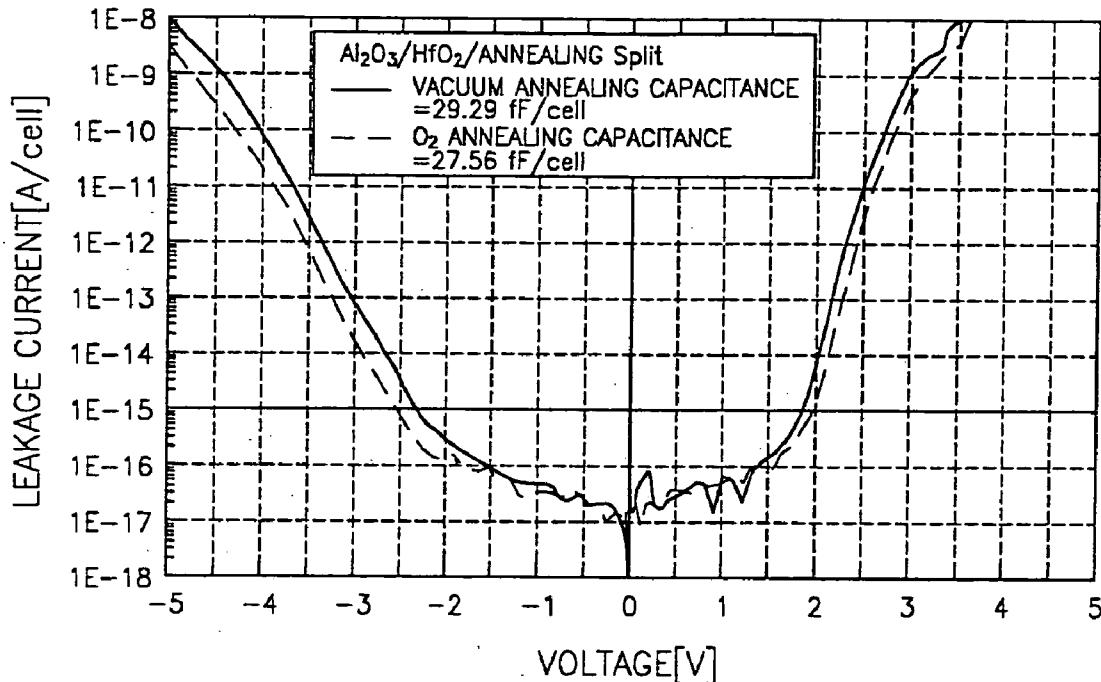


FIG. 1A

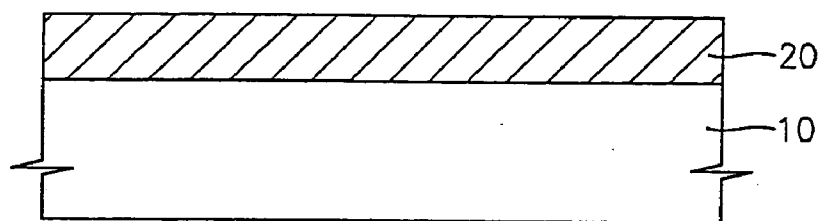


FIG. 1B

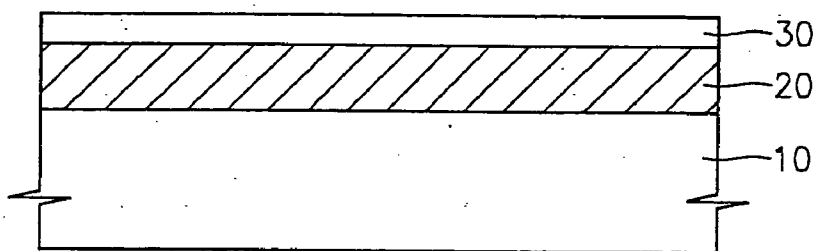


FIG. 1C

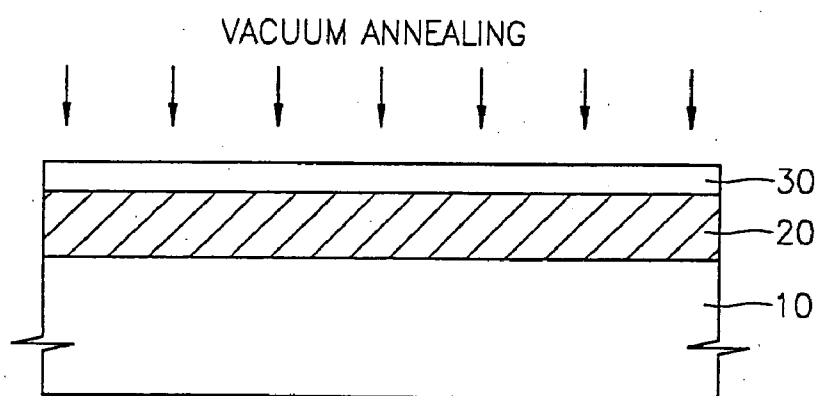


FIG. 1D

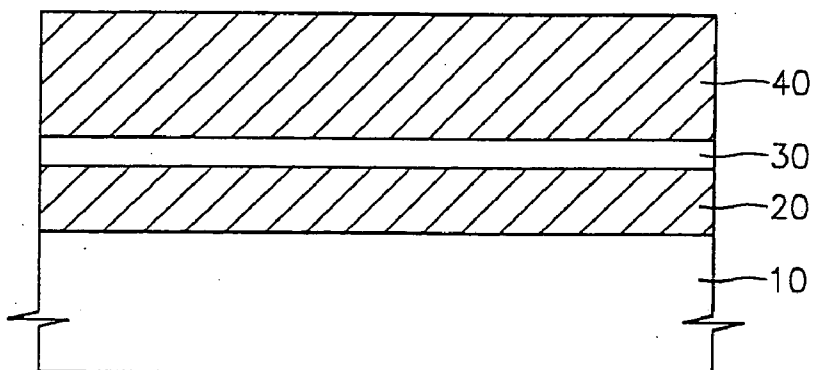


FIG. 2

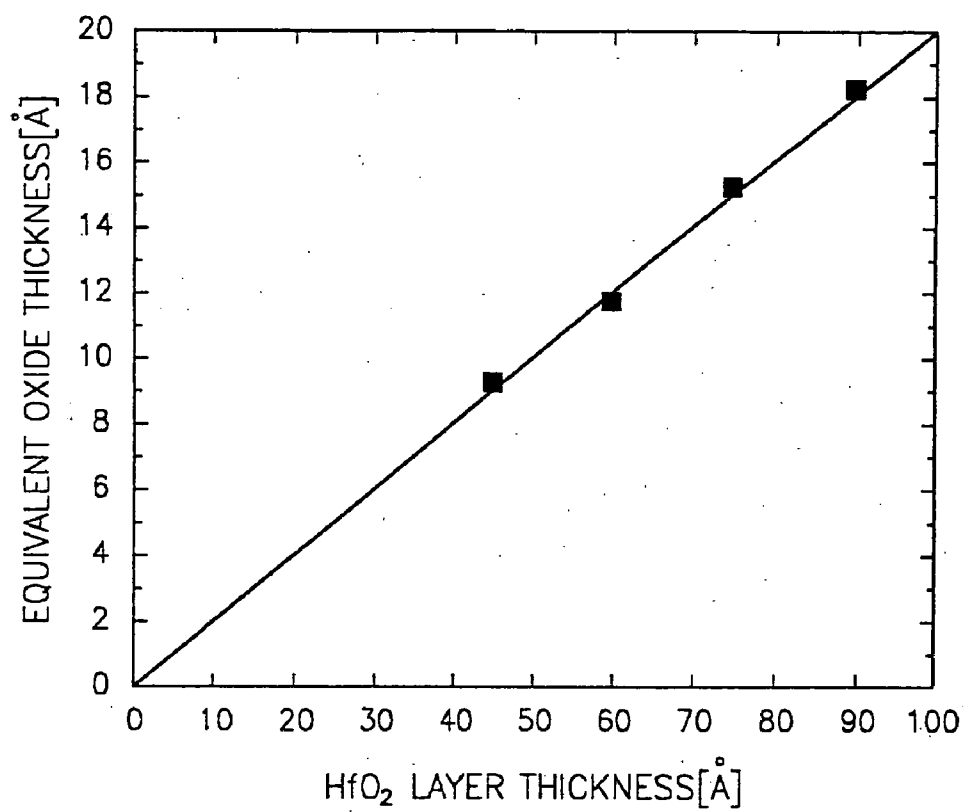


FIG. 3

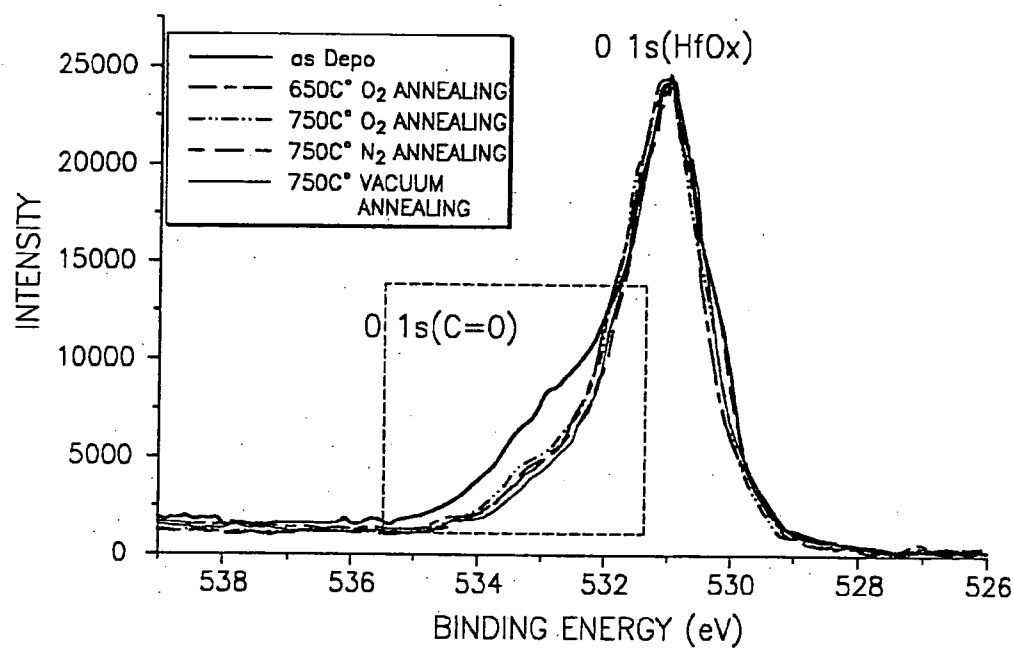


FIG. 4

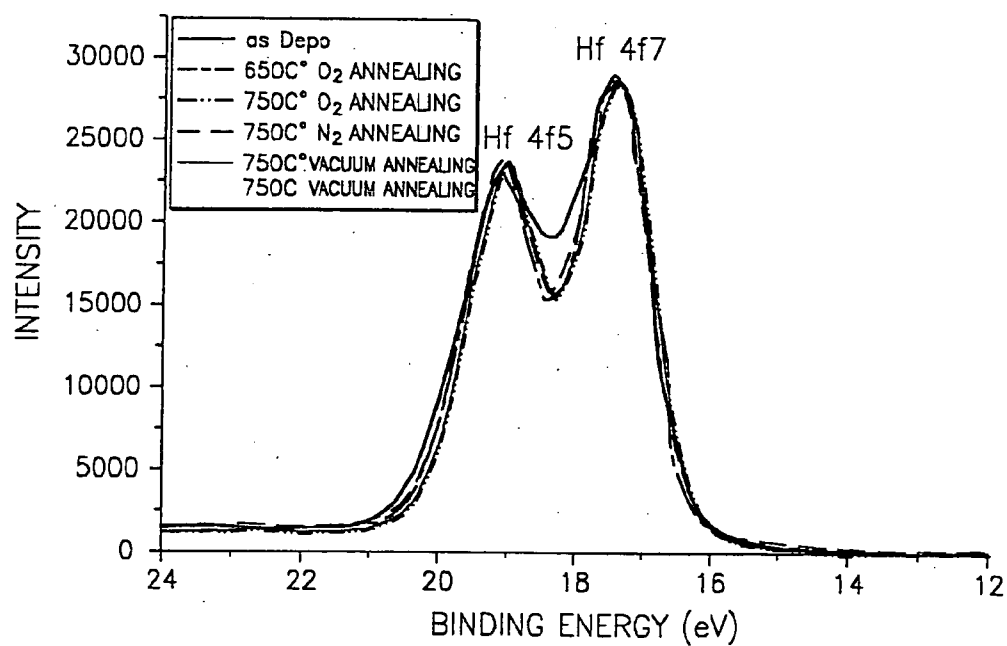


FIG. 5A

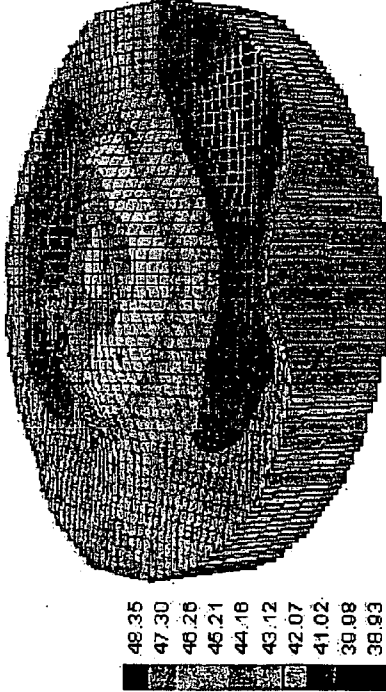
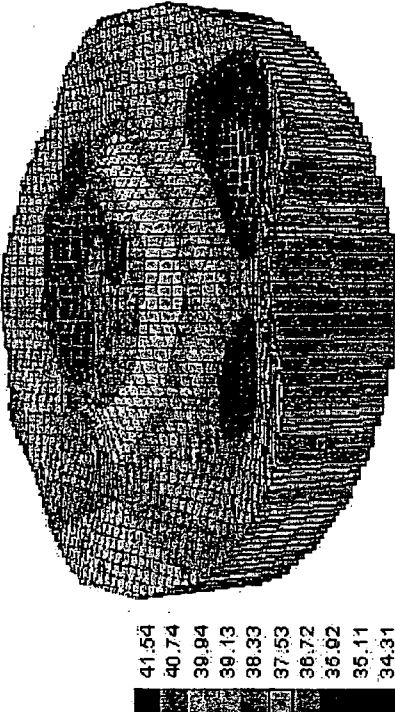
CONDITION	AS-DEPOSITED		750°C, 2min VACUUM ANNEALING	
IMAGE				
	avg : 42.27 Å	range: 13.37 Å	avg : 37.92 Å	range: 10.26 Å
THICKNESS				

FIG. 5B

CONDITION	AFTER-DEPOSITION THICKNESS	AFTER-VACUUM ANNEALING THICKNESS	AFTER-ETCHING THICKNESS (HF, 10sec)	ETCHING RATE
VACUUM ANNEALING	37.2 $\text{\AA}$	33.5 $\text{\AA}$	32.2 $\text{\AA}$	1.8 $\text{\AA}/\text{min}$
AS-DEPOSITED STATE	38.1 $\text{\AA}$	—	2.9 $\text{\AA}$	211.2 $\text{\AA}/\text{min}$

FIG. 6

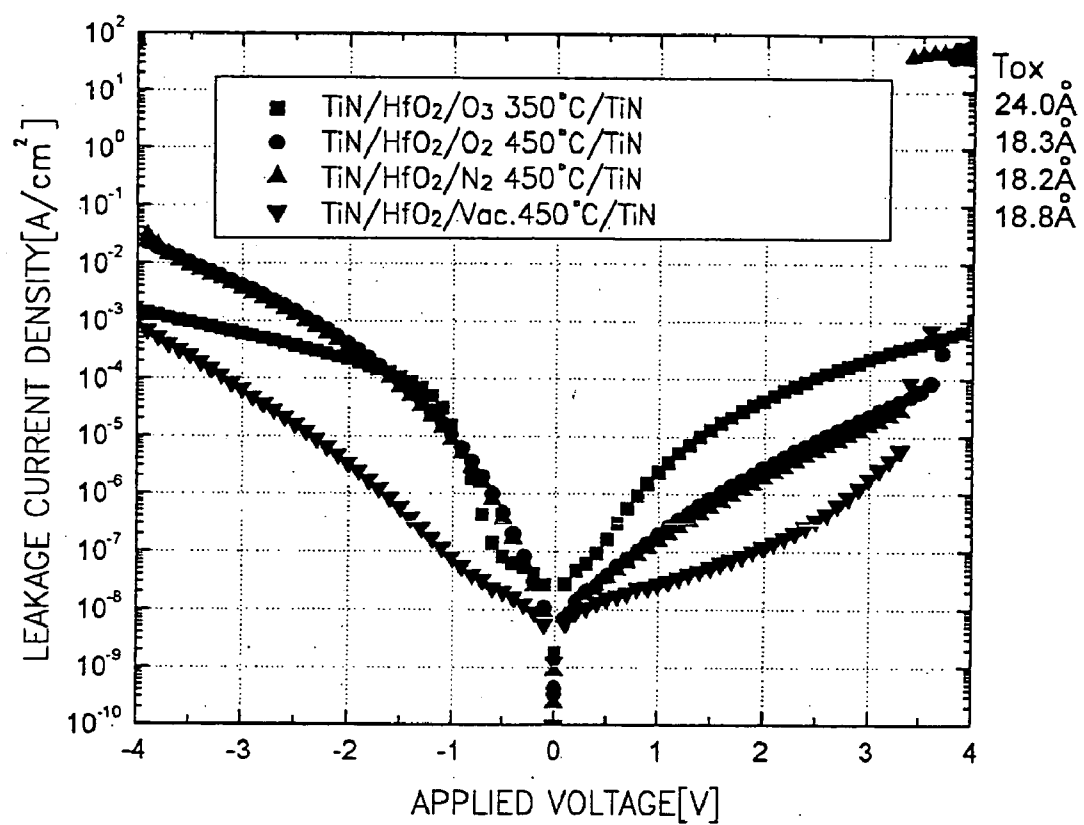


FIG. 7

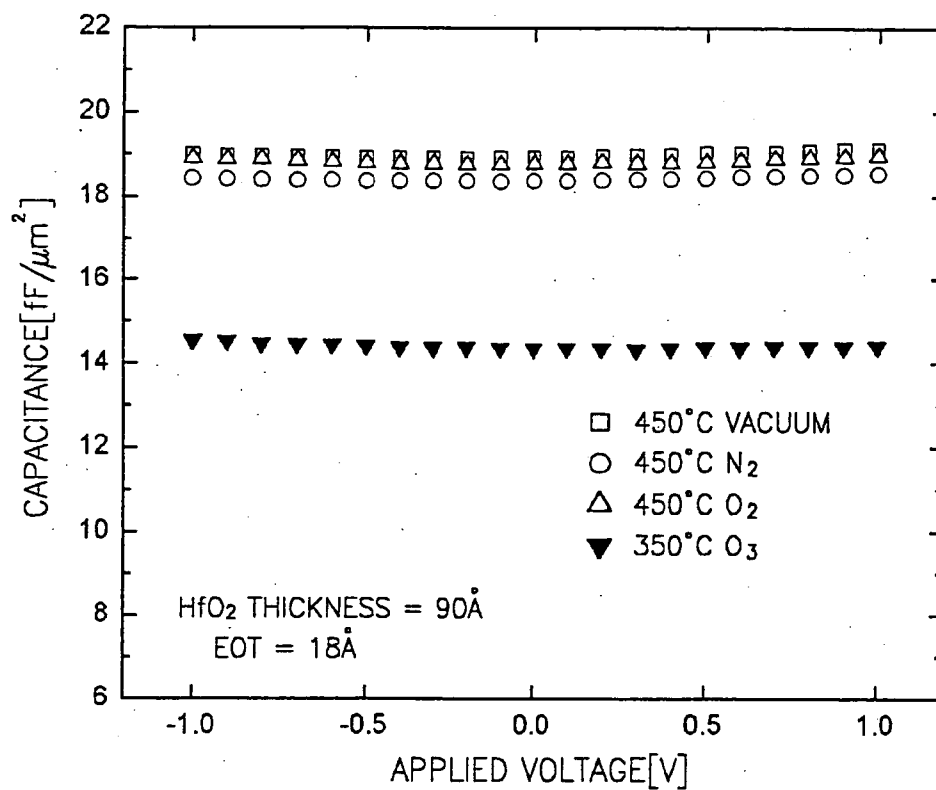




FIG. 8A

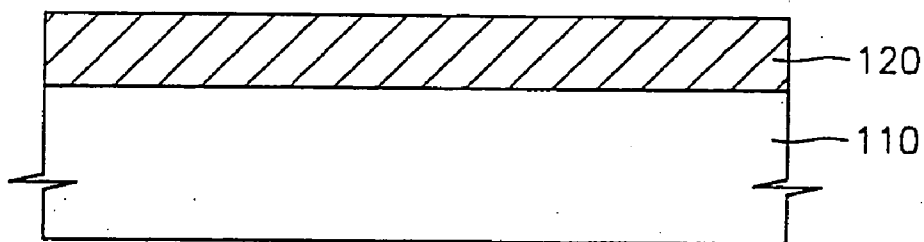


FIG. 8B

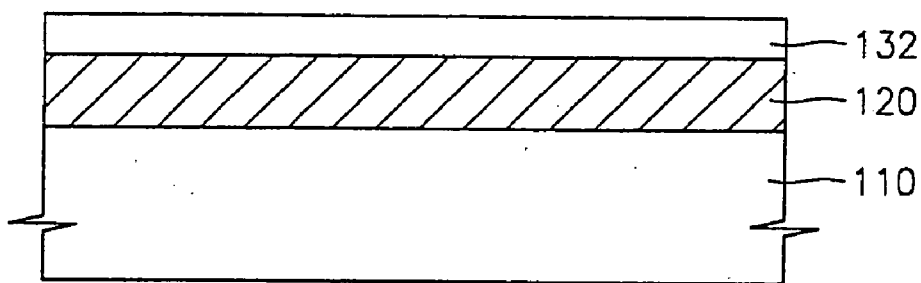


FIG. 8C

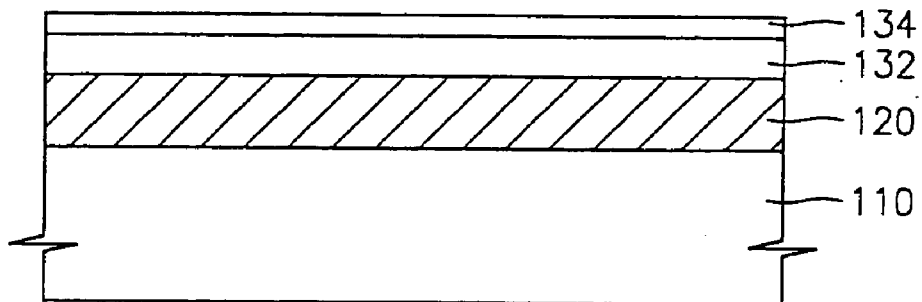


FIG. 8D

VACUUM ANNEALING

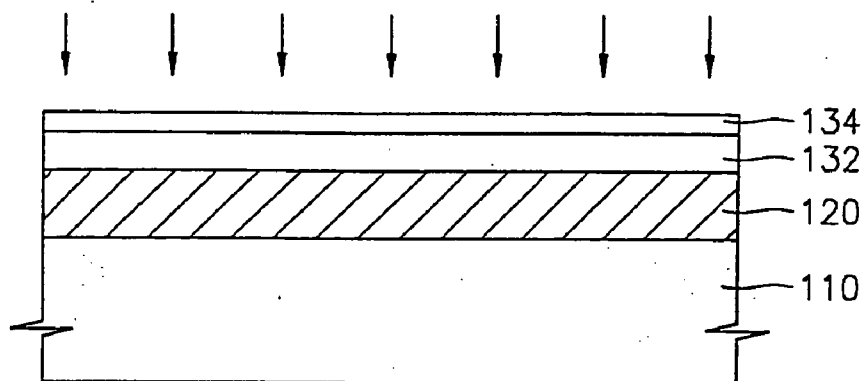


FIG. 8E

O<sub>2</sub> / O<sub>3</sub>

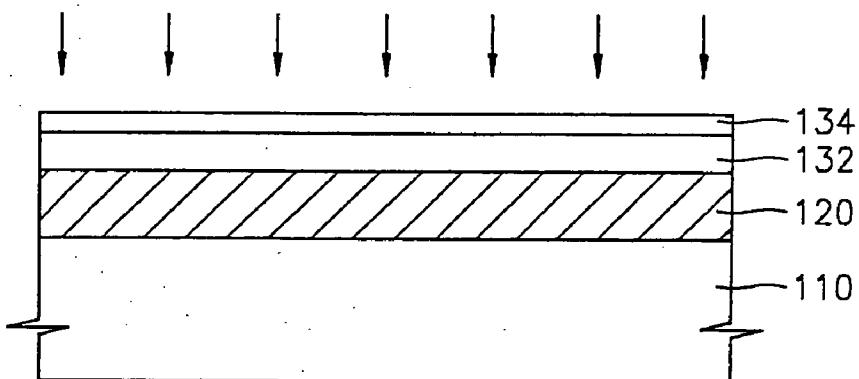


FIG. 8F

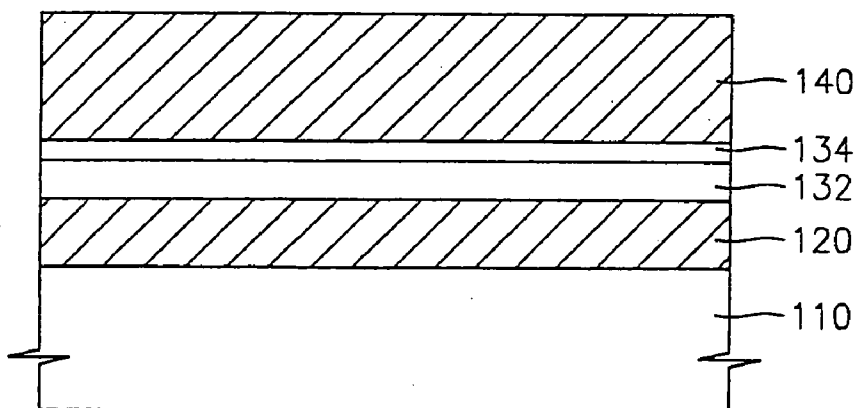


FIG. 9

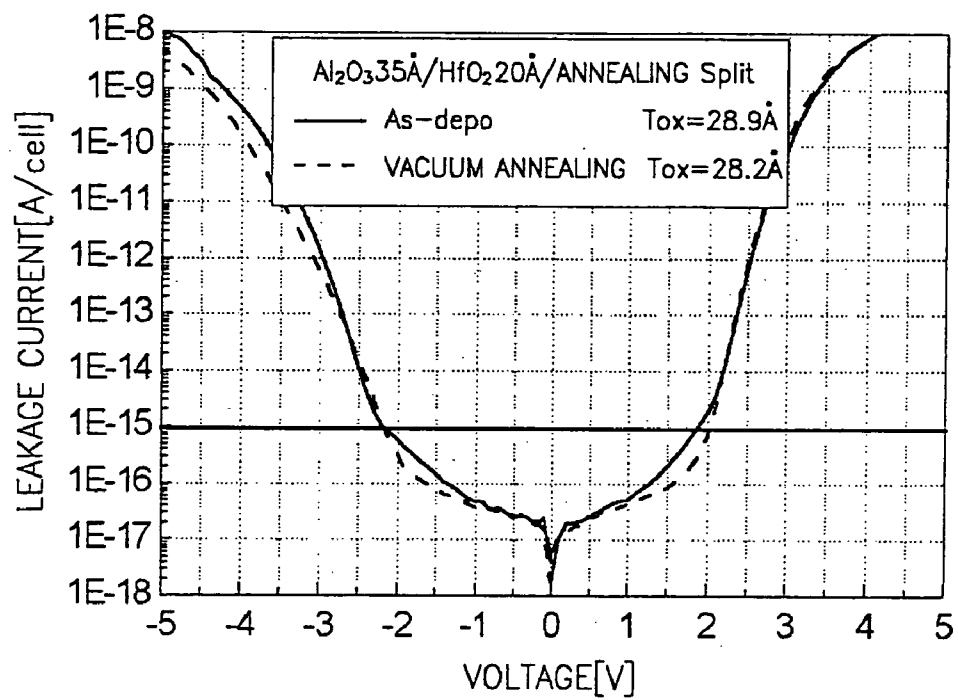


FIG. 10

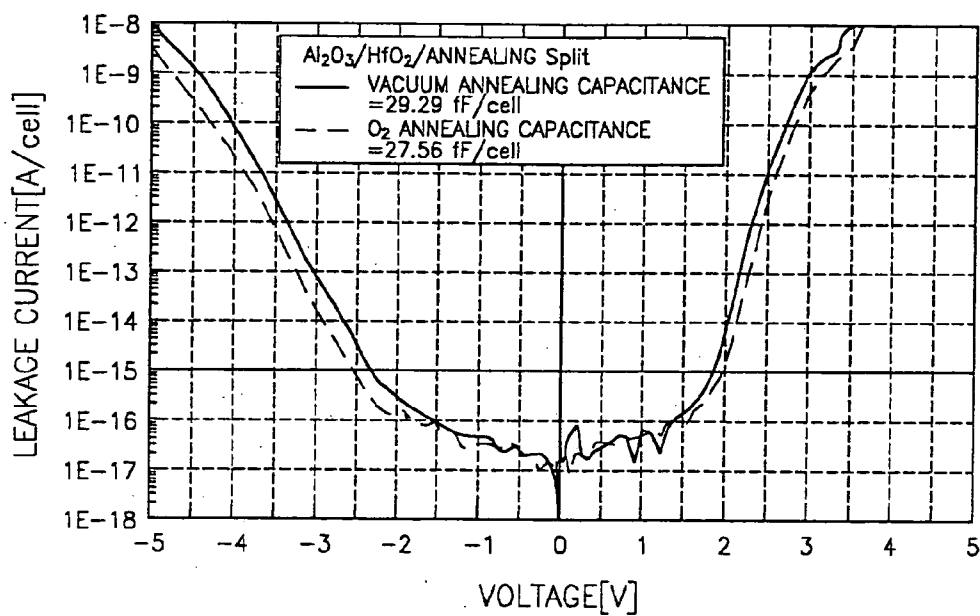


FIG. 11

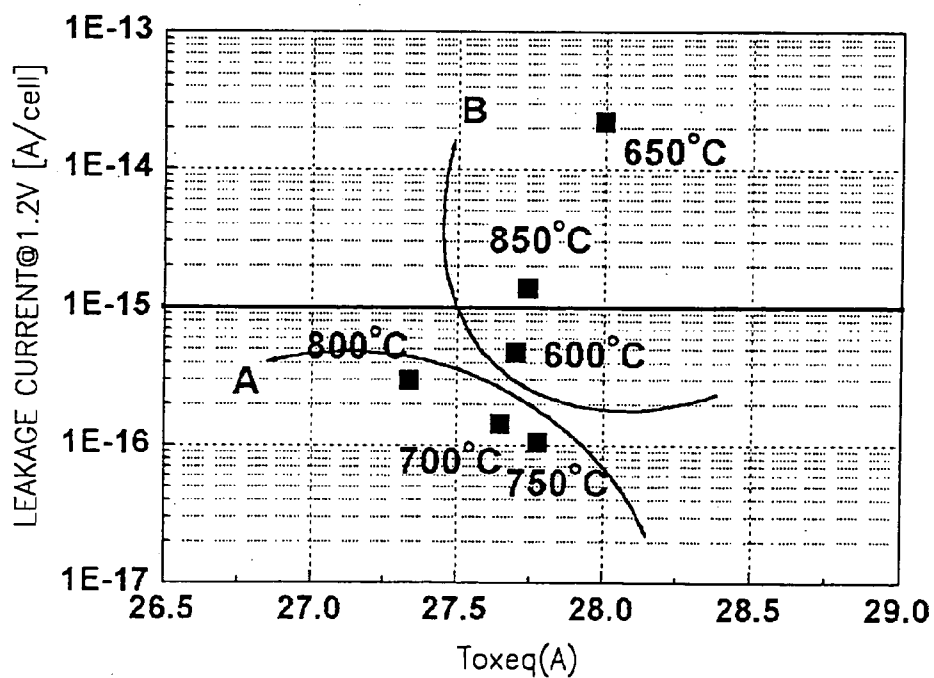


FIG. 12

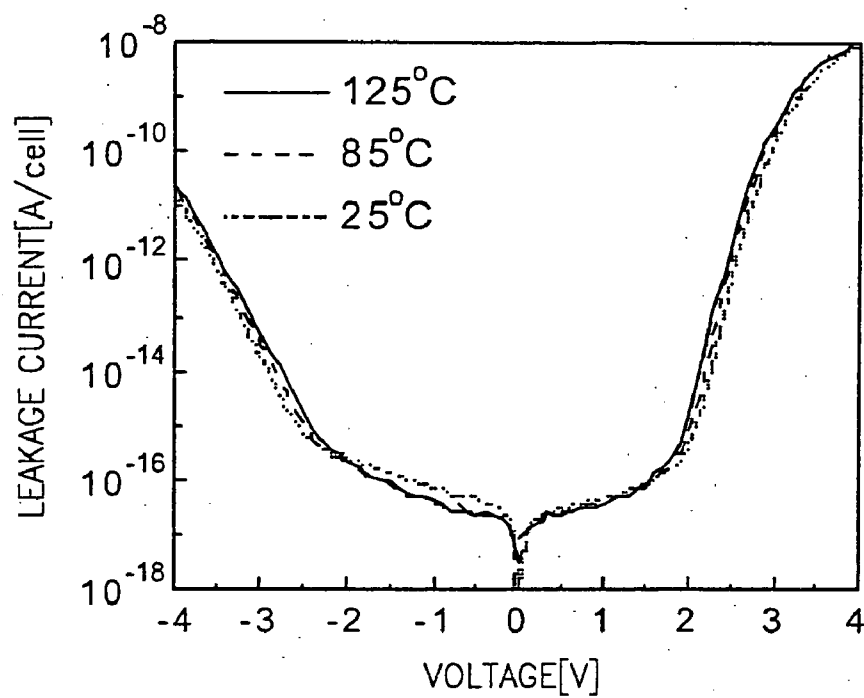


FIG. 13

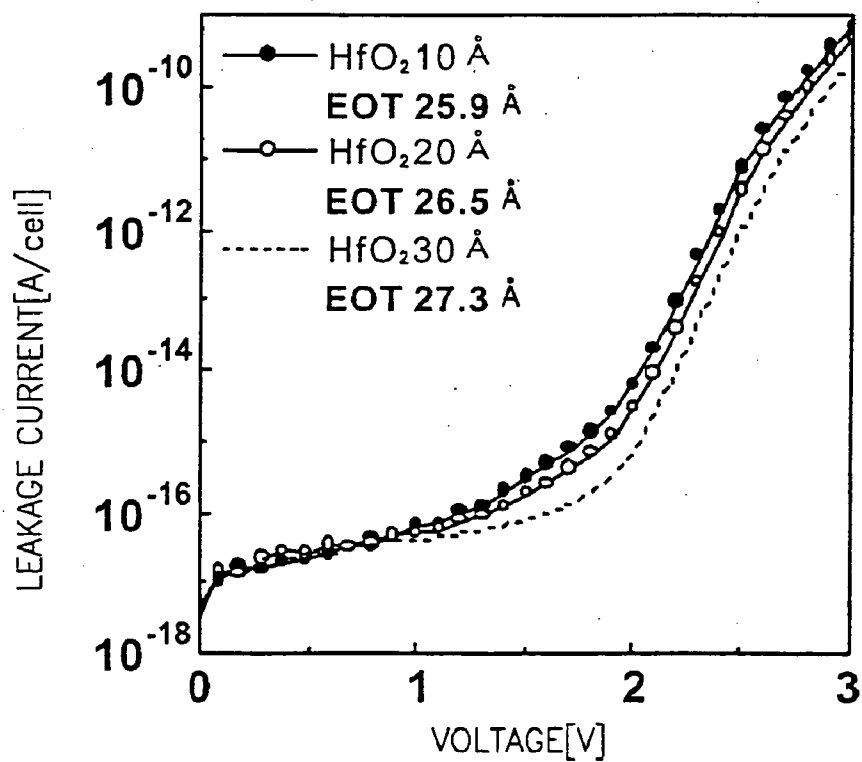


FIG. 14

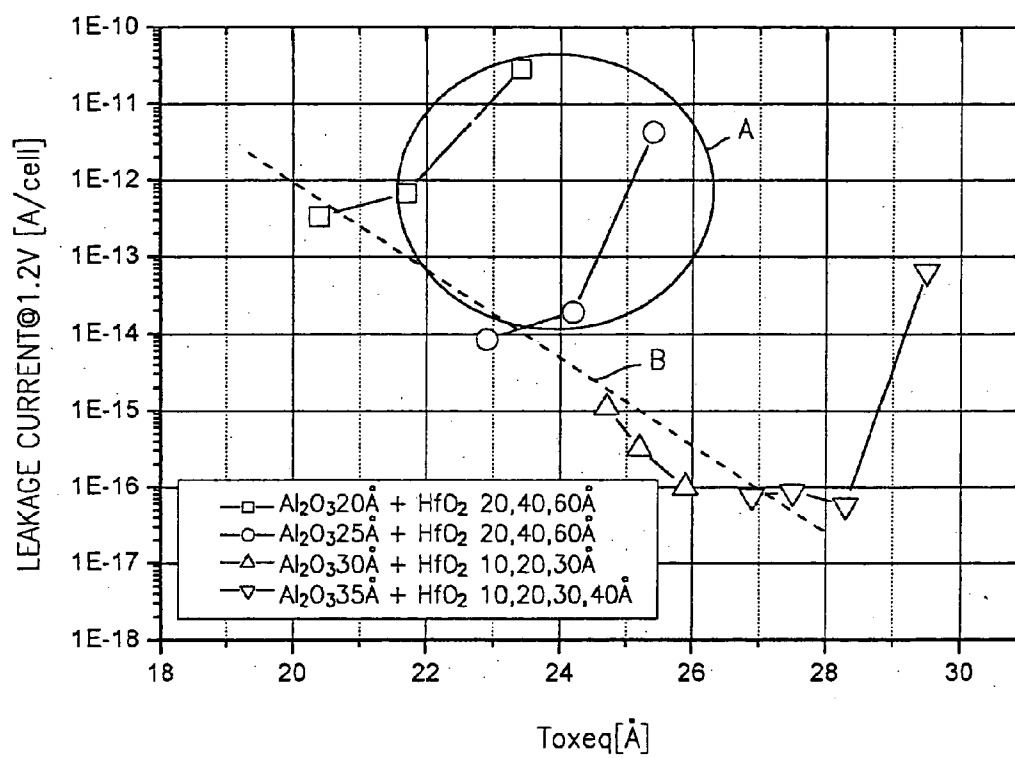


FIG. 15

	[Toxeq(Å)]							HfO <sub>2</sub> THICKNESS(Å)
	10	20	25	30	35	40	50	60
10								
20		20.5				21.8		23.1
25		22.9		23.5		24.2		25.4
30	24.7	25.2		25.9				
35	26.9	27.5		28.3		28.5		
40								
50								
60								
Al <sub>2</sub> O <sub>3</sub> THICKNESS(Å)		NORMAL LEAKAGE CURRENT						LEAKAGE CURRENT DEGRADATION

FIG. 16

LEAKAGE CURRENT[A/cell]

	10	20	25	30	35	40	50	60	HfO <sub>2</sub> THICKNESS(Å)
10									
20		3.21E-13				6.68E-13		2.95E-11	
25		8.35E-15		4.9E-13		1.88E-14		4.31E-12	
30	1.06E-15	3.21E-16		9.98E-17					
35	7.59E-17	8.69E-17		5.78E-17		6.42E-14			
40									
50									
60									
Al <sub>2</sub> O <sub>3</sub> THICKNESS(Å)		NORMAL LEAKAGE CURRENT						LEAKAGE CURRENT DEGRADATION	



FIG. 17

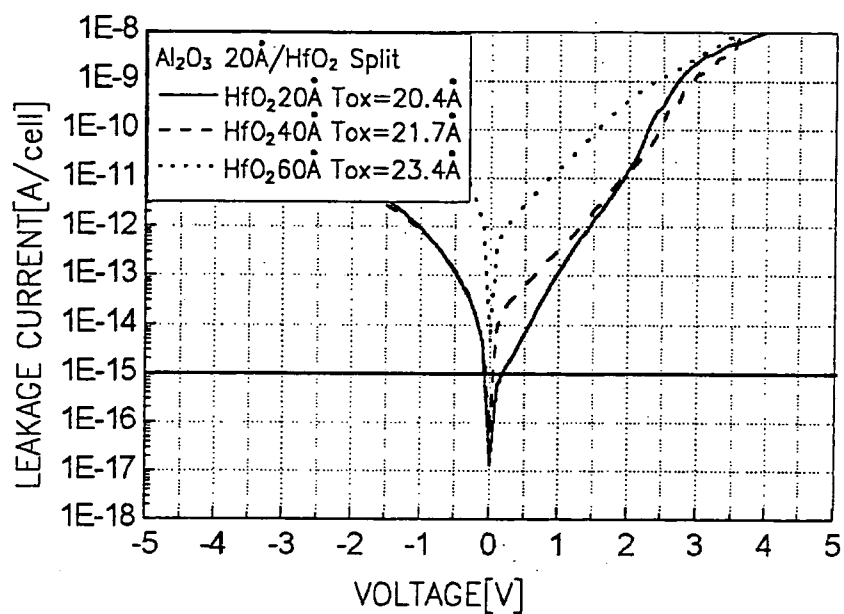


FIG. 18

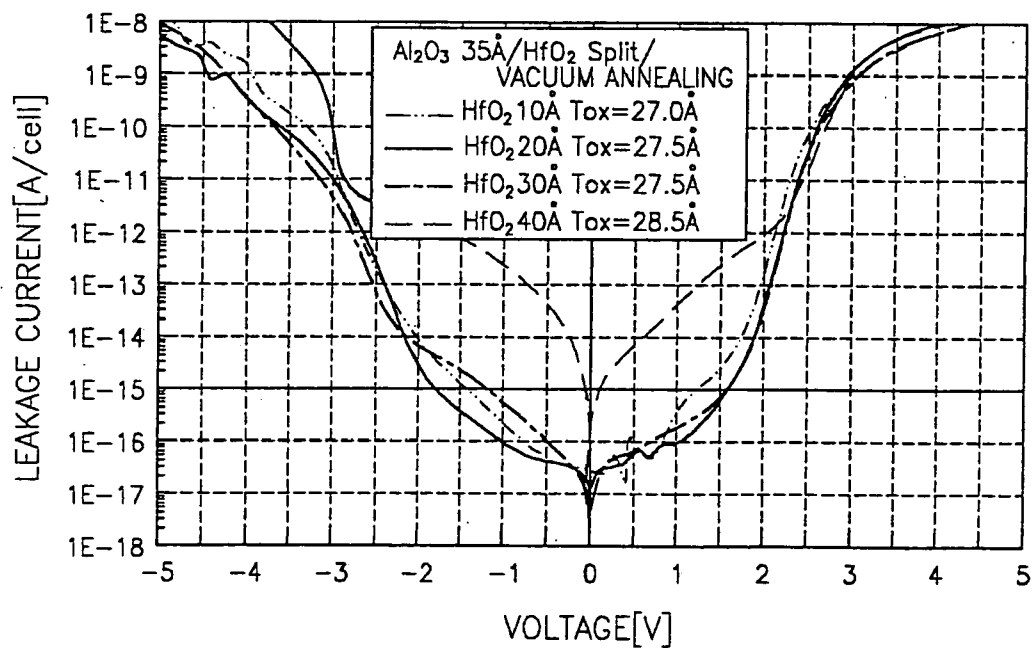


FIG. 19

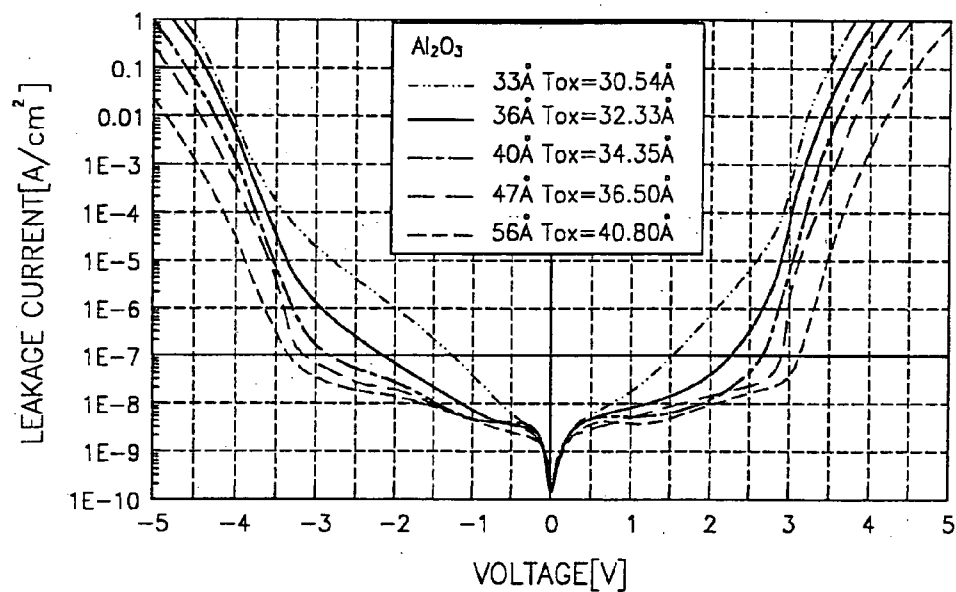


FIG. 20

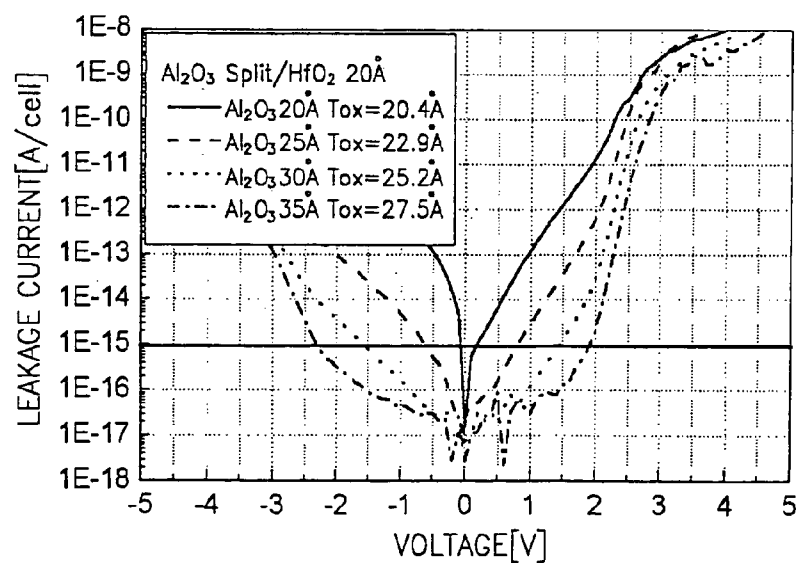


FIG. 21

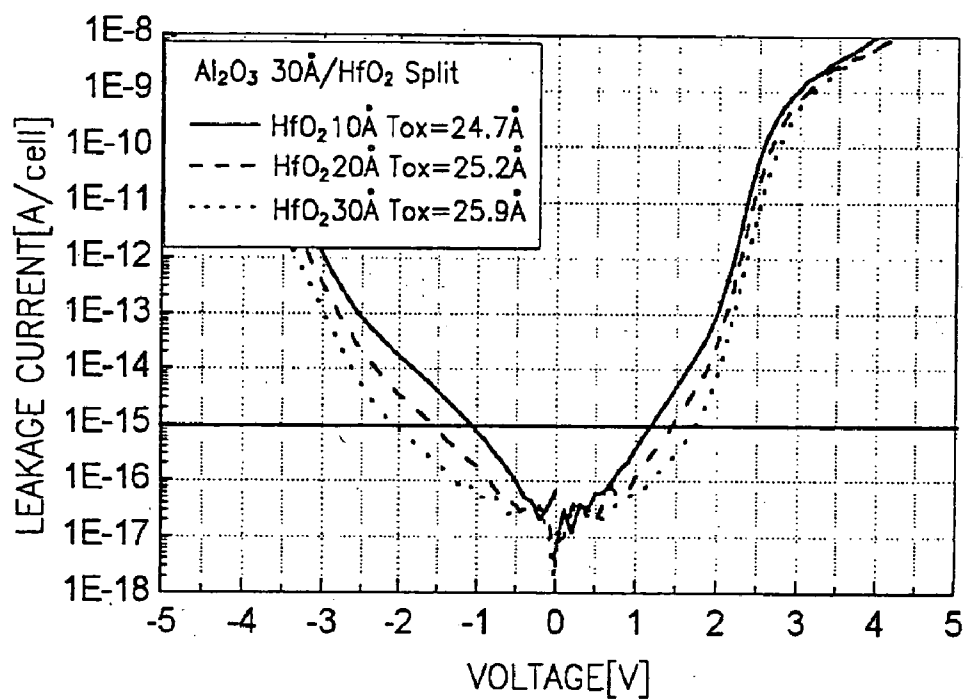


FIG. 22

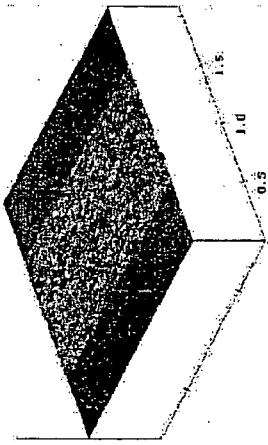
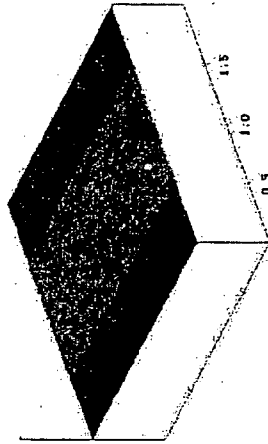
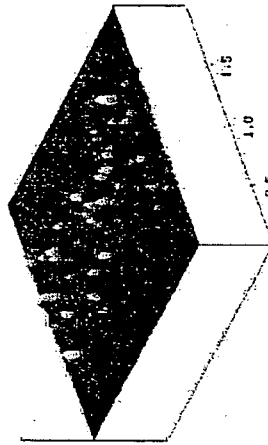
HfO <sub>2</sub> THICKNESS	20 Å	40 Å	60 Å
3D			
RMS ( Å )	1.1	1.2	2.7
MAXIMUM HEIGHT( Å )	10.8	18.7	41.0

FIG. 23

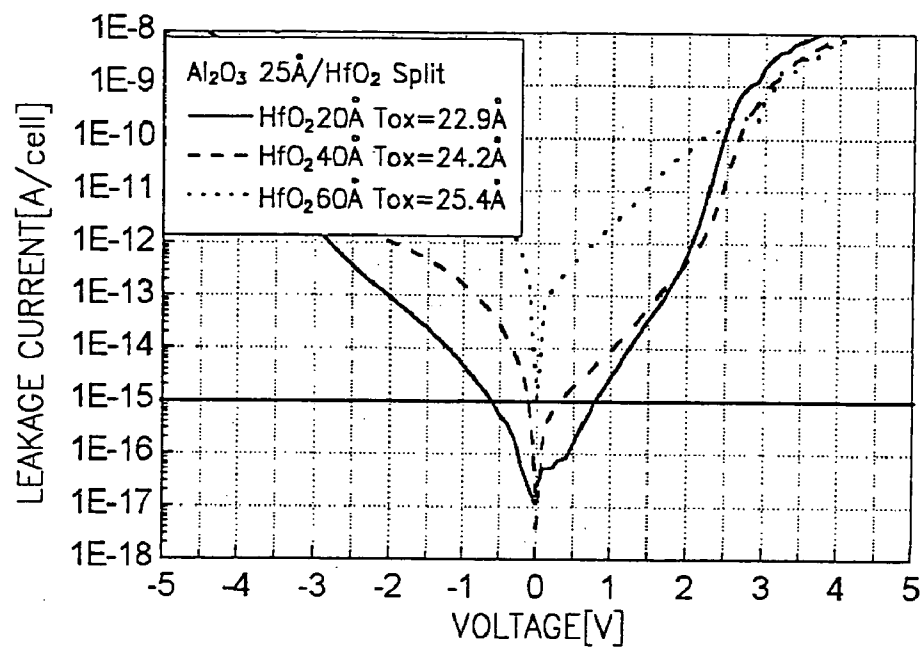


FIG. 24A

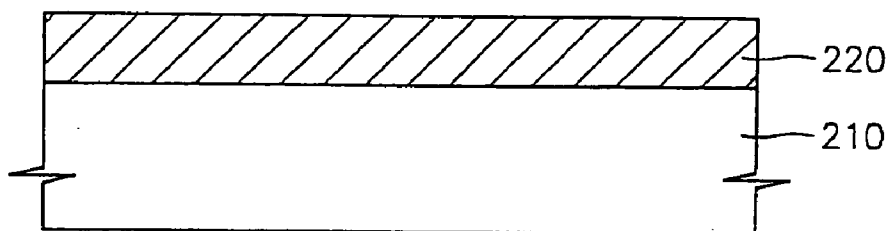


FIG. 24B

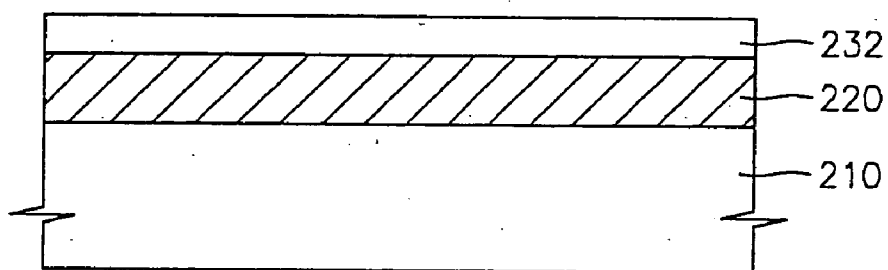


FIG. 24C

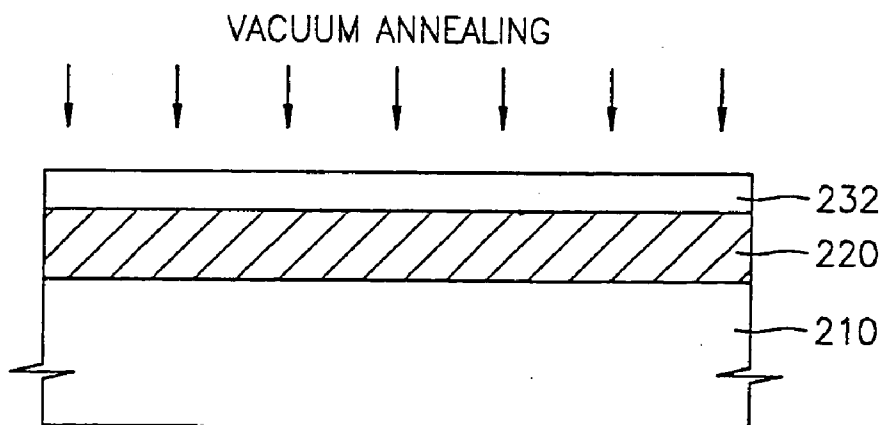


FIG. 24D

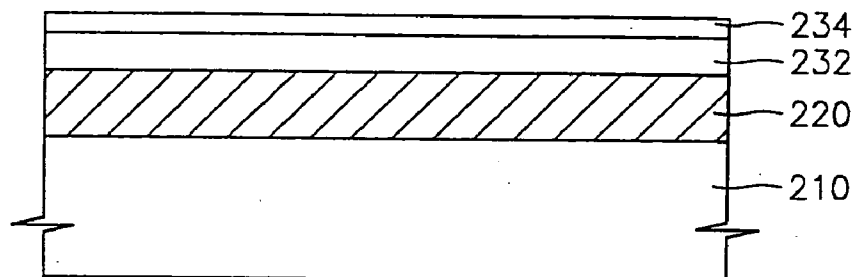


FIG. 24E

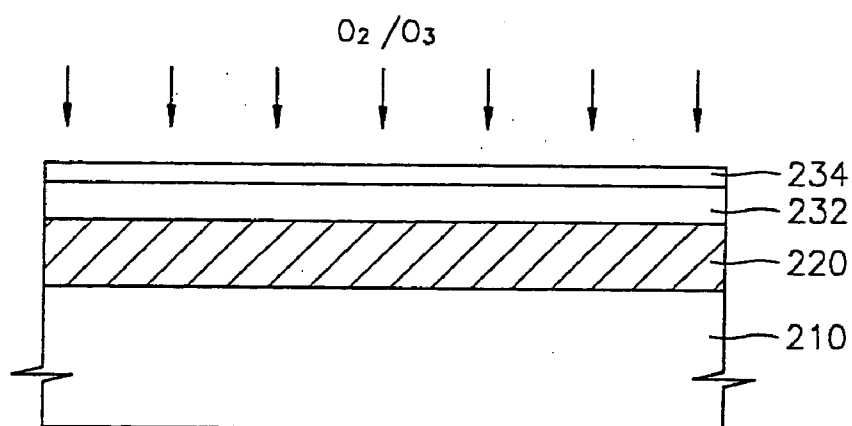


FIG. 24F

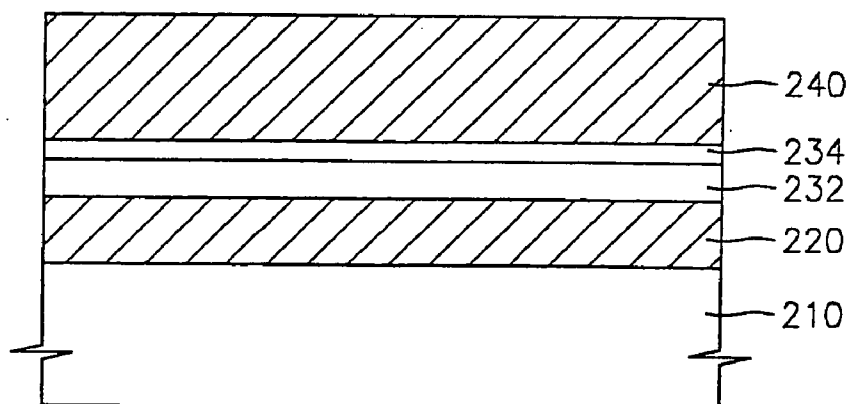


FIG. 25

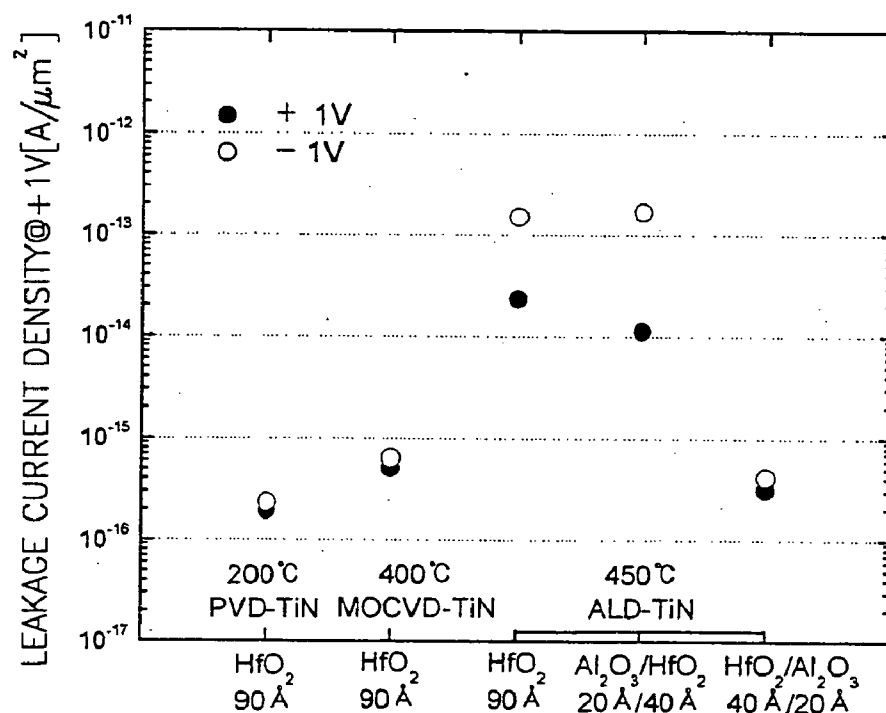


FIG. 26

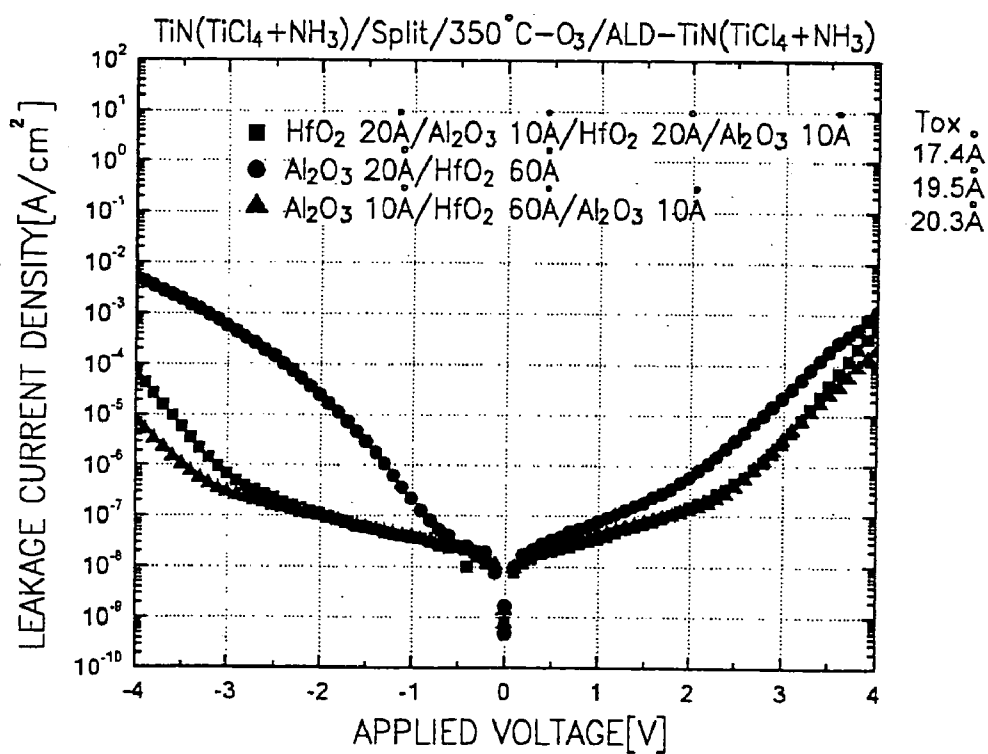




FIG. 27A

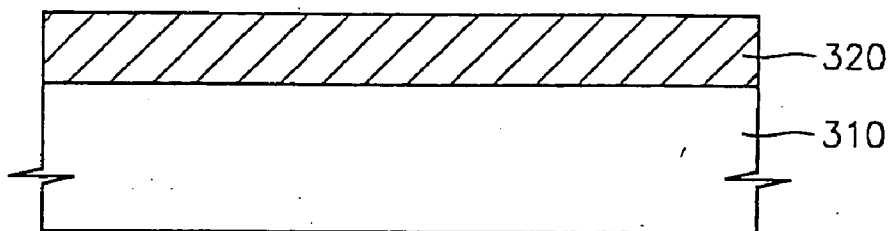


FIG. 27B

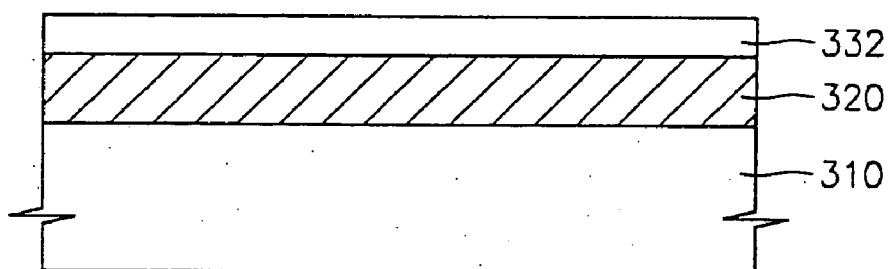


FIG. 27C

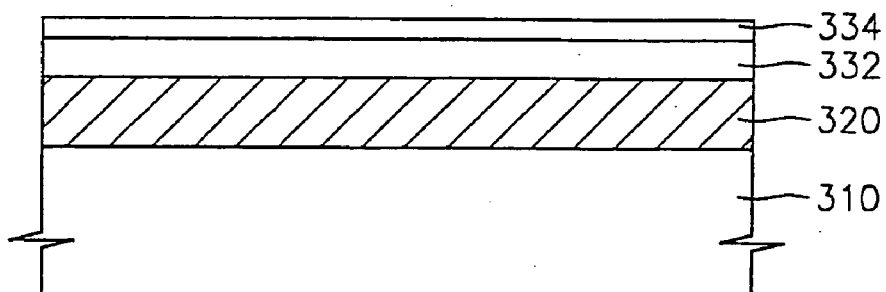


FIG. 27D

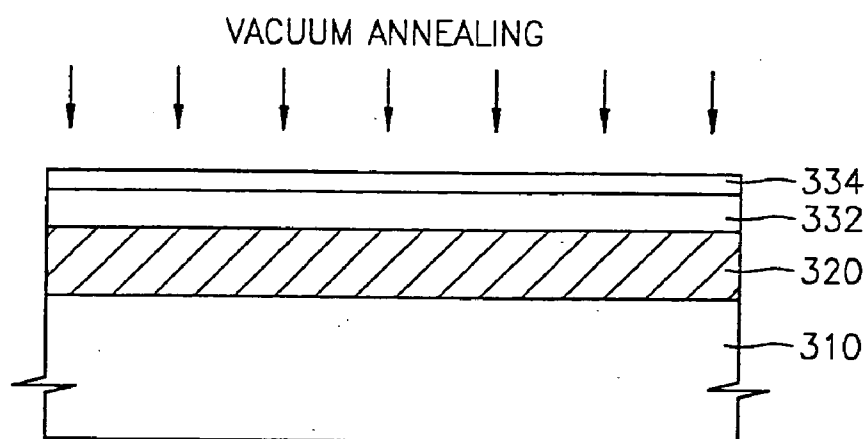


FIG. 27E

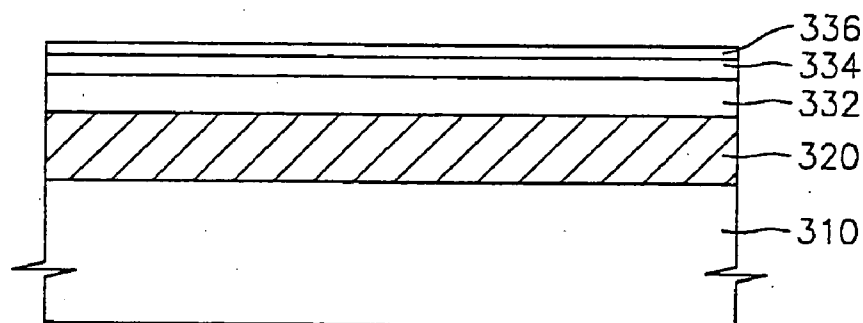
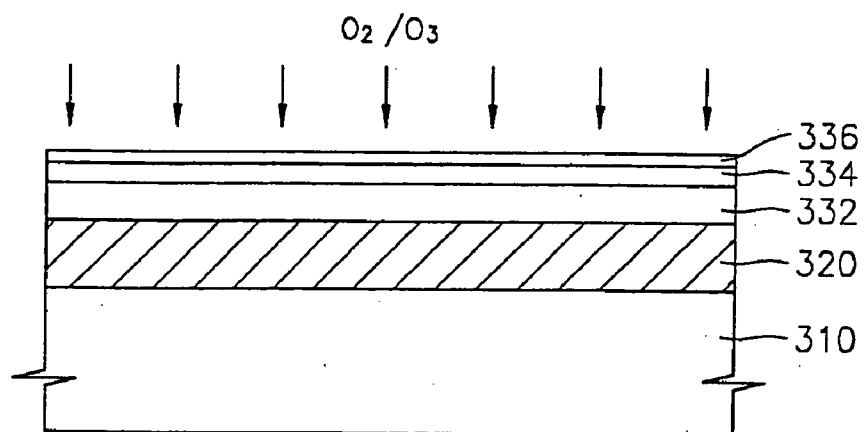
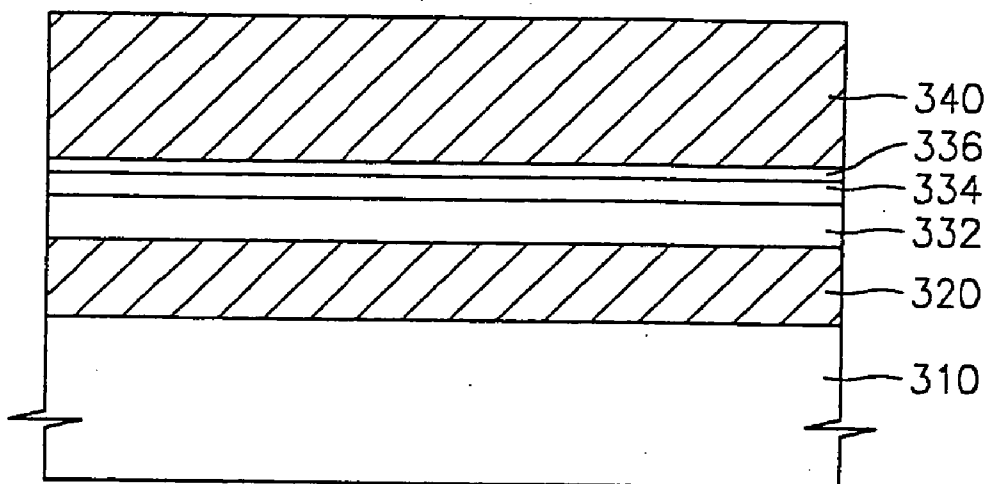


FIG. 27F



-336  
-334  
-332  
-320  
-310

FIG. 27G



## SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

[0001] This application is a Divisional of U.S. patent application Ser. No. 10/452,979, filed Jun. 2, 2003, now pending, which claims priority from Korean Patent Application No. 2002-48404, filed Aug. 16, 2002, which is incorporated by reference in its entirety.

### BACKGROUND OF THE INVENTION

#### [0002] 1. Field of the Invention

[0003] The present invention relates to semiconductor devices and, more particularly, to a semiconductor device, such as a capacitor, having enhanced electrical characteristics. The invention also relates to a method for manufacturing the same.

#### [0004] 2. Description of the Related Art

[0005] To increase the integration density of semiconductor devices, various methods have been employed. These methods include reducing the thickness of a gate or capacitor dielectric layer, or forming a high-k dielectric layer, for example, to increase capacitance.

[0006] Unfortunately, although reducing the dielectric layer thickness increases the capacitance, it also significantly increases leakage current. In addition, forming a high-k dielectric layer often requires the use of a metal electrode, because a conventional polysilicon electrode causes problems such as tunneling and increases leakage current. In the case of such a metal-insulator-metal (MIM) capacitor with a high-k dielectric layer, due to a high-speed dielectric growth process typically required for mass production, the high-k dielectric layer suffers from a substantial amount of oxygen non-stoichiometry. Thus, a thermal process in an oxygen ambient is needed to stabilize the stoichiometry in the lack of oxygen to cure defects occurring in the dielectric layer during the deposition or to remove impurities present in the dielectric layer. When such a thermal process is performed, however, oxygen atoms react with an electrode, thereby growing an unnecessary oxide layer that reduces capacitance.

[0007] To avoid the oxidation, the thermal process may be performed in a low-concentration oxygen ambient, or in an inert gas (e.g.,  $N_2$  or Ar) ambient. This process is, however, ineffective to remove impurities, such as carbon, present in the dielectric layer. Furthermore, thermo-mechanical stresses generated between the electrode and the dielectric layer during the high-temperature thermal process increase leakage current and further increase contact resistance.

[0008] Accordingly, there is an immediate need for novel thermal processing techniques to deal with problems such as described above.

### SUMMARY OF THE INVENTION

[0009] A semiconductor device and a method for forming the same are provided. According to one embodiment, a dielectric layer is formed on a semiconductor substrate or on a lower electrode of a capacitor. Vacuum annealing is performed on the dielectric layer. Thus, impurities remaining in the dielectric layer can be removed, and the dielectric layer can be effectively densified. As a result, the electrical characteristics of the semiconductor device are improved.

For example, the leakage current characteristics of the dielectric layer are improved and capacitance is increased.

### BRIEF DESCRIPTION OF THE DRAWINGS

[0010] The above objects and advantages of the present invention will become more readily apparent through the following detailed description of preferred embodiments thereof, made with reference to the attached drawings, in which:

[0011] **FIGS. 1A through 1D** are partial cross-sectional views of a semiconductor memory device illustrating a method for manufacturing a capacitor of the semiconductor memory device according to a first embodiment of the present invention;

[0012] **FIG. 2** is a graph representing the relationship between an  $HfO_2$  dielectric layer thickness and an equivalent oxide thickness (EOT) in a capacitor manufactured using the method of **FIGS. 1A through 1D**;

[0013] **FIG. 3** is a graph illustrating changes in the binding state of  $HfO_x$  when the  $HfO_2$  dielectric layer is thermally treated using a variety of techniques;

[0014] **FIG. 4** is a graph illustrating Hf binding states when the  $HfO_2$  dielectric layer is thermally treated under different conditions;

[0015] **FIG. 5A** provides a contour mapping of a capacitor region of a semiconductor memory device illustrating a reduction in the thickness of the  $HfO_2$  dielectric layer after vacuum annealing.

[0016] **FIG. 5B** is a table comparing the results of HF wet etching to illustrate the stability of the  $HfO_2$  dielectric layer densified through vacuum annealing;

[0017] **FIG. 6** is a graph comparatively showing the leakage current characteristics of the capacitor manufactured by the method of **FIGS. 1A through 1D** and those of capacitors manufactured by conventional methods;

[0018] **FIG. 7** is a graph representing capacitances of a capacitor of a semiconductor memory device when an  $HfO_2$  dielectric layer formed on a TiN lower electrode of the capacitor by atomic layer deposition (ALD) is thermally treated using different methods;

[0019] **FIGS. 8A through 8F** are partial cross-sectional views illustrating a method for manufacturing a capacitor of a semiconductor memory device according to a second embodiment of the present invention;

[0020] **FIG. 9** is a graph representing electrical characteristics of capacitors formed having a composite  $Al_2O_3/HfO_2$  dielectric layer structure using the method of **FIGS. 8A through 8F**;

[0021] **FIG. 10** is another graph showing electrical characteristics of capacitors formed having a composite  $Al_2O_3/HfO_2$  dielectric layer structure using the method of **FIGS. 8A through 8F**;

[0022] **FIG. 11** is a graph of leakage current variations in relation to the temperature of vacuum anneal performed after the formation of the composite  $Al_2O_3/HfO_2$  dielectric layer;

[0023] FIG. 12 shows current-voltage (I-V) characteristic curves illustrating temperature dependency of the electrical characteristics of capacitors having a composite  $\text{Al}_2\text{O}_3/\text{HfO}_2$  dielectric layer structure;

[0024] FIG. 13 provides current-voltage (I-V) characteristic curves showing electrical characteristic variations with respect to different thicknesses of the  $\text{HfO}_2$  dielectric layer of capacitors having a composite  $\text{Al}_2\text{O}_3/\text{HfO}_2$  dielectric layer structure vacuum annealed at  $750^\circ\text{C}$ , wherein the  $\text{Al}_2\text{O}_3$  dielectric layer has a thickness of 35 Å;

[0025] FIG. 14 is a graph showing leakage current distribution with respect to EOT at different thickness ratios between the  $\text{Al}_2\text{O}_3$  dielectric layer and the  $\text{HfO}_2$  dielectric layer of capacitors having a composite  $\text{Al}_2\text{O}_3/\text{HfO}_2$  dielectric layer structure;

[0026] FIG. 15 is a table of providing EOT data for the test samples represented in FIG. 14;

[0027] FIG. 16 is a table of leakage current data for the test samples represented in FIG. 14;

[0028] FIG. 17 is a graph of leakage current variations with respect to different thicknesses of an  $\text{HfO}_2$  dielectric layer formed on an  $\text{Al}_2\text{O}_3$  dielectric layer having a constant thickness in capacitors having the composite  $\text{Al}_2\text{O}_3/\text{HfO}_2$  dielectric layer structure manufactured according to an embodiment of the present invention;

[0029] FIG. 18 is a graph showing leakage current variations for different thicknesses of an  $\text{HfO}_2$  dielectric layer formed on a constant thickness  $\text{Al}_2\text{O}_3$  dielectric layer in a composite  $\text{Al}_2\text{O}_3/\text{HfO}_2$  dielectric layer;

[0030] FIG. 19 is a comparison graph illustrating leakage current characteristics of capacitors having a single dielectric layer made of  $\text{Al}_2\text{O}_3$ ;

[0031] FIG. 20 is a graph showing leakage current variations resulting from different thicknesses of the  $\text{Al}_2\text{O}_3$  dielectric layer in a composite  $\text{Al}_2\text{O}_3/\text{HfO}_2$  dielectric layer structure having a constant  $\text{HfO}_2$  dielectric layer thickness;

[0032] FIG. 21 is a graph illustrating leakage current variations with respect to different thicknesses of the  $\text{HfO}_2$  dielectric layer formed on a constant thickness  $\text{Al}_2\text{O}_3$  dielectric layer in capacitors having the composite  $\text{Al}_2\text{O}_3/\text{HfO}_2$  dielectric layer structure according to an embodiment of the present invention;

[0033] FIG. 22 provides atomic force microscopic (AFM) images illustrating characteristics of  $\text{HfO}_2$  layers having different thicknesses;

[0034] FIG. 23 is a graph of leakage current variations resulting from different  $\text{HfO}_2$  dielectric layer thicknesses formed on a constant thickness  $\text{Al}_2\text{O}_3$  dielectric layer in capacitors having the composite  $\text{Al}_2\text{O}_3/\text{HfO}_2$  dielectric layer structure according to an embodiment of the present invention;

[0035] FIGS. 24A through 24F are partial cross-sectional views illustrating a method for manufacturing a capacitor of a semiconductor memory device according to a third embodiment of the present invention;

[0036] FIG. 25 is a graph showing the effect of forming an upper electrode on the  $\text{HfO}_2$  dielectric layer on leakage

current characteristics of a capacitor having an  $\text{HfO}_2$  dielectric layer/ $\text{Al}_2\text{O}_3$  Cl-barrier layer structure;

[0037] FIG. 26 is a graph showing electrical characteristics of capacitors having an  $\text{HfO}_2$  dielectric layer/ $\text{Al}_2\text{O}_3$  Cl-barrier layer structure according to an embodiment of the present invention;

[0038] FIGS. 27A through 27G are partial cross-sectional views illustrating a method for manufacturing a capacitor of a semiconductor memory device according to a fourth embodiment of the present invention.

#### DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0039] It should be understood that the exemplary embodiments of the present invention described below may be modified in many different ways without departing from the inventive principles disclosed herein. The scope of the present invention is therefore not limited to these particular embodiments. Rather, these embodiments are provided by way of example and not of limitation.

[0040] In the drawings, the thicknesses of layers and regions are exaggerated for clarity. It will also be understood that when a layer is referred to as being "on" another layer or substrate, it can be directly on the other layer or substrate, or intervening layers may be present.

[0041] FIGS. 1A through 1D illustrate a method of manufacturing a capacitor of a semiconductor memory device according to a first embodiment of the present invention. Referring to FIG. 1A, a lower electrode 20 is formed on a semiconductor substrate 10 to a thickness of approximately tens to hundreds of angstroms (Å). The lower electrode 20 can be formed, for example, of polysilicon, a metal nitride, or a noble metal. For instance, the lower electrode 20 may be formed of a single layer of doped polysilicon, TiN, TaN, WN, Ru, Ir, or Pt, or a composite layer of TiN, TaN, WN, Ru, Ir, or Pt. When the lower electrode 20 is formed of doped polysilicon, the surface of the lower electrode 20 is subjected to rapid thermal nitridation (RTN) to form a silicon nitride layer (not shown) on the lower electrode 20. This prevents the lower electrode 20 from being oxidized during subsequent thermal processes.

[0042] Referring to FIG. 1B, an  $\text{HfO}_2$  dielectric layer 30 is formed on the lower electrode 20 to a thickness of about 20-200 Å. The  $\text{HfO}_2$  dielectric layer 30 can be formed by conventional techniques such as chemical vapor deposition (CVD) or atomic layer deposition (ALD). When the  $\text{HfO}_2$  dielectric layer 30 is formed using CVD, an Hf source material, for example,  $\text{HfCl}_4$ ,  $\text{Hf}(\text{OtBu})_4$ ,  $\text{Hf}(\text{NEtMe})_4$ ,  $\text{Hf}(\text{MMP})_4$ ,  $\text{Hf}(\text{NEt}_2)_4$ , or  $\text{Hf}(\text{NMe}_2)_4$ , and an oxygen gas are used at a temperature of about 400-500° C. and a pressure of about 1-5 torr. When the  $\text{HfO}_2$  dielectric layer 30 is formed using ALD,  $\text{HfCl}_4$  or a metal organic precursor (e.g.,  $\text{Hf}(\text{OtBu})_4$ ,  $\text{Hf}(\text{NEtMe})_4$ ,  $\text{Hf}(\text{MMP})_4$ ,  $\text{Hf}(\text{NEt}_2)_4$ , or  $\text{Hf}(\text{NMe}_2)_4$ ) as an HF source material, and alcohols containing  $\text{H}_2\text{O}$ ,  $\text{H}_2\text{O}_2$ , or —OH radical, or  $\text{O}_2$  or  $\text{O}_3$  plasma as an oxygen source are used at a temperature of about 150-500° C. and a pressure of about 0.1-5 torr. The deposition and removing (purging or pumping) processes are repeated, as in the conventional ALD techniques, until the  $\text{HfO}_2$  dielectric layer 30 reaches a desired thickness.

[0043] Referring to FIG. 1C, the  $\text{HfO}_2$  dielectric layer 30 is thermally treated by vacuum annealing. The vacuum

annealing is performed without supplying an inert gas or a reactant gas onto the  $\text{HfO}_2$  dielectric layer **30**. While evacuating the reaction chamber to a high vacuum level of about  $1 \times 10^{-8}$ – $1$  torr, vacuum annealing is performed on the  $\text{HfO}_2$  dielectric layer **30** at a temperature of about  $200$ – $850^\circ \text{C}$ ., (most preferably, about  $700$ – $800^\circ \text{C}$ . when the lower electrode is formed of polysilicon or about  $400$ – $600^\circ \text{C}$ . when the lower electrode is formed of a metal nitride or a noble metal). Through the vacuum annealing, impurities, such as carbon, which remain on the  $\text{HfO}_2$  dielectric layer **30**, can be effectively removed without degrading the electrical characteristics of the capacitor. The  $\text{HfO}_2$  dielectric layer **30** can therefore become effectively densified.

[0044] Referring to FIG. 1D, an upper electrode **40** is formed on the  $\text{HfO}_2$  dielectric layer **30** to a thickness of about  $50$ – $2000 \text{ \AA}$ . The upper electrode **40** can, for instance, be formed of a single layer of polysilicon, a metal nitride, a noble metal, or a composite layer of these materials. For example, the upper layer **40** may be formed of a single layer of polysilicon, TiN, TaN, WN, Ru, Ir, or Pt, or a composite layer of these materials. Suitable composite layers for the upper electrode **40** include, for example, TiN/polysilicon, TaN/polysilicon, Ru/TiN. The upper electrode **40** may be formed by ALD, CVD, or metal-organic chemical vapor deposition (MOCVD), with the MOCVD technique being more preferred. When the upper electrode **40** is formed by MOCVD, a metal organic material is used as a source metal material. Because a Cl-containing material is not used as the source material, the leakage current characteristic of the capacitor including the  $\text{HfO}_2$  dielectric layer **30** is not degraded.

[0045] FIG. 2 is a graph illustrating the relationship between the thickness of the  $\text{HfO}_2$  dielectric layer and an equivalent oxide thickness (EOT) when the  $\text{HfO}_2$  dielectric layer is formed having a variety of thicknesses on the lower electrode of TiN using the method of FIGS. 1A to 1D, followed by vacuum annealing at  $450^\circ \text{C}$ . As is apparent from FIG. 2, the  $\text{HfO}_2$  dielectric layer thickness and the EOT have a linear relationship. The  $\text{HfO}_2$  dielectric layer formed on the lower TiN electrode has a dielectric constant of 20.

[0046] FIG. 3 illustrates changes in the binding state of HfO detected by X-ray photoelectron spectroscopy (XPS) after the  $\text{HfO}_2$  dielectric layer deposited on a silicon substrate is thermally treated by a variety of techniques. Referring to FIG. 3, immediately after the deposition of the  $\text{HfO}_2$  dielectric layer (as-deposited), a CO bond appears near  $533 \text{ eV}$ . However, as the thermal treatment is performed, the CO bond disappears and a stable  $\text{HfO}_x$  bond is formed.

[0047] FIG. 4 is a graph showing the Hf binding state when the  $\text{HfO}_2$  dielectric layer is thermally treated in different conditions. When vacuum annealing is performed after the deposition of the  $\text{HfO}_2$  dielectric layer, the full width full maximum of Hf 4f7 and Hf 4f5 in the as-deposited state is reduced to result in a deep valley between the two peaks. It is believed that due to an increased number of stable  $\text{HfO}_2$  bonds, more stable  $\text{HfO}_2$  bonding is formed.

[0048] FIG. 5A shows a reduction in the thickness of the  $\text{HfO}_2$  dielectric layer after vacuum annealing. Referring to FIG. 5A, through the vacuum annealing on the  $\text{HfO}_2$  dielectric layer, the thickness of the  $\text{HfO}_2$  dielectric layer is reduced by about 10%, compared to the as-deposited state.

From this result, it is evident that the  $\text{HfO}_2$  dielectric layer becomes denser through the vacuum annealing.

[0049] FIG. 5B is a table illustrating the results of HF wet etching performed to evaluate stability of the  $\text{HfO}_2$  dielectric layer after undergoing the vacuum annealing. To investigate whether the stable bond remains in the  $\text{HfO}_2$  dielectric layer densified through vacuum annealing, wet etching is performed on the  $\text{HfO}_2$  dielectric layer in a HF etchant, after the deposition of the  $\text{HfO}_2$  dielectric layer, and after vacuum annealing on the  $\text{HfO}_2$  dielectric layer at  $750^\circ \text{C}$ . for 2 minutes. The thickness of the  $\text{HfO}_2$  dielectric layer was measured before and after the wet etching and is shown in the table together with the etching rate. Referring to FIG. 5B, when the wet etching is performed in the as-deposited state, most of the  $\text{HfO}_2$  dielectric layer was etched. In contrast, when the wet etching is performed after vacuum annealing, the thickness of the  $\text{HfO}_2$  dielectric layer remains substantially unchanged. The results shown in FIGS. 3, 4, 5A and 5B, demonstrate that the  $\text{HfO}_2$  dielectric layer is further stabilized through vacuum annealing.

[0050] FIG. 6 is a graph comparing leakage current characteristics of capacitors when the  $\text{HfO}_2$  dielectric layer is thermally treated by vacuum annealing when the  $\text{HfO}_2$  dielectric layer is thermally treated by other techniques. In FIG. 6, the EOT for each case is shown. To measure the leakage current characteristics, an  $\text{HfO}_2$  dielectric layer is formed to a thickness of  $90 \text{ \AA}$  on a lower electrode. The lower electrode is formed of a  $200 \text{ \AA}$  thick TiN layer. The  $\text{HfO}_2$  dielectric layer is then thermally treated by a variety of methods. An upper electrode is formed of an  $800 \text{ \AA}$  thick TiN layer on the thermally treated  $\text{HfO}_2$  dielectric layer. As shown, when the  $\text{HfO}_2$  dielectric layer is thermally treated in an  $\text{O}_3$  condition, the leakage current characteristic is significantly degraded, and the EOT is increased. When the  $\text{HfO}_2$  dielectric layer is thermally treated in an  $\text{O}_2$  condition and a  $\text{N}_2$  condition, the EOT does not increase, but the leakage current characteristic degrades, compared with the case where the vacuum annealing is performed.

[0051] FIG. 7 is a graph showing capacitance when the  $\text{HfO}_2$  dielectric layer formed on the TiN lower electrode by ALD is thermally treated using different methods. When the  $\text{HfO}_2$  dielectric layer is thermally treated in an  $\text{O}_3$  condition, the oxygen atoms easily permeate the  $\text{HfO}_2$  dielectric layer even at a low temperature to reach the interface between the  $\text{HfO}_2$  dielectric layer and the TiN lower electrode. Thus, the TiN lower electrode can be easily oxidized. Accordingly, capacitance degradation, and micro lifting between the lower electrode and the  $\text{HfO}_2$  dielectric layer occur. As a result, leakage current increases. In contrast, when the  $\text{HfO}_2$  dielectric layer is thermally treated in a  $\text{N}_2$  ambient or an  $\text{O}_2$  ambient, capacitance is not degraded. Negative leakage current is greatly increased, however, as compared with vacuum annealing.

[0052] FIGS. 8A through 8F are partial cross-sectional views illustrating a method for manufacturing a capacitor of a semiconductor memory device according to a second embodiment of the present invention. Referring to FIG. 8A, a lower electrode **120** is formed on a semiconductor substrate **110** to an approximate thickness of tens to hundreds of angstroms ( $\text{\AA}$ ). The lower electrode **120** can be formed using the same or similar methods described above.

[0053] Referring to FIG. 8B, an  $\text{Al}_2\text{O}_3$  dielectric layer **132** is formed on the lower electrode **120**. Preferably, the  $\text{Al}_2\text{O}_3$

dielectric layer is formed to a thickness of about 20-60 Å. It is preferable that the  $\text{Al}_2\text{O}_3$  dielectric layer be thicker than an  $\text{HfO}_2$  dielectric layer to be formed in a subsequent process. The reason for this will be described later.

[0054] The  $\text{Al}_2\text{O}_3$  dielectric layer 132 may be formed by ALD. In this case, the  $\text{Al}_2\text{O}_3$  dielectric layer 132 is deposited using trimethyl aluminium (TMA) as a first reactant and  $\text{O}_3$  as a second reactant at a temperature of about 200-500° C. and a pressure of about 0.1-5 torr. The deposition and removing (purging or pumping) processes are repeated, as in the conventional ALD techniques, until the  $\text{Al}_2\text{O}_3$  dielectric layer reaches a desired thickness. Suitable first reactants for the  $\text{Al}_2\text{O}_3$  dielectric layer 132 include, for example,  $\text{AlCl}_3$ ,  $\text{AlH}_3\text{N}(\text{CH}_3)_3$ ,  $\text{C}_6\text{H}_{15}\text{AlO}$ ,  $(\text{C}_4\text{H}_9)_2\text{AlH}$ ,  $(\text{CH}_3)_2\text{AlCl}$ ,  $(\text{C}_2\text{H}_5)_3\text{Al}$ , or  $(\text{C}_4\text{H}_9)_3\text{Al}$ , as well as TMA.  $\text{H}_2\text{O}$ ,  $\text{H}_2\text{O}_2$ , or an activated oxidizing agent, such as plasma  $\text{N}_2\text{O}$ , plasma  $\text{O}_2$ , may be used as the second reactant. When the  $\text{Al}_2\text{O}_3$  dielectric layer is formed using  $\text{H}_2\text{O}$  as the second reactant, the device reliability increases, although the dielectric constant and leakage current characteristic are similar to those when  $\text{O}_3$  is used as the second reactant.

[0055] Referring to FIG. 8C, an  $\text{HfO}_2$  dielectric layer 134 is formed on the  $\text{Al}_2\text{O}_3$  dielectric layer 132 to form a composite dielectric layer of  $\text{Al}_2\text{O}_3/\text{HfO}_2$ . The composite dielectric layer of  $\text{Al}_2\text{O}_3/\text{HfO}_2$  has a high dielectric constant and improved leakage current characteristics over the single  $\text{Al}_2\text{O}_3$  dielectric layer, which has good leakage current characteristic but a low dielectric constant, and the single  $\text{HfO}_2$  dielectric layer, which has a high dielectric constant but poor leakage current characteristics. In other words, the electrical characteristics of the capacitor can be improved by forming a composite  $\text{Al}_2\text{O}_3/\text{HfO}_2$  dielectric layer. The  $\text{HfO}_2$  dielectric layer 134 may be formed using the same or similar method described with reference to FIG. 1B. Preferably, the  $\text{HfO}_2$  dielectric layer 134 is formed to a thickness of about 10-60 Å. As described above, it is preferable that the  $\text{HfO}_2$  dielectric layer 134 be formed thinner than the  $\text{Al}_2\text{O}_3$  dielectric layer 132.

[0056] Referring to FIG. 8D, vacuum annealing is performed on the  $\text{HfO}_2$  dielectric layer 134. The vacuum annealing of FIG. 8D is performed using the same or similar method described previously with reference to FIG. 1C. Through vacuum annealing, impurities, such as carbon, which remain on the  $\text{HfO}_2$  dielectric layer 134, can be effectively removed, and the  $\text{HfO}_2$  dielectric layer 134 can become effectively densified.

[0057] Referring to FIG. 8E, the vacuum-annealed  $\text{HfO}_2$  dielectric layer 134 can optionally be thermally treated at a temperature of about 200-600° C., and preferably, about 300-400° C. (Alternatively, the thermal treatment in the oxygen condition is performed before the vacuum annealing described with reference to FIG. 8D.) The  $\text{HfO}_2$  dielectric layer 134 is thermally treated at a pressure of about 5-50 torr in the  $\text{O}_3$  plasma condition, or at a pressure of about 0.1-5 torr in the  $\text{O}_2$  plasma condition. When the thermal treatment is performed in an oxygen condition, as described above with reference to FIG. 8E, the oxidation of the lower electrode 120 due to oxygen diffusion is a concern. However, the oxygen diffusion can be effectively blocked by the  $\text{Al}_2\text{O}_3$  dielectric layer 132 and the densified  $\text{HfO}_2$  dielectric layer 134. Thus, the lower electrode 120 is not oxidized. Specifically, when the lower electrode 120 is formed of

metal, such as a metal nitride or a noble metal, the composite layered structure of the  $\text{Al}_2\text{O}_3$  dielectric layer 132 and the  $\text{HfO}_2$  dielectric layer 134 protects the lower electrode 120 from being oxidized.

[0058] Referring to FIG. 8F, an upper electrode 140 is formed on the  $\text{HfO}_2$  dielectric layer 134 thermally treated in a vacuum or oxygen condition, to a thickness of about 50-2000 Å. The upper electrode 140 may be formed using the same or similar methods described above. As stated above, when the upper electrode 140 is formed by MOCVD, a metal organic material is used as a source metal material. Because a Cl-containing material is not used as the source material, leakage current characteristic of the capacitor including the  $\text{HfO}_2$  dielectric layer 134 is not degraded.

[0059] FIG. 9 is a graph illustrating electrical characteristics of a capacitor having a composite  $\text{Al}_2\text{O}_3/\text{HfO}_2$  dielectric layer. For the electrical characteristics measurement of FIG. 9, after a lower electrode was formed of a phosphorus-doped polysilicon layer, a silicon nitride layer was grown on the lower electrode by RTN. After  $\text{Al}_2\text{O}_3$  and  $\text{HfO}_2$  dielectric layers are sequentially formed, vacuum annealing is performed at 750° C. Next, an upper electrode is formed of a stacked TiN/polysilicon layer structure and annealed at 650° C. for activation. The resultant structure was subjected to photolithography and etching processes to complete a capacitor structure having an aspect ratio of about 10:1. The electrical characteristics thereof were then measured. As shown in FIG. 9, when the composite  $\text{Al}_2\text{O}_3/\text{HfO}_2$  dielectric layer is thermally treated by vacuum annealing, electrical characteristics including leakage current characteristics are improved, compared with the as-deposited state.

[0060] FIG. 10 is a graph illustrating electrical characteristics of capacitors formed having the composite  $\text{Al}_2\text{O}_3/\text{HfO}_2$  dielectric layer that are thermally treated using different methods. As shown in FIG. 10, when the composite  $\text{Al}_2\text{O}_3/\text{HfO}_2$  dielectric layer is thermally treated by vacuum annealing, the electrical characteristics are further improved as compared with when the composite  $\text{Al}_2\text{O}_3/\text{HfO}_2$  dielectric layer is thermally treated by  $\text{O}_2$  annealing. The leakage current characteristics between vacuum annealing and  $\text{O}_2$  annealing are almost the same, but the capacitance is improved by about 10% when vacuum annealing is applied.

[0061] FIG. 11 is a graph of leakage current variations in capacitors having a composite  $\text{Al}_2\text{O}_3/\text{HfO}_2$  dielectric layer in relation to a temperature of vacuum annealing performed after the formation of the composite  $\text{Al}_2\text{O}_3/\text{HfO}_2$  dielectric layer. For the measurement of the leakage current variations of FIG. 11, test samples were manufactured in the same conditions in FIG. 9, except for the vacuum thermal treatment conditions. Referring to FIG. 11, in the vacuum thermal treatment conditions indicated by an arrow "A", the EOT and leakage current are relatively small, thereby evidencing improved electrical characteristics of the capacitors.

[0062] FIG. 12 shows current-voltage (I-V) characteristic curves of capacitors having a composite  $\text{Al}_2\text{O}_3/\text{HfO}_2$  dielectric layer, for evaluating temperature dependency of electrical characteristics of the capacitors. From FIG. 12, it appears that the temperature dependency of the leakage current is apparently negligible up to 125° C.

[0063] FIG. 13 includes I-V characteristic curves showing electrical characteristic variations with respect to different

thicknesses of the  $\text{HfO}_2$  dielectric layer of a composite  $\text{Al}_2\text{O}_3/\text{HfO}_2$  dielectric layer. In this graph, vacuum annealing is performed at  $750^\circ\text{C}$ ., and the  $\text{Al}_2\text{O}_3$  dielectric layer has a thickness of  $35\text{ \AA}$ . Referring to FIG. 13, as the thickness ratio of the  $\text{Al}_2\text{O}_3$  dielectric layer and  $\text{HfO}_2$  dielectric layer is varied, the leakage current characteristic and the EOT change. The applicants evaluated the correlation between the  $\text{Al}_2\text{O}_3$  dielectric layer thickness and the  $\text{HfO}_2$  dielectric layer thickness as follows to ascertain a preferred thickness ratio of the  $\text{Al}_2\text{O}_3$  dielectric layer and the  $\text{HfO}_2$  dielectric layer.

[0064] FIG. 14 is a graph representing leakage current distribution with respect to the EOT at different thickness ratios between an  $\text{Al}_2\text{O}_3$  dielectric layer and an  $\text{HfO}_2$  dielectric layer of capacitors having a composite  $\text{Al}_2\text{O}_3/\text{HfO}_2$  dielectric layer structure. Referring to FIG. 14, in the region surrounded by circle "A", the composite  $\text{Al}_2\text{O}_3/\text{HfO}_2$  dielectric layer structures have an  $\text{Al}_2\text{O}_3$  dielectric layer whose thickness is greater than that of the  $\text{HfO}_2$  dielectric layer. These structures show degradation of leakage current characteristics. In contrast, the composite  $\text{Al}_2\text{O}_3/\text{HfO}_2$  dielectric layer structures shown along a dashed line "B" have a normal leakage current distribution.

[0065] FIGS. 15 and 16 are tables showing the test data of FIG. 14, indicating leakage current degradation occurs with respect to the thickness ratio of the  $\text{Al}_2\text{O}_3$  dielectric layer and the  $\text{HfO}_2$  dielectric layer. The data in FIG. 15 indicate the EOT of each of the sample capacitors, and that of FIG. 16 indicates the leakage current of each of the sample capacitors. In FIGS. 15 and 16, data from circle "A" of FIG. 14 are expressed as "leakage current degradation", and data from dashed line "B" of FIG. 14 are expressed as "normal leakage current".

[0066] FIG. 17 is a graph of leakage current variations with respect to different thicknesses of an  $\text{HfO}_2$  dielectric layer formed on an  $\text{Al}_2\text{O}_3$  dielectric layer having a constant thickness of  $20\text{ \AA}$ . In FIG. 17, when a thickness ratio between the  $\text{Al}_2\text{O}_3$  dielectric layer and the  $\text{HfO}_2$  dielectric layer is less than 1.0 (i.e., when the thickness of the  $\text{Al}_2\text{O}_3$  dielectric layer is smaller than that of  $\text{HfO}_2$  dielectric layer), the leakage current characteristics degrade. When a thickness ratio between the  $\text{Al}_2\text{O}_3$  dielectric layer and the  $\text{HfO}_2$  dielectric layer is greater than 1.0 (i.e., when the thickness of the  $\text{Al}_2\text{O}_3$  dielectric layer is greater than that of  $\text{HfO}_2$  dielectric layer), leakage current characteristics are improved.

[0067] FIG. 18 is a graph of leakage current variations with respect to different thicknesses of an  $\text{HfO}_2$  dielectric layer formed on an  $\text{Al}_2\text{O}_3$  dielectric layer having a thickness of  $35\text{ \AA}$ . In FIG. 18, when a thickness ratio between the  $\text{Al}_2\text{O}_3$  dielectric layer and the  $\text{HfO}_2$  dielectric layer is less than 1.0, the leakage current characteristics degrade. When a thickness ratio between the  $\text{Al}_2\text{O}_3$  dielectric layer and the  $\text{HfO}_2$  dielectric layer is greater than 1.0, the leakage current characteristics are improved.

[0068] FIG. 19 is a comparison graph showing leakage current characteristics of capacitors having a single  $\text{Al}_2\text{O}_3$  dielectric layer. Referring to FIG. 19, as the thickness of the  $\text{Al}_2\text{O}_3$  dielectric layer is reduced, the EOT is reduced. The leakage current of the dielectric layer greatly increases when the  $\text{Al}_2\text{O}_3$  dielectric layer has a thickness of about  $35\text{ \AA}$  or less. From the results of FIG. 19, when the dielectric layer

is constructed of only an  $\text{Al}_2\text{O}_3$  layer, it is apparent that there is a limit to the amount by which the EOT of the dielectric layer can be reduced, namely, to an EOT of about  $30\text{ \AA}$ , considering the leakage current characteristics of the  $\text{Al}_2\text{O}_3$  layer.

[0069] FIG. 20 is a graph illustrating leakage current variations with respect to different thicknesses of an  $\text{Al}_2\text{O}_3$  dielectric layer in a composite  $\text{Al}_2\text{O}_3/\text{HfO}_2$  dielectric layer, in which the  $\text{HfO}_2$  dielectric layer has a constant thickness of  $20\text{ \AA}$ . In FIG. 20, when the  $\text{Al}_2\text{O}_3$  dielectric layer has a thickness of  $20\text{ \AA}$  and  $25\text{ \AA}$ , the leakage current greatly increases in a voltage region of  $2\text{V}$  or less. When the  $\text{Al}_2\text{O}_3$  dielectric layer has a thickness of  $30\text{ \AA}$  and  $35\text{ \AA}$ , the leakage current characteristics are similar to that of a single  $\text{Al}_2\text{O}_3$  dielectric layer although the composite  $\text{Al}_2\text{O}_3/\text{HfO}_2$  dielectric layer structure has a smaller EOT.

[0070] FIG. 21 is a graph of leakage current variations with respect to different thicknesses of an  $\text{HfO}_2$  dielectric layer formed on an  $\text{Al}_2\text{O}_3$  dielectric layer having a constant thickness of  $30\text{ \AA}$ . In FIG. 21, as the thickness of the  $\text{HfO}_2$  dielectric layer is increased, leakage current decreases. Although the degree of improvement in leakage current characteristic is very small, compared with increasing the thickness of the  $\text{Al}_2\text{O}_3$  dielectric layer, it should be noted that increasing the thickness of the  $\text{HfO}_2$  dielectric layer does not greatly affect the EOT.

[0071] Accordingly, leakage current characteristics of a capacitor having a composite  $\text{Al}_2\text{O}_3/\text{HfO}_2$  dielectric layer is largely dependent upon the  $\text{Al}_2\text{O}_3$  dielectric layer thickness, rather the  $\text{HfO}_2$  dielectric layer thickness. To obtain stable leakage current characteristics in the capacitor having a composite  $\text{Al}_2\text{O}_3/\text{HfO}_2$  dielectric layer, it is therefore preferable to provide the  $\text{Al}_2\text{O}_3$  dielectric layer acting as an oxygen barrier layer with a thickness of  $30\text{ \AA}$  or greater.

[0072] In general, as the deposition thickness of the  $\text{HfO}_2$  layer is increased, crystallization occurs during the deposition, which can be identified using an atomic force microscope (AFM). FIG. 22 shows AFM images for different thicknesses of the  $\text{HfO}_2$  layer. As shown in FIG. 22, when the  $\text{HfO}_2$  layer has a thickness of  $60\text{ \AA}$ , surface roughness greatly increases. As the thickness of the  $\text{HfO}_2$  layer increases, partial crystallization occurs within the  $\text{HfO}_2$  layer. Also, the crystallized portion of the  $\text{HfO}_2$  layer grows at a relatively high rate as compared with an amorphous  $\text{HfO}_2$  layer. As is apparent from the AFM images of FIG. 22, when the  $\text{HfO}_2$  layer has a thickness of  $60\text{ \AA}$ , the  $\text{HfO}_2$  layer becomes sharp and rough, thereby increasing surface roughness. According to the results of the AFM analysis, crystallization of the  $\text{HfO}_2$  layer is initiated at a thickness of about  $50\text{ \AA}$ .

[0073] FIG. 23 is a graph showing leakage current variations for different thicknesses of an  $\text{HfO}_2$  dielectric layer formed on a constant thickness  $\text{Al}_2\text{O}_3$  dielectric layer ( $25\text{ \AA}$ ). Although it was expected that the leakage current characteristics would be further improved by increasing the thickness of the  $\text{HfO}_2$  dielectric layer, FIG. 23 shows that the leakage current characteristic is instead degraded as the thickness of the  $\text{HfO}_2$  dielectric layer is increased. This is believed to be a result of the crystallization of the  $\text{HfO}_2$  dielectric layer. In other words, as the thickness of the  $\text{HfO}_2$  dielectric layer is increased, crystalline  $\text{HfO}_2$  grains begin to grow. As the  $\text{HfO}_2$  grains grow into the  $\text{Al}_2\text{O}_3$  layer of the



composite  $\text{Al}_2\text{O}_3/\text{HfO}_2$  dielectric layer structure, they act as leakage current paths within the dielectric layer to degrade the leakage current characteristics thereby.

[0074] The results of the above measurements, indicate that to reduce leakage current in a capacitor having a composite  $\text{Al}_2\text{O}_3/\text{HfO}_2$  dielectric layer structure, the thickness of the  $\text{HfO}_2$  dielectric layer is preferably smaller than the thickness at which crystallization of the  $\text{HfO}_2$  layer is initiated. For example, the thickness is preferably about 40 Å or less, e.g., about 10-40 Å.

[0075] FIGS. 24A through 24F are partial cross-sectional views illustrating a method of manufacturing a capacitor of a semiconductor memory device according to a third embodiment of the present invention.

[0076] When forming a capacitor upper electrode using a source gas containing chlorine atoms, such as  $\text{TiCl}_4$ , leakage current characteristics tend to significantly degrade the operation of a capacitor having an  $\text{HfO}_2$  dielectric layer. Therefore, to improve the leakage current characteristics of the capacitor in which the upper electrode is formed using a Cl-containing source gas, a method for blocking the effect of the Cl atoms is desirable.

[0077] Referring to FIG. 24A, a lower electrode 220 is preferably formed on a semiconductor substrate 210 having a thickness in a range of about tens to hundreds of angstroms (Å). The lower electrode 220 may be formed using the same or similar methods as described above. Referring to FIG. 24B, an  $\text{HfO}_2$  dielectric layer 232 is formed on the lower electrode 220. The  $\text{HfO}_2$  dielectric layer 232 may be formed using the same or similar method as described with reference to FIG. 1B. For example, the  $\text{HfO}_2$  dielectric layer 232 preferably has a thickness of about 20-80 Å.

[0078] Referring to FIG. 24C, the  $\text{HfO}_2$  dielectric layer 232 is preferably thermally treated by vacuum annealing. The vacuum annealing can be performed using the same or similar method as described with reference to FIG. 1C. Through vacuum annealing, impurities, such as carbon, which remain on the  $\text{HfO}_2$  dielectric layer 232 can be effectively removed, and the  $\text{HfO}_2$  dielectric layer 232 can be effectively densified.

[0079] Referring to FIG. 24D, a Cl barrier layer 234 is formed on the  $\text{HfO}_2$  dielectric layer 232 thermally treated by vacuum annealing. When a Cl-containing gas such as  $\text{TiCl}_4$  is used to form an upper electrode of the capacitor including an  $\text{HfO}_2$  dielectric layer, the leakage current characteristics of the capacitor become significantly degraded. In this embodiment, the Cl barrier layer 234 is formed on the  $\text{HfO}_2$  dielectric layer 232 to block the adverse effect of Cl atoms on the upper electrode. The Cl barrier layer 234 can be formed, for example, of  $\text{Al}_2\text{O}_3$ ,  $\text{Ta}_2\text{O}_5$ ,  $\text{SiO}_2$ , or  $\text{Si}_3\text{N}_4$ . The Cl barrier layer 234 is preferably formed to a thickness of about 3-50 Å and, most preferably, to a thickness of about 10-20 Å.

[0080] The Cl barrier layer 234 is formed by CVD or ALD. When the Cl barrier layer 234 is formed of  $\text{Al}_2\text{O}_3$  using CVD, the Cl barrier layer 234 is deposited, for example, using TMA and  $\text{H}_2\text{O}$  at a temperature of about 400-500° C. and a pressure of about 1-5 torr. When the Cl barrier layer 234 is formed of  $\text{Al}_2\text{O}_3$  using ALD, the Cl barrier layer 234 is preferably deposited using TMA as a first reactant and  $\text{O}_3$  as a second reactant at a temperature of

about 250-400° C. and a pressure of about 1-5 torr. The deposition and purging processes are repeated until an  $\text{Al}_2\text{O}_3$  layer reaches the desired thickness. Suitable first reactants for the  $\text{Al}_2\text{O}_3$  layer include, for example,  $\text{AlCl}_3$ ,  $\text{AlH}_3\text{N}(\text{CH}_3)_3$ ,  $\text{C}_6\text{H}_{15}\text{AlO}$ ,  $(\text{C}_4\text{H}_9)_2\text{AlH}$ ,  $(\text{CH}_3)_2\text{AlCl}$ ,  $(\text{C}_2\text{H}_5)_3\text{Al}$ , or  $(\text{C}_4\text{H}_9)_3\text{Al}$ , as well as TMA.  $\text{H}_2\text{O}$ , or an activated oxidizing agent, such as plasma  $\text{N}_2\text{O}$ , plasma  $\text{O}_2$ , may be used as the second reactant.

[0081] Referring to FIG. 24E, the resultant structure having the Cl barrier layer 234 is thermally treated in an  $\text{O}_3$  or  $\text{O}_2$  plasma condition at a temperature of about 250-400° C., and preferably, about 300-400° C. This step can be omitted.

[0082] The Cl barrier layer 234 is thermally treated at a pressure of about 5-50 torr in the  $\text{O}_3$  plasma condition and at a pressure of about 0.1-5 torr in the  $\text{O}_2$  plasma condition.

[0083] Referring to FIG. 24F, an upper electrode 240 is formed on the Cl barrier layer 234 thermally treated in the oxygen condition, to a thickness of about 50-2000 Å. The upper electrode 240 is formed of polysilicon, a metal nitride, or a noble metal. For example, the upper electrode 240 may be formed of a single layer of polysilicon, TiN, TaN, WN, Ru, Ir, or Pt, or a composite layer of these materials. The upper electrode 240 is preferably formed using ALD, CVD, or MOCVD.

[0084] FIG. 25 is a graph showing how forming the upper electrode on the  $\text{HfO}_2$  dielectric layer affects the leakage current characteristics of a capacitor having an  $\text{HfO}_2$  dielectric layer/ $\text{Al}_2\text{O}_3$  Cl-barrier layer structure. Leakage current characteristics for a single  $\text{HfO}_2$  dielectric layer formed by ALD, where the Cl barrier layer was not formed, having an upper electrode formed by a variety of methods, are shown for comparison.

[0085] From FIG. 25, it is evident that the leakage current characteristics of the capacitor are largely dependent upon the method used to form the upper electrode. When the upper electrode ("ALD-TiN") is formed of TiN on the  $\text{HfO}_2$  dielectric layer by ALD using  $\text{TiCl}_4$  and  $\text{NH}_3$  as reactant gases, the leakage current characteristics become significantly degraded. The leakage current characteristic degradation results from Cl radicals generated when the TiN upper electrode is formed by ALD. Therefore, when the upper electrode is directly formed on the  $\text{HfO}_2$  dielectric layer, a physical vapor deposition (PVD) or MOCVD method is desirable to avoid the effect of the Cl radicals on the upper electrode. In a capacitor having an  $\text{HfO}_2$  dielectric layer/ $\text{Al}_2\text{O}_3$  Cl-barrier layer structure, leakage current degradation is prevented by an  $\text{Al}_2\text{O}_3$  Cl-barrier layer while an upper electrode is formed by ALD.

[0086] FIG. 26 is a graph of electrical characteristics of capacitors having the  $\text{Al}_2\text{O}_3$  Cl-barrier layer formed on the  $\text{HfO}_2$  dielectric layer. As shown in FIG. 26, when the TiN upper electrode formed by ALD using  $\text{TiCl}_4$  and  $\text{NH}_3$  as reactant gases contacts the  $\text{Al}_2\text{O}_3$  Cl-barrier layer, the leakage current characteristics are improved when compared with the situation in which the TiN upper electrode directly contacts the  $\text{HfO}_2$  dielectric layer. The  $\text{Al}_2\text{O}_3$  layer, therefore, effectively blocks the Cl radicals during the formation of the upper electrode.

[0087] FIGS. 27A through 27G are partial cross-sectional views illustrating a method for manufacturing a capacitor of a semiconductor memory device according to a

fourth embodiment of the present invention. Referring to **FIG. 27A**, a lower electrode **320** is formed on a semiconductor substrate **310** to a thickness of about tens to hundreds of angstroms (Å). The lower electrode **320** may be formed using the same or similar methods described above.

[0088] Referring to **FIG. 27B**, an  $\text{Al}_2\text{O}_3$  dielectric layer **332** is formed on the lower electrode **320**. The  $\text{Al}_2\text{O}_3$  dielectric layer **332** prevents the lower electrode **320** from being oxidized during subsequent thermal treatment on the dielectric layer when the lower electrode **320** is formed of a metal layer, such as a metal nitride or a noble metal. The  $\text{Al}_2\text{O}_3$  dielectric layer **332** is preferably formed using the method as described with reference to **FIG. 8B**.

[0089] Referring to **FIG. 27C**, an  $\text{HfO}_2$  dielectric layer **334** is formed on the  $\text{Al}_2\text{O}_3$  dielectric layer **332**. The  $\text{HfO}_2$  dielectric layer **334** may be formed using the same method as described with reference to **FIG. 1B** or **8C**.

[0090] Referring to **FIG. 27D**, the  $\text{HfO}_2$  dielectric layer **334** is thermally treated by vacuum annealing. Vacuum annealing is preferably performed using the same method described previously with reference to **FIG. 1C**. Through vacuum annealing, impurities, such as carbon, remaining on the  $\text{HfO}_2$  dielectric layer **334** can be effectively removed, and the  $\text{HfO}_2$  dielectric layer **334** can be effectively densified.

[0091] Referring to **FIG. 27E**, a Cl barrier layer **336** is formed on the  $\text{HfO}_2$  dielectric layer **334** thermally treated by vacuum annealing. The Cl barrier layer **336** is formed using the method described previously with reference to **FIG. 24D**. The formation of the Cl barrier layer **336** blocks the adverse effect of Cl atoms on the upper electrode to be formed in a subsequent process. The Cl barrier layer **336** is formed of, for example,  $\text{Al}_2\text{O}_3$ ,  $\text{Ta}_2\text{O}_5$ ,  $\text{SiO}_2$ , or  $\text{Si}_3\text{N}_4$ . Referring to **FIG. 27E**, the resultant structure having the Cl barrier layer **336** formed by the method described with reference to **FIG. 24E** can then optionally be thermally treated in an  $\text{O}_3$  or  $\text{O}_2$  plasma condition.

[0092] Referring to **FIG. 27G**, an upper electrode **340** is formed to a thickness of about 50-2000 Å on the Cl barrier layer **336**. The upper electrode **340** can be formed of polysilicon, a metal nitride, or a noble metal. For example, the upper layer **340** may be a single layer of doped polysilicon, TiN, TaN, WN, Ru, Ir, or Pt, or a composite layer of these materials. The upper electrode **340** is preferably formed by ALD, CVD, or MOCVD. Although the upper electrode **240** is deposited using a Cl-containing source material, such as  $\text{TiCl}_4$ ,  $\text{TaCl}_5$ ,  $\text{WCl}_6$ , the Cl barrier layer **336** effectively blocks the Cl atoms.

[0093] In the above embodiment, because the  $\text{Al}_2\text{O}_3$  dielectric layer **332** is formed between the lower electrode **320** and the  $\text{HfO}_2$  dielectric layer **334**, and the Cl barrier layer **336** is formed between the  $\text{HfO}_2$  dielectric layer **334** and the upper electrode **340**, the lower electrode **320** can be effectively protected from oxidation during subsequent thermal treatment on the dielectric layer. The adverse effect of the Cl atoms during the formation of the upper electrode **340** can thereby be eliminated. Also, the formation of the  $\text{HfO}_2$  dielectric layer **334** is followed by vacuum thermal treatment, so that impurities can be effectively removed from the  $\text{HfO}_2$  dielectric layer **334**, and the leakage current characteristics of the dielectric layer can be stably maintained.

[0094] In the above-described embodiments, the method for forming a dielectric layer including a  $\text{HfO}_2$  dielectric layer and the subsequent vacuum annealing method have been described in connection with the manufacture of a capacitor of a semiconductor memory device. The embodiments are not, however, intended to limit the scope of the present invention. Rather, the principles of the present invention can be applied to any other highly-integrated semiconductor devices, as long as a dielectric layer is involved. For example, the methods are applicable to the formation of a gate stack including a gate dielectric formed on a semiconductor substrate. In addition, although the vacuum annealing methods have been described with reference to the  $\text{HfO}_2$  dielectric layer in the above embodiments, those skilled in the art will appreciate that vacuum annealing can be performed on a variety of other high-k dielectric layers such as  $\text{Y}_2\text{O}_3$ ,  $\text{Al}_2\text{O}_3$ ,  $\text{TiO}_2$ , BaO, SrO,  $\text{ZrO}_2$ ,  $\text{Ta}_2\text{O}_5$ ,  $\text{Nb}_2\text{O}_5$ , whether as a single layer or a composite layer of these materials.

[0095] Also, the Cl barrier layer can be formed on dielectric layers other than the  $\text{HfO}_2$  dielectric layer and effectively block Cl atoms when the capacitor upper electrode is formed using a Cl-containing source material.

[0096] In conclusion, with embodiments of the present invention, among other things, impurities remaining in the dielectric layer can be effectively removed, and the dielectric layer can be effectively densified. As a result, electrical characteristics of the semiconductor device can be significantly improved. For example, the leakage current is reduced and capacitance is increased.

[0097] While this invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims.

What is claimed is:

1. A method for forming a dielectric layer, the method comprising:

introducing a first reactant into a chamber;

removing the remaining first reactant from the chamber by pumping or purging;

introducing a second reactant into the chamber;

removing the remaining second reactant from the chamber to form a dielectric layer on a semiconductor substrate; and

vacuum annealing the dielectric layer.

2. The method of claim 1, wherein the dielectric layer is a single layer of  $\text{Y}_2\text{O}_3$ ,  $\text{Al}_2\text{O}_3$ ,  $\text{TiO}_2$ , BaO, SrO,  $\text{ZrO}_2$ ,  $\text{Ta}_2\text{O}_5$ ,  $\text{Nb}_2\text{O}_5$ , or a composite layer of  $\text{Y}_2\text{O}_3$ ,  $\text{Al}_2\text{O}_3$ ,  $\text{TiO}_2$ , BaO, SrO,  $\text{ZrO}_2$ ,  $\text{Ta}_2\text{O}_5$ ,  $\text{Nb}_2\text{O}_5$ .

3. The method of claim 1, wherein the vacuum annealing is performed on the dielectric layer at a temperature of about 200-850° C. in a chamber, while evacuating the chamber to a high vacuum level of about  $1 \times 10^{-8}$ -1 torr.

4. A method for forming a dielectric layer, the method comprising:

(a) introducing a first reactant into a chamber;

- (b) removing the remaining first reactant from the chamber by pumping or purging;
- (c) introducing a second reactant into the chamber;
- (d) removing the remaining second reactant from the chamber to form a dielectric layer on a semiconductor substrate;
- (e) repeating said steps (a) through (d); and
- (f) vacuum annealing the dielectric layer.

5. A method for forming a dielectric layer, the method comprising:

- (a) introducing a first reactant into a chamber;

- (b) removing the remaining first reactant from the chamber by pumping or purging;
- (c) introducing a second reactant into the chamber;
- (d) removing the remaining second reactant from the chamber to form a dielectric layer on a semiconductor substrate;
- (e) vacuum annealing the dielectric layer; and
- (f) repeating said steps (a) through (d).

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