

(19) World Intellectual Property Organization
International Bureau(43) International Publication Date
23 February 2006 (23.02.2006)

PCT

(10) International Publication Number
WO 2006/020737 A1(51) International Patent Classification⁷: **H01L 29/12**,
29/76, 21/283, 31/062, 23/48(21) International Application Number:
PCT/US2005/028478

(22) International Filing Date: 10 August 2005 (10.08.2005)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/914,928 10 August 2004 (10.08.2004) US(71) Applicant (for all designated States except US): **TEXAS INSTRUMENTS INCORPORATED** [US/US]; P.O. Box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **CRANK, Sue-Ellen** [US/US]; 831 Lockhaven Lane, Coppell, TX 75019 (US). **SIDDIQUI, Shirin** [US/US]; 8913 Somerville Way, Plano, TX 75025 (US). **RILEY, Deborah, J.** [US/US]; 3208 Walker Drive, Richardson, TX 75082 (US). **HURD, Trace, Quentin** [US/US]; 3913 Hearst Castle Way, Plano, TX 75025 (US). **CHEN, Peijun, J.** [US/US]; 13044 Woodbend Lane, Dallas, TX 75243 (US).(74) Agents: **FRANZ, Warren, L.** et al.; Texas Instruments Incorporated, Deputy General Patent Counsel, P.O. Box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

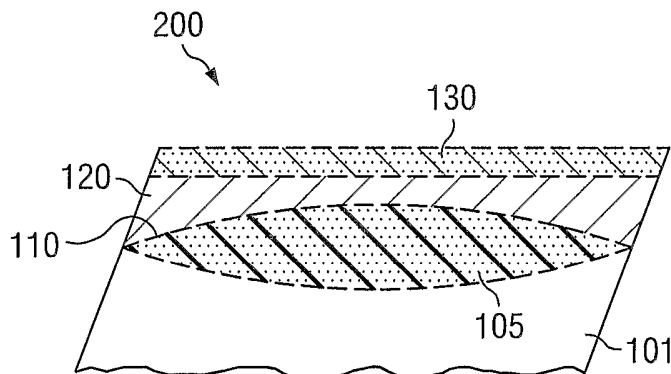
(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

- as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for the following designations AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW, ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG)
- as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii)) for the following designations AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW, ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian

[Continued on next page]

(54) Title: TREATMENT OF SILICON PRIOR TO NICKEL SILICIDE FORMATION



(57) Abstract: A method of preparing a semiconductor die comprises pre-treating exposed silicon (101) to form an oxide (110) prior to silicide (105) formation; and depositing metal (120) on the oxide. In disclosed embodiments, chemical oxide surface pre-treatment retards nickel (Ni) diffusion to provide controlled NiSi silicide formation. This addresses the problem of rapid diffusion of Ni and Ni decoration of Si silicon defects.



patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG)

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

Published:

— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

TREATMENT OF SILICON PRIOR TO NICKEL SILICIDE FORMATION

TECHNICAL FIELD

The subject matter disclosed herein relates generally to semiconductor processing and in particular to a method of preparing a die for silicide formation via treating silicon to form an oxide prior to metal deposition.

BACKGROUND

Integrated circuits are fabricated on the surface of a semiconductor wafer in layers, and later singulated into individual semiconductor devices, or "dies." Many fabrication processes are repeated numerous times, constructing layer after layer until fabrication is complete. Metal layers, which typically increase in number as device complexity increases, include patterns of conductive material that are vertically insulated from one another by alternating layers of insulating material. Conductive traces are also separated within each layer by an insulating, or dielectric, material. Vertical, conductive tunnels called "vias" typically pass through insulating layers to form conductive pathways between adjacent conductive patterns. Defects in semiconductor devices may result from, among other things, diffusion of mobile species and deficiencies in the layers of materials forming device structures.

Metals are commonly employed in fabrication of semiconductor devices. Certain metals, e.g., cobalt, nickel, titanium, and platinum, may be suitable for employment as a constituent in formation of a metal silicide (or "silicide"), which may act as a low resistance contact between metal layers and the silicon substrate in a device. The processes involved in preparing a die for pre-silicide metal deposition and silicide formation may affect silicide film integrity, and the potential for undesirable diffusion of metal in the device.

In application of nickel (Ni) to exposed silicon (Si), there may be problems associated with rapid diffusion of Ni and Ni decoration of Si defects.

SUMMARY

In some embodiments, a method for preparing a die comprises treating exposed silicon to form an oxide, prior to silicide formation and depositing metal on the oxide. The metal may comprise titanium, cobalt, nickel, platinum, palladium, tungsten, molybdenum, or combinations thereof, on the oxide. The oxide may be less than or

equal to about 15 angstroms thick. In various embodiments, treating exposed silicon to form an oxide comprises forming a non-thermal oxide. Treating exposed silicon to form an oxide may also comprise treating the exposed silicon with an oxidizing plasma; alternatively, treating exposed silicon to form an oxide may comprise forming a chemical
5 oxide. In certain other embodiments, treating exposed silicon to form an oxide comprises treating exposed silicon with a solution comprising ammonium hydroxide, hydrogen peroxide, and water; hydrochloric acid, hydrogen peroxide, and water; hydrogen peroxide; ozone; ozonated deionized water; or combinations thereof. The time between treating exposed silicon to form an oxide and depositing metal on the
10 oxide may be in a range from about 0 to about 60 hours.

In embodiments, a method for improving silicide film integrity comprises oxidizing exposed silicon on a die, depositing metal on the oxidized silicon, and heating the die comprising metal on oxidized silicon to form a silicide. The method may further comprise treating the die to expose silicon prior to oxidizing exposed silicon.

15 In other embodiments, a system for forming metal silicide comprises a vessel wherein oxide is formed on a die comprising exposed silicon; and a processing chamber wherein a metal source is disposed to deposit metal on the oxide. The vessel in which oxide is formed may comprise a wet chemical tank, a plasma reactor, or combinations thereof. The processing chamber may deposit metal via sputtering. In
20 certain embodiments, the silicide is formed at a temperature in a range from about 250 to about 500 degrees Celsius.

For Ni deposition onto exposed Si, chemical oxide surface pre-treatment retards nickel (Ni) diffusion to provide controlled NiSi silicide formation. This addresses the problem of rapid diffusion of Ni and Ni decoration of Si silicon defects.

25 BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates a cross-sectional view of materials in a semiconductor device that may be involved in preparing a die for metal silicide formation;

FIG. 2 illustrates another cross-sectional view of materials in a semiconductor device after a metal reacts with silicon to form a metal silicide; and

30 FIG. 3 illustrates a system for preparing a die and carrying out silicide formation.

NOTATION AND NOMENCLATURE

Certain terms are used throughout the following description and claims to refer to particular components. As one skilled in the art will appreciate, companies may refer to a component by different names. This document does not intend to distinguish
5 between components that differ in name but not function. Also employed throughout this document are the terms "including" and "comprising," which are used in an open-ended fashion, and thus should be interpreted to mean "including, but not limited to"

The term "integrated circuit" or "IC" refers to a set of electronic components and their interconnections (internal electrical circuit elements, collectively) that are
10 patterned on the surface of a microchip. The term "semiconductor device" refers generically to an integrated circuit (IC). The term "die" ("dies" for plural) refers generically to an integrated circuit or semiconductor device, which may be a portion of a wafer, in various stages of completion, including the underlying semiconductor substrate, insulating materials, and all circuitry patterned thereon.

15 DETAILED DESCRIPTION OF EMBODIMENTS

FIG. 1 illustrates an embodiment of a semiconductor structure 100 involved in preparing a die for silicide formation. The view of FIG. 1 is a cross-section of a semiconductor structure 100, e.g., a die, die sample, or portion of a wafer, at an intermediate point in the construction of an IC. In various embodiments, preparing for
20 silicide formation comprises treating exposed silicon 101 to form an oxide 110, and depositing a metal 120 on the oxide 110. In certain embodiments, the metal 120 is nickel, which for silicide formation reacts with silicon 101 to form nickel silicide (not shown).

FIG. 2 illustrates an embodiment of a semiconductor structure 200 after
25 formation of silicide 105, where nickel is employed as the metal 120. Formation of nickel silicide 105 is carried out after forming an oxide 110 on exposed silicon 101 and depositing nickel 120 on the oxide 110. FIG. 2 shows nickel silicide 105 formed between silicon 101 and nickel 120. After formation, the oxide 110 may primarily be at the interface of the nickel silicide 105 and any unreacted nickel 120. During formation,
30 the nickel 120 diffuses through the oxide 110 and reacts with the silicon 101 to form

nickel silicide 105. Thus, some of the silicon 101 and some of the nickel 120 are consumed in formation of nickel silicide 105.

The metal 120 can be any metal effective for reacting with silicon to form a silicide that creates a low resistance contact between metal layers and the silicon substrate. As technology advances and the dimensions of structures within semiconductor devices shrink, some metals may be more suitable than others. In some embodiments, the metal 120 comprises titanium, cobalt, nickel, platinum, palladium, tungsten, molybdenum, or combinations thereof. Some examples of considerations when selecting a metal comprise silicon consumption during silicide formation, diffusion rate, thermal stability of the desired phase of silicide, and electrical characteristics, such as junction integrity, contact resistance, and sheet resistance.

The treatment employed to form the oxide affects the characteristics of the oxide, which in turn may impact diffusion of metal to the silicon and silicide integrity. Some pertinent characteristics of the oxide may comprise density, stoichiometry, thickness, hydrogen content, OH⁻ content, and uniformity. In some embodiments, treating exposed silicon forms a non-thermal oxide. Examples of non-thermal oxides comprise chemical oxides and oxides formed via treating exposed silicon with an oxidizing plasma source. Examples of oxidizing plasma sources for treating silicon prior to metal deposition comprise a direct energetic plasma of Ar⁺, He⁺, Ne⁺ in combination with an oxygen source, such as O₂ or H₂O; and a remote plasma that contains reactive oxidizing radicals of O* or OH*. In certain embodiments, chemical oxides are oxides formed via treating exposed silicon with a solution comprising ammonium hydroxide, hydrogen peroxide, and water; hydrochloric acid, hydrogen peroxide, and water; hydrogen peroxide; ozonated deionized water; or combinations thereof.

Effective treatments of exposed silicon to form an oxide typically control oxide thickness. In certain embodiments, as measured by an Opti-Probe® with a desorber manufactured by Thermo-Wave of Fremont, California, the thickness of the oxide may be less than or equal to about 15 angstroms; alternatively, less than or equal to about 12 angstroms; alternatively, less than or equal to about 10 angstroms.

The oxide formed via treating exposed silicon may also be a protective layer for the silicon. Whereas typically the time window between exposing silicon and

depositing pre-silicide metal may have been a concern, forming an oxide on the exposed silicon may reduce such concerns. Thus, the protective oxide layer may add manufacturing robustness. In some embodiments, the time window between exposing silicon and depositing pre-silicide metal is in a range from about 0 to about 24 hours; alternatively, the time window is in a range from about 0 to about 12 hours; alternatively, from about 0 to about 2 hours. In other embodiments, the time window between treating exposed silicon to form an oxide and depositing pre-silicide metal is in a range from about 0 to about 120 hours; alternatively, from about 0 to about 60 hours.

It is believed the oxide on the silicon provides a more desirable surface for the silicon prior to metal deposition. Exposed silicon may be substantially lacking in stability and uniformity, and susceptible to undesirable reactions and diffusion before and after metal deposition. It is believed the oxide layer permits metal diffusion necessary for silicide formation while also providing a more stable surface on the silicon. In at least some cases, the oxide layer may be associated with less variation in island diode leakage and breakdown, less variation in contact resistance, and less variation in transistor gain.

Silicides (or "metal silicides") are typically employed in semiconductor devices to create low resistance contact between metal layers and the silicon substrate. Silicide, which includes a self-aligned silicide or "salicide," is the product of a reaction between metal and silicon. The characteristics of the silicide and silicide formation process may vary substantially depending on the type of metal employed. Silicides of cobalt, for example, may possess higher resistance and consume more silicon during formation than silicides of nickel. Also, the quality of the silicide formed with a single metal may vary depending on reaction conditions. For example, the silicide of nickel with silicon may comprise different phases, e.g., di-nickel silicide (Ni_2Si), nickel disilicide (NiSi_2), and/or nickel silicide (NiSi). Reaction kinetics, e.g., time and temperature, typically determine which silicide phase is formed and/or the proportions of each silicide phase formed. In the case of nickel, NiSi possesses substantially lower resistance and is, thus, typically more desirable in the role of contact silicide. In at least some instances, the desired silicide is NiSi and formation of an oxide on exposed silicon prior to metal deposition may minimize formation of unwanted NiSi_2 and Ni_2Si .

Also provided in the present application is a system 300 for forming silicide, an aspect of which is illustrated by FIG. 3. In some embodiments, the system 300 comprises a vessel 310 and a processing chamber 330. A die (not shown) including exposed silicon is placed in the vessel 310 for processing. The vessel 310 may treat the exposed silicon to form an oxide. Subsequently, the die is transferred from the vessel 310 to the processing chamber 330. A metal source 320 may be disposed in the processing chamber 330 at conditions effective for depositing metal on the oxide. In some embodiments, the processing chamber 330 effects both deposition and silicide formation. Thus, after metal deposition, silicide formation may also be accomplished in the processing chamber 330.

In some embodiments, forming an oxide on exposed silicon in the vessel 310 may be preceded by a process for exposing silicon. Such a process for exposing silicon would not typically be carried out in the vessel 310 where an oxide is formed. Effective techniques for exposing silicon may be those characteristically employed by one skilled in the art. In at least one case, the process for exposing silicon prior to forming an oxide comprises a hydrofluoric acid treatment. Such a hydrofluoric acid treatment may comprise hydrofluoric acid in the gas phase, liquid phase, or combinations thereof. As an example, in order to expose silicon the die may be treated in a chemical bath comprising a 0.2 - 1 percent by volume hydrofluoric acid solution in deionized water at 23 degrees Celsius for 1-10 minutes.

In various embodiments, the vessel 310 receives a die comprising exposed silicon and is set at conditions effective for forming an oxide on the exposed silicon as described above. In certain cases, the vessel 310 may comprise a wet chemical tank, plasma reactor, or combinations thereof. An example of an appropriate wet chemical tank is that found in the F-Wet FC-821L manufactured by DNS Electronics of Sunnyvale, California. An example of conditions appropriate for forming an oxide on exposed silicon in the F-Wet FC-821L may comprise a mixture of 0.1-10 weight percent hydrochloric acid, 0.3-10 weight percent hydrogen peroxide, and the remainder water; and a process time and temperature of 10 minutes at 25 degrees Celsius.

The processing chamber 330 may receive the die comprising oxide on silicon. In at least one embodiment, the processing chamber 330 first deposits metal on

the oxide and then achieves conditions effective for forming the metal silicide. In some cases a protective layer may be deposited on the metal before formation. An example of such a protective layer is a titanium nitride layer. Such a protective layer may help prevent oxidation of the metal. An example of an occasion presenting risk of oxidation is where there is a delay between metal deposition and silicide formation, such as where metal deposition and silicide formation occur in separate chambers as described below. The protective layer may remain on the die during silicide formation. In certain embodiments, the processing chamber 330 may accomplish all of deposition of a metal, deposition of a protective layer, and silicide formation. The deposition(s) may be accomplished via any means effective for putting down a metal and optionally a protective layer as described herein. In various embodiments, the deposition(s) occur via sputtering as would typically be effected by those skilled in the art. An example of a processing chamber suitable for depositing a metal, optionally depositing a protective layer, and forming silicide is the Endura 5500 manufactured by Applied Materials of Santa Clara, California. Conditions effective for silicide formation may comprise a temperature range from about 250 to about 500 degrees Celsius at a pressure in the range from about 10^{-8} to about 760 torr.

Variations among components of the system 300 are practicable. In at least one instance, the system 300 is designed to form self-aligned silicide or "salicide". In some embodiments, a separate deposition chamber (not shown) may precede the processing chamber 330 and accomplish metal deposition following oxide formation in the vessel 310. In cases where a protective layer, e.g., titanium nitride, is needed as well, such a deposition chamber may accomplish deposition, e.g., via sputtering, of both the metal and protective layer. Methods of executing such a deposition may be those methods employed by one skilled in the art. An example of such a deposition chamber is the Endura 5500 manufactured by Applied Materials of Santa Clara, California.

Yet additional components may optionally be employed in the system 300 for forming silicide. In some embodiments, the die having oxidized silicon may be treated in a plasma reactor (not shown) prior to metal deposition. Such a plasma reactor typically exposes the oxidized silicon to a plasma etch. An example of a process sequence including a plasma reactor may be: form oxide on exposed silicon,

expose to plasma etch, deposit metal, and form silicide. Methods of contacting with a plasma etch prior to metal deposition may be those methods typically employed by one skilled in the art. Examples of suitable plasma sources comprise the Pre-Sputter Etch Endura Chamber manufactured by Applied Materials of Santa Clara, California, or the
5 Highlands Ash Chamber manufactured by Mattson of Fremont, California.

In additional embodiments, the system 300 may comprise one piece of equipment. An example of such a scheme would comprise treating exposed silicon to form an oxide, depositing a metal and optionally a protective layer, and forming silicide, all of which may be executed in the same chamber. In at least one embodiment, a
10 processing chamber receives a die comprising exposed silicon, forms a non-thermal oxide on the exposed silicon, deposits nickel on the oxide, and executes silicide formation as described herein.

While various embodiments of the invention have been shown and described, modifications thereof can be made by one skilled in the art without departing
15 from the scope of the invention.

CLAIMS

1. A method of preparing a die, comprising:
prior to silicide formation, treating exposed silicon to form an oxide; and
depositing a metal on the oxide.
2. The method of Claim 1 wherein depositing the metal on the oxide comprises depositing nickel on the oxide.
3. The method of Claim 2, wherein treating exposed silicon to form an oxide comprises forming an oxide that is less than or equal to about 15 angstroms thick.
4. The method of Claim 1 wherein treating exposed silicon to form an oxide comprises forming a non-thermal oxide.
5. The method of Claim 1 or 3, wherein treating the exposed silicon to form an oxide comprises treating the exposed silicon with a solution comprising ammonium hydroxide, hydrogen peroxide, and water; hydrochloric acid, hydrogen peroxide, and water; hydrogen peroxide; ozone; ozonated deionized water; or combinations thereof.
6. The method of Claim 2, further comprising:
heating the die comprising metal on oxidized silicon to form a silicide.
7. The method of Claim 6, wherein treating the die to expose silicon comprises contacting the die with a hydrofluoric acid solution.
8. The method of Claim 1, wherein depositing metal on the oxide comprises depositing titanium, cobalt, nickel, platinum, palladium, tungsten, molybdenum, or combinations thereof.
9. A system for forming metal silicide comprising:

a vessel wherein oxide is formed on a die comprising exposed silicon;
and
a processing chamber wherein a metal source is disposed to deposit
metal on the oxide.

1/1

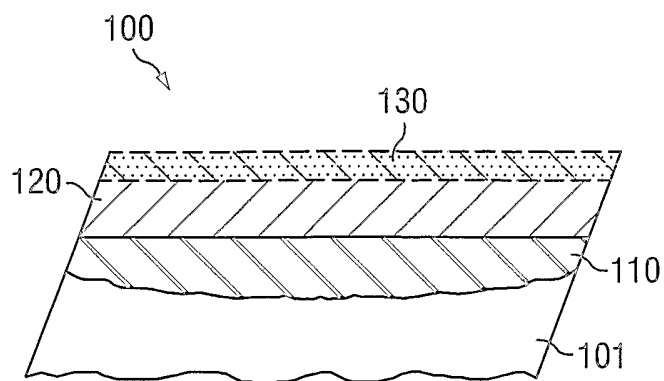


FIG. 1

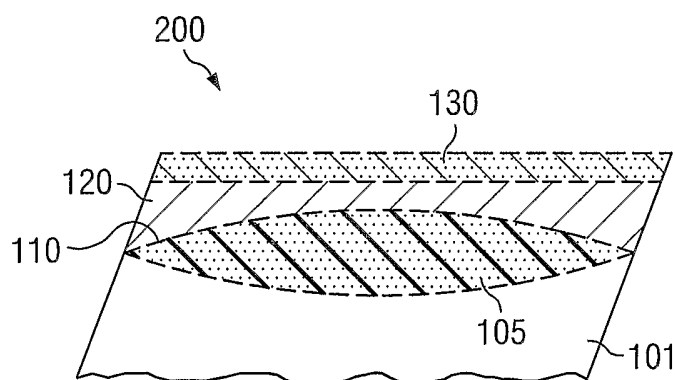


FIG. 2

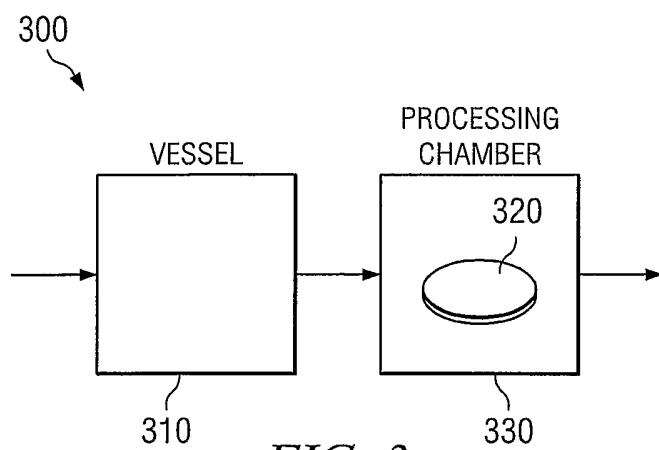


FIG. 3

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US05/28478

A. CLASSIFICATION OF SUBJECT MATTER IPC(7) : H01L 29/12, 29/76, 21/283, 31/062, 23/48 US CL : 438/513,548,621,655 ; 257 406, 412 According to International Patent Classification (IPC) or to both national classification and IPC																	
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) U.S. : 438/513,548,621,655 ; 257 406, 412 Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)																	
C. DOCUMENTS CONSIDERED TO BE RELEVANT <table border="1"> <thead> <tr> <th>Category *</th> <th>Citation of document, with indication, where appropriate, of the relevant passages</th> <th>Relevant to claim No.</th> </tr> </thead> <tbody> <tr> <td>X</td> <td>US 6,737,716 B1 (MATSUO et al) 18 May 2004 (18.05.2004) Fig 2A-E, the whole document</td> <td>1-6,9</td> </tr> <tr> <td>Y</td> <td></td> <td>7-8</td> </tr> <tr> <td>Y</td> <td>US 4,708,904 A (SHIMIZU et al) 24 Nov 1987 (24.11.1987 column 4 lines 25-47</td> <td>1-7</td> </tr> <tr> <td>Y</td> <td>US 5,665,647 A (ISHIGAMI) 9 Sep 1997 (09.09.1997) The whole document</td> <td>1-8</td> </tr> </tbody> </table>			Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.	X	US 6,737,716 B1 (MATSUO et al) 18 May 2004 (18.05.2004) Fig 2A-E, the whole document	1-6,9	Y		7-8	Y	US 4,708,904 A (SHIMIZU et al) 24 Nov 1987 (24.11.1987 column 4 lines 25-47	1-7	Y	US 5,665,647 A (ISHIGAMI) 9 Sep 1997 (09.09.1997) The whole document	1-8
Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.															
X	US 6,737,716 B1 (MATSUO et al) 18 May 2004 (18.05.2004) Fig 2A-E, the whole document	1-6,9															
Y		7-8															
Y	US 4,708,904 A (SHIMIZU et al) 24 Nov 1987 (24.11.1987 column 4 lines 25-47	1-7															
Y	US 5,665,647 A (ISHIGAMI) 9 Sep 1997 (09.09.1997) The whole document	1-8															
☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.																	
* Special categories of cited documents: <table border="0"> <tr> <td>"A" document defining the general state of the art which is not considered to be of particular relevance</td> <td>"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</td> </tr> <tr> <td>"E" earlier application or patent published on or after the international filing date</td> <td>"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone</td> </tr> <tr> <td>"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)</td> <td>"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art</td> </tr> <tr> <td>"O" document referring to an oral disclosure, use, exhibition or other means</td> <td>"&" document member of the same patent family</td> </tr> <tr> <td>"P" document published prior to the international filing date but later than the priority date claimed</td> <td></td> </tr> </table>			"A" document defining the general state of the art which is not considered to be of particular relevance	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention	"E" earlier application or patent published on or after the international filing date	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone	"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art	"O" document referring to an oral disclosure, use, exhibition or other means	"&" document member of the same patent family	"P" document published prior to the international filing date but later than the priority date claimed						
"A" document defining the general state of the art which is not considered to be of particular relevance	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention																
"E" earlier application or patent published on or after the international filing date	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone																
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art																
"O" document referring to an oral disclosure, use, exhibition or other means	"&" document member of the same patent family																
"P" document published prior to the international filing date but later than the priority date claimed																	
Date of the actual completion of the international search 12 December 2005 (12.12.2005)		Date of mailing of the international search report 05 JAN 2006															
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450 Facsimile No. (571) 273-3201		Authorized officer <i>Rhonda J. Bell</i> Thinh T Nguyen Telephone No. 571-272-1790															