A detection circuit includes an under-voltage circuit. The under-voltage circuit includes a first GaN high electron mobility transistor (HEMT) configured to operate as both a voltage comparator and a voltage reference. The detection circuit can also include an over-voltage detection circuit. The over-voltage detection circuit includes a second GaN HEMT that is also configured to operate as both a voltage comparator and a voltage reference. Each of the under-voltage circuit and over-voltage circuit includes a GaN HEMT logic inversion element to provide electrical hysteresis. Also, the under-voltage detection circuit and the over-voltage detection circuit are configured to provide outputs to a single 'power good' terminal. The first GaN HEMT can be configured to use its gate source threshold voltage for voltage comparison and reference. The second GaN HEMT can be configured to use its gate source threshold voltage for voltage comparison and reference.
VOLTAGE DETECTION CIRCUIT

RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Application No. 62/266,083, filed on Dec. 11, 2015, U.S. Provisional Application No. 62/266,086, filed on Dec. 11, 2015, U.S. Provisional Application No. 62/266,094, filed on Dec. 11, 2015, U.S. Provisional Application No. 62/266,099, filed on Dec. 11, 2015 and U.S. Provisional Application No. 62/275,575, filed on Jan. 6, 2016.

[0002] The entire teachings of the above applications are incorporated herein by reference.

BACKGROUND

[0003] Electronic devices such as computers, servers and televisions, among others, employ one or more electrical power conversion circuits to convert one form of electrical energy to another. These circuits also require monitoring circuitry/logic, such as voltage detection circuits, to detect under-voltage and/or over-voltage scenarios. These voltage detection circuits can be used to protect circuits such as transistor gate drivers in half-bridge circuit configurations from under-voltage and/or over-voltage scenarios, which can damage the circuits or impair their functionality.

SUMMARY

[0004] Embodiments of the present disclosure relate to an under-voltage detection circuit that comprises an enhancement mode Gallium Nitride (GaN) high electron mobility transistor (HEMT) configured to operate as both a voltage comparator and a voltage reference. The GaN HEMT can be configured to use its gate source threshold voltage for voltage comparison and reference. The GaN HEMT can be an electrically temperature-stable element over a temperature range of −55°C to 150°C. Additionally, the GaN HEMT is configured as a saturated switch.

[0005] The under-voltage detection circuit can further include a resistor voltage divider in electrical communication with the GaN HEMT gate terminal. The resistor voltage divider can be configured to determine a magnitude of potential at a voltage input terminal that has a higher potential than the GaN HEMT gate terminal. The under-voltage detection circuit can further include a logic state inversion element configured to provide an electrical hysteresis into the circuit by altering the ratio of the resistor voltage divider on the gate threshold voltage of the first GaN HEMT transistor when the gate terminal is below the gate-source threshold voltage (Vgs(th)). The logic state inversion element can be in electrical communication with the gate of the first GaN HEMT via a second, subordinate resistor voltage divider. Other embodiments of the present disclosure relate to a detection circuit. The detection circuit includes an under-voltage detection circuit and an over-voltage detection circuit. The under-voltage detection circuit includes a first GaN high electron mobility transistor (HEMT) configured to operate as both a voltage comparator and a voltage reference. The over-voltage detection circuit includes a second GaN high electron mobility transistor (HEMT) configured to operate as both a voltage comparator and a voltage reference. Both the under-voltage detection circuit and the over-voltage detection circuit can provide outputs to a single power good output terminal when the sensed voltage (VSENSEL) is above an under-voltage threshold and below and over-voltage threshold.

[0008] In other aspects, the under-voltage detection circuit can provide an output to an under-voltage output terminal. Also, the over-voltage detection circuit can provide an output to an over-voltage output terminal.

[0009] The detection circuit can further comprise a first voltage divider and a second voltage divider. The first voltage divider can be in electrical communication with the first GaN HEMT. Also, the first voltage divider can be configured to monitor the magnitude of potential at a first voltage input terminal VSENSE1. The second voltage divider can be in electrical communication with the second GaN HEMT. In addition, the second voltage divider can be configured to monitor the magnitude of potential at a second input terminal VSENSE2.

[0010] In another aspect, the two resistor dividers from the first and second GaN HEMTs may be connected to a common input terminal (VSENSE1) to monitor the potential. This embodiment will be recognized by those skilled in the practice as a “window comparator”.

[0011] In an aspect, both the first GaN HEMT and the second GaN HEMT can be electrically temperature-stable elements at a temperature range of −55°C to 150°C. Additionally, both the first GaN HEMT and the second GaN HEMT can be configured as saturated switches.

[0012] In further aspects, the first GaN HEMT can be configured to employ its gate source threshold voltage for voltage comparison and reference. Similarly, the second GaN HEMT can also be configured to use its gate source threshold voltage for voltage comparison and reference.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] The foregoing will be apparent from the following more particular description of example embodiments of the invention, as illustrated in the accompanying drawings in which like reference characters refer to the same parts throughout the different views. The drawings are not necessarily to scale, emphasis instead being placed upon illustrating embodiments of the present invention.
FIG. 1 is a logical block diagram of a voltage detection circuit implemented in a multi-function circuit according to an example embodiment of the present disclosure.

FIG. 2 is a circuit diagram of a voltage detection circuit that includes under-voltage circuitry and over-voltage circuitry according to an example embodiment of the present disclosure.

FIG. 3 is a circuit diagram of a power good circuit according to an example embodiment of the present disclosure.

FIG. 4 is another circuit diagram of a voltage detection circuit that includes under-voltage circuitry and over-voltage circuitry according to an example embodiment of the present disclosure.

FIG. 5 is another circuit diagram of a power good circuit according to an example embodiment of the present disclosure.

FIG. 6 is a graphical illustration of an output signal of a power good circuit according to an example embodiment of the present disclosure.

DESCRIPTION

A description of example embodiments of the present disclosure follows.

Gallium Nitride (GaN) is a semiconductor material that is technologically maturing at a rapid rate for use in electronic circuits. The properties of GaN materials are superior, in many cases, to existing semiconductor materials systems such as Germanium, Gallium Arsenide, Silicon Carbide and Silicon. Accordingly, GaN can be implemented in circuits as high speed, radiation tolerant transistors.

GaN High Electron Mobility Transistors (HEMTs) are available in two types: depletion mode devices (which are normally on) and enhancement mode devices (which are normally off). Depletion mode GaN HEMTs are commonly used in radio frequency applications in which they are typically biased on at a fixed voltage and current level. A radio frequency signal is then superimposed on top of that biasing condition. The GaN HEMTs do not switch from on state to off-state in this case. Enhancement mode GaN HEMTs are normally off. A gate of a GaN HEMT needs to be enhanced by a voltage at its control gate to enable current flow between source contacts and drain contacts of the GaN HEMT. A margin between the voltage needed to be applied to the control gate to turn on the GaN HEMT and the maximum voltage permitted on the control gate is very small. Accordingly, this small margin poses a number of issues in the switching mode operation of GaN HEMTs. Embodiments of the present disclosure relate to utilizing enhancement mode GaN HEMTs within the concept of a voltage detection circuit. In particular, embodiments of the present disclosure relate to circuits that use only GaN transistors (no silicon transistors).

Because GaN material is a wide band gap material, GaN is intrinsically more functionally robust in and tolerant of radiation environments. Accordingly, embodiments of the present disclosure allow for increased radiation tolerance as compared to circuits and systems which employ silicon Metal Oxide Semiconductor Field Effect Transistor (MOSFET) devices.

An objective of the present disclosure is to provide a circuit designed to eliminate all silicon based transistors. In particular, an objective is to demonstrate that, by using n-channel GaN enhancement mode HEMTs only, a voltage detection circuit can be designed and realized using only GaN HEMTs.

Advantageously, the size of the embodiments disclosed herein can be reduced significantly because GaN transistors are smaller than silicon transistors for a given on-state resistance. Thus, the power density of the circuit designs disclosed herein is greater than presently-employed circuit designs.

Additionally, the circuit designs, using only GaN transistors, disclosed herein are able to switch at higher frequencies because GaN semiconductor materials, in addition to other known benefits, have greater electron mobility and are a wider bandgap material. In addition to the benefits of a GaN semiconductor material, a HEMT transistor requires less gate charge to drive the transistor from one state (on/off) to another (off/on). This means that the circuit, both active and passive components, can be correspondingly smaller because the individual components are required to handle less power due to the lower gate charge value. Accordingly, embodiments of the present disclosure can achieve circuit designs having a much smaller size than conventional designs. The decreased value of the passive components also contributes to increased system power density of embodiments of the present disclosure.

Because GaN materials have a high degree of radiation hardness, the circuit designs disclosed herein have a degree of radiation hardness that is greater than present circuit designs. As such, embodiments of the present disclosure can be applied to various space and military applications that require a high degree of radiation hardness.

FIG. 1 is a logical block diagram of a voltage detection circuit 130 implemented in a multi-function circuit 100. In this implementation, the voltage detection circuit 130 is in electrical communication with a driver circuit 103. The voltage detection circuit 130 is used to detect under-voltage and/or over-voltage conditions of the multi-function circuit 100. In particular, the voltage detection circuit 130 can be used to protect circuits, such as half-bridge drivers, from under-voltage and/or over-voltage scenarios, which can damage or impair the functionality of such circuits.

The voltage detection circuit 130 includes under-voltage circuitry 131 and over-voltage circuitry 132. The under-voltage circuitry 131 is configured to detect an under-voltage condition of the gate driver bias power supply ("VBIAS") of the multi-function circuit 100. In contrast, the over-voltage circuitry 132 is configured to detect an over-voltage condition of the gate driver bias power supply (VBIAS) of the multi-function circuit 100.

Each transistor of both the under-voltage circuitry 131 and the over-voltage circuitry 132 can be an enhancement mode Gallium Nitride (GaN) high electron mobility transistor (HEMT). Embodiments of the present disclosure utilize a single enhancement mode GaN HEMT to perform the function of both a voltage comparator and a voltage reference in each of the under-voltage circuitry 131 and the over-voltage circuitry 132. In particular, embodiments of the present disclosure exploit inherent characteristics of GaN HEMTs that include a low Vgs threshold and a stable Vgs threshold drift over temperature. For instance, embodiments of the present disclosure utilize a gate source threshold voltage as both a reference and comparator. For example, when the gate-source voltage is below the threshold voltage (Vgsth), the drain-source connection assumes a high
impedance (i.e. “open”) state which may be employed to indicate a high logic state; and when the gate-source voltage exceeds the threshold voltage \( V_{\text{gs(th)}} \), the drain-source connection assumes a low impedance (i.e. “closed”) state which may be employed to indicate a low logic state. Thusly, the gate-source threshold voltage is employed as a voltage threshold detection point and the drain-source connection is employed to display/assume the logic state of the voltage presented to the gate-source of the GaN HEMT.

In this example, the voltage detection circuit 130 is in electrical communication with an enhancement mode GaN HEMT power control circuit 103. However, a skilled artisan can appreciate that the voltage detection circuit 130 can be implemented in any circuitry that would benefit from detecting and responding to under-voltage and/or over-voltage conditions.

In an example, the multi-function circuit 100 can be configured to operate as a half-bridge driver circuit. In such a configuration, the multi-function circuit 100 drives power switch circuitry 102. The power switch circuitry 102 includes complementary power transistors (e.g., power switches) 113-114. The power switches 113-114 can be Gallium Nitride (GaN) enhancement mode high electron mobility transistors (HEMTs). Further, each transistor comprising the entire multi-function circuit 100 can be a GaN HEMT. Each of the transistors can further be configured as saturated switches.

The first power switch (e.g., the high-side power switch) 114 is referenced to an output voltage terminal ‘TOUT’. In addition, the first power switch 114 is in electrical communication with an input power supply terminal ‘VDD’. The first power switch 114 is further connected to a first driver circuit (e.g., a high-side circuit) that includes a first high speed gate driver 110, level shift circuitry 120, and shoot-thru/ disable logic circuitry 125. The first driver circuit is configured to control the first power switch 114 (i.e., change an “ON/OFF” state of the first power switch 114).

The second power switch (e.g., the low-side power switch) 113 is referenced to a ground terminal ‘GND’. Additionally, the second power switch 114 is in electrical communication with an output terminal ‘BOUT’. The second power switch is further connected to a second driver circuit (e.g., low-side circuit) that includes a second high speed driver 115 and shoot-thru/ disable logic circuitry 125. The second driver circuit is configured to control the second power switch 114 (i.e., change an “ON/OFF” state of the first power switch 114).

The first driver circuitry and the second driver circuitry can be configured as independent driving circuits. For example, each of the first driver circuitry and second driver circuitry can be single independent discrete circuits. Alternatively, each of the first driver circuitry and second driver circuitry can be configured in a single discrete circuit as independently operating high side and low side circuits, respectively. In other configurations, the first driver circuitry and second driver circuitry can be configured as a half-bridge converter circuit. In a half-bridge configuration, the output terminal ‘TOUT’ and the output terminal ‘BOUT’ are electrically connected as a single output terminal to drive an external load.

FIG. 2 is a circuit diagram of a voltage detection circuit 200 that includes under-voltage circuit 231 and over-voltage circuit 232.

The under-voltage detection circuitry 231 is used to detect an undervoltage condition for a voltage potential at terminal VSENSE1. The over-voltage detection 232 is used to detect an over-voltage condition for a voltage potential at terminal VSENSE2.

The under-voltage circuitry 231 includes an undervoltage divider (R1, R2). The undervoltage divider (R1, R2) is configured to detect a magnitude of the voltage potential at terminal VSENSE1. Also, the under-voltage circuitry 231 includes a temperature stable undervoltage detection/comparison element (Q1) configured to determine a magnitude of a voltage potential at terminal VSENSE1. The undervoltage circuitry 231 also includes a blocking diode (D1) that is in electrical communication with a hysteresis resistor (R3). Further, the under-voltage circuitry 231 includes a logic state inversion element (Q2) and biasing resistors (R4, R5). The undervoltage circuitry 231 exploits gate-source threshold \( V_{\text{gs(th)}} \) characteristics of GaN HEMT devices, whereby the \( V_{\text{gs(th)}} \) varies by a small percentage over a -55 C to +150 C temperature range, thus enabling a single HEMT transistor (Q1) to act as a temperature-stable voltage reference and accurate voltage comparator.

The over-voltage circuitry 232 includes an overvoltage divider (R6, R7). The overvoltage divider (R6, R7) is configured to detect a magnitude of the potentials at terminal VSENSE1. Also, the over-voltage circuitry 232 includes a temperature stable overvoltage detection/comparison element (Q3) configured to determine a magnitude of a voltage potential at terminal VSENSE2. The overvoltage circuitry 232 also includes a blocking diode (D2) in electrical communication with a hysteresis resistor R8. Further, the overvoltage circuitry 232 includes a logic state inversion element (Q4) and biasing resistors (R9, R10). The overvoltage circuitry 232 exploits gate-source threshold \( V_{\text{gs(th)}} \) characteristics of GaN HEMT devices, whereby the \( V_{\text{gs(th)}} \) varies by a small percentage over the -55 C to +150 C temperature range, thus enabling a single HEMT transistor (Q3) to act as a temperature-stable voltage reference and accurate voltage comparator.

**Under-Voltage Detection Circuit**

In FIG. 2, transistors (Q1, Q2) are used for voltage detection in the under-voltage detection circuit 231. Each of the transistors (Q1, Q2) is configured as a saturated switch. The under-voltage detection circuit 231 includes an undervoltage divider (R1, R2) to divide the voltage potential of a voltage received from the terminal VSENSE1. The divided voltage potential is presented to a gate terminal of the temperature stable under-voltage detection/comparison element (Q1).

When the potential at the gate terminal of the under-voltage detection/comparison element (Q1) is less than \( V_{\text{gs(th)}} \) of the gate, the under-voltage detection/comparison element (Q1) is in an “OFF” state. Accordingly, a drain terminal of the under-voltage detection/comparison element (Q1), which is also a gate terminal of the logic state inversion element (Q2), has a voltage magnitude corresponding to a voltage at terminal VBIAS. Accordingly, the logic state inversion element (Q2) is in an “ON” state. Thus, a drain terminal of the logic state inversion element (Q2) assumes a potential of GROUND. The GROUND potential at the drain terminal of the logic state inversion element (Q2) indicates that the voltage potential at the terminal VSENSE1...
is in an under-voltage condition. Consequently, an under-voltage signal is presented to the output terminal ‘UV’.

With the drain terminal of the logic state inversion element (Q2) at GROUND, the cathode of the blocking diode (D1) is also at GROUND potential. In this condition, the hysteresis resistor (R3) is considered to be essentially in parallel with the voltage divider resistor (R2). Hence, this condition causes a lower composite resistance to be present at the gate terminal of the temperature stable under-voltage detection/comparison element (Q1). Accordingly, the threshold voltage at the terminal VSENSE1, when the voltage potential rises (with the hysteresis resistor R3 engaged in the circuit) above the under-voltage condition, is defined by:

$$\text{VSENSE1}(+) = \left( V_{gs(th)Q1} \cdot K2 \cdot \frac{R1}{R2} \right) - V_{TD(D1)} - R1 \cdot \frac{R1}{R3} \quad \text{(EQ1)}$$

When the potential at VSENSE1 exceeds the threshold defined by EQ1, a voltage at the gate terminal of the under-voltage detection/comparison element (Q1) exceeds $V_{gs(th)}$. In this condition, the under-voltage detection/comparison element (Q1) is caused to turn “ON”. Consequently, the logic state inversion element (Q2) is caused to be turned “OFF”, and a potential at the cathode of the blocking diode (D1) assumes a potential of −VBIAS. A potential of VBIAS at the drain of the logic state inversion element (Q2) provides an indication that a potential at the terminal VSENSE1 is no longer in the under-voltage condition.

The blocking diode (D1) is then caused to be reverse-biased, and as a result the hysteresis resistor (R3) is isolated from the gate terminal of the under-voltage detection/comparison element (Q1). The voltage divider (R1, R2) now divides VSENSE1 voltage at the gate terminal of the under-voltage detection/comparison element (Q1), and the VSENSE1 threshold potential to enter the under-voltage condition is defined by:

$$\text{VSENSE1}(-) = \left( V_{gs(th)Q1} \cdot K2 \right) \quad \text{(EQ2)}$$

Accordingly, there are now two separate threshold points for the potential VSENSE1 where the state of the drain of Q1 changes. Those skilled in the practice will recognize this functionality in the under voltage detection circuit as ‘hysteresis’.

Over-Voltage Detection Circuit

In FIG. 2, the elements Q3 and Q4, diode D2 and resistors R7 through R10 of the over-voltage detection circuit 232 perform similar functions as their corresponding elements Q1 and Q2, diode D1 and resistors R1 through R6 in the under-voltage detection circuit 231. However, an over-voltage indication for a voltage potential at the terminal VSENSE2 is presented from a drain terminal of the over-voltage detection/comparison element (Q3). Accordingly, when the voltage potential at the terminal VSENSE2 is less than an over-voltage threshold defined by:

$$\text{VSENSE2}(+) = \left( V_{gs(th)Q3} \cdot \left(1 + \frac{R7}{R6} + \frac{R7}{R8} \right) \right) - V_{TD(D2)} \cdot \frac{R7}{R8} \quad \text{(EQ3)}$$

the drain of the over-voltage detection/comparison element (Q3) is at a voltage corresponding to a voltage potential at the terminal VBIAS. The over-voltage detection circuit 232 is then configured to provide an indication at output terminal (‘OV’) that the potential at VSENSE2 is below an over-voltage condition.

When the voltage at potential VSENSE2 exceeds the over-voltage threshold as defined by:

$$\text{VSENSE2}(-) = \left( V_{gs(th)Q3} \cdot \left(1 + \frac{R8}{R7} \right) \right) \quad \text{(EQ4)}$$

the drain of the over-voltage detection/comparison element (Q3) is considered to be at the potential of the GROUND terminal. In this condition, an indication signal is presented to the output terminal (‘OV’) that the potential at VSENSE2 is above the over-voltage condition.

FIG. 3 is a circuit diagram of a power good circuit 300 according to an example embodiment of the present disclosure. Because the under-voltage circuitry 231 and over-voltage circuitry 232 present a potential referenced to the potential at the GROUND terminal to their respective indicated output terminals (‘UV’, ‘OV’) as illustrated in FIG. 2, the output terminals can be combined. Accordingly, the power good circuit 300 includes a single power good output terminal (‘PG’) that receives output signals from both the under-voltage circuitry 331 and over-voltage circuitry 332. Additionally, sensed signals from the terminal VSENSE1 and the terminal VSENSE2 may similarly be combined into a single terminal VSENSE. This variation allows a magnitude of a single voltage potential to be monitored to verify that the voltage potential remains within a range that is considered operationally wholesome. However, if the potential falls outside of this range an indication (output ‘PG’ falling to GROUND potential) is given to indicate this condition. This variation shown in FIG. 3 is colloquially know as a window detector or window comparator, and the output signal at the ‘PG’ output terminal is shown in FIG. 6 for the various conditions of the VSENSE potential.

FIG. 4 is another circuit diagram of a voltage detection circuit 400 that includes under-voltage circuitry 431 and over-voltage circuitry 432 according to an example embodiment of the present disclosure.

The under-voltage detection circuitry 431 is used to detect an under-voltage condition for a voltage potential at terminal VSENSE1. The over-voltage detection circuit 432 is used to detect an over-voltage condition for a voltage potential at terminal VSENSE2.

The under-voltage circuitry 431 includes an under-voltage divider (R1, R2). The under-voltage divider (R1, R2) is configured to detect a magnitude of the voltage potential at terminal VSENSE1. Also, the under-voltage circuitry 431 includes a temperature stable under-voltage detection/comparison element (Q1) configured to determine a magnitude of a voltage potential at terminal VSENSE1. The under-voltage circuitry 431 also includes a blocking diode (D1) that is in electrical communication with a hyst-
tervesis resistor (R3). Further, the under-voltage circuitry 431 includes a logic state inversion element (Q2) and biasing resistors (R4, R5). The under-voltage circuitry 431 exploits gate-source threshold (Vgs(th)) characteristics of GaN HEMT devices, whereby the Vgs(th) varies by a small percentage over a -55°C to +150°C temperature range, thus enabling a single HEMT transistor (Q1) to act as a temperature-stable voltage reference and accurate voltage comparator.

[0052] The over-voltage circuitry 432 includes an over-voltage divider (R8, R7). The over-voltage divider (R6, R7) is configured to detect a magnitude of the potentials at terminal VSENSE1. Also, the over-voltage circuitry 432 includes a temperature stable over-voltage detection/comparison element (Q3) configured to determine a magnitude of a voltage potential at terminal VSENSE2. The over-voltage circuitry 432 also includes a hysteresis resistor (R6). Further, the over-voltage circuitry 432 includes a logic state inversion element (Q4) and biasing resistor (R9). The over-voltage circuitry 432 exploits gate-source threshold (Vgs (th)) characteristics of GaN HEMT devices, whereby the Vgs(th) varies by a small percentage over the -55°C to +150°C temperature range, thus enabling a single HEMT transistor (Q3) to act as a temperature-stable voltage reference and accurate voltage comparator.

Under-Voltage Detection Circuit

[0053] In FIG. 4, transistors (Q1, Q2) are used for voltage detection in the under-voltage detection circuit 431. Each of the transistors (Q1, Q2) is configured as a saturated switch. The under-voltage detection circuit 431 includes an under-voltage divider (R1, R2) to divide the voltage potential of a voltage received from the terminal VSENSE1. The divided voltage potential is presented to a gate terminal of the temperature stable under-voltage detection/comparison element (Q1).

[0054] When the potential at the gate terminal of the under-voltage detection/comparison element (Q1) is less than Vgs(th) of the gate, the under-voltage detection/comparison element (Q1) is in an "OFF" state. Accordingly, a drain terminal of the under-voltage detection/comparison element (Q1), which is also a gate terminal of the logic state inversion element (Q2), has a voltage magnitude corresponding to a voltage at the terminal VBIAS. Accordingly, the logic state inversion element (Q2) is in an "ON" state. Thus, a drain terminal of the logic state inversion element (Q2) assumes a potential corresponding to the terminal GROUND. The GROUND potential at the drain terminal of the logic state inversion element (Q2) indicates that the voltage potential at the terminal VSENSE1 is in an under-voltage condition. Consequently, an under-voltage signal is presented to the output terminal UV.

[0055] With the drain terminal of the logic state inversion element (Q2) at GROUND, a cathode of the blocking diode (D1) is also at GROUND potential. In this condition, the hysteresis resistor (R3) is considered to be essentially in parallel with the voltage divider resistor (R2). Hence, this condition causes a lower composite resistance to be present at the gate terminal of the temperature stable under-voltage detection/comparison element (Q1). Accordingly, the threshold voltage at the terminal VSENSE1, when the voltage potential rises (with the hysteresis resistor R3 included/engaged in the circuit) above the under-voltage condition, is defined by:

\[
VSENSE1(+) = \left[ Vgs(th)(Q1) \left(1 + \frac{R1}{R2} \right) \right] - \left[ Vf(D1) \cdot \frac{R1}{R3} \right] 
\]

[0056] When the potential at VSENSE1 exceeds the threshold defined by EQ1, a voltage at the gate terminal of the under-voltage detection/comparison element (Q1) exceeds Vgs(th). In this condition, the under-voltage detection/comparison element (Q1) is caused to turn ‘ON’. Consequently, the logic state inversion element (Q2) is caused to be turned ‘OFF’, and a potential at a cathode of the blocking diode (D1) assumes a potential of ~VBIAS. A potential of VBIAS at the drain of the logic state inversion element (Q2) provides an indication that a potential at the terminal VSENSE1 is no longer in the under-voltage condition.

Over-Voltage Detection Circuit

[0058] In FIG. 4, the elements Q3 and Q4, and resistors R6 through R8 of the over-voltage detection circuit 432 serve as a voltage detector with hysteresis for a gate of the over-voltage detection/comparison element (Q3). In basic terms, said elements function in a similar manner to the function performed by corresponding elements Q1 and Q2, diode D1 and resistors R1 through R6 of the under-voltage detection circuit 431. However, an over-voltage indication for a voltage potential at the terminal VSENSE2 is presented from a drain terminal of the over-voltage detection/comparison element (Q3). In this embodiment, element Q4 is employed to insert hysteresis into the circuit by the off/on state of its drain-source connection. In addition, hysteresis occurs when the VSENSE2 potential falls below the threshold value. When a voltage potential at the terminal VSENSE2 is less than an over-voltage threshold, or the over-voltage detection/comparison element (Q3) is in an “OFF” (and element Q4 is in an “ON”) state condition as defined by:

\[
VSENSE2(+) = \left[ Vgs(th)(Q3) \left(1 + \frac{R8}{R7 + R1 + \text{on}(Q4)} \right) \right] 
\]

As such, a drain of over-voltage detection/comparison element (Q3) is at voltage potential corresponding to the terminal VBIAS. Thus, an indication is provided to the output terminal (“OV”) that indicates that the voltage potential at the terminal VSENSE2 is below the over-voltage condition.

[0059] When the voltage potential at the terminal VSENSE2 exceeds the over-voltage threshold, the over-
voltage detection/comparison element (Q3) is in an “ON” state condition (and element Q4 is in an “OFF” state condition) as defined by:

\[ V_{SENSE} = V_{GS}(Q3) \left[ 1 + \frac{R_B}{(R_T + R_O)} \right] \]  

(EQ 8)

In this condition, a drain terminal of the over-voltage detection/comparison element (Q3) corresponds to the voltage potential at the terminal GROUND. Thus, an indication is provided to the output terminal (‘OV’) that indicates that the voltage potential at the terminal VSENSE2 is above the over-voltage condition.

[0060] FIG. 5 is another circuit diagram of a power good circuit 500 according to an example embodiment of the present disclosure.

[0061] Because the under-voltage circuitry 431 and over-voltage circuitry 432 present a voltage potential corresponding to the terminal GROUND at their respective indicated output terminals (“UV”, “OV”) as illustrated in FIG. 4, the output terminals (“UV”, “OV”) can be combined. Accordingly, the power good circuit 500 includes a single power good output terminal (“PG”) that receives output signals from both the under-voltage circuitry 531 and over-voltage circuitry 532. Additionally, sensed signals from the terminal VSENSE1 and the terminal VSENSE2 may similarly be combined into a single terminal VSENSE. This variation allows a magnitude of a single voltage potential to be monitored to verify that the voltage potential remains within a range that is considered wholesome. However, if the potential falls outside of this range an indication (PG to GROUND potential) is given to indicate this condition. This variation shown in FIG. 5 is collogiually know as a window detector or window comparator, and the output signal at the PG output terminal is shown in FIG. 6 for the various conditions of the VSENSE potential.

[0062] FIG. 6 is a graphical illustration of an output signal 611 of a power good circuit (e.g., circuit 500 of FIG. 3 and circuit 500 of FIG. 5) with different input conditions at the input VSENSE input 605 that change in magnitude with time (601) with regards to the various under-voltage and over-voltage thresholds, according to an example embodiment of the present disclosure. The threshold points 606 correspond to the UV– and UV+ voltage thresholds (VSENSE1– and VSENSE1+, respectively) and the OV– and OV+ voltage thresholds (VSENSE2– and VSENSE2+, respectively).

[0063] The graph 608 is a representation of the logic state of the output ‘PG’ with respect to a time-varying voltage signal at a terminal VSENSE (e.g., the terminal VSENSE of FIG. 5). The graph 608 indicates the state of output ‘PG’ 604 with respect to ground 603 and with respect to time 607. As illustrated, as the VSENSE potential assumes different values above and below each threshold voltage (VSENSE1–, VSENSE1+, VSENSE2– and VSENSE2+), the output ‘PG’ changes state according to the potential provided to the gates of monitoring transistors Q1 (for under voltage) and Q3 (for over voltage), in accordance with EQ1 through EQ8 in correspondence to circuit 500 of FIG. 3 or circuit 500 of FIG. 5.

[0064] The graph 608 is mapped to a graph of the logic state of the power good output signal (‘PG’) 611 which is a measurement of voltage with respect to VBIAS 612 over time 607. This graph is a pictorial indication of the state of output ‘PG’ as the input VSENSE varies with time and reveals how the output ‘PG’ may be suitably employed to be in electrical communication with a circuit that is sensitive to or damaged by the level of the input VSENSE if this potential is beneath or above a certain range of voltage values, such as the multi-function circuit indicated in FIG. 1.

[0065] While the present disclosure has been particularly shown and described with references to example embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the scope of the present disclosure encompassed by the appended claims.

What is claimed is:

1. An under-voltage detection circuit comprising: a GaN high electron mobility transistor (HEMT) configured to operate as both a voltage comparator and a voltage reference.

2. The circuit of claim 1, wherein the GaN HEMT is configured to use its gate source threshold voltage for voltage comparison and reference.

3. The circuit of claim 1, wherein the GaN HEMT is an electrically temperature-stable element over a temperature range of ~55°C to 150°C.

4. The circuit of claim 1, wherein the GaN HEMT is configured as a saturated switch that includes a drain-source connection, wherein a drain-source off/on state is determined by a gate-source threshold voltage (Vgs(th)), wherein the drain-source connection is off when the gate-source voltage is less than Vgs(th); and wherein the drain source connection is on when the gate-source voltage exceeds Vgs(th).

5. The circuit of claim 4, further comprising a voltage divider in electrical communication with the GaN HEMT, the voltage divider configured to determine a magnitude of potential at a voltage input terminal, the voltage input terminal having a potential that is greater than the gate-source threshold voltage potential Vgs(th).

6. The circuit of claim 1 further comprising a logic state inversion element configured to provide electrical hysteresis, the logic state inversion element in electrical communication with a gate of the GaN HEMT.

7. An over-voltage detection circuit comprising: a GaN high electron mobility transistor (HEMT) configured to operate as both a voltage comparator and a voltage reference.

8. The circuit of claim 7, wherein the GaN HEMT is configured to use its gate source threshold voltage for voltage comparison and reference.

9. The circuit of claim 8, wherein the GaN HEMT is an electrically temperature-stable element over a temperature range of ~55°C to 150°C.

10. The circuit of claim 9, wherein the GaN HEMT is configured as a saturated switch that includes a drain-source connection, wherein a drain-source off/on state is determined by a gate-source threshold voltage (Vgs(th)), wherein the drain-source connection is off when the gate-source voltage is less than Vgs(th); and wherein the drain source connection is on when the gate-source voltage exceeds Vgs(th).

11. The circuit of claim 10, further comprising a voltage divider in electrical communication with the GaN HEMT, the voltage divider configured to determine a magnitude of
potential at a voltage input terminal whose potential is greater than the gate-source threshold voltage potential $V_{gs(th)}$.

12. The circuit of claim 11 further comprising a logic state inversion element configured to provide electrical hysteresis, the logic state inversion element in electrical communication with the gate of the GaN HEMT, the logic state inversion element being a GaN high electron mobility transistor (HEMT).

13. A detection circuit comprising:
an under-voltage detection circuit including a first GaN high electron mobility transistor (HEMT) configured to operate as both a voltage comparator and a voltage reference; and
an over-voltage detection circuit including a second GaN high electron mobility transistor (HEMT) configured to operate as both a voltage comparator and a voltage reference.

14. The circuit of claim 13 wherein both the under-voltage detection circuit and the over-voltage detection circuit provide outputs to a single power good output terminal.

15. The circuit of claim 14 wherein the under-voltage detection circuit provides an output to an under-voltage output terminal.

16. The circuit of claim 15 wherein the over-voltage detection circuit provides an output to an over-voltage output terminal.

17. The circuit of claim 16 further comprising:
a first voltage divider in electrical communication with the first GaN HEMT, the first voltage divider configured to determine a magnitude of potential at a terminal whose potential is greater than the gate-source threshold voltage potential $V_{gs(th)}$ of the first GaN HEMT in the under voltage detection circuit; and
a second voltage divider in electrical communication with the second GaN HEMT, the second voltage divider configured to determine a magnitude of potential at a terminal whose potential is greater than the gate-source threshold voltage potential $V_{gs(th)}$ of the second GaN HEMT in the over voltage detection circuit.

18. The circuit of claim 17, wherein both the first GaN HEMT and the second GaN HEMT are electrically temperature-stable elements at a temperature range of $-55^\circ$ C. to $150^\circ$ C.

19. The circuit of claim 18, wherein both the first GaN HEMT and the second GaN HEMT are configured as saturated switches.

20. The circuit of claim 19 further comprising at least one logic state inversion element configured to provide electrical hysteresis to the under voltage detection circuit and the over voltage detection circuit, the at least one logic state inversion element in electrical communication with a gate of each of the first GaN HEMT and second GaN HEMT; and
where the at least one logic state inversion element is a GaN high electron mobility transistor (HEMT).

21. The circuit of claim 20, wherein:
the first GaN HEMT is configured to use its gate source threshold voltage for voltage comparison and reference; and
the second GaN HEMT is configured to use its gate source threshold voltage for voltage comparison and reference.

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