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(54) Title: THREE-DIMENSIONAL MEMORY DEVICE WITH ON-AXIS SELF-ALIGNED DRAIN-SELECT-LEVEL ISOLATION STRUCTURE AND METHODS OF MANUFACTURING THE SAME

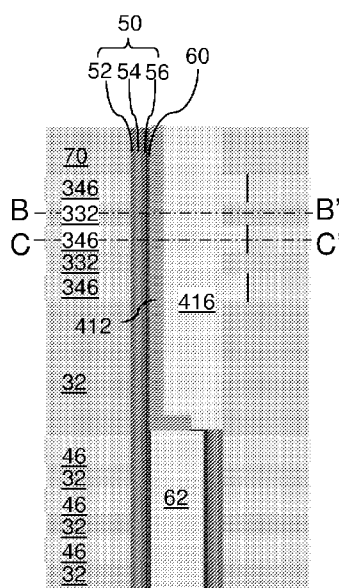


FIG. 41A

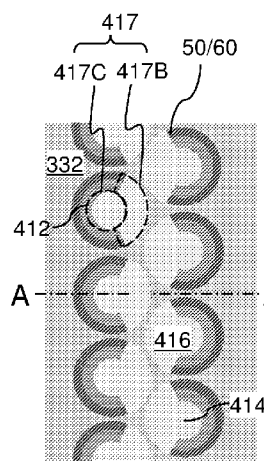


FIG. 41B

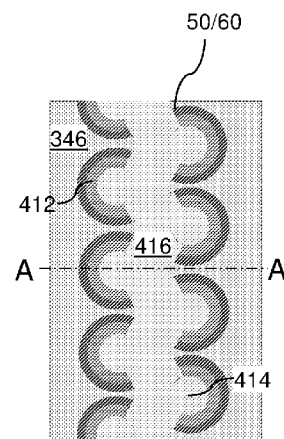


FIG. 41C

(57) Abstract: A three-dimensional memory device includes an alternating stack of insulating layers and electrically conductive layers located over a substrate, memory openings vertically extending through the alternating stack, and memory stack structures located within a respective one of the memory openings. A multi-pillared dielectric isolation structure extends through upper sections of a neighboring pair of memory openings. The multi-pillared dielectric isolation structure includes a plurality of dielectric pillar portions located within a respective one of the memory openings, and at least one horizontally-extending portion adjoining each of the plurality of dielectric pillar portions and located between a vertically neighboring pair of insulating layers within the alternating stack. The at least one horizontally-extending portion laterally separates laterally neighboring strips of at least one electrically conductive layer

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- *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

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**THREE-DIMENSIONAL MEMORY DEVICE WITH ON-AXIS SELF-ALIGNED
DRAIN-SELECT-LEVEL ISOLATION STRUCTURE AND METHODS OF
MANUFACTURING THE SAME**

RELATED APPLICATION

[0001] The present application claims the benefit of priority of U.S. Non-Provisional Patent Application Serial No. 16/352,157 filed on March 13, 2019, the entire content of which is incorporated herein by reference.

FIELD

[0002] The present disclosure relates generally to the field of semiconductor devices, and particular to a three-dimensional memory device with on-axis self-aligned drain-select-level isolation structures and methods of manufacturing the same.

BACKGROUND

[0003] Three-dimensional vertical NAND strings having one bit per cell are disclosed in an article by T. Endoh et al., titled “Novel Ultra High Density Memory With A Stacked-Surrounding Gate Transistor (S-SGT) Structured Cell”, IEDM Proc. (2001) 33-36.

SUMMARY

[0004] According to an aspect of the present disclosure, a three-dimensional memory device is provided, which comprises: an alternating stack of insulating layers and electrically conductive layers located over a substrate; memory openings vertically extending through the alternating stack; memory stack structures located within a respective one of the memory openings, wherein each of the memory stack structures comprises a memory film and a vertical semiconductor channel; and a multi-pillared dielectric isolation structure comprising

a plurality of dielectric pillar portions located within a respective one of the memory openings and at least one horizontally-extending portion adjoining each of the plurality of dielectric pillar portions and located between a vertically neighboring pair of insulating layers within the alternating stack and laterally separating laterally neighboring strips of at least one electrically conductive layer within the alternating stack.

[0005] According to another aspect of the present disclosure, a method of forming a three-dimensional memory device is provided, which comprises: forming an alternating stack of insulating layers and spacer material layers over a substrate, wherein the spacer material layers are formed as, or are subsequently replaced with, electrically conductive layers; forming memory openings vertically extending through the alternating stack; forming memory stack structures within the memory openings, wherein each of the memory stack structures comprises a memory film and a vertical semiconductor channel having a cylindrical configuration; forming discrete corner cavities by removing an upper corner portion of each memory stack structure within two neighboring rows of memory openings using at least one etch process; forming at least one laterally-extending cavity by laterally recessing portions of the electrically conductive layers from the discrete corner cavities; and forming a multi-pillared dielectric isolation structure by depositing a dielectric material in volumes of the at least one laterally-extending cavity and in the discrete corner cavities.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] FIG. 1 is a schematic vertical cross-sectional view of a first exemplary structure after formation of at least one peripheral device, and a semiconductor material layer according to a first embodiment of the present disclosure.

[0007] FIG. 2 is a schematic vertical cross-sectional view of the first exemplary structure

after formation of an alternating stack of insulating layers and sacrificial material layers according to the first embodiment of the present disclosure.

[0008] FIG. 3 is a schematic vertical cross-sectional view of the first exemplary structure after formation of stepped terraces and a retro-stepped dielectric material portion according to the first embodiment of the present disclosure.

[0009] FIG. 4A is a schematic vertical cross-sectional view of the first exemplary structure after formation of memory openings and support openings according to the first embodiment of the present disclosure.

[0010] FIG. 4B is a top-down view of the first exemplary structure of FIG. 4A. The vertical plane A – A' is the plane of the cross-section for FIG. 4A.

[0011] FIGS. 5A – 5E are sequential schematic vertical cross-sectional views of a memory opening within the first exemplary structure during a first set of processing steps for forming a lower memory opening fill structure according to the first embodiment of the present disclosure.

[0012] FIGS. 6A – 6F are sequential schematic vertical cross-sectional views of a memory opening within the first exemplary structure during a second set of processing steps for forming a lower memory opening fill structure according to the first embodiment of the present disclosure.

[0013] FIG. 7A is a vertical cross-sectional view of a memory opening within the first exemplary structure after formation of an in-process upper memory opening fill structure according to the first embodiment of the present disclosure.

[0014] FIG. 7B is a top-down view of a region of the first exemplary structure at the processing steps of FIG. 7A.

[0015] FIG. 7C is a vertical cross-sectional view of a memory opening within a first

alternative embodiment of the first exemplary structure after formation of an in-process upper memory opening fill structure according to the first embodiment of the present disclosure.

[0016] FIG. 7D is a top-down view of a region of the alternative embodiment of the first exemplary structure at the processing steps of FIG. 7C.

[0017] FIG. 8A is a schematic vertical cross-sectional view of the first exemplary structure after formation of in-process memory opening fill structures and in-process support pillar structures according to the first embodiment of the present disclosure.

[0018] FIG. 8B is a partial see-through top-down view of the first exemplary structure of FIG. 8A. The vertical plane A – A' is the plane of the schematic vertical cross-sectional view of FIG. 8A.

[0019] FIG. 9A is a schematic vertical cross-sectional view of the first exemplary structure after formation of a sacrificial planarization stopper layer and backside trenches according to the first embodiment of the present disclosure.

[0020] FIG. 9B is a partial see-through top-down view of the first exemplary structure of FIG. 9A. The vertical plane A – A' is the plane of the schematic vertical cross-sectional view of FIG. 9A.

[0021] FIG. 10 is a schematic vertical cross-sectional view of the first exemplary structure after formation of backside recesses according to the first embodiment of the present disclosure.

[0022] FIGS. 11A – 11D are sequential vertical cross-sectional views of a region of the first exemplary structure during formation of electrically conductive layers according to the first embodiment of the present disclosure.

[0023] FIG. 12 is a schematic vertical cross-sectional view of the first exemplary structure at the processing step of FIG. 11D.

[0024] FIG. 13 is a schematic vertical cross-sectional view of the first exemplary structure after removal of a deposited conductive material from within the backside trench according to the first embodiment of the present disclosure.

[0025] FIG. 14A is a schematic vertical cross-sectional view of the first exemplary structure after formation of an insulating spacer and a backside contact structure according to the first embodiment of the present disclosure.

[0026] FIG. 14B is a magnified view of a region of the first exemplary structure of FIG. 14A.

[0027] FIG. 15 is a schematic vertical cross-sectional view of the first exemplary structure after removal of the sacrificial planarization stopper layer according to the first embodiment of the present disclosure.

[0028] FIG. 16A is a vertical cross-sectional view of a memory opening within the first exemplary structure at the processing steps of FIG. 15A.

[0029] FIG. 16B is a top-down view of a region of the first exemplary structure at the processing steps of FIGS. 15 and 16A.

[0030] FIG. 17A is a schematic vertical cross-sectional view of the first exemplary structure after formation of a patterned etch mask layer according to the first embodiment of the present disclosure.

[0031] FIG. 17B is a partial see-through top-down view of the first exemplary structure of FIG. 17A. The vertical plane A – A' is the plane of the schematic vertical cross-sectional view of FIG. 17A.

[0032] FIG. 18A is a vertical cross-sectional view of a memory opening within the first exemplary structure at the processing steps of FIGS. 17A and 17B.

[0033] FIG. 18B is a horizontal cross-sectional view of a region of the first exemplary

structure along the plane B – B' of FIG. 18A. The vertical plane A – A' is the plane of the vertical cross-sectional view of FIG. 18A.

[0034] FIG. 18C is a top-down view of a region of the first exemplary structure at the processing steps of FIGS. 17A, 17B, 18A, and 18B. The vertical plane A – A' is the plane of the vertical cross-sectional view of FIG. 18A.

[0035] FIG. 19A is a vertical cross-sectional view of a memory opening within the first exemplary structure after formation of discrete corner cavities according to the first embodiment of the present disclosure.

[0036] FIG. 19B is a horizontal cross-sectional view of a region of the first exemplary structure along the plane B – B' of FIG. 19A. The vertical plane A – A' is the plane of the vertical cross-sectional view of FIG. 18A.

[0037] FIG. 19C is a top-down view of a region of the first exemplary structure at the processing steps of FIGS. 19A and 19B. The vertical plane A – A' is the plane of the vertical cross-sectional view of FIG. 18A.

[0038] FIG. 20A is a vertical cross-sectional view of a memory opening within the first exemplary structure after formation of laterally-extending cavities according to the first embodiment of the present disclosure.

[0039] FIG. 20B is a horizontal cross-sectional view of a region of the first exemplary structure along the plane B – B' of FIG. 20A. The vertical plane A – A' is the plane of the vertical cross-sectional view of FIG. 20A.

[0040] FIG. 20C is a horizontal cross-sectional view of a region of the first exemplary structure along the plane C – C' of FIG. 20A. The vertical plane A – A' is the plane of the vertical cross-sectional view of FIG. 20A.

[0041] FIG. 21A is a vertical cross-sectional view of a memory opening within the first

exemplary structure after removal of remaining portions of the in-process upper memory opening fill structures and formation of an integrated cavity according to the first embodiment of the present disclosure.

[0042] FIG. 21B is a horizontal cross-sectional view of a region of the first exemplary structure along the plane B – B' of FIG. 21A. The vertical plane A – A' is the plane of the vertical cross-sectional view of FIG. 21A.

[0043] FIG. 21C is a horizontal cross-sectional view of a region of the first exemplary structure along the plane C – C' of FIG. 21A. The vertical plane A – A' is the plane of the vertical cross-sectional view of FIG. 21A.

[0044] FIG. 22A is a vertical cross-sectional view of a memory opening within the first exemplary structure after formation of a dielectric fill material layer according to the first embodiment of the present disclosure.

[0045] FIG. 22B is a horizontal cross-sectional view of a region of the first exemplary structure along the plane B – B' of FIG. 22A. The vertical plane A – A' is the plane of the vertical cross-sectional view of FIG. 22A.

[0046] FIG. 22C is a horizontal cross-sectional view of a region of the first exemplary structure along the plane C – C' of FIG. 22A. The vertical plane A – A' is the plane of the vertical cross-sectional view of FIG. 22A.

[0047] FIG. 23A is a vertical cross-sectional view of a memory opening within the first exemplary structure after formation of dielectric isolation structures according to the first embodiment of the present disclosure.

[0048] FIG. 23B is a horizontal cross-sectional view of a region of the first exemplary structure along the plane B – B' of FIG. 23A. The vertical plane A – A' is the plane of the vertical cross-sectional view of FIG. 23A.

[0049] FIG. 23C is a horizontal cross-sectional view of a region of the first exemplary structure along the plane C – C' of FIG. 23A. The vertical plane A – A' is the plane of the vertical cross-sectional view of FIG. 23A.

[0050] FIG. 24A is a vertical cross-sectional view of a memory opening within the first exemplary structure after formation of tubular gate electrodes according to the first embodiment of the present disclosure.

[0051] FIG. 24B is a horizontal cross-sectional view of a region of the first exemplary structure along the plane B – B' of FIG. 24A. The vertical plane A – A' is the plane of the vertical cross-sectional view of FIG. 24A.

[0052] FIG. 24C is a horizontal cross-sectional view of a region of the first exemplary structure along the plane C – C' of FIG. 24A. The vertical plane A – A' is the plane of the vertical cross-sectional view of FIG. 24A.

[0053] FIG. 25A is a vertical cross-sectional view of a memory opening within the first exemplary structure after formation of a drain-select-level gate dielectric layer according to the first embodiment of the present disclosure.

[0054] FIG. 25B is a vertical cross-sectional view of a memory opening within the first exemplary structure after formation of a first drain-select-level channel layer according to the first embodiment of the present disclosure.

[0055] FIG. 25C is a vertical cross-sectional view of a memory opening within the first exemplary structure after formation of an opening extending to a connection channel portion according to the first embodiment of the present disclosure.

[0056] FIG. 26A is a vertical cross-sectional view of a memory opening within the first exemplary structure after formation of a second drain-select-level channel layer and a drain-select-level dielectric core according to the first embodiment of the present disclosure.

[0057] FIG. 26B is a horizontal cross-sectional view of a region of the first exemplary structure along the plane B – B' of FIG. 26A. The vertical plane A – A' is the plane of the vertical cross-sectional view of FIG. 26A.

[0058] FIG. 27A is a vertical cross-sectional view of a memory opening within the first exemplary structure after formation of an annular dielectric spacer and a drain region according to the first embodiment of the present disclosure.

[0059] FIG. 27B is a horizontal cross-sectional view of a region of the first exemplary structure along the plane B – B' of FIG. 27A. The vertical plane A – A' is the plane of the vertical cross-sectional view of FIG. 27A.

[0060] FIG. 28A is a schematic vertical cross-sectional view of the first exemplary structure after the processing steps of FIGS. 27A and 27B.

[0061] FIG. 28B is a top-down view of the first exemplary structure of FIG. 27A. The vertical plane A – A' is the plane of the schematic vertical cross-sectional view of FIG. 27A.

[0062] FIG. 29 is a top-down view of an alternative configuration for the first exemplary structure of FIGS. 28A and 28B according to the first embodiment of the present disclosure.

[0063] FIG. 30A is a schematic vertical cross-sectional view of the first exemplary structure after formation of a contact level dielectric layer and additional contact via structures according to the first embodiment of the present disclosure.

[0064] FIG. 30B is a top-down view of the first exemplary structure of FIG. 30A. The vertical plane A – A' is the plane of the schematic vertical cross-sectional view of FIG. 30A.

[0065] FIG. 31 is a schematic vertical cross-sectional view of a region of a second exemplary structure after formation of a dielectric core within a memory opening according to a second embodiment of the present disclosure.

[0066] FIG. 32A is a vertical cross-sectional view of a memory opening within the

second exemplary structure after formation of a continuous dielectric liner according to the second embodiment of the present disclosure.

[0067] FIG. 32B is a horizontal cross-sectional view of a region of the second exemplary structure along the plane B – B' of FIG. 32A. The vertical plane A – A' is the plane of the vertical cross-sectional view of FIG. 32A.

[0068] FIG. 33A is a vertical cross-sectional view of a memory opening within the second exemplary structure after formation of a semiconductor fill material portion according to the second embodiment of the present disclosure.

[0069] FIG. 33B is a horizontal cross-sectional view of a region of the second exemplary structure along the plane B – B' of FIG. 33A. The vertical plane A – A' is the plane of the vertical cross-sectional view of FIG. 33A.

[0070] FIG. 34A is a vertical cross-sectional view of a memory opening within the second exemplary structure after replacement of the sacrificial material layers with electrically conductive layers according to the second embodiment of the present disclosure.

[0071] FIG. 34B is a horizontal cross-sectional view of a region of the second exemplary structure along the plane B – B' of FIG. 34A. The vertical plane A – A' is the plane of the vertical cross-sectional view of FIG. 34A.

[0072] FIG. 35A is a schematic vertical cross-sectional view of the second exemplary structure after formation of a patterned etch mask layer according to the second embodiment of the present disclosure.

[0073] FIG. 35B is a partial see-through top-down view of the second exemplary structure of FIG. 35A. The vertical plane A – A' is the plane of the schematic vertical cross-sectional view of FIG. 35A.

[0074] FIG. 36A is a vertical cross-sectional view of a memory opening within the

second exemplary structure at the processing steps of FIGS. 35A and 35B.

[0075] FIG. 36B is a horizontal cross-sectional view of a region of the second exemplary structure along the plane B – B' of FIG. 36A. The vertical plane A – A' is the plane of the vertical cross-sectional view of FIG. 36A.

[0076] FIG. 37A is a vertical cross-sectional view of a memory opening within the second exemplary structure after removal of unmasked portions of dielectric liners according to the second embodiment of the present disclosure.

[0077] FIG. 37B is a horizontal cross-sectional view of a region of the second exemplary structure along the plane B – B' of FIG. 37A. The vertical plane A – A' is the plane of the vertical cross-sectional view of FIG. 37A.

[0078] FIG. 38A is a vertical cross-sectional view of a memory opening within the second exemplary structure after etching portions of the vertical semiconductor channels and the memory films that underlie openings in the patterned etch mask layer and formation of discrete corner cavities according to the second embodiment of the present disclosure.

[0079] FIG. 38B is a horizontal cross-sectional view of a region of the second exemplary structure along the plane B – B' of FIG. 38A. The vertical plane A – A' is the plane of the vertical cross-sectional view of FIG. 38A.

[0080] FIG. 39A is a vertical cross-sectional view of a memory opening within the second exemplary structure after formation of laterally-extending cavities according to the second embodiment of the present disclosure.

[0081] FIG. 39B is a horizontal cross-sectional view of a region of the second exemplary structure along the plane B – B' of FIG. 39A. The vertical plane A – A' is the plane of the vertical cross-sectional view of FIG. 39A.

[0082] FIG. 39C is a horizontal cross-sectional view of a region of the second exemplary

structure along the plane C – C' of FIG. 39A. The vertical plane A – A' is the plane of the vertical cross-sectional view of FIG. 39A.

[0083] FIG. 40A is a vertical cross-sectional view of a memory opening within the second exemplary structure after removal of remaining portions of the semiconductor fill material portions according to the second embodiment of the present disclosure.

[0084] FIG. 40B is a horizontal cross-sectional view of a region of the second exemplary structure along the plane B – B' of FIG. 40A. The vertical plane A – A' is the plane of the vertical cross-sectional view of FIG. 40A.

[0085] FIG. 40C is a horizontal cross-sectional view of a region of the second exemplary structure along the plane C – C' of FIG. 40A. The vertical plane A – A' is the plane of the vertical cross-sectional view of FIG. 40A.

[0086] FIG. 41A is a vertical cross-sectional view of a memory opening within the second exemplary structure after formation of multi-pillared dielectric isolation structures according to the second embodiment of the present disclosure.

[0087] FIG. 41B is a horizontal cross-sectional view of a region of the second exemplary structure along the plane B – B' of FIG. 41A. The vertical plane A – A' is the plane of the vertical cross-sectional view of FIG. 41A.

[0088] FIG. 41C is a horizontal cross-sectional view of a region of the second exemplary structure along the plane C – C' of FIG. 41A. The vertical plane A – A' is the plane of the vertical cross-sectional view of FIG. 41A.

[0089] FIG. 42A is a vertical cross-sectional view of a memory opening within the second exemplary structure after formation of drain regions according to the second embodiment of the present disclosure.

[0090] FIG. 42B is a top-down view of a region of the second exemplary structure along

the plane B – B' of FIG. 42A. The vertical plane A – A' is the plane of the vertical cross-sectional view of FIG. 42A.

[0091] FIG. 42C is a horizontal cross-sectional view of a region of the second exemplary structure along the plane C – C' of FIG. 42A. The vertical plane A – A' is the plane of the vertical cross-sectional view of FIG. 42A.

[0092] FIG. 43 is a vertical cross-sectional view of a memory opening within an alternative configuration of the second exemplary structure after deposition of a sacrificial semiconductor material layer and an ion implantation process according to the second embodiment of the present disclosure.

[0093] FIG. 44 is a vertical cross-sectional view of a memory opening within the alternative configuration of the second exemplary structure after removal of corner portions of the semiconductor fill material portions according to the second embodiment of the present disclosure.

[0094] FIG. 45 is a vertical cross-sectional view of a memory opening within the alternative configuration of the second exemplary structure after formation of discrete corner cavities according to the second embodiment of the present disclosure.

[0095] FIG. 46 is a vertical cross-sectional view of a memory opening within the alternative configuration of the second exemplary structure after formation of laterally-extending cavities according to the second embodiment of the present disclosure.

[0096] FIG. 47 is a vertical cross-sectional view of a memory opening within the alternative configuration of the second exemplary structure after removal of remaining portions of the sacrificial semiconductor material layer and formation of multi-pillared dielectric isolation structures according to the second embodiment of the present disclosure.

[0097] FIG. 48 is a vertical cross-sectional view of a memory opening within the

alternative configuration of the second exemplary structure after vertically recessing dielectric pillar portions of the multi-pillared dielectric isolation structures according to the second embodiment of the present disclosure.

[0098] FIG. 49 is a vertical cross-sectional view of a memory opening within the alternative configuration of the second exemplary structure after formation of drain regions according to the second embodiment of the present disclosure.

[0099] FIG. 50A is a schematic vertical cross-sectional view of the second exemplary structure after the processing steps of FIG. 49.

[0100] FIG. 50B is a top-down view of the second exemplary structure of FIG. 50A. The vertical plane A – A' is the plane of the schematic vertical cross-sectional view of FIG. 50A.

[0101] FIG. 51 is a top-down view of an alternative configuration for the second exemplary structure of FIGS. 50A and 50B according to the second embodiment of the present disclosure.

[0102] FIG. 52A is a schematic vertical cross-sectional view of the second exemplary structure after formation of a contact level dielectric layer and additional contact via structures according to the second embodiment of the present disclosure.

[0103] FIG. 52B is a top-down view of the second exemplary structure of FIG. 52A. The vertical plane A – A' is the plane of the schematic vertical cross-sectional view of FIG. 52A.

[0104] FIG. 53 is a vertical cross-sectional view of a memory die including the first or second exemplary structure according to an embodiment of the present disclosure.

DETAILED DESCRIPTION

[0105] As discussed above, various embodiments of the present disclosure are directed to a three-dimensional memory device having on-axis, self-aligned drain-select-level isolation structures and methods of manufacturing the same, the various aspects of which are described

below. The embodiments of the disclosure can be used to form various structures including a multilevel memory structure, non-limiting examples of which include semiconductor devices such as three-dimensional monolithic memory array devices comprising a plurality of NAND memory strings.

[0106] The drawings are not drawn to scale. Multiple instances of an element may be duplicated where a single instance of the element is illustrated, unless absence of duplication of elements is expressly described or clearly indicated otherwise. Ordinals such as “first,” “second,” and “third” are used merely to identify similar elements, and different ordinals may be used across the specification and the claims of the instant disclosure. The same reference numerals refer to the same element or similar element. Unless otherwise indicated, elements having the same reference numerals are presumed to have the same composition and the same function. Unless otherwise indicated, a “contact” between elements refers to a direct contact between elements that provides an edge or a surface shared by the elements. As used herein, a first element located “on” a second element can be located on the exterior side of a surface of the second element or on the interior side of the second element. As used herein, a first element is located “directly on” a second element if there exist a physical contact between a surface of the first element and a surface of the second element. As used herein, a “prototype” structure or an “in-process” structure refers to a transient structure that is subsequently modified in the shape or composition of at least one component therein.

[0107] As used herein, a “layer” refers to a material portion including a region having a thickness. A layer may extend over the entirety of an underlying or overlying structure, or may have an extent less than the extent of an underlying or overlying structure. Further, a layer may be a region of a homogeneous or inhomogeneous continuous structure that has a thickness less than the thickness of the continuous structure. For example, a layer may be

located between any pair of horizontal planes between, or at, a top surface and a bottom surface of the continuous structure. A layer may extend horizontally, vertically, and/or along a tapered surface. A substrate may be a layer, may include one or more layers therein, or may have one or more layer thereupon, thereabove, and/or therebelow.

[0108] As used herein, a first surface and a second surface are “vertically coincident” with each other if the second surface overlies or underlies the first surface and there exists a vertical plane or a substantially vertical plane that includes the first surface and the second surface. A substantially vertical plane is a plane that extends straight along a direction that deviates from a vertical direction by an angle less than 5 degrees. A vertical plane or a substantially vertical plane is straight along a vertical direction or a substantially vertical direction, and may, or may not, include a curvature along a direction that is perpendicular to the vertical direction or the substantially vertical direction.

[0109] A monolithic three-dimensional memory array is a memory array in which multiple memory levels are formed above a single substrate, such as a semiconductor wafer, with no intervening substrates. The term “monolithic” means that layers of each level of the array are directly deposited on the layers of each underlying level of the array. In contrast, two dimensional arrays may be formed separately and then packaged together to form a non-monolithic memory device. For example, non-monolithic stacked memories have been constructed by forming memory levels on separate substrates and vertically stacking the memory levels, as described in U.S. Patent No. 5,915,167 titled “Three-dimensional Structure Memory.” The substrates may be thinned or removed from the memory levels before bonding, but as the memory levels are initially formed over separate substrates, such memories are not true monolithic three-dimensional memory arrays. The three-dimensional memory devices of various embodiments of the present disclosure include a monolithic three-

dimensional NAND string memory device, and can be fabricated using the various embodiments described herein.

[0110] Generally, a semiconductor package (or a “package”) refers to a unit semiconductor device that can be . attached to a circuit board through a set of pins or solder balls. A semiconductor package may include a semiconductor chip (or a “chip”) or a plurality of semiconductor chips that are bonded thereamongst, for example, by flip-chip bonding or another chip-to-chip bonding. A package or a chip may include a single semiconductor die (or a “die”) or a plurality of semiconductor dies. A die is the smallest unit that can independently execute external commands or report status. Typically, a package or a chip with multiple dies is capable of simultaneously executing as many external commands as the total number of planes therein. Each die includes one or more planes. Identical concurrent operations can be executed in each plane within a same die, although there may be some restrictions. In case a die is a memory die, i.e., a die including memory elements, concurrent read operations, concurrent write operations, or concurrent erase operations can be performed in each plane within a same memory die. In a memory die, each plane contains a number of memory blocks (or “blocks”), which are the smallest unit that can be erased by in a single erase operation. Each memory block contains a number of pages, which are the smallest units that can be selected for programming. A page is also the smallest unit that can be selected for a read operation.

[0111] Referring to FIG. 1, a first exemplary structure according to the first embodiment of the present disclosure is illustrated, which can be used, for example, to fabricate a device structure containing vertical NAND memory devices. The first exemplary structure includes a substrate (9, 10), which can be a semiconductor substrate. The substrate can include a substrate semiconductor layer 9 and an optional semiconductor material layer 10. The

substrate semiconductor layer 9 maybe a semiconductor wafer or a semiconductor material layer, and can include at least one elemental semiconductor material (e.g., single crystal silicon wafer or layer), at least one III-V compound semiconductor material, at least one II-VI compound semiconductor material, at least one organic semiconductor material, or other semiconductor materials known in the art. The substrate can have a major surface 7, which can be, for example, a topmost surface of the substrate semiconductor layer 9. The major surface 7 can be a semiconductor surface. In one embodiment, the major surface 7 can be a single crystalline semiconductor surface, such as a single crystalline semiconductor surface.

[0112] As used herein, a “semiconducting material” refers to a material having electrical conductivity in the range from 1.0×10^{-5} S/m to 1.0×10^5 S/m. As used herein, a “semiconductor material” refers to a material having electrical conductivity in the range from 1.0×10^{-5} S/m to 1.0 S/m in the absence of electrical dopants therein, and is capable of producing a doped material having electrical conductivity in a range from 1.0 S/m to 1.0×10^5 S/m upon suitable doping with an electrical dopant. As used herein, an “electrical dopant” refers to a p-type dopant that adds a hole to a valence band within a band structure, or an n-type dopant that adds an electron to a conduction band within a band structure. As used herein, a “conductive material” refers to a material having electrical conductivity greater than 1.0×10^5 S/m. As used herein, an “insulator material” or a “dielectric material” refers to a material having electrical conductivity less than 1.0×10^{-5} S/m. As used herein, a “heavily doped semiconductor material” refers to a semiconductor material that is doped with electrical dopant at a sufficiently high atomic concentration to become a conductive material either as formed as a crystalline material or if converted into a crystalline material through an anneal process (for example, from an initial amorphous state), i.e., to have electrical conductivity greater than 1.0×10^5 S/m. A “doped semiconductor material” may be a

heavily doped semiconductor material, or may be a semiconductor material that includes electrical dopants (i.e., p-type dopants and/or n-type dopants) at a concentration that provides electrical conductivity in the range from 1.0×10^{-5} S/m to 1.0×10^5 S/m. An “intrinsic semiconductor material” refers to a semiconductor material that is not doped with electrical dopants. Thus, a semiconductor material may be semiconducting or conductive, and may be an intrinsic semiconductor material or a doped semiconductor material. A doped semiconductor material can be semiconducting or conductive depending on the atomic concentration of electrical dopants therein. As used herein, a “metallic material” refers to a conductive material including at least one metallic element therein. All measurements for electrical conductivities are made at the standard condition.

[0113] At least one semiconductor device 700 for a peripheral circuitry can be formed on a portion of the substrate semiconductor layer 9. The at least one semiconductor device can include, for example, field effect transistors. For example, at least one shallow trench isolation structure 720 can be formed by etching portions of the substrate semiconductor layer 9 and depositing a dielectric material therein. A gate dielectric layer, at least one gate conductor layer, and a gate cap dielectric layer can be formed over the substrate semiconductor layer 9, and can be subsequently patterned to form at least one gate structure (750, 752, 754, 758), each of which can include a gate dielectric 750, a gate electrode (752, 754), and a gate cap dielectric 758. The gate electrode (752, 754) may include a stack of a first gate electrode portion 752 and a second gate electrode portion 754. At least one gate spacer 756 can be formed around the at least one gate structure (750, 752, 754, 758) by depositing and anisotropically etching a dielectric liner. Active regions 730 can be formed in upper portions of the substrate semiconductor layer 9, for example, by introducing electrical dopants using the at least one gate structure (750, 752, 754, 758) as masking structures.

Additional masks may be used as needed. The active region 730 can include source regions and drain regions of field effect transistors. A first dielectric liner 761 and a second dielectric liner 762 can be optionally formed. Each of the first and second dielectric liners (761, 762) can comprise a silicon oxide layer, a silicon nitride layer, and/or a dielectric metal oxide layer. As used herein, silicon oxide includes silicon dioxide as well as non-stoichiometric silicon oxides having more or less than two oxygen atoms for each silicon atoms. Silicon dioxide is preferred. In an illustrative example, the first dielectric liner 761 can be a silicon oxide layer, and the second dielectric liner 762 can be a silicon nitride layer. The least one semiconductor device for the peripheral circuitry can contain a driver circuit for memory devices to be subsequently formed, which can include at least one NAND device.

[0114] A dielectric material such as silicon oxide can be deposited over the at least one semiconductor device, and can be subsequently planarized to form a planarization dielectric layer 770. In one embodiment the planarized top surface of the planarization dielectric layer 770 can be coplanar with a top surface of the dielectric liners (761, 762). Subsequently, the planarization dielectric layer 770 and the dielectric liners (761, 762) can be removed from an area to physically expose a top surface of the substrate semiconductor layer 9. As used herein, a surface is “physically exposed” if the surface is in physical contact with vacuum, or a gas phase material (such as air).

[0115] The optional semiconductor material layer 10, if present, can be formed on the top surface of the substrate semiconductor layer 9 prior to, or after, formation of the at least one semiconductor device 700 by deposition of a single crystalline semiconductor material, for example, by selective epitaxy. The deposited semiconductor material can be the same as, or can be different from, the semiconductor material of the substrate semiconductor layer 9. The deposited semiconductor material can be any material that can be used for the substrate

semiconductor layer 9 as described above. The single crystalline semiconductor material of the semiconductor material layer 10 can be in epitaxial alignment with the single crystalline structure of the substrate semiconductor layer 9. Portions of the deposited semiconductor material located above the top surface of the planarization dielectric layer 770 can be removed, for example, by chemical mechanical planarization (CMP). In this case, the semiconductor material layer 10 can have a top surface that is coplanar with the top surface of the planarization dielectric layer 770.

[0116] The region (i.e., area) of the at least one semiconductor device 700 is herein referred to as a peripheral device region 200. The region in which a memory array is subsequently formed is herein referred to as a memory array region 100. A staircase region 300 for subsequently forming stepped terraces of electrically conductive layers can be provided between the memory array region 100 and the peripheral device region 200.

[0117] Referring to FIG. 2, a stack of an alternating plurality of first material layers and second material layers is formed over the top surface of the substrate (9, 10). As used herein, a “material layer” refers to a layer including a material throughout the entirety thereof. As used herein, an alternating plurality of first elements and second elements refers to a structure in which instances of the first elements and instances of the second elements alternate. Each first material layer includes a first material, and each second material layer includes a second material that is different from the first material.

[0118] . In one embodiment, each first material layer can be an insulating layer 32 or a drain-select-level insulating layer 332, and each second material layer can be a word-line-level sacrificial material layer 42 or a drain-select-level sacrificial material layer 342. A vertically alternating sequence of the word-line-level insulating layers 32 and the word-line-level sacrificial material layers 42 can be formed. The topmost one of the word-line-level

insulating layers 32 can have a greater thickness than underlying word-line-level insulating layers 32. For example, the word-line-level insulating layers 32 other than the topmost insulating layer 32 can have a thickness in a range from 20 nm to 60 nm, and the topmost insulating layer 32 can have a thickness in a range from 30 nm to 150 nm, although lesser and greater thicknesses can also be used. The word-line-level sacrificial material layers 42 can have a thickness in a range from 20 nm to 60 nm. A vertically alternating sequence of drain-select-level sacrificial material layers 342 and drain-select-level insulating layers 332 can be subsequently formed. The drain-select-level insulating layers 332 can have a thickness in a range from 20 nm to 60 nm, and the drain-select-level sacrificial material layers 342 can have a thickness in a range from 20 nm to 60 nm. An insulating cap layer 70 can be subsequently formed.

[0119] The word-line-level insulating layers 32, the drain-select-level insulating layers 332, and the insulating cap layer 70 are herein collectively referred to as insulating layers (32, 332, 70). The word-line-level sacrificial material layers 42 and the drain-select-level sacrificial material layers (42, 342) are herein collectively referred to as sacrificial material layers (42, 342). The layer stack including the word-line-level insulating layers 32, the word-line-level sacrificial material layers 42, the drain-select-level insulating layers 332, the drain-select-level sacrificial material layers 342, and the insulating cap layer 70 is herein referred to as an alternating stack (32, 42, 332, 342, 70). The word-line-level insulating layers 32, the drain-select-level insulating layers 332, and the insulating cap layer 70 can be composed of the first material, and the word-line-level sacrificial material layers 42 and the drain-select-level sacrificial material layers 342 can be composed of a second material different from that of word-line-level insulating layers 32. Insulating materials that can be used for the word-line-level insulating layers 32, the drain-select-level insulating layers 332, and the insulating

cap layer 70 include, but are not limited to, silicon oxide (including doped or undoped silicate glass), silicon nitride, silicon oxynitride, organosilicate glass (OSG), spin-on dielectric materials, dielectric metal oxides that are commonly known as high dielectric constant (high-k) dielectric oxides (e.g., aluminum oxide, hafnium oxide, etc.) and silicates thereof, dielectric metal oxynitrides and silicates thereof, and organic insulating materials. In one embodiment, the first material of the word-line-level insulating layers 32, the drain-select-level insulating layers 332, and the insulating cap layer 70 can be silicon oxide.

[0120] The second material of the word-line-level sacrificial material layers 42 and the drain-select-level sacrificial material layers 342 is a sacrificial material that can be removed selective to the first material of the word-line-level insulating layers 32. As used herein, a removal of a first material is “selective to” a second material if the removal process removes the first material at a rate that is at least twice the rate of removal of the second material. The ratio of the rate of removal of the first material to the rate of removal of the second material is herein referred to as a “selectivity” of the removal process for the first material with respect to the second material.

[0121] The word-line-level sacrificial material layers 42 and the drain-select-level sacrificial material layers 342 may comprise an insulating material, a semiconductor material, or a conductive material. The second material of the word-line-level sacrificial material layers 42 and the drain-select-level sacrificial material layers 342 can be subsequently replaced with electrically conductive electrodes which can function, for example, as control gate electrodes of a vertical NAND device. Non-limiting examples of the second material include silicon nitride, an amorphous semiconductor material (such as amorphous silicon), and a polycrystalline semiconductor material (such as polysilicon). In one embodiment, the word-line-level sacrificial material layers 42 and the drain-select-level sacrificial material

layers 342 can be spacer material layers that comprise silicon nitride or a semiconductor material including at least one of silicon and germanium.

[0122] In one embodiment, the word-line-level insulating layers 32, the drain-select-level insulating layers 332, and the insulating cap layer 70 can include silicon oxide, and sacrificial material layers can include silicon nitride sacrificial material layers. The first material of the word-line-level insulating layers 32, the drain-select-level insulating layers 332, and the insulating cap layer 70 can be deposited, for example, by chemical vapor deposition (CVD). For example, if silicon oxide is used for the word-line-level insulating layers 32, the drain-select-level insulating layers 332, and the insulating cap layer 70, tetraethyl orthosilicate (TEOS) can be used as the precursor material for the CVD process. The second material of the word-line-level sacrificial material layers 42 and the drain-select-level sacrificial material layers 342 can be formed, for example, CVD or atomic layer deposition (ALD).

[0123] . While the descriptions of the present disclosure refer to an embodiment in which the word-line-level sacrificial material layers 42 and the drain-select-level sacrificial material layers 342 are formed as spacer material layers that are formed between each vertically neighboring pair of the word-line-level insulating layers 32, the drain-select-level insulating layers 332, and the insulating cap layer 70, in other embodiments electrically conductive layers are formed as spacer material layers in lieu of the word-line-level sacrificial material layers 42 and the drain-select-level sacrificial material layers 342. In this case, steps for replacing the spacer material layers with electrically conductive layers can be omitted.

[0124] Referring to FIG. 3, stepped surfaces are formed at a peripheral region of the alternating stack (32, 42, 332, 342, 70), which is herein referred to as a terrace region. As used herein, “stepped surfaces” refer to a set of surfaces that include at least two horizontal surfaces and at least two vertical surfaces such that each horizontal surface is adjoined to a

first vertical surface that extends upward from a first edge of the horizontal surface, and is adjoined to a second vertical surface that extends downward from a second edge of the horizontal surface. A stepped cavity is formed within the volume from which portions of the alternating stack (32, 42, 332, 342, 70) are removed through formation of the stepped surfaces. A “stepped cavity” refers to a cavity having stepped surfaces.

[0125] The terrace region is formed in the staircase region 300, which is located between the memory array region 100 and the peripheral device region 200 containing the at least one semiconductor device for the peripheral circuitry. The stepped cavity can have various stepped surfaces such that the horizontal cross-sectional shape of the stepped cavity changes in steps as a function of the vertical distance from the top surface of the substrate (9, 10). In one embodiment, the stepped cavity can be formed by repetitively performing a set of processing steps. The set of processing steps can include, for example, an etch process of a first type that vertically increases the depth of a cavity by one or more levels, and an etch process of a second type that laterally expands the area to be vertically etched in a subsequent etch process of the first type. As used herein, a “level” of a structure including alternating plurality is defined as the relative position of a pair of a first material layer and a second material layer within the structure.

[0126] . Each word-line-level sacrificial material layer 42 other than a topmost word-line-level sacrificial material layer 42 within the alternating stack (32, 42, 332, 342, 70) laterally extends farther than any overlying word-line-level sacrificial material layer 42 within the alternating stack (32, 42, 332, 342, 70) in the terrace region. The terrace region includes stepped surfaces of the alternating stack (32, 42, 332, 342, 70) that continuously extend from a bottommost layer within the alternating stack (32, 42, 332, 342, 70) to a topmost layer within the alternating stack (32, 42, 332, 342, 70).

[0127] A retro-stepped dielectric material portion 65 (i.e., an insulating fill material portion) can be formed in the stepped cavity by deposition of a dielectric material therein. For example, a dielectric material such as silicon oxide can be deposited in the stepped cavity. Excess portions of the deposited dielectric material can be removed from above the top surface of the insulating cap layer 70, for example, by chemical mechanical planarization (CMP). The remaining portion of the deposited dielectric material filling the stepped cavity constitutes the retro-stepped dielectric material portion 65. As used herein, a “retro-stepped” element refers to an element that has stepped surfaces and a horizontal cross-sectional area that increases monotonically as a function of a vertical distance from a top surface of a substrate on which the element is present. If silicon oxide is used for the retro-stepped dielectric material portion 65, the silicon oxide of the retro-stepped dielectric material portion 65 may, or may not, be doped with dopants such as B, P, and/or F.

[0128] Referring to FIGS. 4A and 4B, a lithographic material stack (not shown) including at least a photoresist layer can be formed over the insulating cap layer 70 and the retro-stepped dielectric material portion 65, and can be lithographically patterned to form openings therein. The openings include a first set of openings formed over the memory array region 100 and a second set of openings formed over the staircase region 300. The pattern in the lithographic material stack can be transferred through the insulating cap layer 70 or the retro-stepped dielectric material portion 65, and through the alternating stack (32, 42, 332, 342, 70) by at least one anisotropic etch that uses the patterned lithographic material stack as an etch mask. Portions of the alternating stack (32, 42, 332, 342, 70) underlying the openings in the patterned lithographic material stack are etched to form memory openings 49 and support openings 19. As used herein, a “memory opening” refers to a structure in which memory elements, such as a memory stack structure, is subsequently formed. As used herein, a

“support opening” refers to a structure in which a support structure (such as a support pillar structure) that mechanically supports other elements is subsequently formed. The memory openings 49 are formed through the insulating cap layer 70 and the entirety of the alternating stack (32, 42, 332, 342, 70) in the memory array region 100. The support openings 19 are formed through the retro-stepped dielectric material portion 65 and the portion of the alternating stack (32, 42, 332, 342, 70) that underlie the stepped surfaces in the staircase region 300.

[0129] The memory openings 49 extend through the entirety of the alternating stack (32, 42, 332, 342, 70). The support openings 19 extend through a subset of layers within the alternating stack (32, 42, 332, 342, 70). The chemistry of the anisotropic etch process used to etch through the materials of the alternating stack (32, 42, 332, 342, 70) can alternate to optimize etching of the first and second materials in the alternating stack (32, 42, 332, 342, 70). The anisotropic etch can be, for example, a series of reactive ion etches. The sidewalls of the memory openings 49 and the support openings 19 can be substantially vertical, or can be tapered. The patterned lithographic material stack can be subsequently removed, for example, by ashing.

[0130] The memory openings 49 and the support openings 19 can extend from the top surface of the alternating stack (32, 42, 332, 342, 70) to at least the horizontal plane including the topmost surface of the semiconductor material layer 10. In one embodiment, an overetch into the semiconductor material layer 10 may be optionally performed after the top surface of the semiconductor material layer 10 is physically exposed at a bottom of each memory opening 49 and each support opening 19. The overetch may be performed prior to, or after, removal of the lithographic material stack. In other words, the recessed surfaces of the semiconductor material layer 10 may be vertically offset from the un-recessed top surfaces of

the semiconductor material layer 10 by a recess depth. The recess depth can be, for example, in a range from 1 nm to 50 nm, although lesser and greater recess depths can also be used. The overetch is optional, and may be omitted. If the overetch is not performed, the bottom surfaces of the memory openings 49 and the support openings 19 can be coplanar with the topmost surface of the semiconductor material layer 10.

[0131] Each of the memory openings 49 and the support openings 19 may include a sidewall (or a plurality of sidewalls) that extends substantially perpendicular to the topmost surface of the substrate. A two-dimensional array of memory openings 49 can be formed in the memory array region 100. A two-dimensional array of support openings 19 can be formed in the staircase region 300. The substrate semiconductor layer 9 and the semiconductor material layer 10 collectively constitutes a substrate (9, 10), which can be a semiconductor substrate. Alternatively, the semiconductor material layer 10 may be omitted, and the memory openings 49 and the support openings 19 can be extend to a top surface of the substrate semiconductor layer 9.

[0132] Referring to FIG. 5A, a memory opening 49 in the first exemplary structure of FIGS. 4A and 4B is illustrated. The memory opening 49 extends through the insulating cap layer 70, the alternating stack (32, 42, 332, 342, 70), and optionally into an upper portion of the semiconductor material layer 10. At this processing step, each support opening 19 can extend through the retro-stepped dielectric material portion 65, a subset of layers in the alternating stack (32, 42, 332, 342, 70), and optionally through the upper portion of the semiconductor material layer 10. The recess depth of the bottom surface of each memory opening with respect to the top surface of the semiconductor material layer 10 can be in a range from 0 nm to 30 nm, although greater recess depths can also be used. Optionally, the word-line-level sacrificial material layers 42 can be laterally recessed partially to form lateral

recesses (not shown), for example, by an isotropic etch.

[0133] Referring to FIG. 5B, an optional pedestal channel portion (e.g., an epitaxial pedestal) 11 can be formed at the bottom portion of each memory opening 49 and each support openings 19, for example, by selective epitaxy. Each pedestal channel portion 11 comprises a single crystalline semiconductor material in epitaxial alignment with the single crystalline semiconductor material of the semiconductor material layer 10. In one embodiment, the top surface of each pedestal channel portion 11 can be formed above a horizontal plane including the top surface of a bottommost word-line-level sacrificial material layer 42. In this case, a source select gate electrode can be subsequently formed by replacing the bottommost word-line-level sacrificial material layer 42 with a conductive material layer. The pedestal channel portion 11 can be a portion of a transistor channel that extends between a source region to be subsequently formed in the substrate (9, 10) and a drain region to be subsequently formed in an upper portion of the memory opening 49. A memory cavity 49' is present in the unfilled portion of the memory opening 49 above the pedestal channel portion 11. In one embodiment, the pedestal channel portion 11 can comprise single crystalline silicon. In one embodiment, the pedestal channel portion 11 can have a doping of the first conductivity type, which is the same as the conductivity type of the semiconductor material layer 10 that the pedestal channel portion contacts. If a semiconductor material layer 10 is not present, the pedestal channel portion 11 can be formed directly on the substrate semiconductor layer 9, which can have a doping of the first conductivity type.

[0134] Referring to FIG. 5C, a stack of layers including a blocking dielectric layer 52, a charge storage layer 54, a tunneling dielectric layer 56, and an optional first semiconductor channel layer 601 can be sequentially deposited in the memory openings 49.

[0135] The blocking dielectric layer 52 can include a single dielectric material layer or a

stack of a plurality of dielectric material layers. In one embodiment, the blocking dielectric layer can include a dielectric metal oxide layer consisting essentially of a dielectric metal oxide. As used herein, a dielectric metal oxide refers to a dielectric material that includes at least one metallic element and at least oxygen. The dielectric metal oxide may consist essentially of the at least one metallic element and oxygen, or may consist essentially of the at least one metallic element, oxygen, and at least one non-metallic element such as nitrogen. In one embodiment, the blocking dielectric layer 52 can include a dielectric metal oxide having a dielectric constant greater than 7.9, i.e., having a dielectric constant greater than the dielectric constant of silicon nitride.

[0136] Non-limiting examples of dielectric metal oxides include aluminum oxide (Al_2O_3), hafnium oxide (HfO_2), lanthanum oxide (La_2O_3), yttrium oxide (Y_2O_3), tantalum oxide (Ta_2O_5), silicates thereof, nitrogen-doped compounds thereof, alloys thereof, and stacks thereof. The dielectric metal oxide layer can be deposited, for example, by chemical vapor deposition (CVD), atomic layer deposition (ALD), pulsed laser deposition (PLD), liquid source misted chemical deposition, or a combination thereof. The thickness of the dielectric metal oxide layer can be in a range from 1 nm to 20 nm, although lesser and greater thicknesses can also be used. The dielectric metal oxide layer can subsequently function as a dielectric material portion that blocks leakage of stored electrical charges to control gate electrodes. In one embodiment, the blocking dielectric layer 52 includes aluminum oxide. In one embodiment, the blocking dielectric layer 52 can include multiple dielectric metal oxide layers having different material compositions.

[0137] Alternatively or additionally, the blocking dielectric layer 52 can include a dielectric semiconductor compound such as silicon oxide, silicon oxynitride, silicon nitride, or a combination thereof. In one embodiment, the blocking dielectric layer 52 can include

silicon oxide. In this case, the dielectric semiconductor compound of the blocking dielectric layer 52 can be formed by a conformal deposition method such as low pressure chemical vapor deposition, atomic layer deposition, or a combination thereof. The thickness of the dielectric semiconductor compound can be in a range from 1 nm to 20 nm, although lesser and greater thicknesses can also be used. Alternatively, the blocking dielectric layer 52 can be omitted, and a backside blocking dielectric layer can be formed after formation of backside recesses on surfaces of memory films to be subsequently formed.

[0138] Subsequently, the charge storage layer 54 can be formed. In one embodiment, the charge storage layer 54 can be a continuous layer or patterned discrete portions of a charge trapping material including a dielectric charge trapping material, which can be, for example, silicon nitride. Alternatively, the charge storage layer 54 can include a continuous layer or patterned discrete portions of a conductive material such as doped polysilicon or a metallic material that is patterned into multiple electrically isolated portions (e.g., floating gates), for example, by being formed within lateral recesses into word-line-level sacrificial material layers 42. In one embodiment, the charge storage layer 54 includes a silicon nitride layer. In one embodiment, the word-line-level sacrificial material layers 42 and the word-line-level insulating layers 32 can have vertically coincident sidewalls, and the charge storage layer 54 can be formed as a single continuous layer.

[0139] In another embodiment, the word-line-level sacrificial material layers 42 can be laterally recessed with respect to the sidewalls of the word-line-level insulating layers 32, and a combination of a deposition process and an anisotropic etch process can be used to form the charge storage layer 54 as a plurality of memory material portions that are vertically spaced apart. While the descriptions in the present disclosure refer to an embodiment in which the charge storage layer 54 is a single continuous layer, in other embodiments the charge storage

layer 54 is replaced with a plurality of memory material portions (which can be charge trapping material portions or electrically isolated conductive material portions) that are vertically spaced apart.

[0140] The charge storage layer 54 can be formed as a single charge storage layer of homogeneous composition, or can include a stack of multiple charge storage layers. The multiple charge storage layers, if used, can comprise a plurality of spaced-apart floating gate material layers that contain conductive materials (e.g., metal such as tungsten, molybdenum, tantalum, titanium, platinum, ruthenium, and alloys thereof, or a metal silicide such as tungsten silicide, molybdenum silicide, tantalum silicide, titanium silicide, nickel silicide, cobalt silicide, or a combination thereof) and/or semiconductor materials (e.g., polycrystalline or amorphous semiconductor material including at least one elemental semiconductor element or at least one compound semiconductor material). Alternatively or additionally, the charge storage layer 54 may comprise an insulating charge trapping material, such as one or more silicon nitride segments. Alternatively, the charge storage layer 54 may comprise conductive nanoparticles such as metal nanoparticles, which can be, for example, ruthenium nanoparticles. The charge storage layer 54 can be formed, for example, by chemical vapor deposition (CVD), atomic layer deposition (ALD), physical vapor deposition (PVD), or any suitable deposition technique for storing electrical charges therein. The thickness of the charge storage layer 54 can be in a range from 2 nm to 20 nm, although lesser and greater thicknesses can also be used.

[0141] The tunneling dielectric layer 56 includes a dielectric material through which charge tunneling can be performed under suitable electrical bias conditions. The charge tunneling may be performed through hot-carrier injection or by Fowler-Nordheim tunneling induced charge transfer depending on the mode of operation of the monolithic three-

dimensional NAND string memory device to be formed. The tunneling dielectric layer 56 can include silicon oxide, silicon nitride, silicon oxynitride, dielectric metal oxides (such as aluminum oxide and hafnium oxide), dielectric metal oxynitride, dielectric metal silicates, alloys thereof, and/or combinations thereof. In one embodiment, the tunneling dielectric layer 56 can include a stack of a first silicon oxide layer, a silicon oxynitride layer, and a second silicon oxide layer, which is commonly known as an ONO stack. In one embodiment, the tunneling dielectric layer 56 can include a silicon oxide layer that is substantially free of carbon or a silicon oxynitride layer that is substantially free of carbon. The thickness of the tunneling dielectric layer 56 can be in a range from 2 nm to 20 nm, although lesser and greater thicknesses can also be used.

[0142] The optional first semiconductor channel layer 601 includes a semiconductor material such as at least one elemental semiconductor material, at least one III-V compound semiconductor material, at least one II-VI compound semiconductor material, at least one organic semiconductor material, or other semiconductor materials known in the art. In one embodiment, the first semiconductor channel layer 601 includes amorphous silicon or polysilicon. The first semiconductor channel layer 601 can be formed by a conformal deposition method such as low pressure chemical vapor deposition (LPCVD). The thickness of the first semiconductor channel layer 601 can be in a range from 2 nm to 10 nm, although lesser and greater thicknesses can also be used. A memory cavity 49' is formed in the volume of each memory opening 49 that is not filled with the deposited material layers (52, 54, 56, 601).

[0143] Referring to FIG. 5D, the optional first semiconductor channel layer 601, the tunneling dielectric layer 56, the charge storage layer 54, and the blocking dielectric layer 52 are sequentially anisotropically etched using at least one anisotropic etch process. The

portions of the first semiconductor channel layer 601, the tunneling dielectric layer 56, the charge storage layer 54, and the blocking dielectric layer 52 located above the top surface of the insulating cap layer 70 can be removed by the at least one anisotropic etch process.

Further, the horizontal portions of the first semiconductor channel layer 601, the tunneling dielectric layer 56, the charge storage layer 54, and the blocking dielectric layer 52 at a bottom of each memory cavity 49' can be removed to form openings in remaining portions thereof. Each of the first semiconductor channel layer 601, the tunneling dielectric layer 56, the charge storage layer 54, and the blocking dielectric layer 52 can be etched by a respective anisotropic etch process using a respective etch chemistry, which may, or may not, be the same for the various material layers.

[0144] Each remaining portion of the first semiconductor channel layer 601 can have a tubular configuration. The charge storage layer 54 can comprise a charge trapping material or a floating gate material. In one embodiment, each charge storage layer 54 can include a vertical stack of charge storage regions that store electrical charges upon programming. In one embodiment, the charge storage layer 54 can be a charge storage layer in which each portion adjacent to the word-line-level sacrificial material layers 42 constitutes a charge storage region.

[0145] A surface of the pedestal channel portion 11 (or a surface of the semiconductor material layer 10 in case the pedestal channel portions 11 are not used) can be physically exposed underneath the opening through the first semiconductor channel layer 601, the tunneling dielectric layer 56, the charge storage layer 54, and the blocking dielectric layer 52. Optionally, the physically exposed semiconductor surface at the bottom of each memory cavity 49' can be vertically recessed so that the recessed semiconductor surface underneath the memory cavity 49' is vertically offset from the topmost surface of the pedestal channel

portion 11 (or of the semiconductor material layer 10 in case pedestal channel portions 11 are not used) by a recess distance. A tunneling dielectric layer 56 is located over the charge storage layer 54. A set of a blocking dielectric layer 52, a charge storage layer 54, and a tunneling dielectric layer 56 in a memory opening 49 constitutes a memory film 50, which includes a plurality of charge storage regions (comprising the charge storage layer 54) that are insulated from surrounding materials by the blocking dielectric layer 52 and the tunneling dielectric layer 56. In one embodiment, the first semiconductor channel layer 601, the tunneling dielectric layer 56, the charge storage layer 54, and the blocking dielectric layer 52 can have vertically coincident sidewalls.

[0146] Referring to FIGS. 5E and 6A, a second semiconductor channel layer 602 can be deposited directly on the semiconductor surface of the pedestal channel portion 11 or the semiconductor material layer 10 if the pedestal channel portion 11 is omitted, and directly on the first semiconductor channel layer 601. The second semiconductor channel layer 602 includes a semiconductor material such as at least one elemental semiconductor material, at least one III-V compound semiconductor material, at least one II-VI compound semiconductor material, at least one organic semiconductor material, or other semiconductor materials known in the art. In one embodiment, the second semiconductor channel layer 602 includes amorphous silicon or polysilicon. The second semiconductor channel layer 602 can be formed by a conformal deposition method such as low pressure chemical vapor deposition (LPCVD). The thickness of the second semiconductor channel layer 602 can be in a range from 2 nm to 10 nm, although lesser and greater thicknesses can also be used. The second semiconductor channel layer 602 may partially fill the memory cavity 49' in each memory opening, or may fully fill the cavity in each memory opening.

[0147] The materials of the first semiconductor channel layer 601 and the second

semiconductor channel layer 602 are collectively referred to as a semiconductor channel material. In other words, the semiconductor channel material is a set of all semiconductor material in the first semiconductor channel layer 601 and the second semiconductor channel layer 602. The first semiconductor channel layer 601 and the second semiconductor channel layer 602 are collectively referred to as a semiconductor channel material layer 60L.

[0148] Referring to FIG. 6B, a dielectric material such as silicon oxide can be deposited in the memory cavities 49', and can be vertically recessed to the level of the topmost insulating layer 32. Each remaining portion of the dielectric material constitutes a dielectric core 62. A memory cavity 49' having a reduced depth is present above each dielectric core 62.

[0149] Referring to FIG. 6C, a connection channel material layer 360L can be deposited in the memory cavities 49'. The connection channel material layer 360L includes a doped semiconductor material having a doping of the first conductivity type, i.e., the same conductivity type as the doping of the semiconductor channel material layer 60L.

[0150] Referring to FIG. 6D, the connection channel material layer 360L and the semiconductor channel material layer 60L are recessed such that top surfaces of remaining portions of the connection channel material layer 360L and the semiconductor channel material layer 60L are formed below the horizontal plane including the top surface of the topmost insulating layer 32. Each remaining portion of the semiconductor channel material layer 60L constitutes a vertical semiconductor channel 60, and each remaining portion of the connection channel material layer 360L constitutes a connection channel portion 360.

[0151] Referring to FIG. 6E, a series of isotropic etch processes can be performed to remove physically exposed portions of the memory film 50. Each combination of a memory film 50 and a vertical semiconductor channel 60 in a memory opening 49 constitutes a

memory stack structure 55.

[0152] Referring to FIG. 6F, an oxidation process can be performed to convert a top portion of each connection channel portion 360 into a semiconductor oxide plate 362, which may be a silicon oxide plate. Each set of material portions located in a memory opening 49 constitutes a lower memory opening fill structure. Each set of material portions located in a support opening 19 constitutes a lower support pillar structure.

[0153] Referring to FIGS. 7A, 7B, 8A, and 8B, a sacrificial material liner is conformally deposited and anisotropically etched to form a sacrificial spacer 312. The sacrificial spacers 312 can include a semiconductor material such as amorphous silicon or polysilicon. A sacrificial fill material such as silicon oxide can be deposited in each sacrificial spacer 312. Excess portions of the sacrificial fill material can be removed from above the horizontal plane including the top surface of the insulating cap layer 70. Each remaining portion of the sacrificial fill material constitutes a sacrificial pillar structure 314. A set of all material portions filling a memory opening 49 constitutes an in-process memory opening fill structure 58'. A set of all material portions filling a support opening 19 constitutes an in-process support pillar structure 20'.

[0154] Formation of the sacrificial pillar structures 314 is optional. In an alternative embodiment, formation of the sacrificial pillar structures 314 may be omitted by increasing the thickness of the sacrificial material liner such that the entire volume of each memory cavity 49' is filled with the material of the sacrificial material liner. In this case, the sacrificial spacers 312 can fill the entirety of each memory cavity 49'. A resulting structure is illustrated in FIGS. 7C and 7D. In case the sacrificial pillar structures 314 are omitted, a subsequent processing step for removing the sacrificial pillar structures can also be omitted.

[0155] Referring to FIGS. 9A and 9B, a sacrificial planarization stopper layer 373 can be

formed over the alternating stack (32, 42, 332, 342, 70) and over the in-process memory opening fill structures 58' and the in-process support pillar structures 20'. The sacrificial planarization stopper layer 373 includes a dielectric material that is different from the dielectric material of the word-line-level sacrificial material layers 42. For example, the sacrificial planarization stopper layer 373 can include silicon oxide. The sacrificial planarization stopper layer 373 can have a thickness in a range from 50 nm to 500 nm, although lesser and greater thicknesses can also be used.

[0156] A photoresist layer (not shown) can be applied over the sacrificial planarization stopper layer 373, and is lithographically patterned to form openings in areas between clusters of in-process memory opening fil structures 58'. The pattern in the photoresist layer can be transferred through the sacrificial planarization stopper layer 373, the alternating stack (32, 42, 332, 342, 70) and/or the retro-stepped dielectric material portion 65 using an anisotropic etch to form backside trenches 79, which vertically extend from the top surface of the sacrificial planarization stopper layer 373 at least to the top surface of the substrate (9, 10), and laterally extend through the memory array region 100 and the staircase region 300.

[0157] In one embodiment, the backside trenches 79 can laterally extend along a first horizontal direction hd1 and can be laterally spaced apart one from another along a second horizontal direction hd2 that is perpendicular to the first horizontal direction hd1. The in-process memory opening fil structures 58' can be arranged in rows that extend along the first horizontal direction hd1. Each backside trench 79 can have a uniform width that is invariant along the lengthwise direction (i.e., along the first horizontal direction hd1). In one embodiment, the backside trenches 79 can include a source contact opening in which a source contact via structure can be subsequently formed. The photoresist layer can be removed, for example, by ashing.

[0158] Referring to FIGS. 10 and 11A, an etchant that selectively etches the second material of the word-line-level sacrificial material layers 42 and the drain-select-level sacrificial material layers 342 with respect to the first material of the word-line-level insulating layers 32, the drain-select-level insulating layers 332, and the insulating cap layer 70 can be introduced into the backside trenches 79, for example, using an etch process. FIG. 11A illustrates a region of the first exemplary structure of FIG. 10. Word-line-level backside recesses 43 are formed in volumes from which the word-line-level sacrificial material layers 42 are removed. Drain-select-level backside recesses 343 are formed in volumes from which the drain-select-level sacrificial material layers 342 are removed. The removal of the second material of the sacrificial material layers (42, 342) can be selective to the first material of the insulating layers (32, 342, 70), the material of the retro-stepped dielectric material portion 65, the semiconductor material of the semiconductor material layer 10, and the material of the outermost layer of the memory films 50. In one embodiment, the sacrificial material layers (42, 342) can include silicon nitride, and the materials of the insulating layers (32, 342, 70) and the retro-stepped dielectric material portion 65 can be selected from silicon oxide and dielectric metal oxides.

[0159] The etch process that removes the second material selective to the first material and the outermost layer of the memory films 50 can be a wet etch process using a wet etch solution, or can be a gas phase (dry) etch process in which the etchant is introduced in a vapor phase into the backside trenches 79. For example, if the sacrificial material layers (42, 342) include silicon nitride, the etch process can be a wet etch process in which the first exemplary structure is immersed within a wet etch tank including phosphoric acid, which etches silicon nitride selective to silicon oxide, silicon, and various other materials used in the art. The in-process memory opening fill structures 58', the in-process support pillar structure

20', the retro-stepped dielectric material portion 65, and the memory stack structures 55 provide structural support while the backside recesses (43, 343) are present within volumes previously occupied by the sacrificial material layers (42, 342).

[0160] Each backside recess (43, 343) can be a laterally extending cavity having a lateral dimension that is greater than the vertical extent of the cavity. In other words, the lateral dimension of each backside recess (43, 343) can be greater than the height of the backside recess (43, 343). A plurality of backside recesses (43, 343) can be formed in the volumes from which the second material of the sacrificial material layers (42, 342) is removed. The memory openings in which the memory stack structures 55 are formed are herein referred to as front side openings or front side cavities in contrast with the backside recesses (43, 343). In one embodiment, the memory array region 100 comprises an array of monolithic three-dimensional NAND strings having a plurality of device levels disposed above the substrate (9, 10). In this case, each backside recess (43, 343) can define a space for receiving a respective word line of the array of monolithic three-dimensional NAND strings.

[0161] Each of the plurality of backside recesses (43, 343) can extend substantially parallel to the top surface of the substrate (9, 10). A backside recess (43, 343) can be vertically bounded by a top surface of an underlying insulating layer (32, 342) and a bottom surface of an overlying insulating layer (32, 342, 70). In one embodiment, each backside recess (43, 343) can have a uniform height throughout.

[0162] Physically exposed surface portions of the optional pedestal channel portions 11 and the semiconductor material layer 10 can be converted into dielectric material portions by thermal conversion and/or plasma conversion of the semiconductor materials into dielectric materials. For example, thermal conversion and/or plasma conversion can be used to convert a surface portion of each pedestal channel portion 11 into a tubular dielectric spacer 116, and

to convert each physically exposed surface portion of the semiconductor material layer 10 into a planar dielectric portion 616. In one embodiment, each tubular dielectric spacer 116 can be topologically homeomorphic to a torus, i.e., generally ring-shaped. As used herein, an element is topologically homeomorphic to a torus if the shape of the element can be continuously stretched without destroying a hole or forming a new hole into the shape of a torus. The tubular dielectric spacers 116 include a dielectric material that includes the same semiconductor element as the pedestal channel portions 11 and additionally includes at least one non-metallic element such as oxygen and/or nitrogen such that the material of the tubular dielectric spacers 116 is a dielectric material. In one embodiment, the tubular dielectric spacers 116 can include a dielectric oxide, a dielectric nitride, or a dielectric oxynitride of the semiconductor material of the pedestal channel portions 11. Likewise, each planar dielectric portion 616 includes a dielectric material that includes the same semiconductor element as the semiconductor material layer and additionally includes at least one non-metallic element such as oxygen and/or nitrogen such that the material of the planar dielectric portions 616 is a dielectric material. In one embodiment, the planar dielectric portions 616 can include a dielectric oxide, a dielectric nitride, or a dielectric oxynitride of the semiconductor material of the semiconductor material layer 10.

[0163] Referring to FIG. 11B, a backside blocking dielectric layer 44 can be optionally formed. The backside blocking dielectric layer 44, if present, comprises a dielectric material that functions as a control gate dielectric for the control gates to be subsequently formed in the backside recesses (43, 343). In case the blocking dielectric layer 52 is present within each memory opening, the backside blocking dielectric layer 44 is optional. In case the blocking dielectric layer 52 is omitted, the backside blocking dielectric layer 44 is present.

[0164] The backside blocking dielectric layer 44 can be formed in the backside recesses

(43, 343) and on a sidewall of the backside trench 79. The backside blocking dielectric layer 44 can be formed directly on horizontal surfaces of the insulating layers (32, 342, 70) and sidewalls of the memory stack structures 55 within the backside recesses (43, 343). If the backside blocking dielectric layer 44 is formed, formation of the tubular dielectric spacers 116 and the planar dielectric portion 616 prior to formation of the backside blocking dielectric layer 44 is optional. In one embodiment, the backside blocking dielectric layer 44 can be formed by a conformal deposition process such as atomic layer deposition (ALD). The backside blocking dielectric layer 44 can consist essentially of aluminum oxide. The thickness of the backside blocking dielectric layer 44 can be in a range from 1 nm to 15 nm, such as 2 to 6 nm, although lesser and greater thicknesses can also be used.

[0165] The dielectric material of the backside blocking dielectric layer 44 can be a dielectric metal oxide such as aluminum oxide, a dielectric oxide of at least one transition metal element, a dielectric oxide of at least one Lanthanide element, a dielectric oxide of a combination of aluminum, at least one transition metal element, and/or at least one Lanthanide element. Alternatively or additionally, the backside blocking dielectric layer 44 can include a silicon oxide layer. The backside blocking dielectric layer 44 can be deposited by a conformal deposition method such as chemical vapor deposition or atomic layer deposition. The backside blocking dielectric layer 44 is formed on the sidewalls of the backside trenches 79, horizontal surfaces and sidewalls of the insulating layers (32, 342, 70), the portions of the sidewall surfaces of the memory stack structures 55 that are physically exposed to the backside recesses (43, 343), and a top surface of the planar dielectric portion 616. A backside cavity 79' is present within the portion of each backside trench 79 that is not filled with the backside blocking dielectric layer 44.

[0166] Referring to FIG. 11C, a metallic barrier layer 46A can be deposited in the

backside recesses (43, 343). The metallic barrier layer 46A includes an electrically conductive metallic material that can function as a diffusion barrier layer and/or adhesion promotion layer for a metallic fill material to be subsequently deposited. The metallic barrier layer 46A can include a conductive metallic nitride material such as TiN, TaN, WN, or a stack thereof, or can include a conductive metallic carbide material such as TiC, TaC, WC, or a stack thereof. In one embodiment, the metallic barrier layer 46A can be deposited by a conformal deposition process such as chemical vapor deposition (CVD) or atomic layer deposition (ALD). The thickness of the metallic barrier layer 46A can be in a range from 2 nm to 8 nm, such as from 3 nm to 6 nm, although lesser and greater thicknesses can also be used. In one embodiment, the metallic barrier layer 46A can consist essentially of a conductive metal nitride such as TiN.

[0167] Referring to FIGS. 11D and 12, a metal fill material is deposited in the plurality of backside recesses (43, 343), on the sidewalls of the at least one the backside trench 79, and over the top surface of the sacrificial planarization stopper layer 373 to form a metallic fill material layer 46B. The metallic fill material can be deposited by a conformal deposition method, which can be, for example, chemical vapor deposition (CVD), atomic layer deposition (ALD), electroless plating, electroplating, or a combination thereof. In one embodiment, the metallic fill material layer 46B can consist essentially of at least one elemental metal. The at least one elemental metal of the metallic fill material layer 46B can be selected, for example, from tungsten, cobalt, ruthenium, titanium, and tantalum. In one embodiment, the metallic fill material layer 46B can consist essentially of a single elemental metal. In one embodiment, the metallic fill material layer 46B can be deposited using a fluorine-containing precursor gas such as WF₆. In one embodiment, the metallic fill material layer 46B can be a tungsten layer including a residual level of fluorine atoms as impurities.

The metallic fill material layer 46B is spaced from the insulating layers (32, 342, 70) and the memory stack structures 55 by the metallic barrier layer 46A, which is a metallic barrier layer that blocks diffusion of fluorine atoms therethrough.

[0168] A plurality of electrically conductive layers (46, 346) can be formed in the plurality of backside recesses (43, 343), and a continuous electrically conductive material layer 46L can be formed on the sidewalls of each backside trench 79 and over the sacrificial planarization stopper layer 373. Each electrically conductive layer (46, 346) includes a portion of the metallic barrier layer 46A and a portion of the metallic fill material layer 46B that are located between a vertically neighboring pair of dielectric material layers such as a pair of insulating layers (32, 342, 70). The continuous electrically conductive material layer 46L includes a continuous portion of the metallic barrier layer 46A and a continuous portion of the metallic fill material layer 46B that are located in the backside trenches 79 or above the sacrificial planarization stopper layer 373.

[0169] Each sacrificial material layer (42, 342) can be replaced with an electrically conductive layer (46, 346). A backside cavity 79' is present in the portion of each backside trench 79 that is not filled with the backside blocking dielectric layer 44 and the continuous electrically conductive material layer 46L. A tubular dielectric spacer 116 laterally surrounds a pedestal channel portion 11. A bottommost electrically conductive layer (such as a bottommost one of the word-line-level electrically conductive layer 46) laterally surrounds each tubular dielectric spacer 116 upon formation of the electrically conductive layers (46, 346).

[0170] Referring to FIG. 13, the deposited metallic material of the continuous electrically conductive material layer 46L is etched back from the sidewalls of each backside trench 79 and from above the sacrificial planarization stopper layer 373, for example, by an isotropic

wet etch, an anisotropic dry etch, or a combination thereof. Each remaining portion of the deposited metallic material in the backside recesses (43, 343) constitutes an electrically conductive layer (46, 346). The electrically conductive layers (46, 346) include word-line-level electrically conductive layers 46 that are formed in the volumes of the word-line-level backside recesses 43 and drain-select-level electrically conductive layers 346 that are formed in the volumes of the drain-select-level backside recesses 343. Each electrically conductive layer (46, 346) can be a conductive line structure. Thus, the sacrificial material layers (42, 342) are replaced with the electrically conductive layers (46, 346).

[0171] Each electrically conductive layer (46, 346) can function as a combination of a plurality of control gate electrodes located at a same level and a word line electrically interconnecting, i.e., electrically connecting, the plurality of control gate electrodes located at the same level. The plurality of control gate electrodes within each electrically conductive layer (46, 346) are the control gate electrodes for the vertical memory devices including the memory stack structures 55. In other words, each electrically conductive layer (46, 346) can be a word line that functions as a common control gate electrode for the plurality of vertical memory devices.

[0172] In one embodiment, the removal of the continuous electrically conductive material layer 46L can be selective to the material of the backside blocking dielectric layer 44. In this case, a horizontal portion of the backside blocking dielectric layer 44 can be present at the bottom of each backside trench 79. In another embodiment, the removal of the continuous electrically conductive material layer 46L may not be selective to the material of the backside blocking dielectric layer 44 or, the backside blocking dielectric layer 44 may not be used. The planar dielectric portions 616 can be removed during removal of the continuous electrically conductive material layer 46L. A backside cavity 79' is present within each

backside trench 79.

[0173] Referring to FIGS. 14A and 14B, an insulating material liner can be formed in the backside trenches 79 and over the sacrificial planarization stopper layer 373 by a conformal deposition process. Exemplary conformal deposition processes include, but are not limited to, chemical vapor deposition and atomic layer deposition. The insulating material liner includes an insulating material such as silicon oxide, silicon nitride, a dielectric metal oxide, an organosilicate glass, or a combination thereof. In one embodiment, the insulating material liner can include silicon oxide. The insulating material liner can be formed, for example, by low pressure chemical vapor deposition (LPCVD) or atomic layer deposition (ALD). The thickness of the insulating material liner can be in a range from 1.5 nm to 60 nm, although lesser and greater thicknesses can also be used.

[0174] If a backside blocking dielectric layer 44 is present, the insulating material liner can be formed directly on surfaces of the backside blocking dielectric layer 44 and directly on the sidewalls of the electrically conductive layers (46, 346). If a backside blocking dielectric layer 44 is not used, the insulating material liner can be formed directly on sidewalls of the insulating layers (32, 342, 70) and directly on sidewalls of the electrically conductive layers (46, 346).

[0175] An anisotropic etch is performed to remove horizontal portions of the insulating material liner from above the sacrificial planarization stopper layer 373 and at the bottom of each backside trench 79. Each remaining portion of the insulating material liner constitutes an insulating spacer 74. A backside cavity 79' is present within a volume surrounded by each insulating spacer 74. A top surface of the semiconductor material layer 10 can be physically exposed at the bottom of each backside trench 79.

[0176] A source region 61 can be formed at a surface portion of the semiconductor

material layer 10 under each backside cavity 79' by implantation of electrical dopants into physically exposed surface portions of the semiconductor material layer 10. Each source region 61 is formed in a surface portion of the substrate (9, 10) that underlies a respective opening through the insulating spacer 74. Due to the straggle of the implanted dopant atoms during the implantation process and lateral diffusion of the implanted dopant atoms during a subsequent activation anneal process, each source region 61 can have a lateral extent greater than the lateral extent of the opening through the insulating spacer 74.

[0177] An upper portion of the semiconductor material layer 10 that extends between the source region 61 and the plurality of pedestal channel portions 11 constitutes a horizontal semiconductor channel 59 for a plurality of field effect transistors. The horizontal semiconductor channel 59 is connected to multiple vertical semiconductor channels 60 through respective pedestal channel portions 11. The horizontal semiconductor channel 59 contacts the source region 61 and the plurality of pedestal channel portions 11. A bottommost electrically conductive layer (such as a bottommost one of the word-line-level electrically conductive layer 46) provided upon formation of the electrically conductive layers (46, 346) within the alternating stack (32, 46) can comprise a source-side select gate electrode for the field effect transistors. Each source region 61 is formed in an upper portion of the substrate (9, 10). Semiconductor channels (59, 11, 60) extend between each source region 61 and a respective set of drain regions 63. The semiconductor channels (59, 11, 60) include the vertical semiconductor channels 60 of the memory stack structures 55.

[0178] A backside contact via structure 76 can be formed within each backside cavity 79'. Each contact via structure 76 can fill a respective backside cavity 79'. The contact via structures 76 can be formed by depositing at least one conductive material in the remaining unfilled volume (i.e., the backside cavity 79') of the backside trench 79. For example, the at

least one conductive material can include a conductive liner 76A and a conductive fill material portion 76B. The conductive liner 76A can include a conductive metallic liner such as TiN, TaN, WN, TiC, TaC, WC, an alloy thereof, or a stack thereof. The thickness of the conductive liner 76A can be in a range from 3 nm to 30 nm, although lesser and greater thicknesses can also be used. The conductive fill material portion 76B can include a metal or a metallic alloy. For example, the conductive fill material portion 76B can include W, Cu, Al, Co, Ru, Ni, an alloy thereof, or a stack thereof.

[0179] The at least one conductive material can be planarized using the sacrificial planarization stopper layer 373 overlying the alternating stack (32, 46) as a stopping layer. If chemical mechanical planarization (CMP) process is used, the sacrificial planarization stopper layer 373 can be used as a CMP stopping layer. Each remaining continuous portion of the at least one conductive material in the backside trenches 79 constitutes a backside contact via structure 76.

[0180] The backside contact via structure 76 extends through the alternating stack (32, 46), and contacts a top surface of the source region 61. If a backside blocking dielectric layer 44 is used, the backside contact via structure 76 can contact a sidewall of the backside blocking dielectric layer 44.

[0181] Referring to FIGS. 15, 16A, and 16B, the sacrificial planarization stopper layer 373 and an upper portion of each insulating spacer 73 can be removed from above the horizontal plane including the top surface of the insulating cap layer 70, for example, by a recess etch process, which may use an isotropic etch process or an anisotropic etch process. The backside contact via structures 76 may be vertically recessed so that the top surfaces of backside contact via structures 76 are at about the level of the top surface of the insulating cap layer 70.

[0182] Referring to FIGS. 17A, 17B, and 18A – 18C, a patterned etch mask layer 307 can be formed over the insulating cap layer 70 and the retro-stepped dielectric material portion 65. The patterned etch mask layer 307 can be a lithographically patterned photoresist layer. The patterned etch mask layer 307 can include elongated openings (such as rectangular openings) that laterally extend along the first horizontal direction hd1. Each elongated opening in the patterned etch mask layer 307 partially overlies a neighboring pair of rows of in-process memory opening fill structures 58'.

[0183] Referring to FIGS. 19A – 19C, an anisotropic etch process that etches the material of the 312 selective to the materials of the insulating cap layer 70 and the sacrificial pillar structures 314 can be performed. Unmasked portions of the sacrificial spacer 312 can be etched underneath each elongated opening in the patterned etch mask layer 307 to form discrete corner cavities 313. The discrete corner cavities 313 can have a semi-tubular shape. Sidewalls of the drain-select-level electrically conductive layers 346 are physically exposed on an outer sidewall of each discrete corner cavity 313.

[0184] Referring to FIGS. 20A – 20C, an isotropic etchant that etches the material(s) of the drain-select-level electrically conductive layers 346 selective to the materials of the insulating cap layer 70, the drain-select-level insulating layers 332, and the sacrificial pillar structures 314 can be introduced into the discrete corner cavities 313. Physically exposed sidewalls of the drain-select-level electrically conductive layers 346 can be laterally recessed in an isotropic etch process using the isotropic etchant. A laterally-extending cavity 315 that laterally extend along the first horizontal direction hd1 can be formed at each level of the drain-select-level electrically conductive layers 346 within each area of the elongated opening in the patterned etch mask layer 307. Each drain-select-level electrically conductive layer 346 can be divided into multiple strips with a cut at the location of each elongated

opening in the patterned etch mask layer 307. The patterned etch mask layer 307 can be removed after, or prior to, the isotropic etch process.

[0185] Referring to FIGS. 21A – 21C, remaining portions of each in-process upper memory stack structure overlying a semiconductor oxide plate 362 can be removed selective to the insulating cap layer 70, the drain-select-level insulating layers 332, and the drain-select-level electrically conductive layers 346. In one embodiment, the sacrificial spacers 312 can include polysilicon and the sacrificial pillar structures 314 can include borosilicate glass, and the insulating cap layer 70 and the drain-select-level insulating layers 332 can include undoped silicate glass. A pillar-shaped cavity 317 can be formed above each physically exposed semiconductor oxide plate 362. Each pillar-shaped cavity 317 is connected to at least one laterally-extending cavity 315. An integrated cavity (315, 317) including the volumes of at least one laterally-extending cavity 315 and two rows of pillar-shaped cavities 317 can be formed between each neighboring pair of strips of the drain-select-level electrically conductive layers 46.

[0186] Referring to FIGS. 22A – 22C, a dielectric liner 320L is deposited in the integrated cavities (315, 317) to fill each volume of the laterally-extending cavities 315. The thickness of the dielectric liner 320L is selected such that the laterally-extending cavities 315 are filled with the dielectric liner 320L and a void 317' is present in an upper region of each memory opening 49. The dielectric liner 320L can include silicon oxide.

[0187] Referring to FIGS. 23A – 23C, an isotropic etch process can be performed to remove portions of the dielectric liner 320L from inside the memory openings 49 and the support openings 19. Each remaining portion of the dielectric liner 320L filling a respective one of the laterally-extending cavities 315 constitutes a dielectric isolation structure 320. Each dielectric isolation structure 320 includes a pair of lengthwise sidewalls that laterally

extend along the first horizontal direction hd1. Each lengthwise sidewall includes a laterally alternating sequence of vertical straight segments and vertical concave segments. A pillar-shaped cavity 317' is formed in an upper portion of each memory opening 49 and each support opening 19.

[0188] Referring to FIGS. 24A – 24C, a conductive material such as doped polysilicon can be conformally deposited in the pillar-shaped cavities 317' and over the insulating cap layer 70. The conductive material is anisotropically etched to form tubular conductive material portions, which constitute tubular gate electrodes 330. A void 317' is present inside each tubular gate electrode 330.

[0189] Referring to FIG. 25A, a drain-select-level gate dielectric layer 150 can be formed over the tubular gate electrodes 330. The drain-select-level gate dielectric layer 150 can include a layer stack of a first gate dielectric layer 152, a second gate dielectric layer 154, and a third gate dielectric layer 156. For example, the first gate dielectric layer 152 can include silicon oxide, the second gate dielectric layer 154 can include silicon nitride, and the third gate dielectric layer 156 can include silicon oxide.

[0190] Referring to FIG. 25B, a first drain-select-level channel layer 161 including a doped semiconductor material having a doping of the first conductivity type can be conformally deposited. The first drain-select-level channel layer 161 can include doped polysilicon.

[0191] Referring to FIG. 25C, an anisotropic etch process is performed to remove horizontal portions of the first drain-select-level channel layer 161 and the drain-select-level gate dielectric layer 150, and a center portion of each semiconductor oxide plate 362 that is not covered by vertically-extending portions of the drain-select-level gate dielectric layer 150, the first drain-select-level channel layer 161, and the tubular gate electrodes 330. An

opening extending to a top surface of a connection channel portion 360 is formed through each semiconductor oxide plate 362.

[0192] Referring to FIGS. 26A and 26B, a second drain-select-level channel layer is deposited conformally on each connection channel portion 360 and each remaining portion of the first drain-select-level channel layer, and fills the openings through the semiconductor oxide plates 362. A dielectric material such as borosilicate glass or phosphosilicate glass can be deposited in remaining voids in the memory openings 49 and the support openings 19. Excess portions of the dielectric material and the second drain-select-level channel layer can be removed from above the horizontal plane including the top surface of the insulating cap layer 70 by a planarization process such as a recess etch process and/or chemical mechanical planarization process. Each contiguous combination of remaining portions of the first drain-select-level channel layer 161 and the second drain-select-level channel layer constitutes a drain-select-level channel 160. Each remaining portion of the dielectric material constitutes a drain-select-level dielectric core 162.

[0193] Referring to FIGS. 27A, 27B, 28A, and 28B, an upper end portion of each tubular gate electrode 330 can be vertically recessed selective to the insulating cap layer 70 and the drain-select-level dielectric cores 162 by a recess etch. A dielectric material such as silicon nitride or undoped silicate glass can be deposited in the recessed volumes to form annular dielectric caps 340. An upper portion of each drain-select-level dielectric core 162 can be vertically recessed to form cylindrical recesses. A doped semiconductor material having a doping of a second conductivity type is deposited in the cylindrical recesses to form drain regions 63. The second conductivity type is the opposite of the first conductivity type. For example, if the first conductivity type is p-type, the second conductivity type is n-type, and vice versa.

[0194] The set of all material portions within each memory opening 49 after formation of the drain region 63 is herein referred to as a memory opening fill structure 58. The set of all material portions within each support opening 19 after formation of drain regions is herein referred to as a support pillar structure. A first subset of the memory opening fill structures 58 can be arranged in rows that laterally extend along the first horizontal direction, and contacts the dielectric isolation structures 320. Each dielectric isolation structure 320 contacts a pair of rows of memory stack structures 58.

[0195] At least two rows (such as three rows, four rows, etc.) of memory opening fill structures 58 can be provided between a laterally neighboring pair of dielectric isolation structures 320. More than two rows of memory opening fill structures 58 can be provided between each laterally neighboring pair of dielectric isolation structures 320.

[0196] FIG. 29 illustrates an alternative layout for the dielectric isolation structures 320 for an alternative configuration in which each strip of drain-select-level electrically conductive layers 346 that are laterally spaced apart by the dielectric isolation structures 320 contacts, and controls, two rows of memory stack structures 58.

[0197] Referring to FIGS. 30A and 30B, a contact level dielectric layer 73 can be formed over the insulating cap layer 70 and the retro-stepped dielectric material portion 65. Contact via structures (88, 86, 8P) can be formed through the contact level dielectric layer 73, and optionally through the retro-stepped dielectric material portion 65. For example, drain contact via structures 88 can be formed through the contact level dielectric layer 73 on each drain region 63. Word line contact via structures 86 can be formed on the electrically conductive layers (46, 346) through the contact level dielectric layer 73, and through the retro-stepped dielectric material portion 65. Peripheral device contact via structures 8P can be formed through the retro-stepped dielectric material portion 65 directly on respective

nodes of the peripheral devices.

[0198] Referring to FIG. 31, a region of a second exemplary structure is illustrated, which can be the same as the first exemplary structure at the processing steps of FIG. 6B. A memory opening 49 of the second exemplary structure is illustrated after formation of a dielectric core 62 therein. A memory cavity 49' is present over the dielectric core 62. Each vertical semiconductor channel 60 can vertically extend thorough the layers of the alternating stack (32, 42, 332, 342, 70), and can contact a respective sidewall of the insulating cap layer 70. A combination of a memory film 50 and a vertical semiconductor channel 60 within each memory opening 49 constitutes a memory stack structure 55 configured to store electrical charges within a vertical stack of memory elements therein. The vertical stack of memory elements can include portions of the charge storage layers located at each level of the sacrificial material layers (42, 342). A memory cavity 49' is present within an upper portion of each memory opening 49.

[0199] Referring to FIGS. 32A and 32B, a continuous dielectric liner 412L including a dielectric material such as a doped silicate glass is deposited at peripheral regions of each memory cavity 49' in the memory openings 49. The doped silicate glass can include a dielectric material having a greater etch rate in hydrofluoric acid than undoped silicate glass. For example, the doped silicate glass can include borosilicate glass or phosphosilicate glass.

[0200] Referring to FIGS. 33A and 33B, a semiconductor fill material is deposited within each unfilled volume in the memory openings 49 and in the support openings 19. The semiconductor fill material includes a material that can be removed selective to the materials of the insulating cap layer 70 and the continuous dielectric liner 412L. For example, the semiconductor fill material can include amorphous silicon or polysilicon. Portions of the semiconductor fill material and the continuous dielectric liner 412L located above the

horizontal plane including the top surface of the insulating cap layer 70 can be removed by a planarization process. Each remaining portion of the semiconductor fill material is herein referred to as a semiconductor fill material portion 414. Each remaining portion of the continuous dielectric liner 412L in the memory openings 49 and the support openings 19 constitutes a dielectric liner 412. Each dielectric liner 412 includes a tubular portion and bottom cap portion adjoined to the tubular portion. A vertical stack of a dielectric core 62 and a semiconductor fill material portion 414 is formed within each volume that is laterally surrounded by a respective one of the memory stack structures 55. A set of all material portions located within a memory opening 49 is herein referred to as an in-process memory opening fill structure 158. A set of all material portions located within a support opening 49 is herein referred to as an in-process support pillar structure.

[0201] Referring to FIGS. 34A and 34B, the processing steps of FIGS. 9A and 9B, 10, 11A – 11D, 12, 13, 14A and 14B, and 15 can be sequentially performed to form a sacrificial planarization stopper layer 373, backside trenches 79, backside recesses (43, 343), electrically conductive layers (46, 346), source regions 61, horizontal semiconductor channels 59, insulating spacers 74, and backside contact structures 76, and to remove the sacrificial planarization stopper layer 373.

[0202] Referring to FIGS. 35A, 35B, 36A, and 36B, a patterned etch mask layer 307 can be formed over the insulating cap layer 70, the retro-stepped dielectric material portion 65, the in-process memory opening fill structures 158, and the in-process support pillar structures 120. The patterned etch mask layer 307 can be a lithographically patterned photoresist layer. The patterned etch mask layer 307 can include elongated openings (such as rectangular openings) that laterally extend along the first horizontal direction hd1. Each elongated opening in the patterned etch mask layer 307 partially overlies a neighboring pair of rows of

in-process memory opening fill structures 158. In one embodiment, each elongated opening in the patterned etch mask layer 307 can include a pair of straight edges. Each of the straight edges of an elongated opening can overlie two neighboring rows of memory openings 49 that are filled in-process memory opening fill structures 158.

[0203] Referring to FIGS. 37A and 37B, an anisotropic etch process is performed to remove unmasked portions of the dielectric liners 412 within the areas of the elongated openings in the patterned etch mask layer 307. The anisotropic etch process can be selective to the materials of the insulating cap layer 70 and the semiconductor fill material portions 414. In one embodiment, the dielectric liners 412 can include a doped silicate glass such as borosilicate glass or organosilicate glass, or amorphous carbon, the insulating cap layer 70 can include undoped silicate glass, and the semiconductor fill material portions 414 can include amorphous silicon or polysilicon. Discrete corner cavities 413 are formed in volumes from which portions of the dielectric liners 412 are removed. A peripheral portion of a top surface of an underlying dielectric core 62 can be physically exposed at the bottom of each discrete corner cavity 413.

[0204] Referring to FIGS. 38A and 38B, portions of the vertical semiconductor channels 60 that underlie the elongated openings in the patterned etch mask layer 307 are etched by an isotropic etch process around the discrete corner cavities 413. The discrete corner cavities 413 are expanded to incorporate the volumes from which the vertical semiconductor channels 60 are removed. Portions of the memory films 50 adjacent to the discrete corner cavities 413 can be removed, for example, using a sequence of isotropic etch processes. In one embodiment, the sequence of isotropic etch processes can include a sequence of wet etch processes that etch the materials of the tunneling dielectric layer 56, the charge storage layer 54, and the blocking dielectric layer 52. The volumes of the discrete corner cavities 413 are

expanded upon removal of the physically exposed portions of the memory films 50. Thus, the discrete corner cavities 413 are formed by removing an upper corner portion of each memory stack structure 55 within the memory openings 49 using at least one etch process. A subset of the discrete corner cavities 413 is formed within the two neighboring rows of memory openings 49 underneath each elongated opening in the patterned etch mask layer 307. The patterned etch mask layer 307 can be removed, for example, by ashing.

[0205] Referring to FIGS. 39A – 39C, an isotropic etch process that uses an isotropic etchant that etches a material of the electrically conductive layers (46, 346) selective to a material of the insulating layers (32, 332, 70) is performed to laterally recess the portions of the electrically conductive layers (46, 346) from the discrete corner cavities 413. The isotropic etchant etches the material(s) of the drain-select-level electrically conductive layers 346 selective to the materials of the insulating cap layer 70, the insulating layers (32, 332), the memory films 50, the dielectric cores 62, and the semiconductor fill material portions 414 can be introduced into the discrete corner cavities 413. Physically exposed sidewalls of the drain-select-level electrically conductive layers 346 can be laterally recessed in an isotropic etch process using the isotropic etchant.

[0206] At least one laterally-extending cavity 415 is formed by laterally recessing portions of the at least one drain-select-level electrically conductive layer 346 from the discrete corner cavities 413. If multiple drain-select-level electrically conductive layers 346 are present, a plurality of laterally-extending cavities 415 can be formed by laterally recessing portions of the drain-select-level electrically conductive layers 346 from the discrete corner cavities 413. The lateral recess distance of the isotropic etch process is greater than one half of the minimum separation distance between the memory openings 49.

[0207] A laterally-extending cavity 415 that laterally extends along the first horizontal

direction hd1 can be formed at each level of the drain-select-level electrically conductive layers 346 within each area of the elongated opening in the patterned etch mask layer 307. At least one laterally-extending cavity 415 laterally connects two neighboring rows of memory openings 49. In one embodiment, a vertical stack of a plurality of laterally-extending cavities 415 laterally connects two neighboring rows of memory openings 49. Each of the at least one laterally-extending cavity 415 connects the discrete corner cavities 413 within the two rows of memory openings 49 to provide a continuous cavity.

[0208] The continuous cavity is herein referred to as an integrated cavity (413, 415), and includes all volumes of the discrete corner cavities 413 in the two rows of memory openings 49 and the at least one laterally-extending cavity 415. Each drain-select-level electrically conductive layer 346 can be divided into multiple strips with a cut at the location of each elongated opening in the patterned etch mask layer 307. The patterned etch mask layer 307 can be removed after, or prior to, the isotropic etch process.

[0209] Referring to FIGS. 40A – 40C, remaining portions of the semiconductor fill material portions 414 can be removed selective to the drain-select-level electrically conductive layers 346, the insulating layers (32, 332, 70), dielectric cores 62, and the dielectric liners 412. For example, if the semiconductor fill material portions 414 include a semiconductor material (such as amorphous silicon or polysilicon), the semiconductor fill material portions 414 can be removed using a wet etch process using hot trimethyl-2 hydroxyethyl ammonium hydroxide (“hot TMY”) or tetramethyl ammonium hydroxide (TMAH).

[0210] Referring to FIGS. 41A – 41C, a dielectric material such as a doped silicate glass (such as borosilicate glass or phosphosilicate glass) or organosilicate glass can be deposited in the volumes of the integrated cavities (413, 415) using a conformal deposition process.

Excess portions of the dielectric material can be removed from above the horizontal plane including the top surface of the insulating cap layer 70. Each continuous remaining portion of the dielectric material filling a respective integrated cavity (413, 415) constitutes a multi-pillared dielectric isolation structure 416. Each multi-pillared dielectric isolation structure 416 is formed by depositing a dielectric material in volumes of the at least one laterally-extending cavity 415 and in the discrete corner cavities 413.

[0211] Each multi-pillared dielectric isolation structure 416 includes a plurality of dielectric pillar portions 417 that fills a volume of a respective one of the discrete corner cavities 413 and at least one horizontally-extending portion adjoining each of the plurality of dielectric pillar portions 417, filling a volume of a respective one of the at least one laterally-extending cavity 415, located between a vertically neighboring pair of insulating layers (such as a vertically neighboring pair of drain-select-level insulating layers 332, a drain-select-level insulating layer 332 and an insulating cap layer 70, or a drain-select-level insulating layer 332 and a topmost word-line-level insulating layer 32) within the alternating stack (32, 46, 332, 346, 70), and laterally separating remaining portions of at least one electrically conductive layer (such as the at least one drain-select-level electrically conductive layer 346) within the alternating stack (32, 46, 332, 346, 70).

[0212] The multi-pillared dielectric isolation structures 416 fill volumes formed by removal of the semiconductor fill material portions 414. In one embodiment, each multi-pillared dielectric isolation structure 416 can include a plurality of horizontally-extending portions that laterally extend along the first horizontal direction hd1 and contact a top surface of an underlying one of the insulating layers (332 or 32) within the alternating stack (32, 332, 70), and contact a bottom surface of an overlying one of the insulating layers (332 or 70) within the alternating stack (32, 332, 70).

[0213] In one embodiment, each of the memory openings 49 with the two rows of memory openings 49 includes one of the plurality of dielectric pillar portions 417 and one of the memory stack structures 58. In one embodiment, each of the plurality of dielectric pillar portions 417 comprises: a cylindrical dielectric pillar portion 417C centered at a vertical axis passing through a geometrical center of a respective one of the memory openings 49 and azimuthally extending around the vertical axis by 360 degrees; and a block arc pillar portion 417B centered at the vertical axis, adjoined to one side of the cylindrical dielectric pillar portion 417C, and azimuthally extends around the vertical axis by an angle in a range from 30 degrees to 270 degrees.

[0214] Referring to FIGS. 42A – 42C, upper portions of the multi-pillared dielectric isolation structures 416 located in the memory openings 49 can be vertically recessed to form drain cavities. A doped semiconductor material having a doping of the second conductivity type is deposited in the drain cavities to form drain regions 63. Each drain region 63 can include a cylindrical drain segment 63C having a cylindrical shape and a block arc drain segment 63B that vertically extends with a uniform horizontal cross-sectional shape of a block arc, i.e., a shape of a segment of an annulus with a limited range of the azimuthal angle.

[0215] The set of all material portions within each memory opening 49 after formation of the drain region 63 is herein referred to as a memory opening fill structure 58. The set of all material portions within each support opening 19 after formation of drain regions is herein referred to as a support pillar structure. A first subset of the memory opening fill structures 58 can be arranged in rows that laterally extend along the first horizontal direction hd1, and contacts a multi-pillared dielectric isolation structure 416. Each multi-pillared dielectric isolation structure 416 contacts a pair of rows of memory stack structures 58.

[0216] At least two rows (such as three rows, four rows, etc.) of memory opening fill

structures 58 can be provided between a laterally neighboring pair of multi-pillared dielectric isolation structures 416. More than two rows of memory opening fill structures 58 can be provided between each laterally neighboring pair of dielectric isolation structures 320.

[0217] Referring to FIG. 43, a region including a memory opening 49 in an alternative configuration of the second exemplary structure is illustrated. The alternative configuration of the second exemplary structure can be derived from the second exemplary structure of FIGS. 34A and 34B by depositing a sacrificial semiconductor material layer 424L, forming a patterned etch mask layer 307 having the same pattern as the patterned etch mask layer 307 of FIGS. 35A, 35B, 36A, and 36B, and implanting electrical dopants into physically exposed portions of the sacrificial semiconductor material layer 424L that are laterally spaced from the straight edges of the patterned etch mask layer 307. The sacrificial semiconductor material layer 424L can be deposited as an undoped semiconductor material layer such as an undoped amorphous silicon layer or an undoped polysilicon layer. The electrical dopants used in the ion implantation process may be p-type dopants such as B or n-type dopants such as P, As, or Sb. A tilt angle of the ion implantation process can be selected such that implanted portions 424I of the sacrificial semiconductor material layer 424L does not cover portions of the dielectric liners 412 within the areas of the elongated openings in the patterned etch mask layer 307.

[0218] Referring to FIG. 44, an etch process is performed that etches the undoped semiconductor material of the unimplanted and unmasked portions of the sacrificial semiconductor material layer 424L selective to the implanted portions 424I of the sacrificial semiconductor material layer 424L. An anisotropic etch process or an isotropic etch process may be performed to remove the unimplanted and unmasked portions of the sacrificial semiconductor material layer 424L. Subsequently, unmasked portions of the dielectric liners

412 can be removed by an anisotropic etch process selective to the material of the implanted portions 424I of the sacrificial semiconductor material layer 424L. Optionally, unmasked portions of the semiconductor fill material portions 414 may be removed collaterally during the etch process that etches the unimplanted and unmasked portions of the sacrificial semiconductor material layer 424L and/or during the anisotropic etch process that etches the unmasked portions of the semiconductor fill material portions 414. A discrete corner cavity 413 is formed within a void of each memory opening 49 that is formed by removal of the etched material portions.

[0219] Referring to FIG. 45, portions of the vertical semiconductor channels 60 that underlie the elongated openings in the patterned etch mask layer 307 are etched by an isotropic etch process around the discrete corner cavities 413. The discrete corner cavities 413 are expanded to incorporate the volumes from which the vertical semiconductor channels 60 are removed. Portions of the memory films 50 adjacent to the discrete corner cavities 413 can be removed, for example, using a sequence of isotropic etch processes. In one embodiment, the sequence of isotropic etch processes can include a sequence of wet etch processes that etch the materials of the tunneling dielectric layer 56, the charge storage layer 54, and the blocking dielectric layer 52. The volumes of the discrete corner cavities 413 are expanded upon removal of the physically exposed portions of the memory films 50. Thus, the discrete corner cavities 413 are formed by removing an upper corner portion of each memory stack structure 55 within the memory openings 49 using at least one etch process. A subset of the discrete corner cavities 413 is formed within the two neighboring rows of memory openings 49 underneath each elongated opening in the patterned etch mask layer 307. The patterned etch mask layer 307 can be removed, for example, by ashing.

[0220] Referring to FIG. 46, an isotropic etch process that uses an isotropic etchant that

etches a material of the electrically conductive layers (46, 346) selective to the materials of the insulating layers (32, 332, 70), the semiconductor fill material portions 414, the sacrificial semiconductor material layer 424L is performed to laterally recess the portions of the electrically conductive layers (46, 346) from the discrete corner cavities 413. The isotropic etchant that etches the material(s) of the drain-select-level electrically conductive layers 346 selective to the materials of the insulating cap layer 70, the insulating layers (32, 332), the memory films 50, the dielectric cores 62, and the semiconductor fill material portions 414 can be introduced into the discrete corner cavities 413. Physically exposed sidewalls of the drain-select-level electrically conductive layers 346 can be laterally recessed in an isotropic etch process using the isotropic etchant.

[0221] At least one laterally-extending cavity 415 is formed by laterally recessing portions of the at least one drain-select-level electrically conductive layer 346 from the discrete corner cavities 413. If multiple drain-select-level electrically conductive layers 346 are present, a plurality of laterally-extending cavities 415 can be formed by laterally recessing portions of the drain-select-level electrically conductive layers 346 from the discrete corner cavities 413. The lateral recess distance of the isotropic etch process is greater than one half of the minimum separation distance between the memory openings 49.

[0222] A laterally-extending cavity 415 that laterally extends along the first horizontal direction hd1 can be formed at each level of the drain-select-level electrically conductive layers 346 within each area of the elongated opening in the patterned etch mask layer 307. At least one laterally-extending cavity 415 laterally connects two neighboring rows of memory openings 49. In one embodiment, a vertical stack of a plurality of laterally-extending cavities 415 laterally connects two neighboring rows of memory openings 49. Each of the at least one laterally-extending cavity 415 connects the discrete corner cavities 413 within the two

rows of memory openings 49 to provide a continuous cavity.

[0223] The continuous cavity is herein referred to as an integrated cavity (413, 415), and includes all volumes of the discrete corner cavities 413 in the two rows of memory openings 49 and the at least one laterally-extending cavity 415. Each drain-select-level electrically conductive layer 346 can be divided into multiple strips with a cut at the location of each elongated opening in the patterned etch mask layer 307. The patterned etch mask layer 307 can be removed after, or prior to, the isotropic etch process.

[0224] Referring to FIG. 47, remaining portions of the sacrificial semiconductor material layer 424L and the semiconductor fill material portions 414 can be removed selective to the drain-select-level electrically conductive layers 346, the insulating layers (32, 332, 70), dielectric cores 62, and the dielectric liners 412. For example, if the semiconductor fill material portions 414 include a semiconductor material (such as amorphous silicon or polysilicon), the semiconductor fill material portions 414 can be removed using a wet etch process using hot trimethyl-2 hydroxyethyl ammonium hydroxide ("hot TMY"), tetramethyl ammonium hydroxide (TMAH), or a potassium oxide (KOH) solution.

[0225] A dielectric material such as a doped silicate glass (such as borosilicate glass or phosphosilicate glass) or organosilicate glass can be deposited in the volumes of the integrated cavities (413, 415) using a conformal deposition process. Excess portions of the dielectric material can be removed from above the horizontal plane including the top surface of the insulating cap layer 70. Each continuous remaining portion of the dielectric material filling a respective integrated cavity (413, 415) constitutes a multi-pillared dielectric isolation structure 416. Each multi-pillared dielectric isolation structure 416 is formed by depositing a dielectric material in volumes of the at least one laterally-extending cavity 415 and in the discrete corner cavities 413.

[0226] Each multi-pillared dielectric isolation structure 416 includes a plurality of dielectric pillar portions 417 that fills a volume of a respective one of the discrete corner cavities 413 and at least one horizontally-extending portion adjoining each of the plurality of dielectric pillar portions 417, filling a volume of a respective one of the at least one laterally-extending cavity 415, located between a vertically neighboring pair of insulating layers (such as a vertically neighboring pair of drain-select-level insulating layers 332, a drain-select-level insulating layer 332 and an insulating cap layer 70, or a drain-select-level insulating layer 332 and a topmost word-line-level insulating layer 32) within the alternating stack (32, 46, 332, 346, 70), and laterally separating remaining portions of at least one electrically conductive layer (such as the at least one drain-select-level electrically conductive layer 346) within the alternating stack (32, 46, 332, 346, 70).

[0227] The multi-pillared dielectric isolation structures 416 fill volumes formed by removal of the semiconductor fill material portions 414. In one embodiment, each multi-pillared dielectric isolation structure 416 can include a plurality of horizontally-extending portions that laterally extend along the first horizontal direction $hd1$, contact a top surface of an underlying one of the insulating layers (332 or 32) within the alternating stack (32, 332, 70) and contact a bottom surface of an overlying one of the insulating layers (332 or 70) within the alternating stack (32, 332, 70).

[0228] Referring to FIG. 48, upper portions of the multi-pillared dielectric isolation structures 416 located in the memory openings 49 can be vertically recessed to form drain cavities.

[0229] Referring to FIGS. 49, 50A, and 50B, a doped semiconductor material having a doping of the second conductivity type is deposited in the drain cavities to form drain regions 63. Each drain region 63 can include a cylindrical drain segment 63C having a cylindrical

shape and a block arc drain segment 63B that vertically extends with a uniform horizontal cross-sectional shape of a block arc, i.e., a shape of a segment of an annulus with a limited range of the azimuthal angle.

[0230] The set of all material portions within each memory opening 49 after formation of the drain region 63 is herein referred to as a memory opening fill structure 58. The set of all material portions within each support opening 19 after formation of drain regions is herein referred to as a support pillar structure. A first subset of the memory opening fill structures 58 can be arranged in rows that laterally extend along the first horizontal direction hd1, and contacts a multi-pillared dielectric isolation structure 416. Each multi-pillared dielectric isolation structure 416 contacts a pair of rows of memory stack structures 58.

[0231] At least two rows (such as three rows, four rows, etc.) of memory opening fill structures 58 can be provided between a laterally neighboring pair of multi-pillared dielectric isolation structures 416. More than two rows of memory opening fill structures 58 can be provided between each laterally neighboring pair of dielectric isolation structures 320.

[0232] FIG. 51 is a top-down view of an alternative configuration for the second exemplary structure of FIGS. 50A and 50B according to the second embodiment of the present disclosure. FIG. 51 illustrates an alternative layout for the multi-pillared dielectric isolation structures 416 in which each strip of drain-select-level electrically conductive layers 346 that are laterally spaced apart by the multi-pillared dielectric isolation structures 416 contacts and controls two rows of memory stack structures 58.

[0233] Referring to FIGS. 52A and 52B, a contact level dielectric layer 73 can be formed over the insulating cap layer 70 and the retro-stepped dielectric material portion 65. Contact via structures (88, 86, 8P) can be formed through the contact level dielectric layer 73, and optionally through the retro-stepped dielectric material portion 65. For example, drain

contact via structures 88 can be formed through the contact level dielectric layer 73 on each drain region 63. Word line contact via structures 86 can be formed on the electrically conductive layers (46, 346) through the contact level dielectric layer 73, and through the retro-stepped dielectric material portion 65. Peripheral device contact via structures 8P can be formed through the retro-stepped dielectric material portion 65 directly on respective nodes of the peripheral devices.

[0234] Referring to FIG. 53, a memory die 900 can be provided by forming additional interconnect-level dielectric material layers 960 including metal interconnect structures 980 over the first exemplary structure or the second exemplary structure. The metal interconnect structures 980 can include bit lines 98 that are electrically connected to a respective subset of the drain regions 63 through a respective subset of the drain contact via structures 88.

Bonding pads 988 can be formed on top of the metal interconnect structures 980.

[0235] Referring to all drawings and according to various embodiments of the present disclosure, a three-dimensional memory device is provided, which comprises: an alternating stack of insulating layers (32, 332, 70) and electrically conductive layers (46, 346) located over a substrate (9, 10); memory openings 49 vertically extending through the alternating stack (32, 46, 332, 346, 70); memory stack structures located within a respective one of the memory openings, wherein each of the memory stack structures 55 comprises a memory film 50 and a vertical semiconductor channel 60; and a multi-pillared dielectric isolation structure 416 comprising a plurality of dielectric pillar portions 417 located within a respective one of the memory openings 49 and at least one horizontally-extending portion adjoining each of the plurality of dielectric pillar portions 417 and located between a vertically neighboring pair of insulating layers (32, 332, 70) within the alternating stack (32, 46, 332, 346, 70) and laterally separating laterally neighboring strips of at least one electrically conductive layer (such as the

drain-select-level electrically conductive layers 346) within the alternating stack (32, 46, 332, 346, 70).

[0236] In one embodiment, an entirety of the multi-pillared dielectric isolation structure 416 is a structure of integral construction and has a homogeneous composition throughout. As used herein, a structure of “integral construction” refers to a structure of a single continuous piece including a single structural component therein without any physically observable interface that divides the structure into multiple portions.

[0237] Each memory opening fill structure 58 that contacts a dielectric pillar portion 417 of a multi-pillared dielectric isolation structure 416 is herein referred to as a first memory opening fill structure 58. Each memory opening fill structure 58 that does not contact any dielectric pillar portion 417 of a multi-pillared dielectric isolation structure 416 is herein referred to as a second memory opening fill structure 58. Each second memory opening fill structure 58 includes a semiconductor fill material portion 414 that is laterally surrounded by a respective dielectric liner 412 that azimuthally extends around a vertical axis passing through the second memory opening fill structure by 360 degrees.

[0238] In one embodiment, each of the vertical semiconductor channels 60 comprises: a tubular semiconductor channel portion including a top surface that contacts a bottom surface of a respective one of the plurality of dielectric pillar portions 417; and a semitubular semiconductor channel portion adjoined to an upper end of the tubular semiconductor channel portion and contacting sidewalls of the respective one of the plurality of dielectric pillar portions 417.

[0239] In one embodiment, the three-dimensional memory device comprises drain regions 63 contacting a respective one of the semitubular semiconductor channel portions and having a cylindrical drain segment 63C and a block arc drain segment 63B.

[0240] In one embodiment, the plurality of dielectric pillar portions 417 contacts bottom surfaces of the drain regions 63.

[0241] In one embodiment, each of the memory films 50 comprises: a tubular memory film portion including a top surface that contacts a bottom surface of one of the plurality of dielectric pillar portions 417; and a semitubular memory film portion adjoined to an upper end of the tubular memory film portion and contacting sidewalls of the one of the plurality of dielectric pillar portions 417.

[0242] In one embodiment, the three-dimensional memory device further comprises: dielectric liners 412 located within the memory openings 49 and contacting a sidewall of a respective one of the semitubular semiconductor channel portions and a sidewalls of a respective one of the plurality of dielectric pillar portions 417; and dielectric cores 62 located within the memory openings 49, contacting a bottom surface of a respective one of the plurality of dielectric pillar portions 417, and laterally surrounded by a respective one of the tubular semiconductor channel portions.

[0243] In one embodiment, dielectric pillar portions 417 within the plurality of dielectric pillar portions 417 are laterally spaced from each other by one of the insulating layers (such as each of the drain-select-level insulating layers 332) within the alternating stack (32, 46, 332, 346, 70), wherein the one of the insulating layers (such as each of the drain-select-level insulating layers 332) laterally encircles and encloses each of the memory openings 49 within two rows of memory openings 49.

[0244] In one embodiment, each of the memory openings 49 with the two rows of memory openings 49 includes one of the plurality of dielectric pillar portions 417 and one of the memory stack structures 58.

[0245] In one embodiment, each of the plurality of dielectric pillar portions 417

comprises: a cylindrical dielectric pillar portion 417C centered at a vertical axis passing through a geometrical center of a respective one of the memory openings 49 and azimuthally extending around the vertical axis by 360 degrees; and a block arc pillar portion 417B centered at the vertical axis, adjoined to one side of the cylindrical dielectric pillar portion 417C, and azimuthally extending around the vertical axis by an angle in a range from 30 degrees to 270 degrees.

[0246] In one embodiment, the alternating stack (32, 46, 332, 346, 70) comprises a terrace region in which each electrically conductive layer (46, 346) other than a topmost electrically conductive layer (such as the topmost one of the drain-select-level electrically conductive layer 346) within the alternating stack (32, 46, 332, 346, 70) laterally extends farther than any overlying electrically conductive layer (46, 346) within the alternating stack (32, 46, 332, 346, 70); the terrace region includes stepped surfaces of the alternating stack (32, 46, 332, 346, 70) that continuously extend from a bottommost layer within the alternating stack (32, 46, 332, 346, 70) to a topmost layer within the alternating stack (32, 46, 332, 346, 70); and support pillar structures 20 extend through the stepped surfaces and through a retro-stepped dielectric material portion 65 that overlies the stepped surfaces.

[0247] In one embodiment, the three-dimensional memory device comprises a backside blocking dielectric layer 44 disposed between each neighboring pair of an electrically conductive layer (46, 346) and an insulating layer (32, 332, 70) and extending from a bottommost layer within the alternating stack (32, 46, 332, 346, 70) to a topmost layer within the alternating stack (32, 46, 332, 346, 70), wherein pedestal channel portions underlying a respective one of the vertical semiconductor channels are laterally spaced from the backside blocking dielectric layer 44 by tubular dielectric spacers 116.

[0248] In one embodiment, at least one horizontally-extending portion comprises a

plurality of horizontally-extending portions that laterally extend along a first horizontal direction hd1, contact a top surface of an underlying one of the insulating layers (such as a topmost one of the word-line-level insulating layers 32 or a drain-select-level insulating layer 332) within the alternating stack (32, 46, 332, 346, 70), and contact a bottom surface of an overlying one of the insulating layers (such as the insulating cap layer 70 or one of the drain-select-level insulating layer 332) within the alternating stack (32, 46, 332, 346, 70) .

[0249] The exemplary structures can include a three-dimensional memory device. In one embodiment, the three-dimensional memory device comprises a monolithic three-dimensional NAND memory device. The electrically conductive layers 46 can comprise, or can be electrically connected to, a respective word line of the monolithic three-dimensional NAND memory device. The substrate (9, 10) can comprise a silicon substrate. The vertical NAND memory device can comprise an array of monolithic three-dimensional NAND strings over the silicon substrate. At least one memory cell (comprising a portion of a charge storage layer 54 at a level of a word-line-level electrically conductive layer 46) in a first device level of the array of monolithic three-dimensional NAND strings can be located over another memory cell (comprising another portion of the charge storage layer 54 at a level of another word-line-level electrically conductive layer 46) in a second device level of the array of monolithic three-dimensional NAND strings. The silicon substrate can contain an integrated circuit comprising a driver circuit (comprising a subset of the least one semiconductor device 700) for the memory device located thereon. The electrically conductive layers 46 can comprise a plurality of control gate electrodes having a strip shape extending substantially parallel to the top surface of the substrate (9, 10), e.g., between a pair of backside trenches 79. The plurality of control gate electrodes comprises at least a first control gate electrode located in a first device level and a second control gate electrode located in a second device

level. The array of monolithic three-dimensional NAND strings can comprise: a plurality of semiconductor channels (59, 11, 60), wherein at least one end portion (such as a vertical semiconductor channel 60) of each of the plurality of semiconductor channels (59, 11, 60) extends substantially perpendicular to a top surface of the substrate (9, 10) and comprising a respective one of the vertical semiconductor channels 60; and a plurality of charge storage elements (comprising portions of the memory films 50, i.e., portions of the charge storage layer 54). Each charge storage element can be located adjacent to a respective one of the plurality of semiconductor channels (59, 11, 60).

[0250] The dielectric isolation structures (320, 416) of various embodiments of the present disclosure can be used to provide electrical isolation between neighboring pairs of strips of each drain-select-level electrically conductive layer 346 while enabling formation of the memory openings 49 and the memory stack structures 58 as a periodic two-dimensional array including multiple rows that extend along the lengthwise direction of the backside trenches 79 and having a uniform inter-row pitch between neighboring pairs of rows. The memory stack structures 58 can be formed without allocation of any extra space for providing electrical isolation between neighboring pairs of strips of drain-select-level isolation structures.

[0251] Although the foregoing refers to particular preferred embodiments, it will be understood that the claims are not so limited. It will occur to those of ordinary skill in the art that various modifications may be made to the disclosed embodiments and that such modifications are intended to be within the scope of the claims. Compatibility is presumed among all embodiments that are not alternatives of one another. The word “comprise” or “include” contemplates all embodiments in which the word “consist essentially of” or the word “consists of” replaces the word “comprise” or “include,” unless explicitly stated

otherwise. Where an embodiment using a particular structure and/or configuration is illustrated in the present disclosure, it is understood that the claims may be practiced with any other compatible structures and/or configurations that are functionally equivalent provided that such substitutions are not explicitly forbidden or otherwise known to be impossible to one of ordinary skill in the art. All of the publications, patent applications and patents cited herein are incorporated herein by reference in their entirety.

WHAT IS CLAIMED IS:

1. A three-dimensional memory device comprising:

an alternating stack of insulating layers and electrically conductive layers located over a substrate;

memory openings vertically extending through the alternating stack;

memory stack structures located within a respective one of the memory openings, wherein each of the memory stack structures comprises a memory film and a vertical semiconductor channel; and

a multi-pillared dielectric isolation structure comprising a plurality of dielectric pillar portions located within a respective one of the memory openings and at least one horizontally-extending portion adjoining each of the plurality of dielectric pillar portions and located between a vertically neighboring pair of insulating layers within the alternating stack and laterally separating laterally neighboring strips of at least one electrically conductive layer within the alternating stack.

2. The three-dimensional memory device of Claim 1, wherein an entirety of the multi-pillared dielectric isolation structure is a structure of integral construction and has a homogeneous composition throughout.

3. The three-dimensional memory device of Claim 1, wherein each of the vertical semiconductor channels comprises:

a tubular semiconductor channel portion including a top surface that contacts a bottom surface of a respective one of the plurality of dielectric pillar portions; and

a semitubular semiconductor channel portion adjoined to an upper end of the tubular semiconductor channel portion and contacting sidewalls of the respective one of the plurality of dielectric pillar portions.

4. The three-dimensional memory device of Claim 3, further comprising drain regions contacting a respective one of the semitubular semiconductor channel portions and having a cylindrical drain segment and a block arc drain segment.

5. The three-dimensional memory device of Claim 4, wherein the plurality of dielectric pillar portions contacts bottom surfaces of the drain regions.

6. The three-dimensional memory device of Claim 3, wherein each of the memory films comprises:

a tubular memory film portion including a top surface that contacts a bottom surface of one of the plurality of dielectric pillar portions; and

a semitubular memory film portion adjoined to an upper end of the tubular memory film portion and contacting sidewalls of the one of the plurality of dielectric pillar portions.

7. The three-dimensional memory device of Claim 3, further comprising:

dielectric liners located within the memory openings and contacting a sidewall of a respective one of the semitubular semiconductor channel portions and a sidewall of a respective one of the plurality of dielectric pillar portions; and

dielectric cores located within the memory openings, contacting a bottom surface of a respective one of the plurality of dielectric pillar portions, and laterally surrounded by a

respective one of the tubular semiconductor channel portions.

8. The three-dimensional memory device of Claim 1, wherein dielectric pillar portions within the plurality of dielectric pillar portions are laterally spaced from each other by one of the insulating layers within the alternating stack, wherein the one of the insulating layers laterally encircles and encloses each of the memory openings.

9. The three-dimensional memory device of Claim 1, wherein each of the memory openings includes one of the plurality of dielectric pillar portions and one of the memory stack structures.

10. The three-dimensional memory device of Claim 1, wherein each of the plurality of dielectric pillar portions comprises:

a cylindrical dielectric pillar portion centered at a vertical axis passing through a geometrical center of a respective one of the memory openings and azimuthally extending around the vertical axis by 360 degrees; and

a block arc pillar portion centered at the vertical axis, adjoined to one side of the cylindrical dielectric pillar portion, and azimuthally extending around the vertical axis by an angle in a range from 30 degrees to 270 degrees.

11. The three-dimensional memory device of Claim 1, wherein:

the alternating stack comprises a terrace region in which each electrically conductive layer other than a topmost electrically conductive layer within the alternating stack laterally extends farther than any overlying electrically conductive layer within the alternating stack;

the terrace region includes stepped surfaces of the alternating stack that continuously extend from a bottommost layer within the alternating stack to a topmost layer within the alternating stack; and

support pillar structures extend through the stepped surfaces and through a retro-stepped dielectric material portion that overlies the stepped surfaces.

12. The three-dimensional memory device of Claim 11, further comprising a backside blocking dielectric layer disposed between each neighboring pair of an electrically conductive layer and an insulating layer and extending from a bottommost layer within the alternating stack to a topmost layer within the alternating stack, wherein pedestal channel portions underlying a respective one of the vertical semiconductor channels are laterally spaced from the backside blocking dielectric layer by tubular dielectric spacers.

13. The three-dimensional memory device of Claim 1, wherein the at least one horizontally-extending portion comprises a plurality of horizontally-extending portions that laterally extend along a first horizontal direction, contact a top surface of an underlying one of the insulating layers within the alternating stack and contact a bottom surface of an overlying one of the insulating layers within the alternating stack.

14. A method of forming a three-dimensional memory device, comprising:

forming an alternating stack of insulating layers and spacer material layers over a substrate, wherein the spacer material layers are formed as, or are subsequently replaced with, electrically conductive layers;

forming memory openings vertically extending through the alternating stack;

forming memory stack structures within the memory openings, wherein each of the memory stack structures comprises a memory film and a vertical semiconductor channel having a cylindrical configuration;

forming discrete corner cavities by removing an upper corner portion of each memory stack structure within two neighboring rows of memory openings using at least one etch process;

forming at least one laterally-extending cavity by laterally recessing portions of the electrically conductive layers from the discrete corner cavities; and

forming a multi-pillared dielectric isolation structure by depositing a dielectric material in volumes of the at least one laterally-extending cavity and in the discrete corner cavities.

15. The method of Claim 14, further comprising:

forming a patterned etch mask layer including an elongated opening over the memory stack structures and the alternating stack, wherein straight edges of the elongated opening overlie the two neighboring rows of memory openings;

etching portions of the vertical semiconductor channels that underlie the elongated opening in the patterned etch mask layer; and

etching portions of the memory films adjacent to cavities formed by etching portions of the vertical semiconductor channels, wherein the discrete corner cavities are formed within the two neighboring rows of memory openings.

16. The method of Claim 14, further comprising performing an isotropic etch process that uses an etchant that etches a material of the electrically conductive layers selective to a

material of the insulating layers to laterally recess the portions of the electrically conductive layers from the discrete corner cavities, wherein a lateral recess distance of the isotropic etch process is greater than one half of a minimum separation distance between the memory openings, and each of the at least one laterally-extending cavity connects the discrete corner cavities to provide a continuous cavity that includes all volumes of the discrete corner cavities.

17. The method of Claim 16, wherein forming the multi-pillared dielectric isolation structure comprises forming:

- a plurality of dielectric pillar portions that fills a volume of a respective one of the discrete corner cavities; and

- at least one horizontally-extending portion adjoining each of the plurality of dielectric pillar portions, filling a volume of a respective one of the at least one laterally-extending cavity, located between a vertically neighboring pair of insulating layers within the alternating stack, and laterally separating remaining portions of at least one electrically conductive layer within the alternating stack.

18. The method of Claim 14, further comprising:

- forming a vertical stack of a dielectric core and a semiconductor fill material portion within each volume that is laterally surrounded by a respective one of the memory stack structures; and

- removing remaining portions of the semiconductor fill material portions after formation of the discrete corner cavities, wherein the multi-pillared dielectric isolation structure fills volumes formed by removal of the semiconductor fill material portions.

19. The method of Claim 14, further comprising:

forming drain cavities by recessing upper portions of the multi-pillared dielectric isolation structure located in the memory openings; and

forming drain regions by depositing a doped semiconductor material in the drain cavities.

20. The method of Claim 14, wherein:

the at least one laterally-extending cavity comprises a plurality of laterally-extending cavities; and

multi-pillared dielectric isolation structure comprises a plurality of horizontally-extending portions that laterally extend along a first horizontal direction, contact a top surface of an underlying one of the insulating layers within the alternating stack and contact a bottom surface of an overlying one of the insulating layers within the alternating stack.

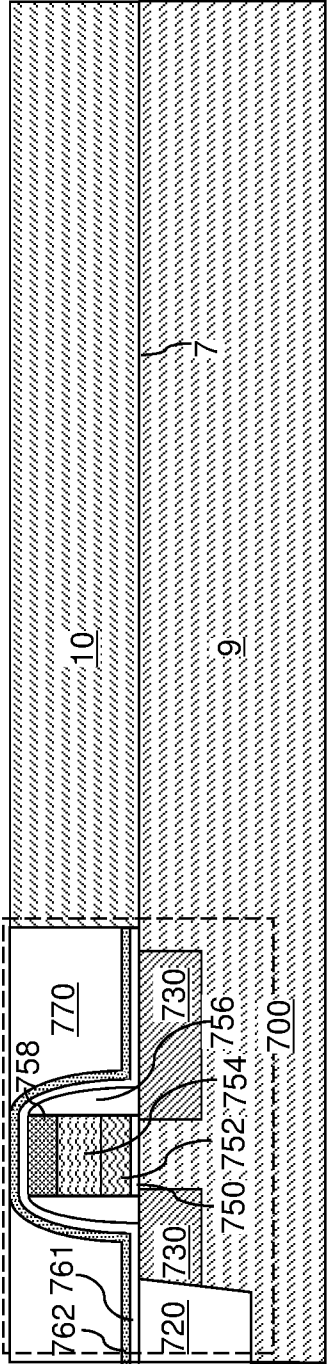


FIG. 1

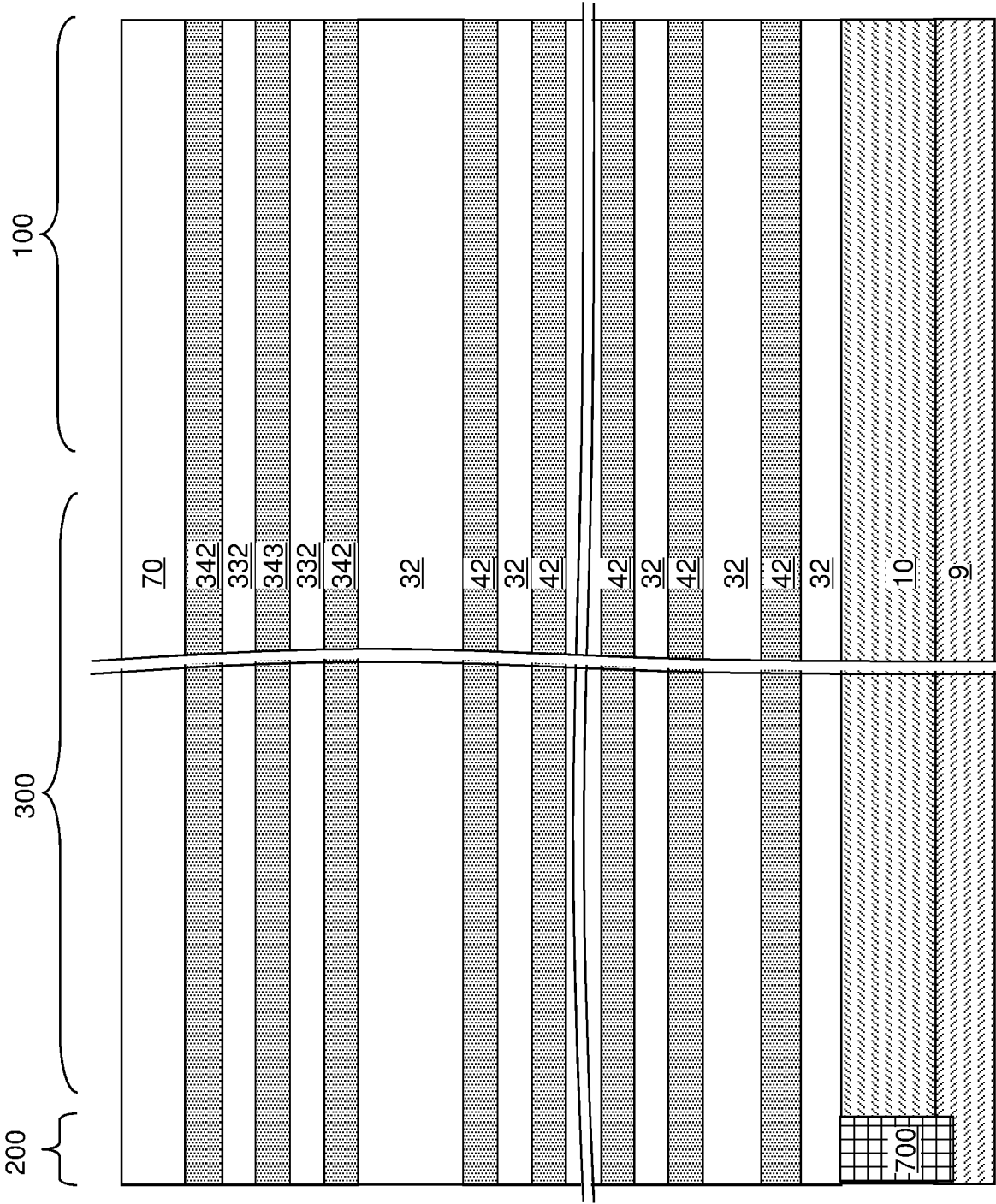


FIG. 2

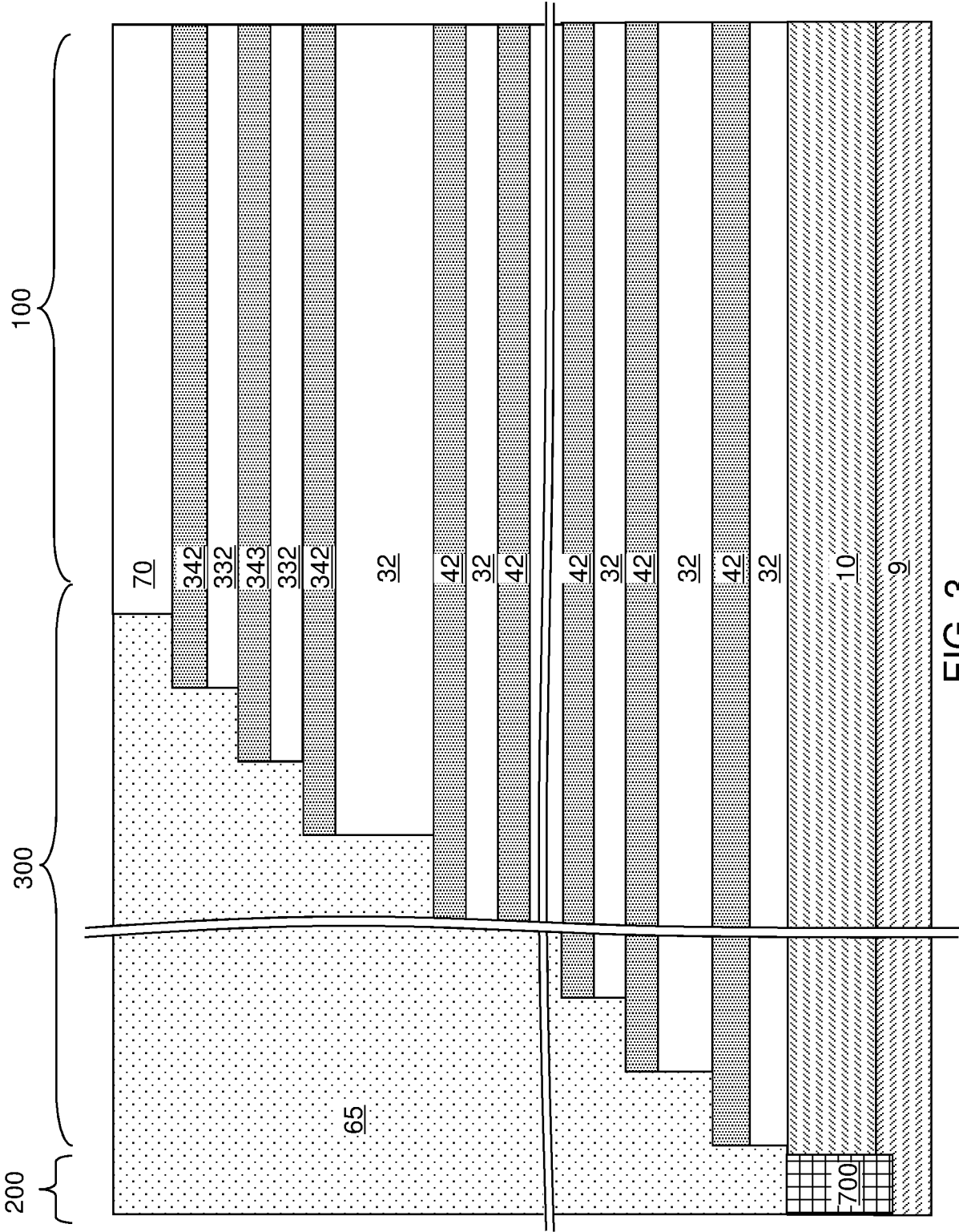


FIG. 3

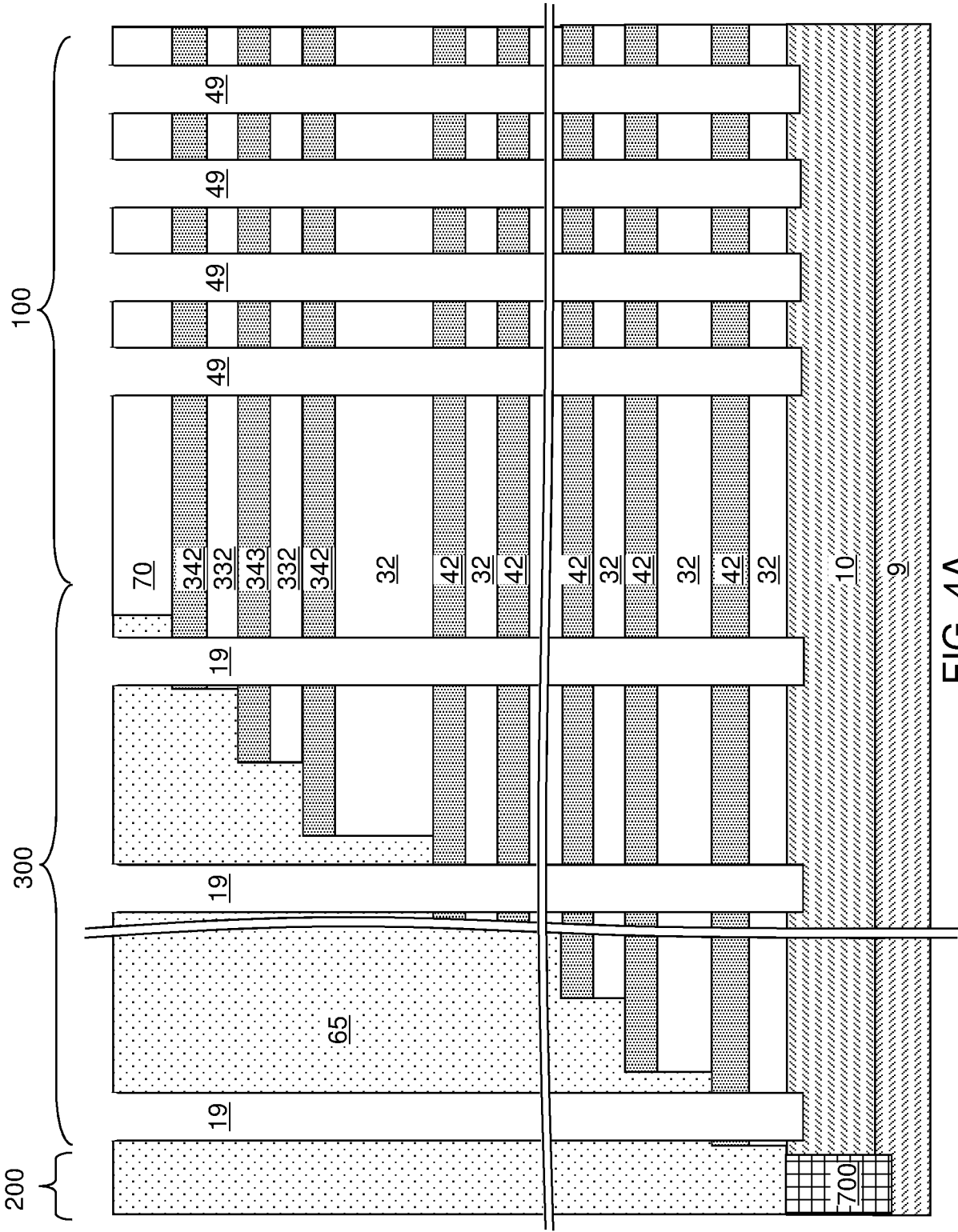


FIG. 4A

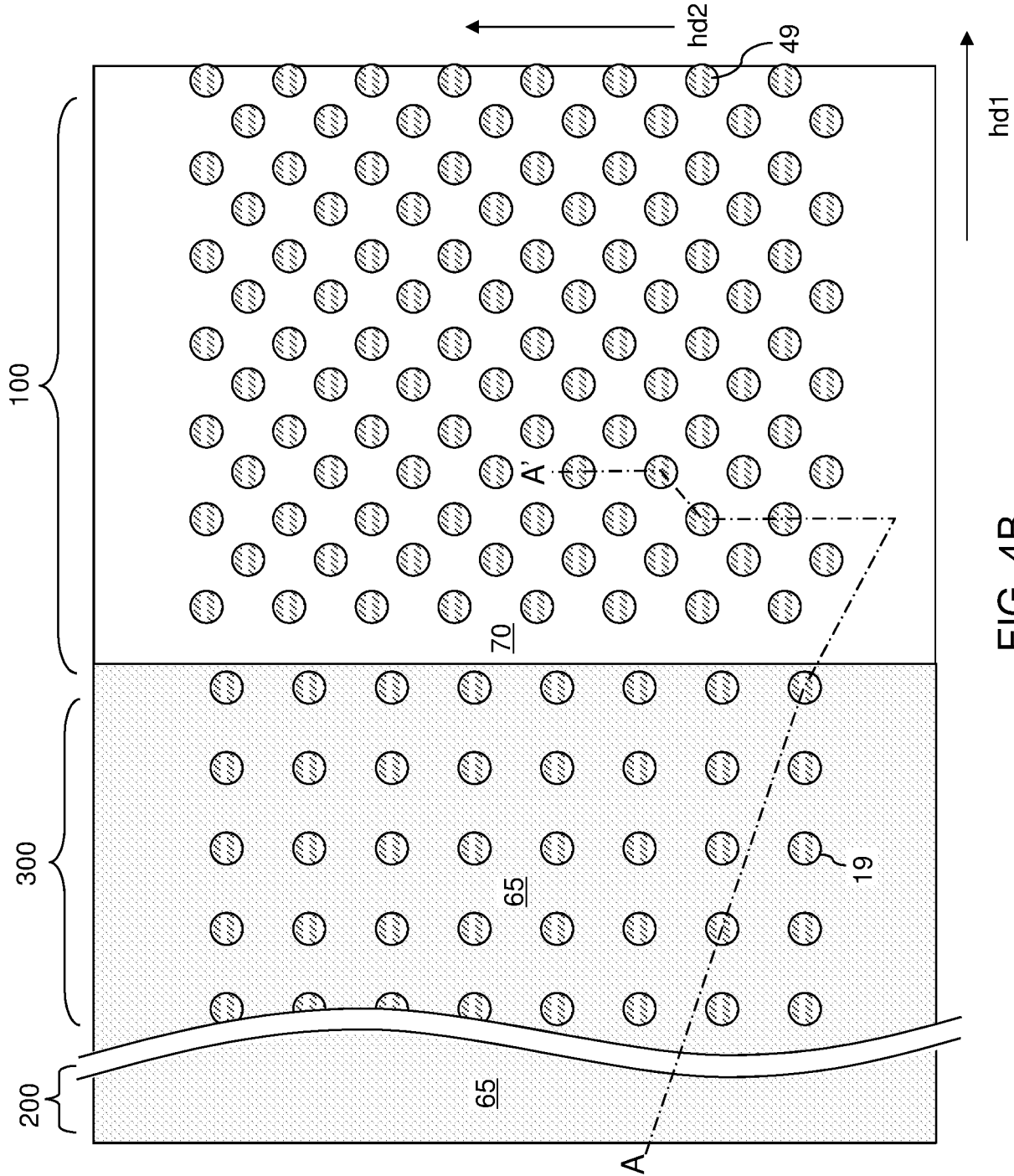


FIG. 4B

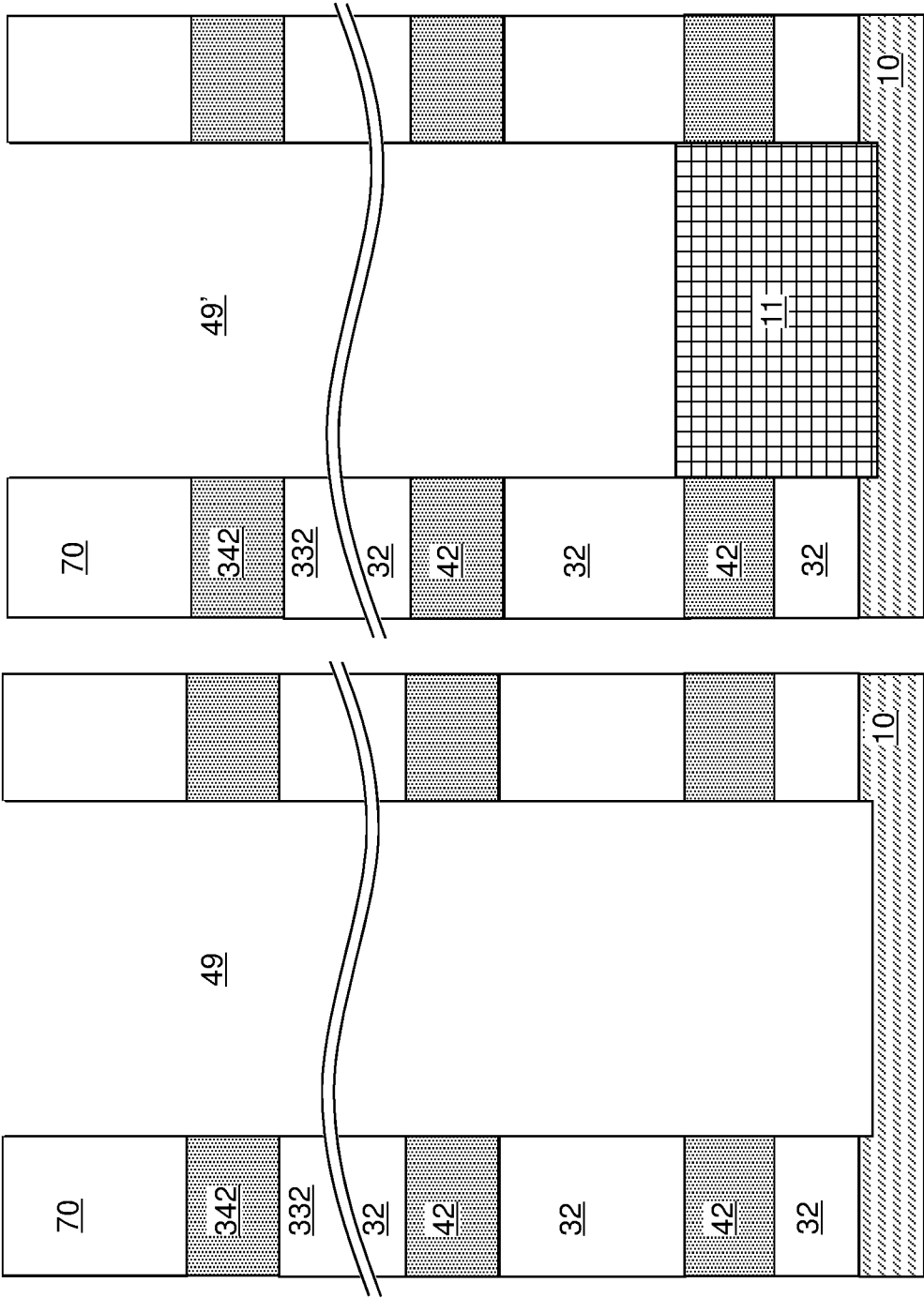


FIG. 5B

FIG. 5A

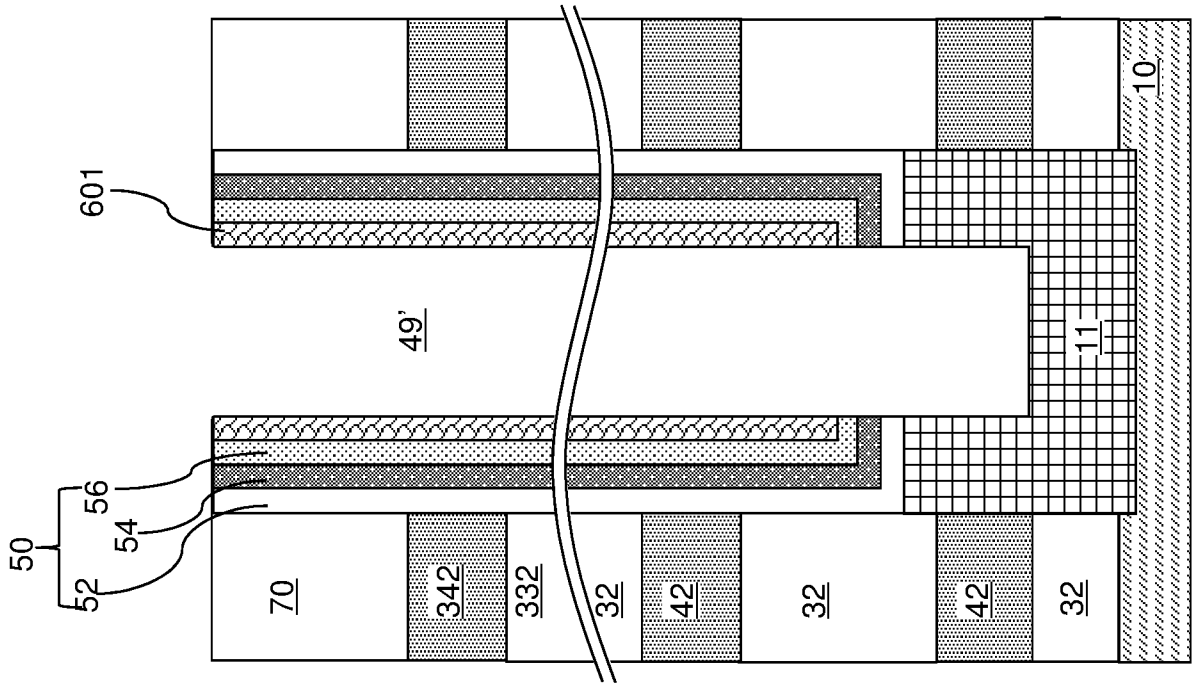


FIG. 5D

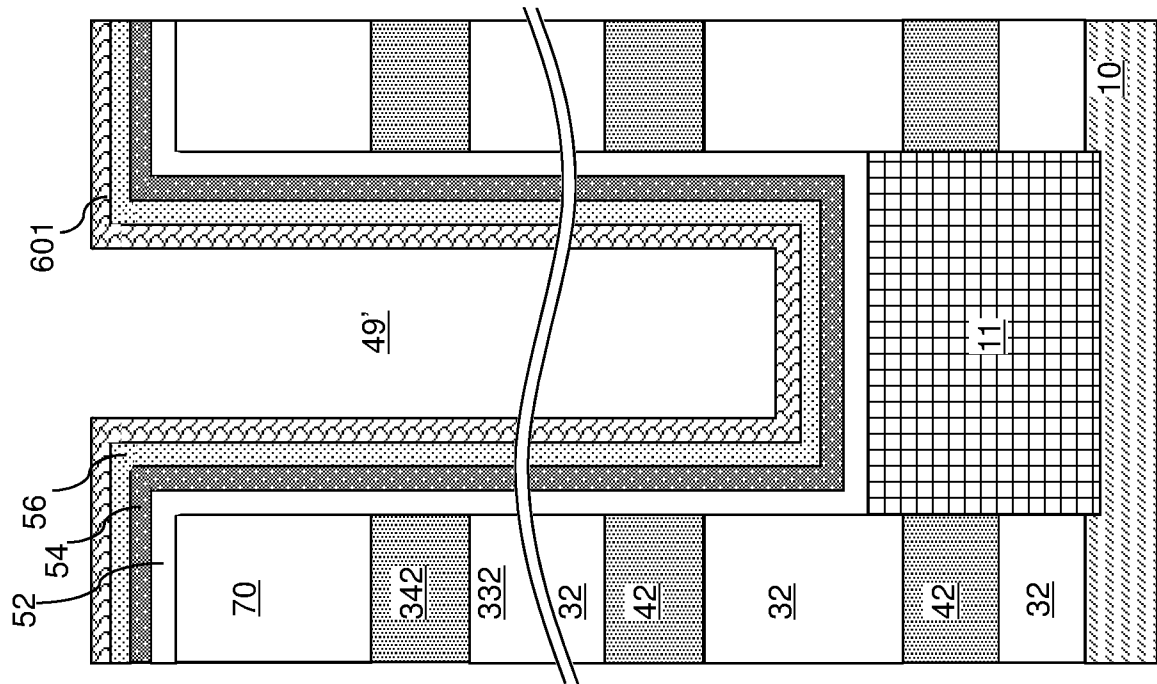


FIG. 5C

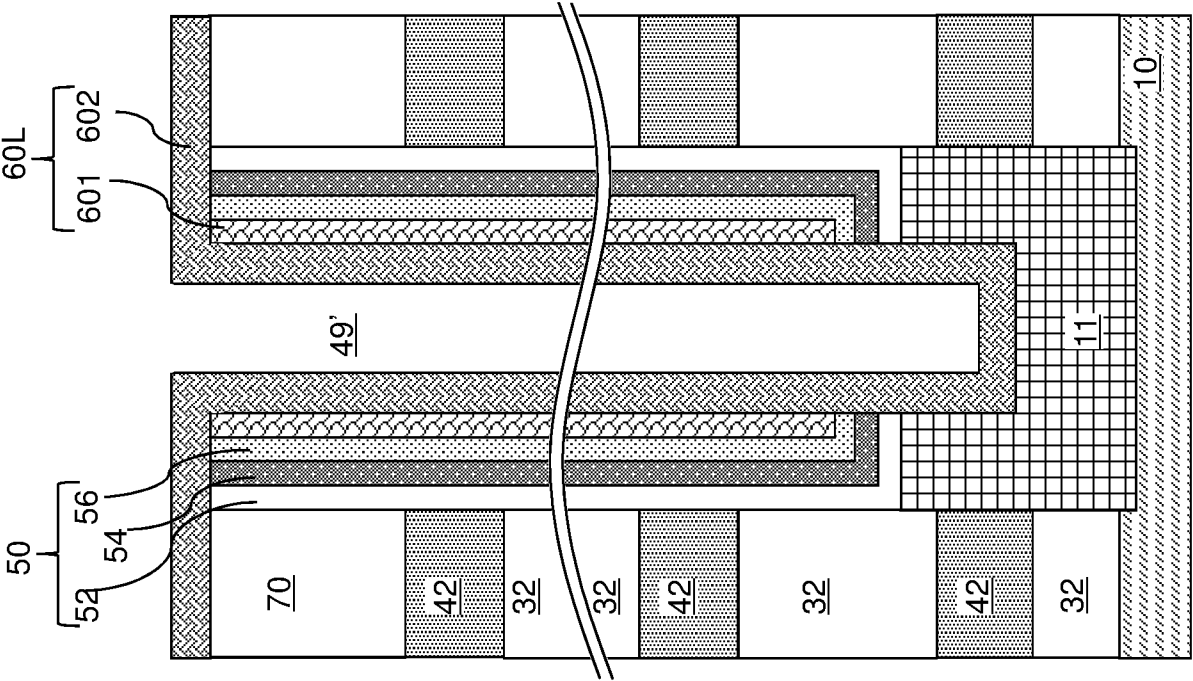


FIG. 5E

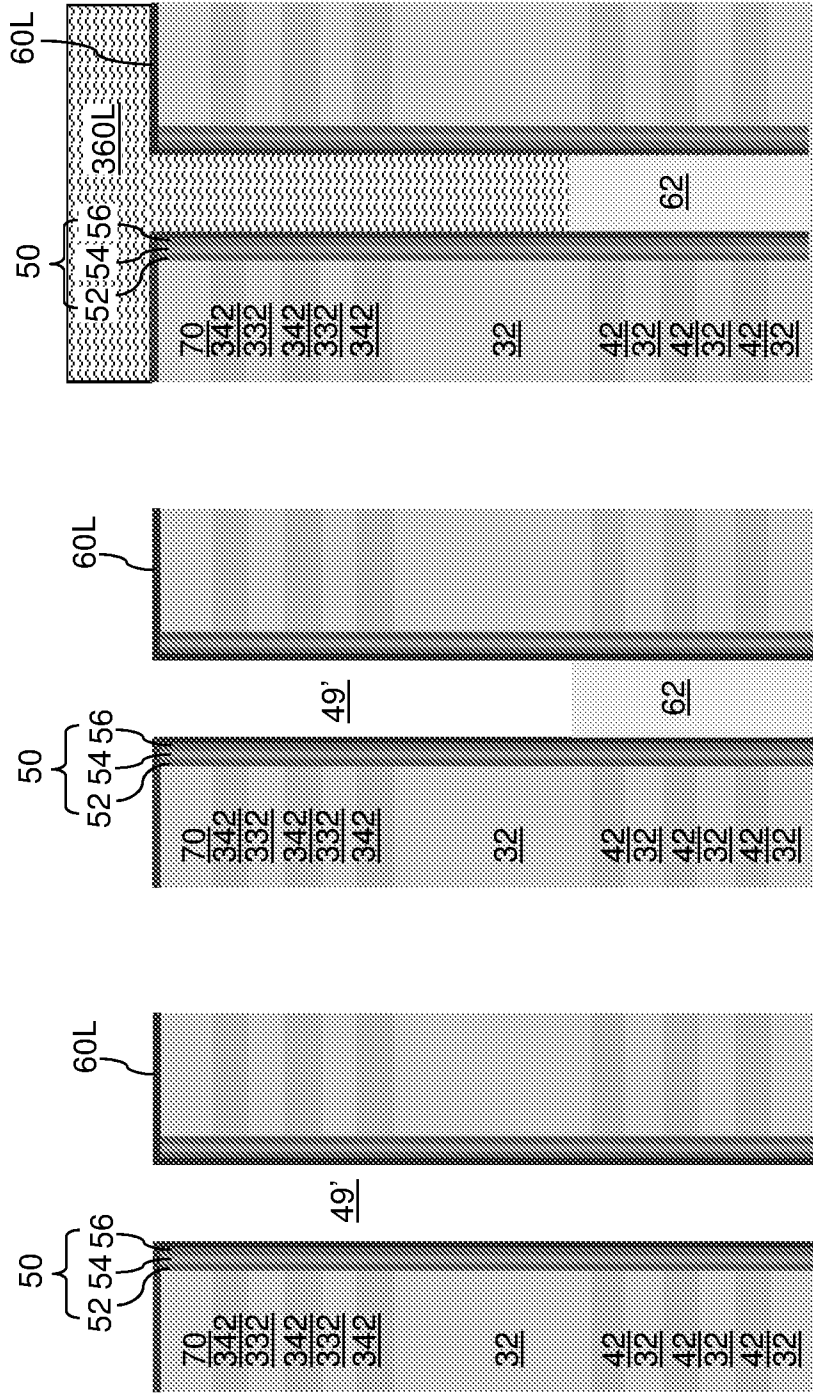


FIG. 6C

FIG. 6B

FIG. 6A

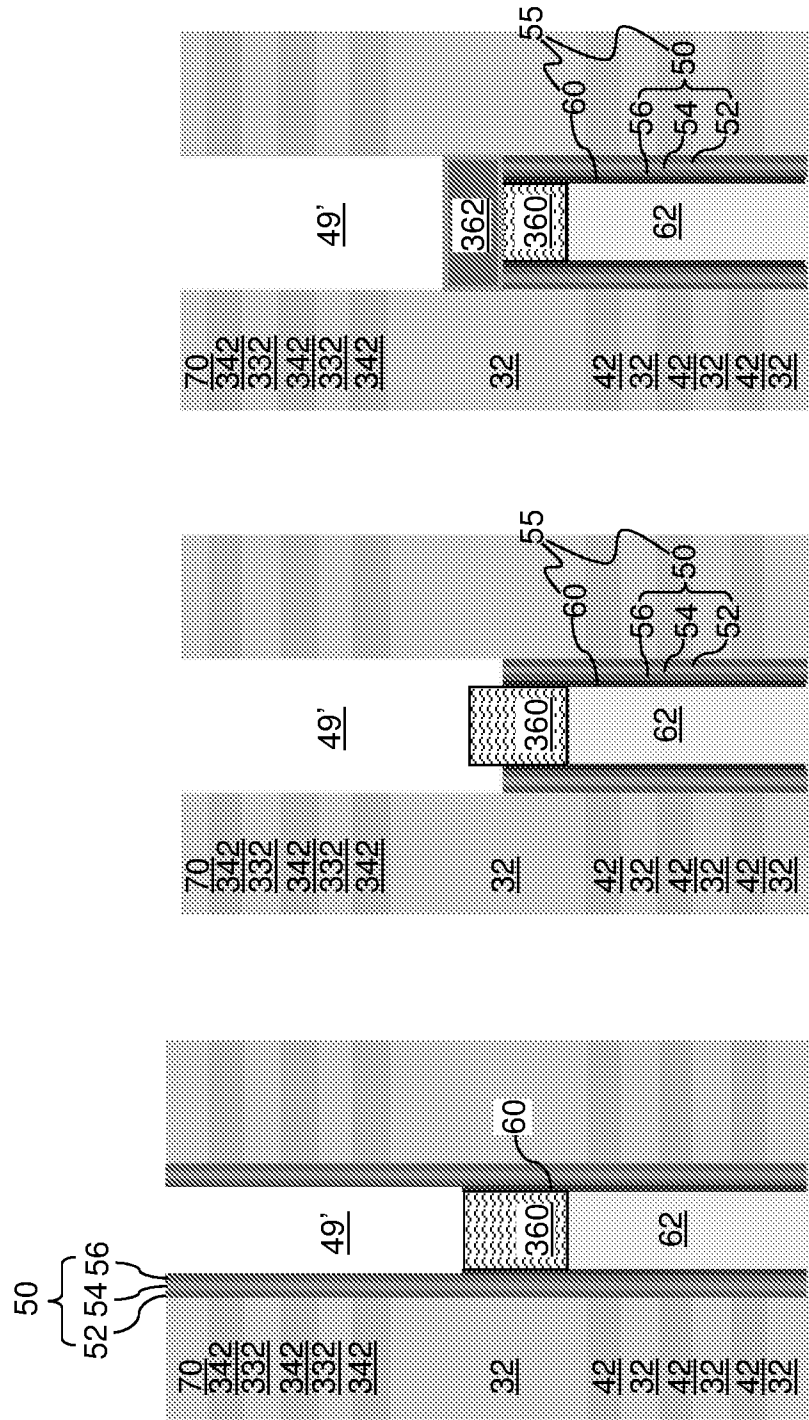


FIG. 6F

FIG. 6E

FIG. 6D

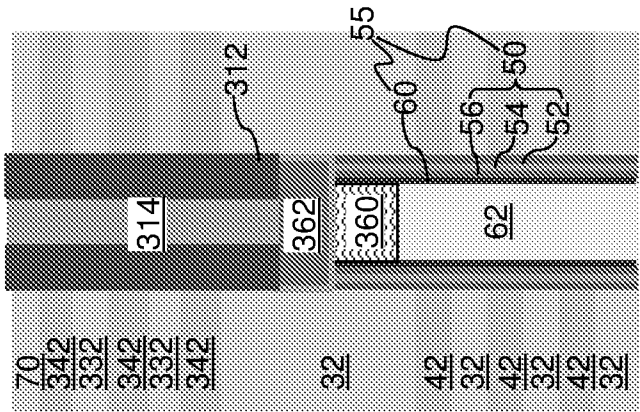


FIG. 7A

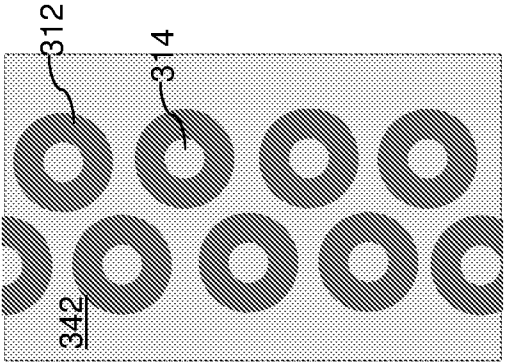


FIG. 7B

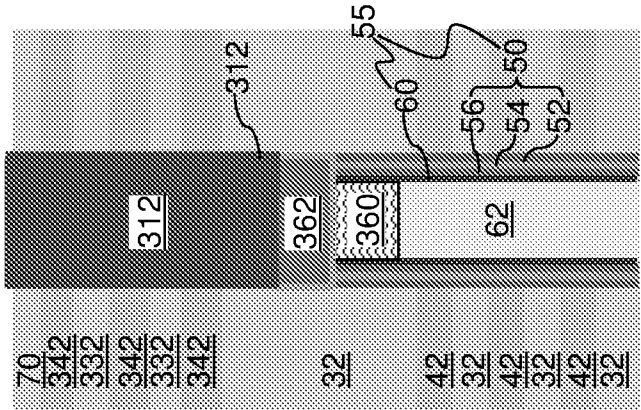


FIG. 7C

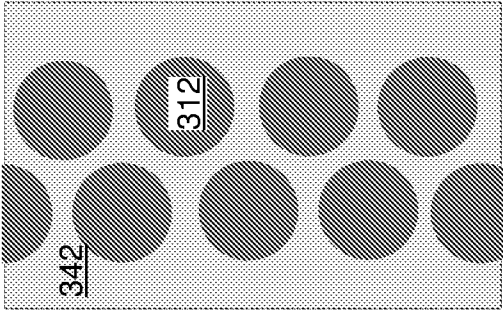
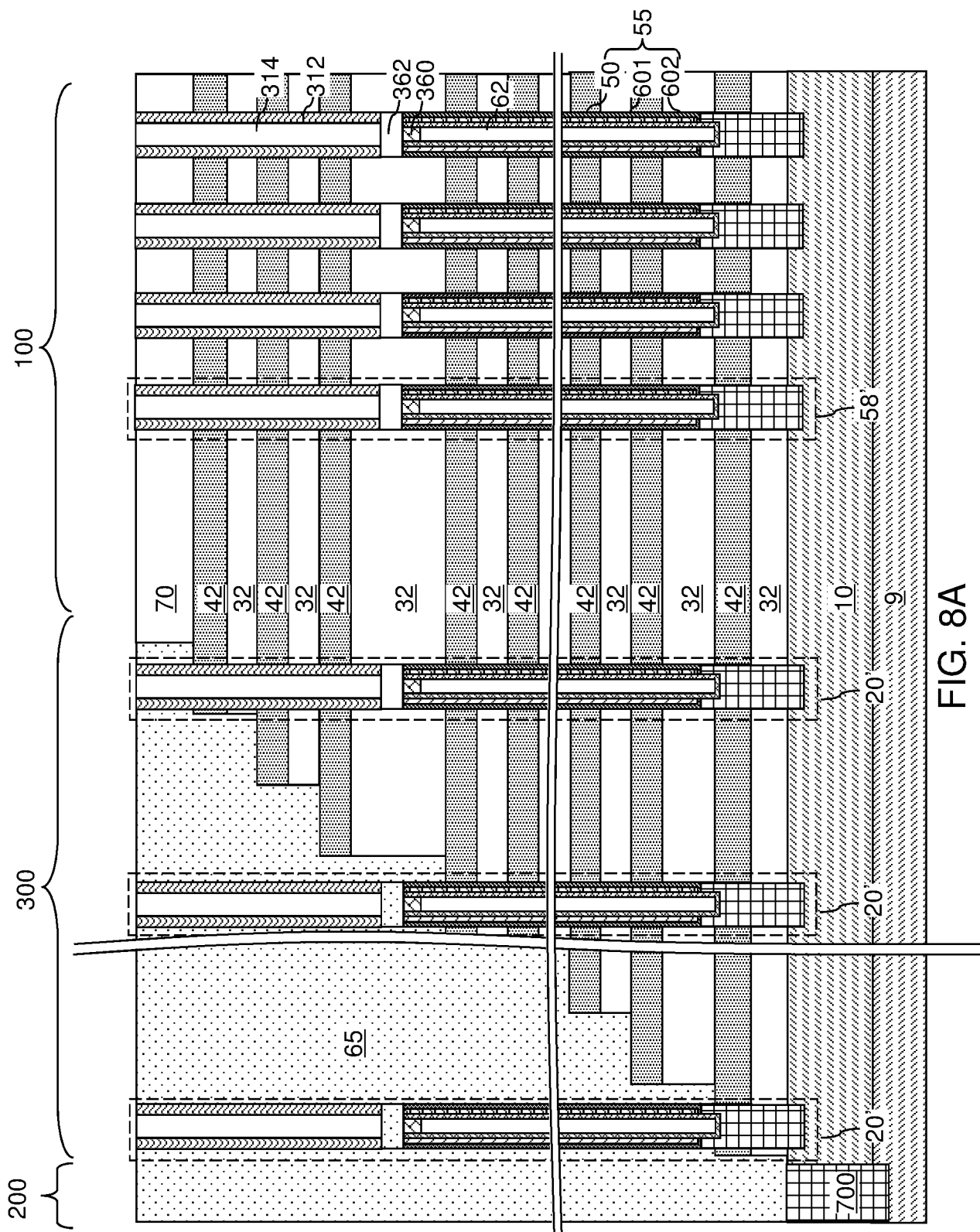


FIG. 7D



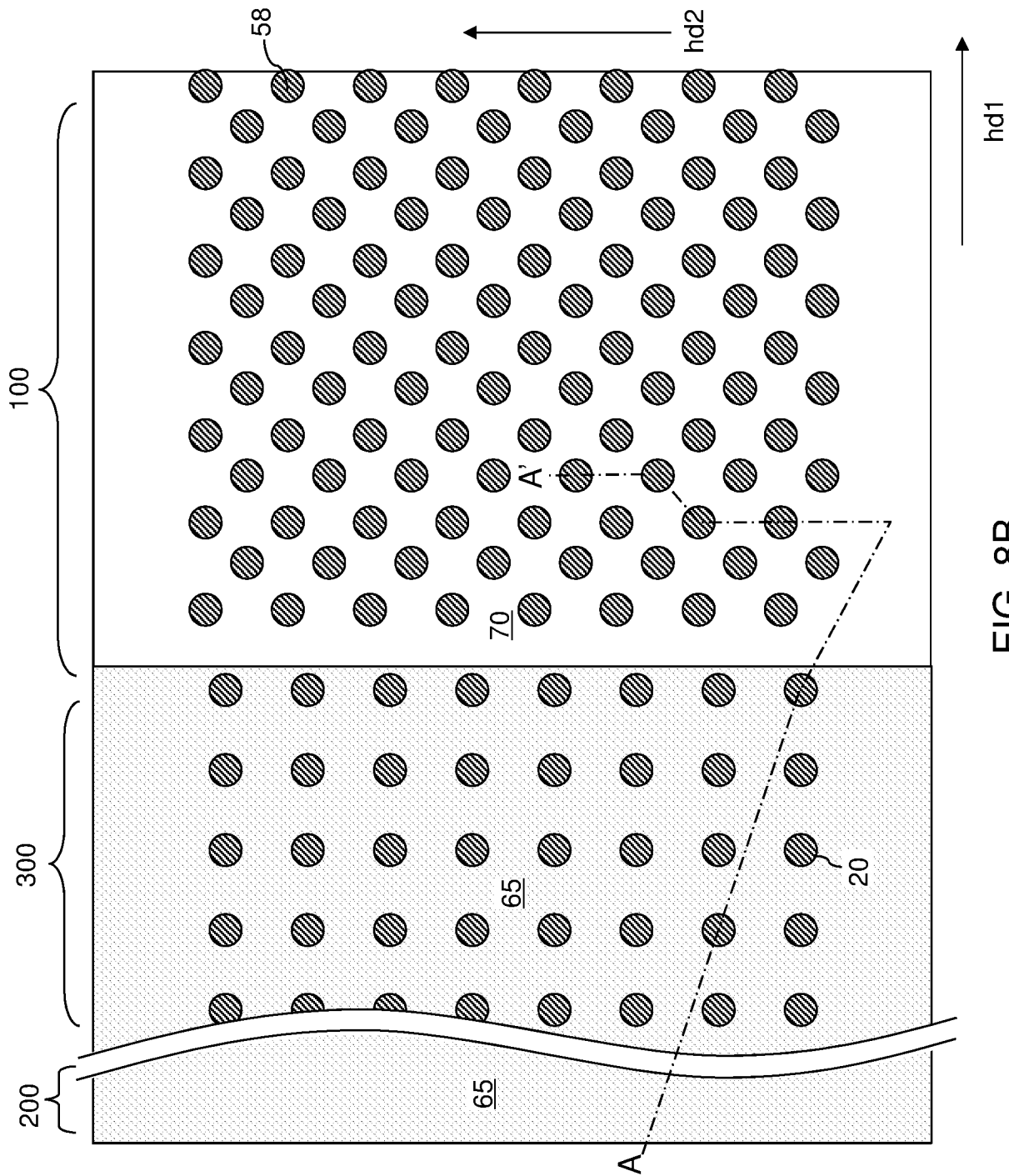
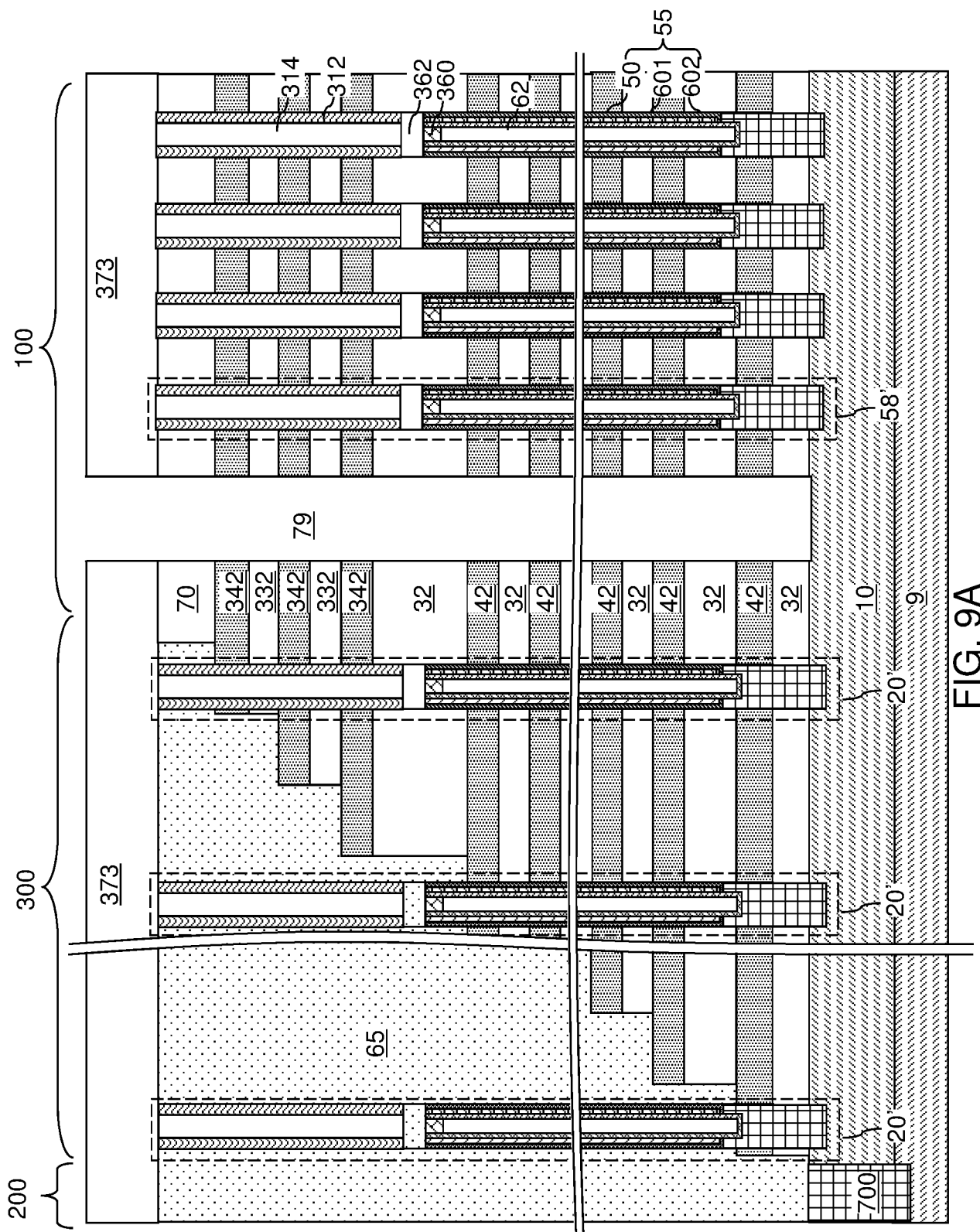
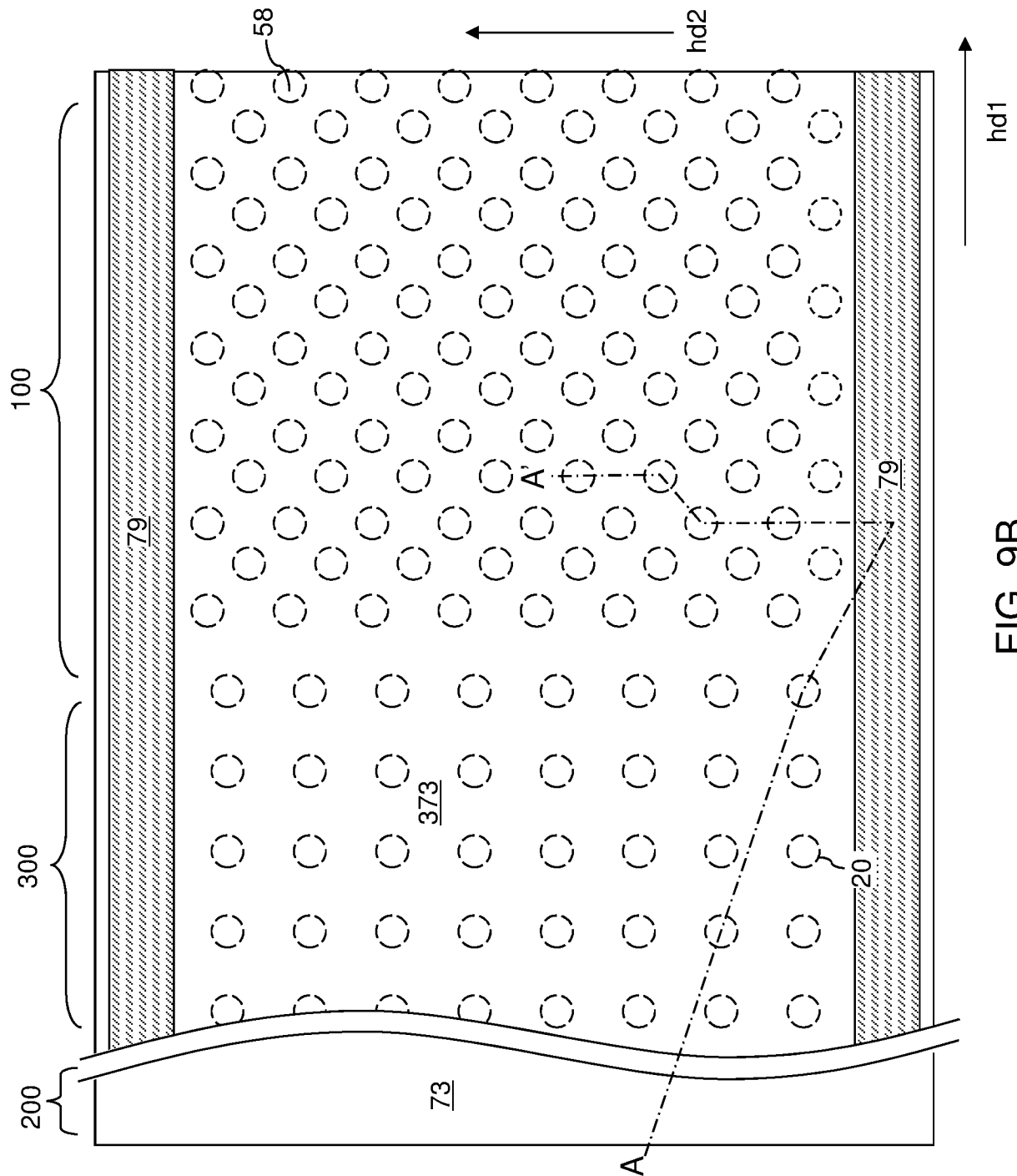
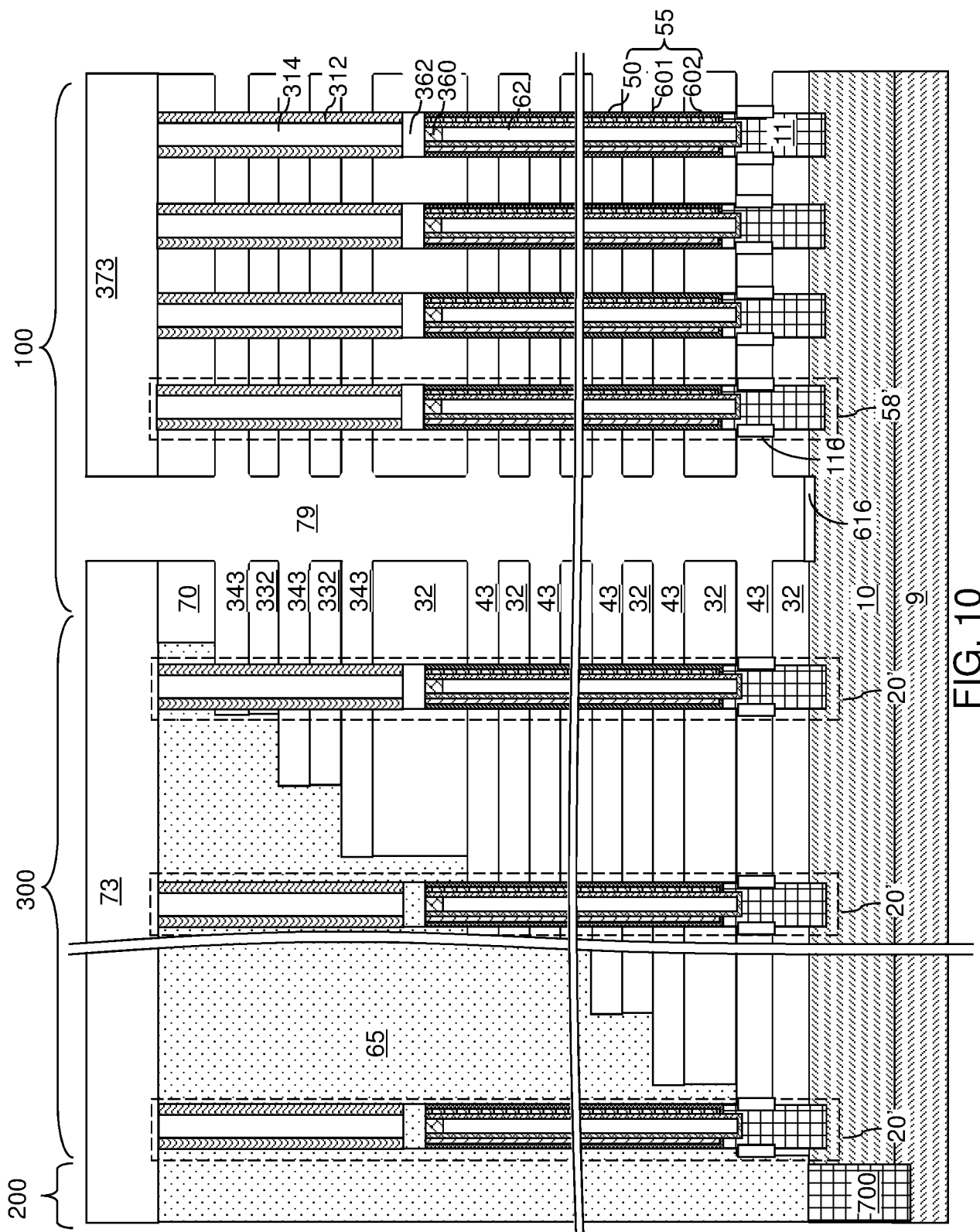


FIG. 8B





17/63



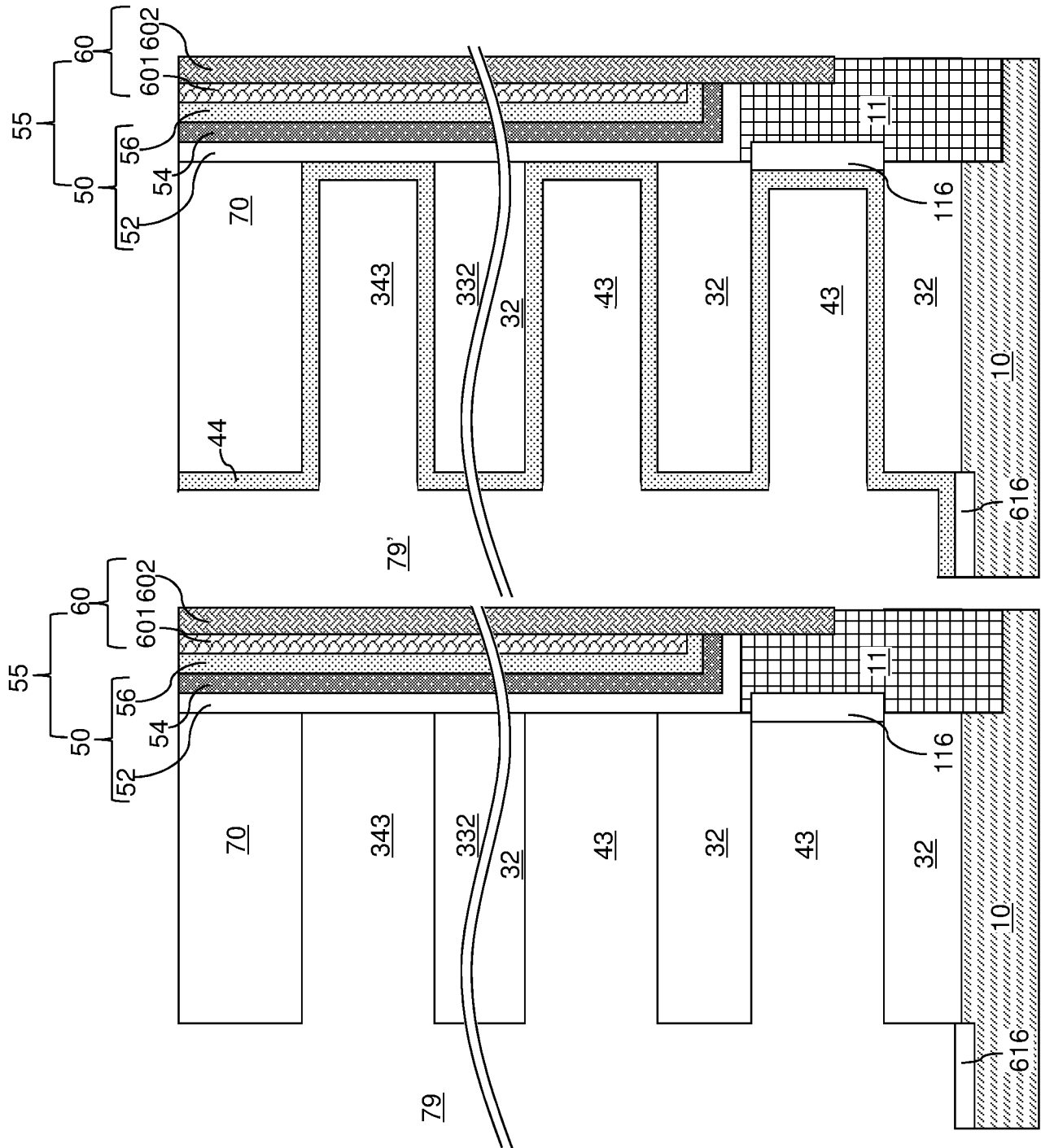
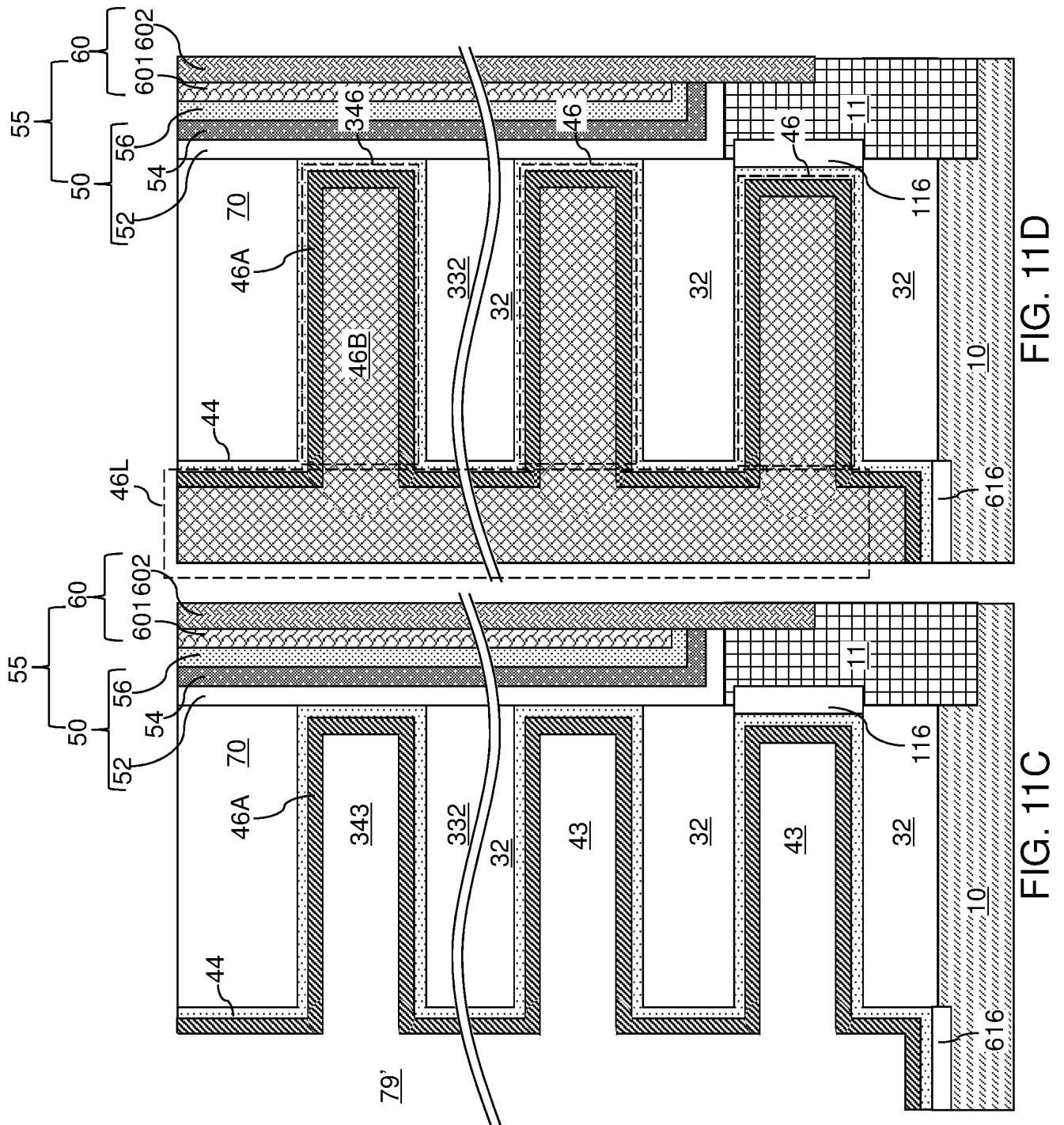


FIG. 11B

FIG. 11A



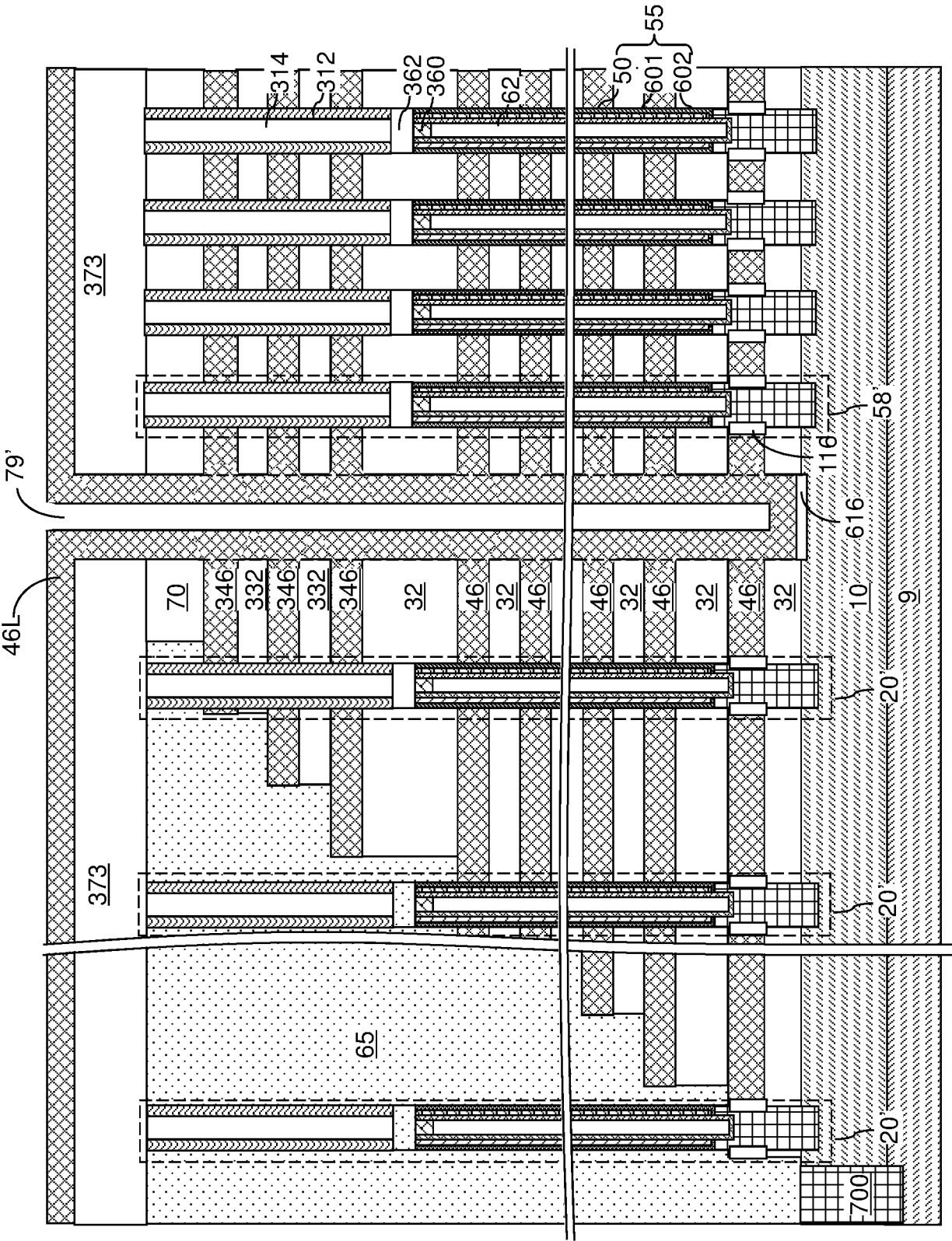


FIG. 12

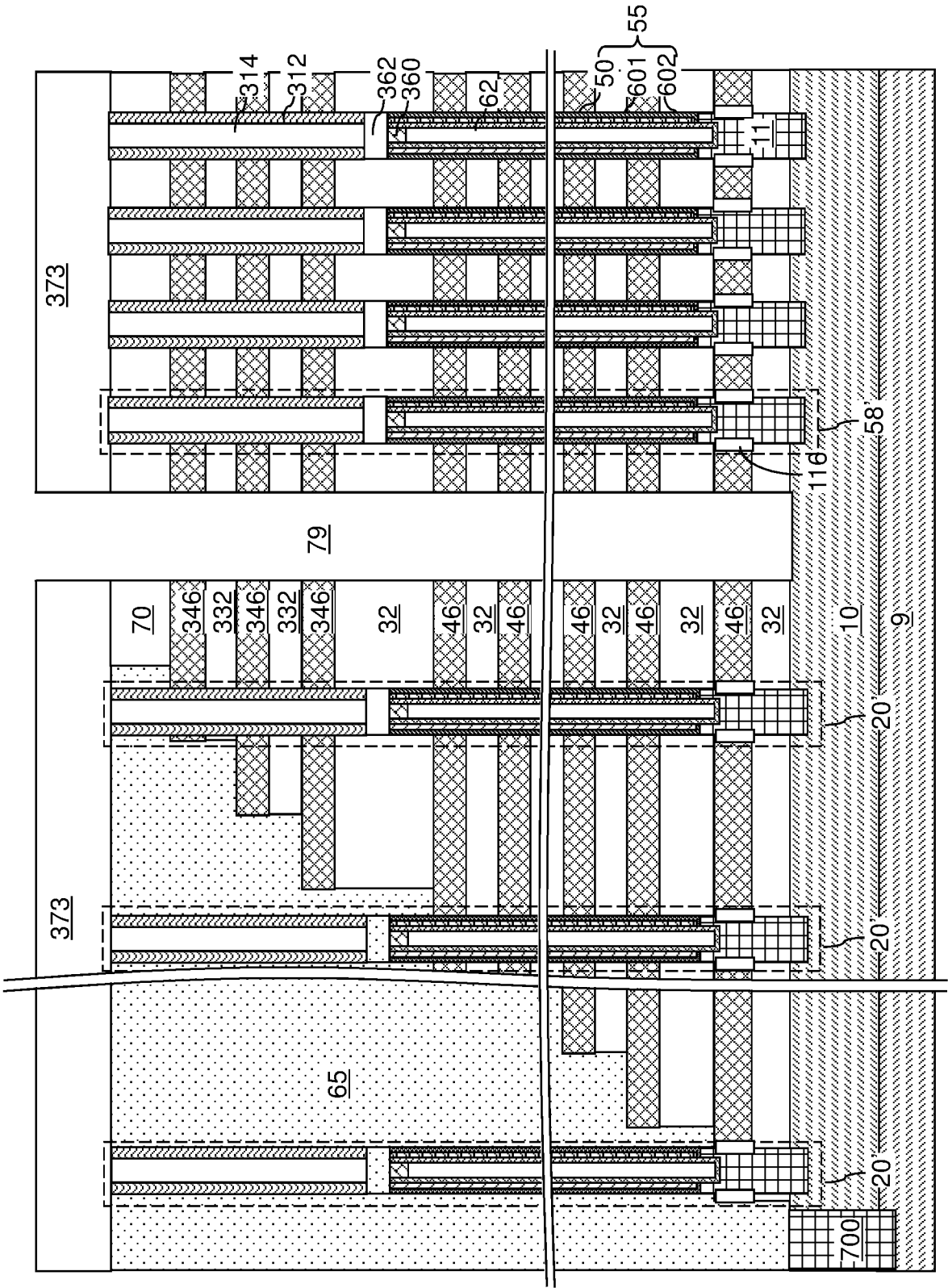


FIG. 13

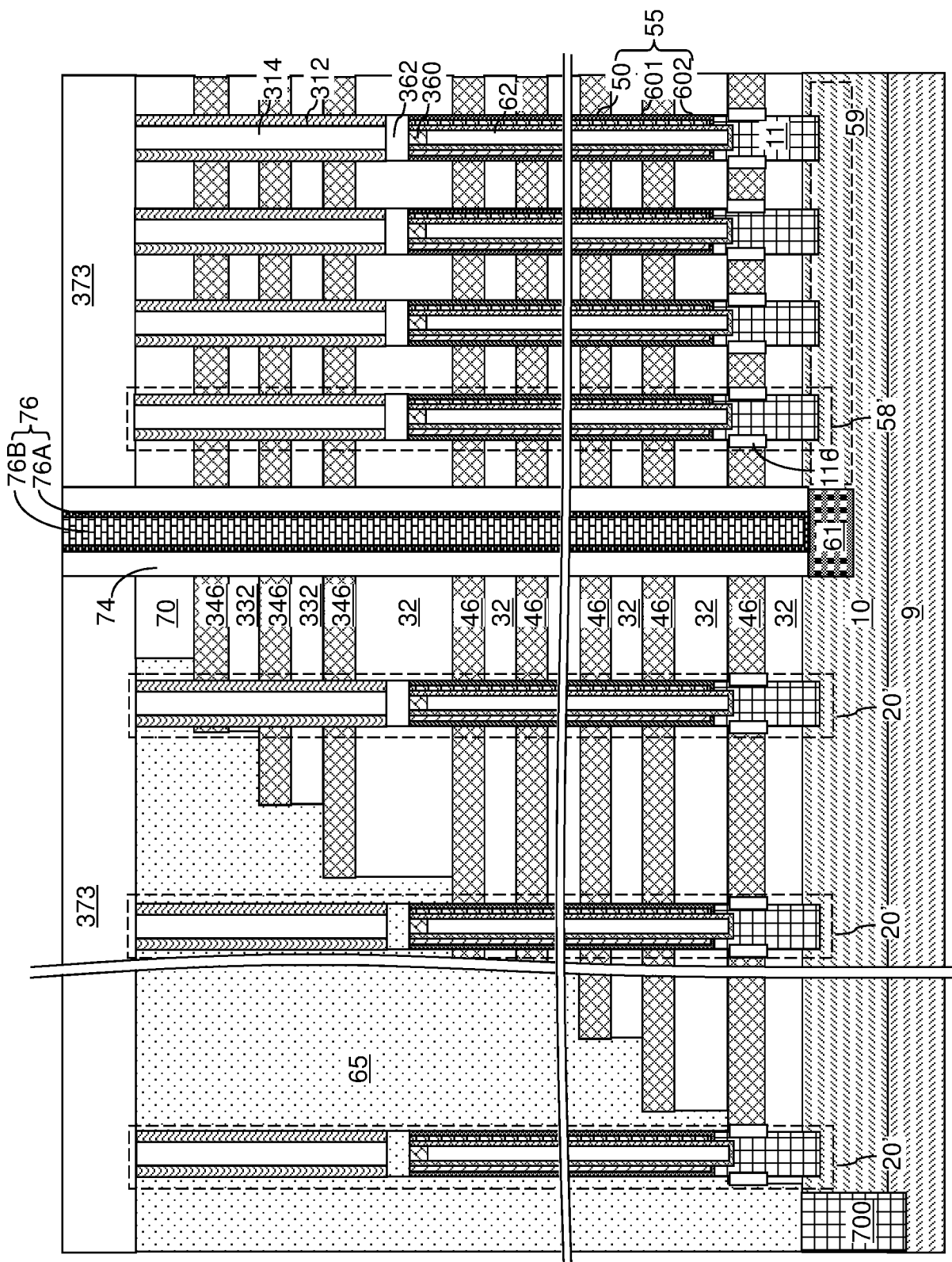


FIG. 14A

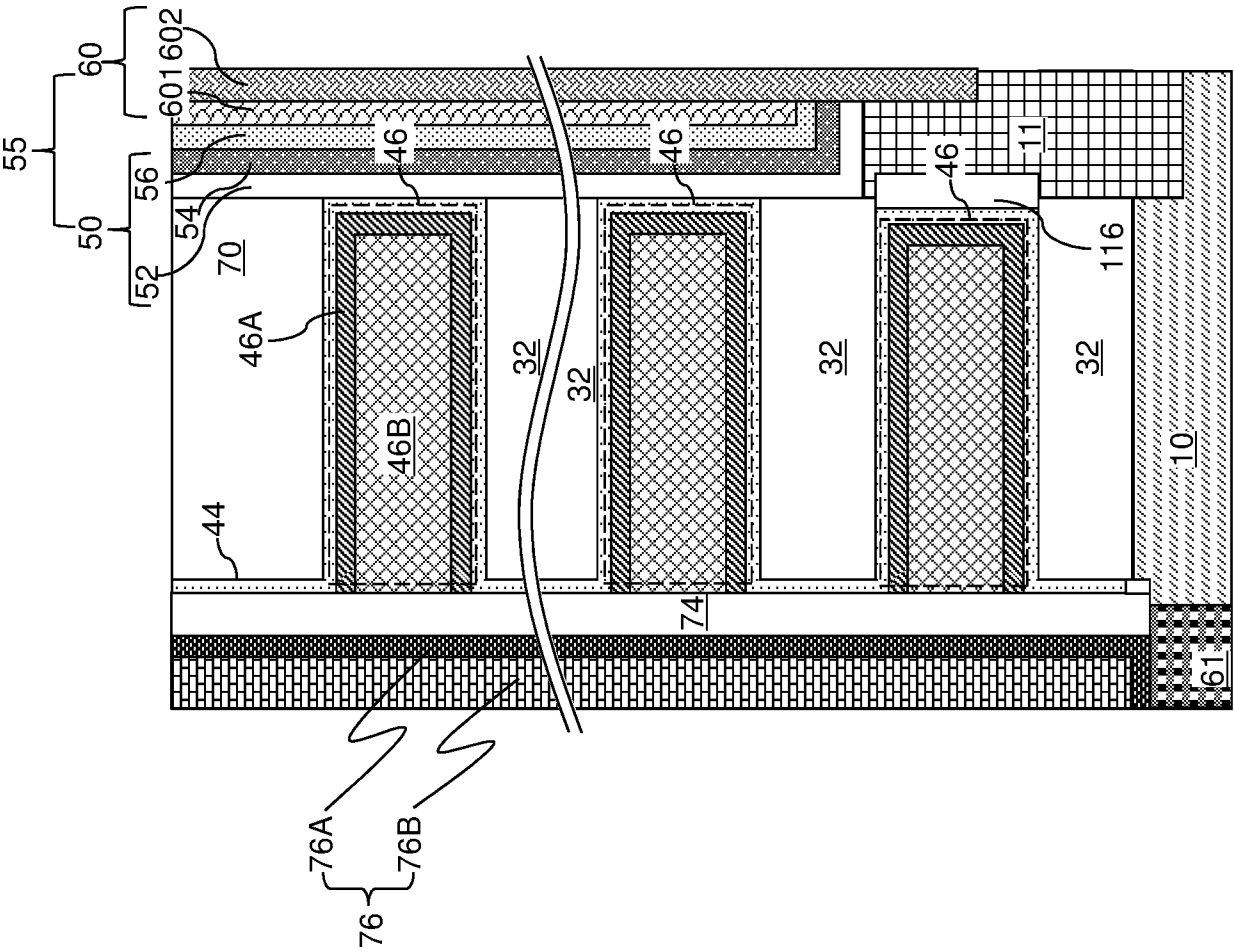


FIG. 14B

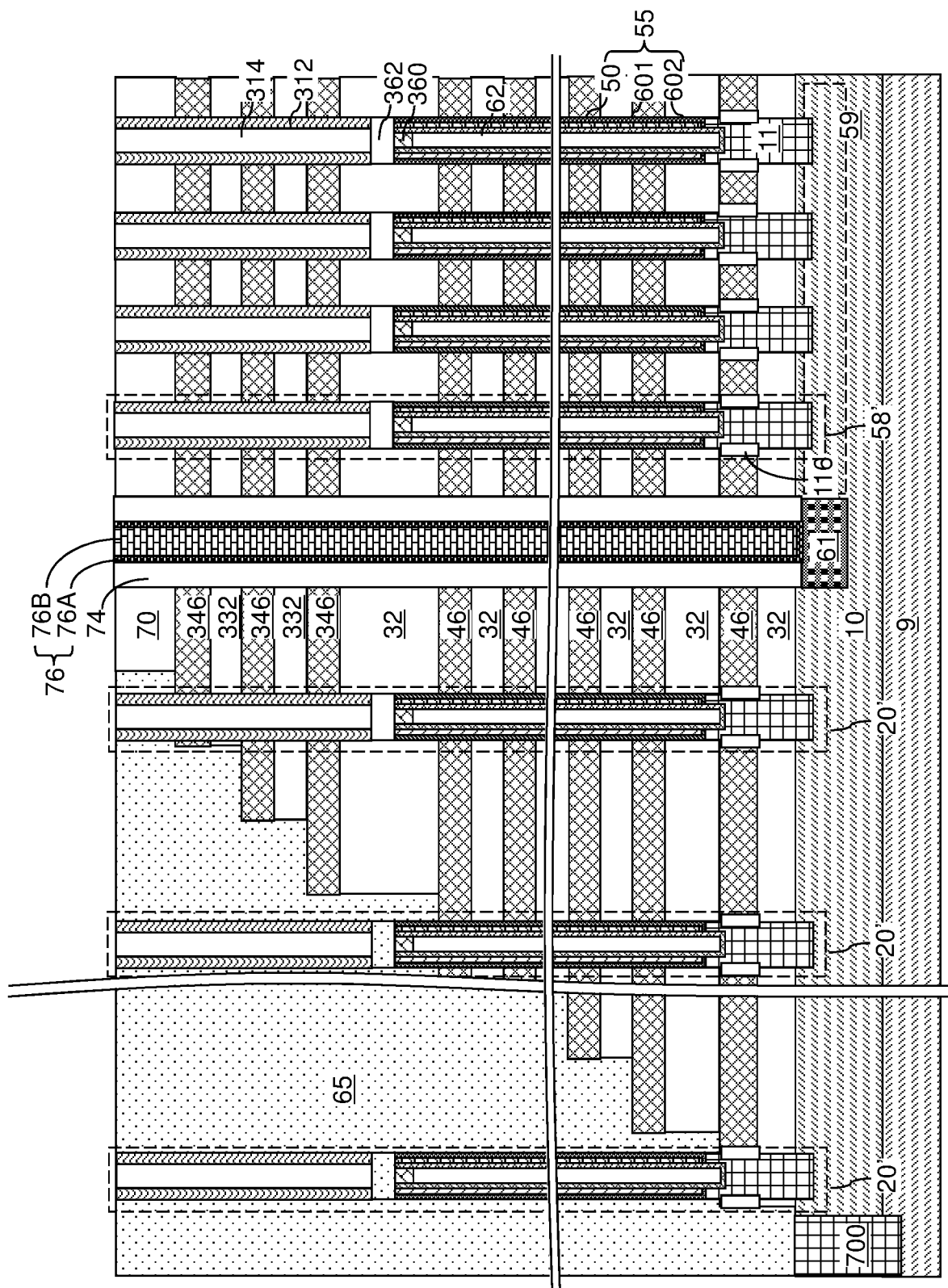


FIG. 15

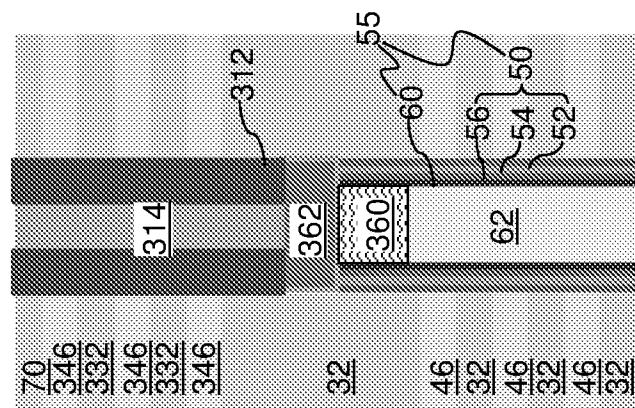


FIG. 16A

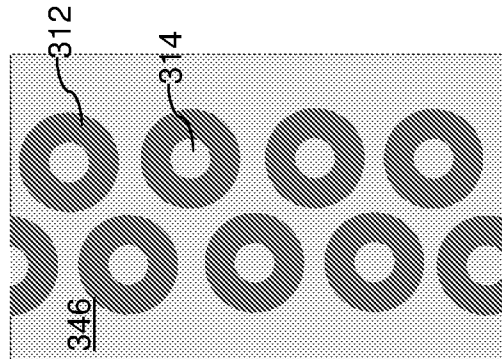


FIG. 16B

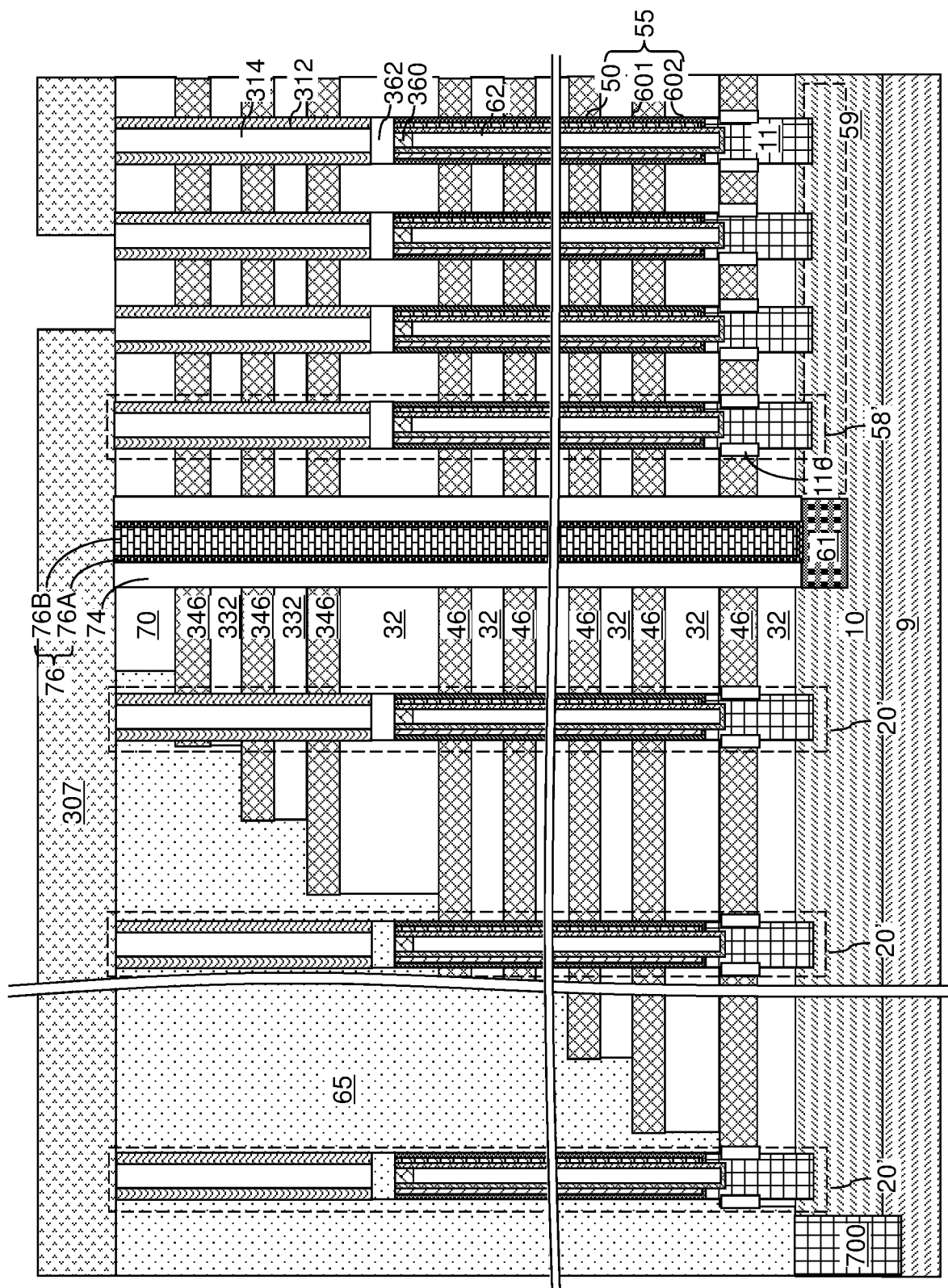


FIG. 17A

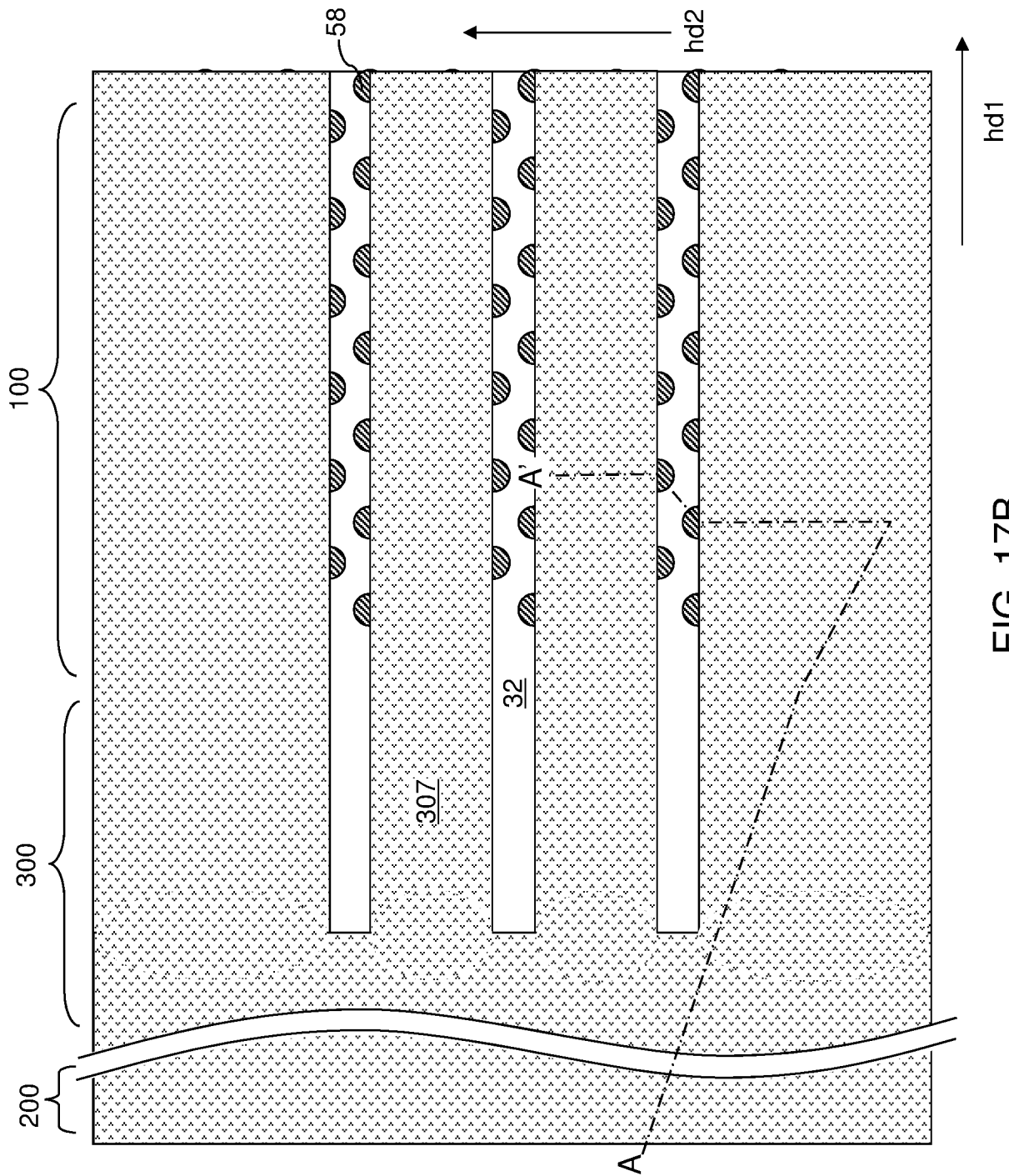


FIG. 17B

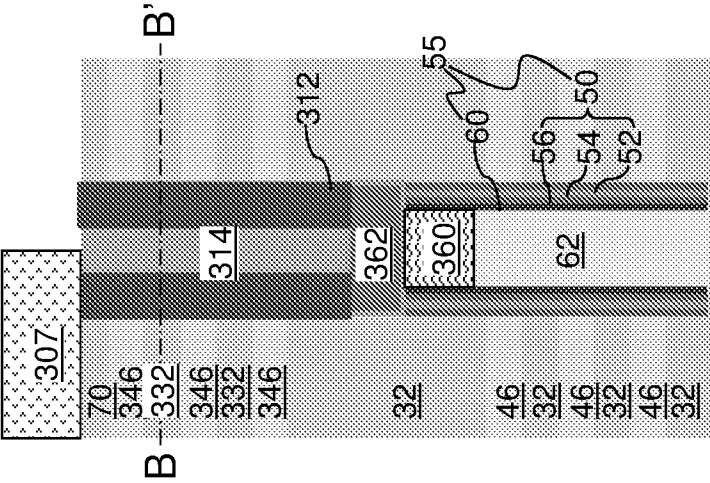


FIG. 18A

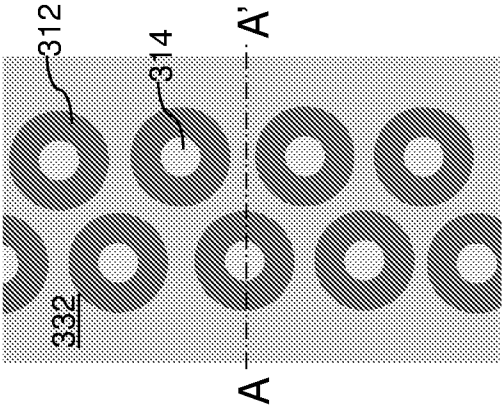


FIG. 18B

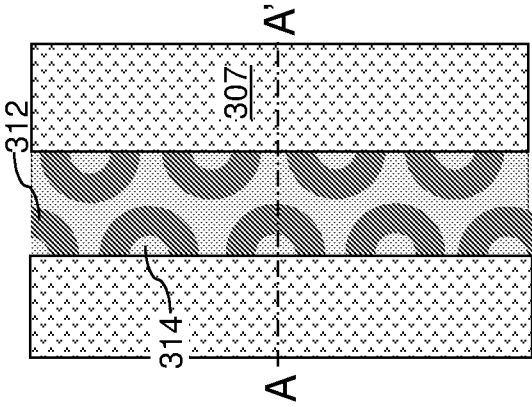


FIG. 18C

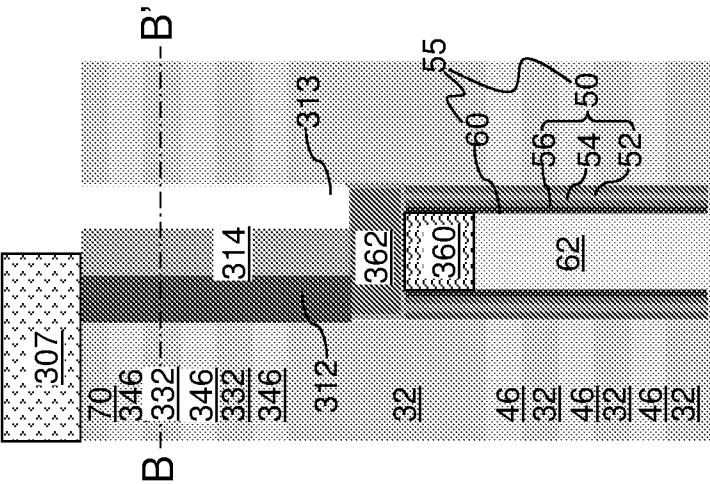


FIG. 19A

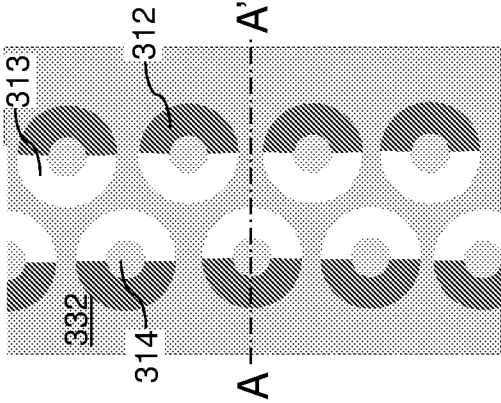


FIG. 19B

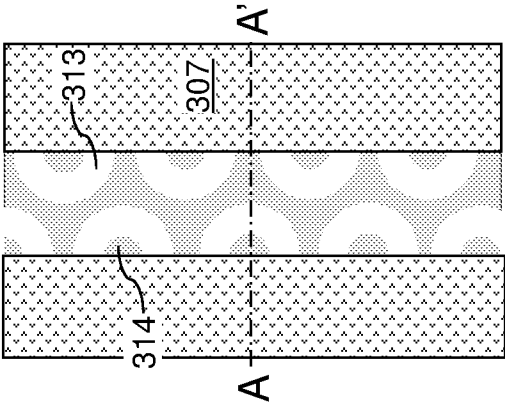


FIG. 19C

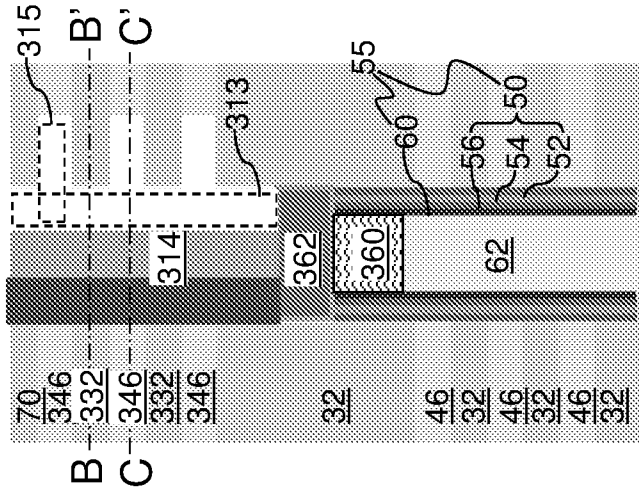


FIG. 20A

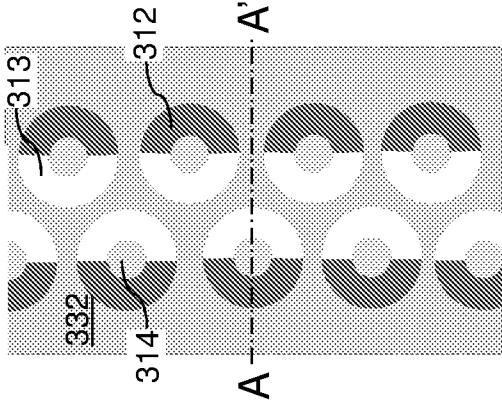


FIG. 20B

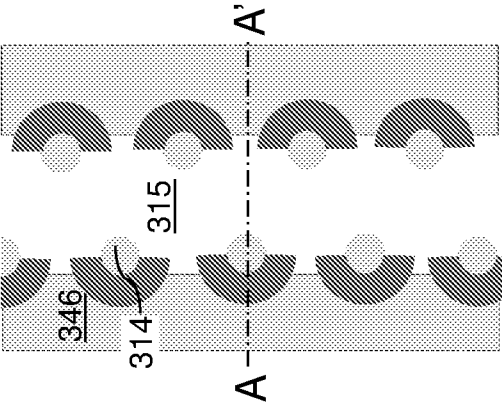


FIG. 20C

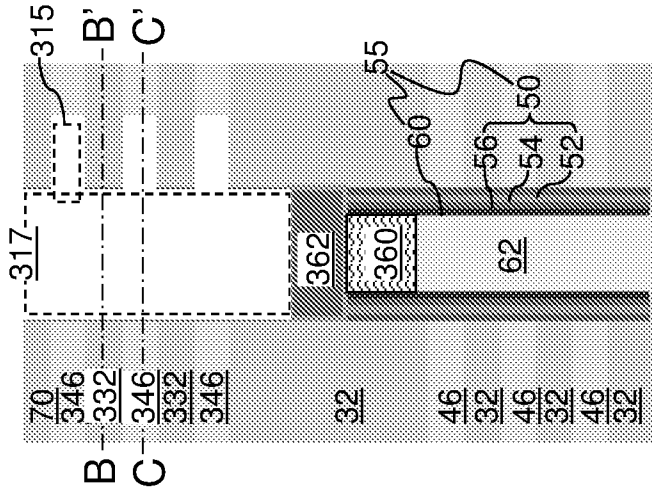


FIG. 21A

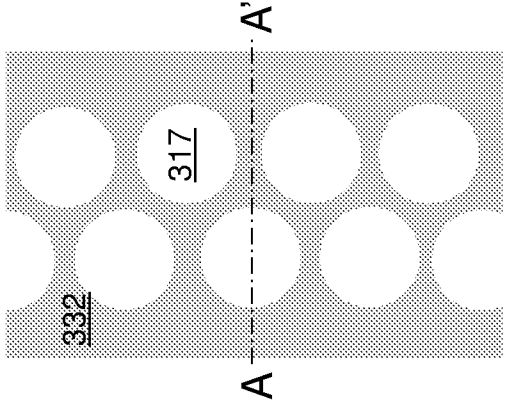


FIG. 21B

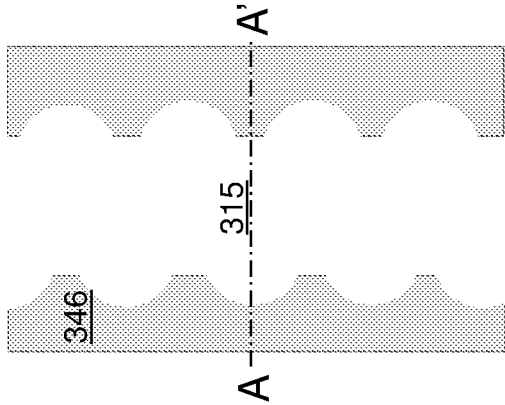


FIG. 21C

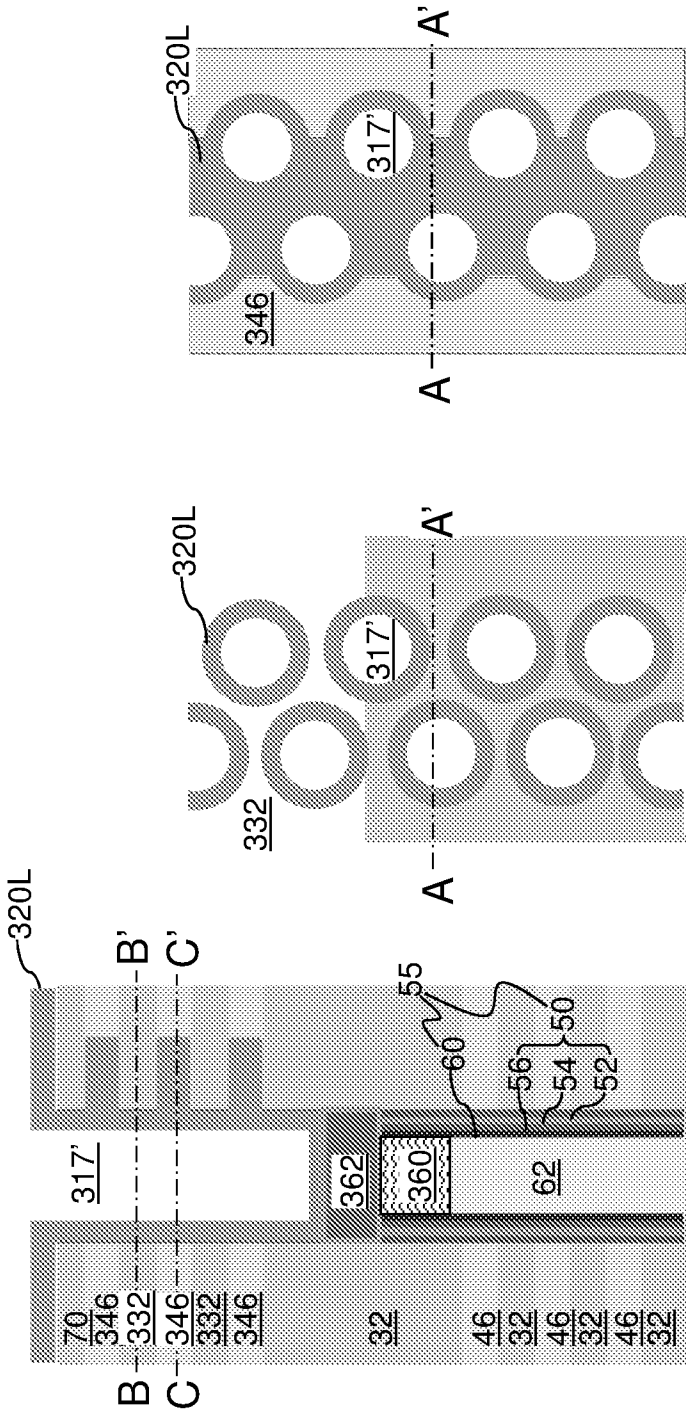


FIG. 22A

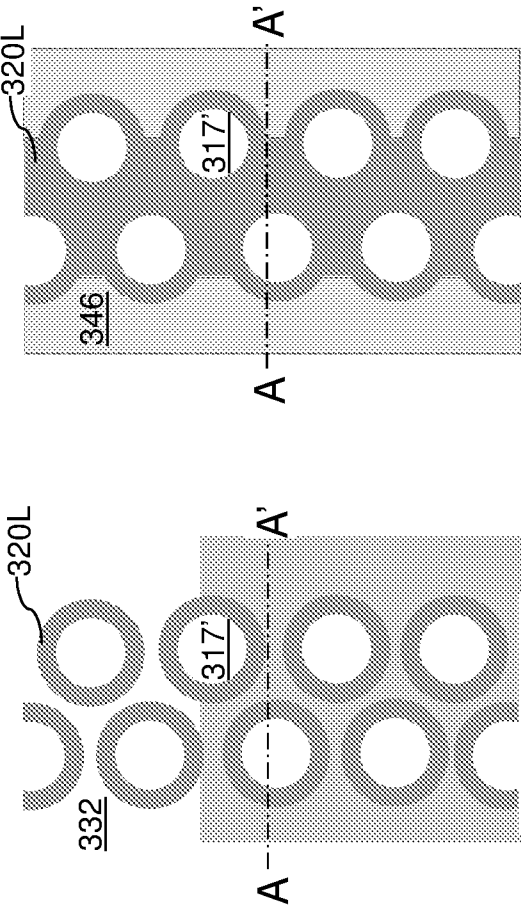


FIG. 22B

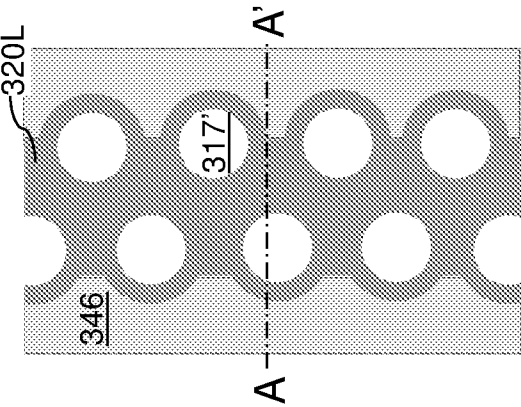


FIG. 22C

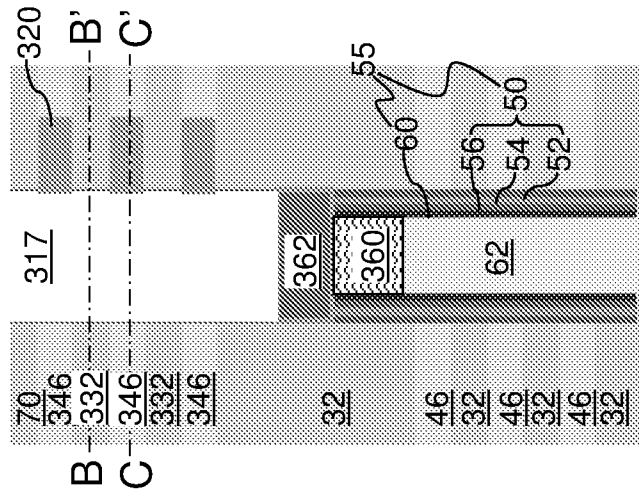


FIG. 23A

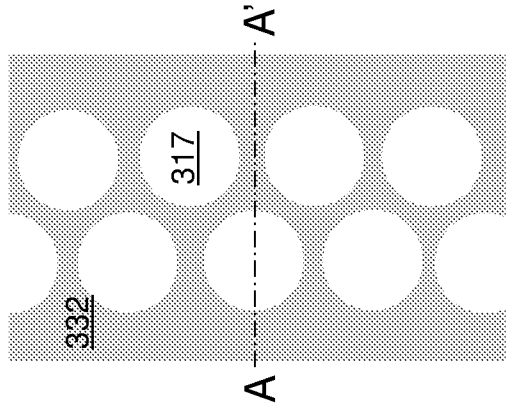


FIG. 23B

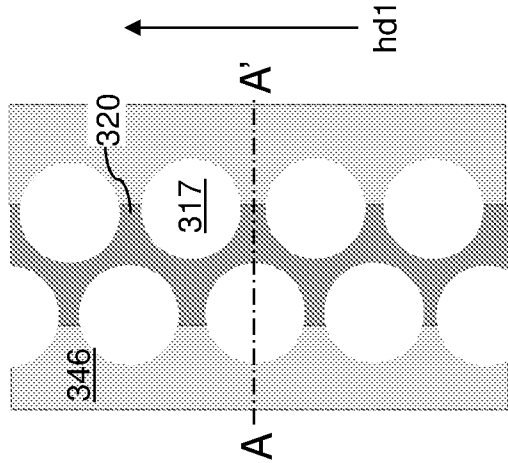


FIG. 23C

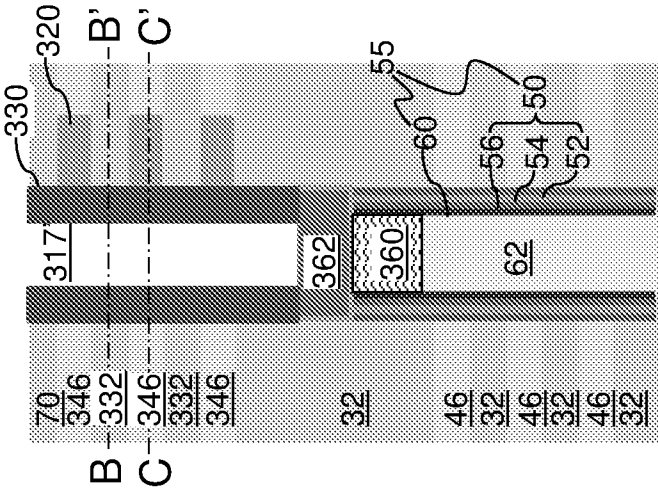


FIG. 24A

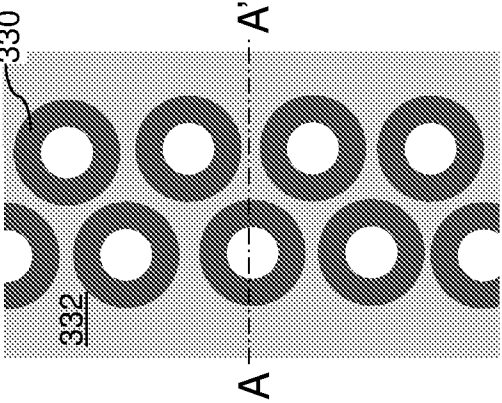


FIG. 24B

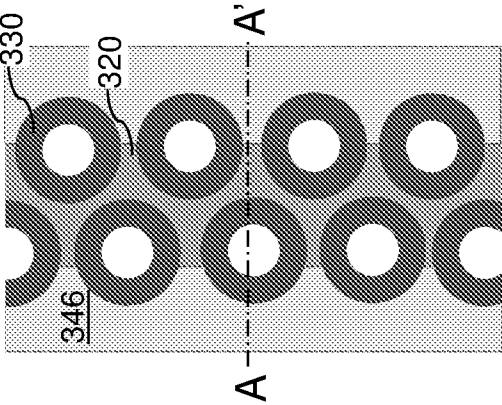


FIG. 24C

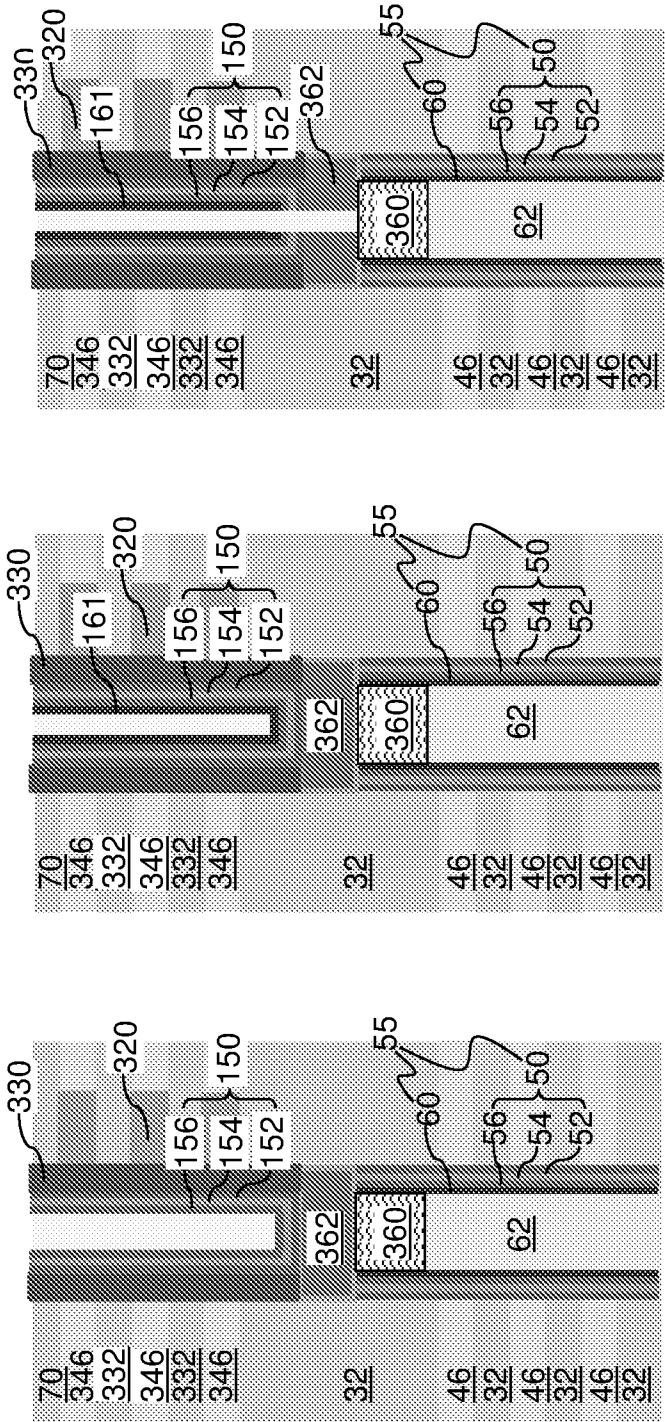


FIG. 25C

FIG. 25B

FIG. 25A

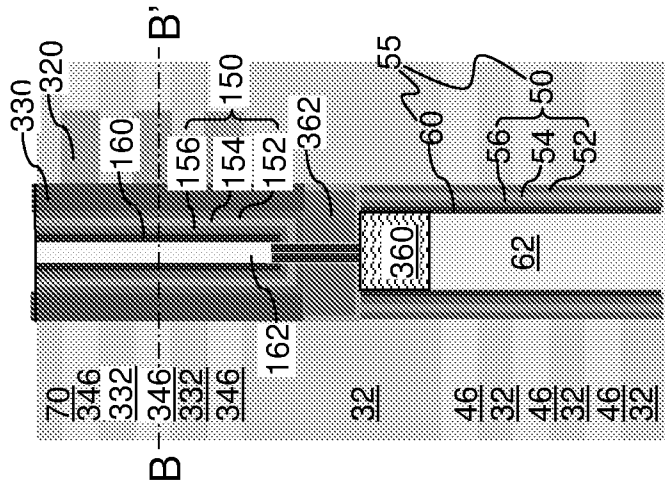


FIG. 26A

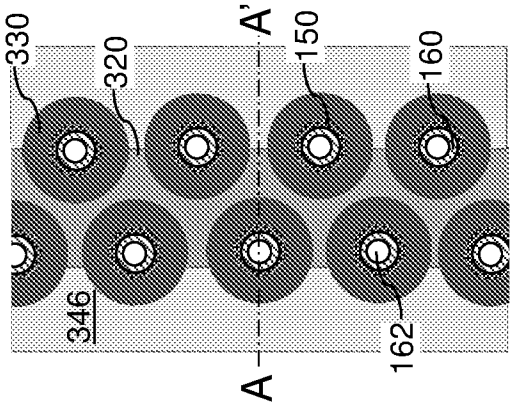


FIG. 26B

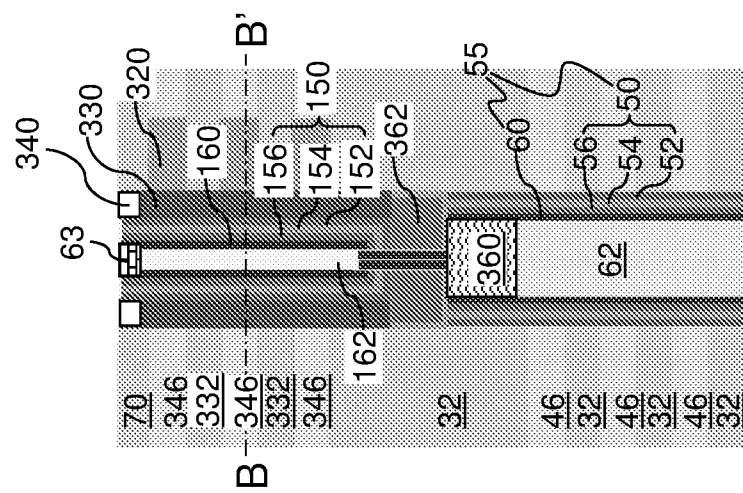


FIG. 27A

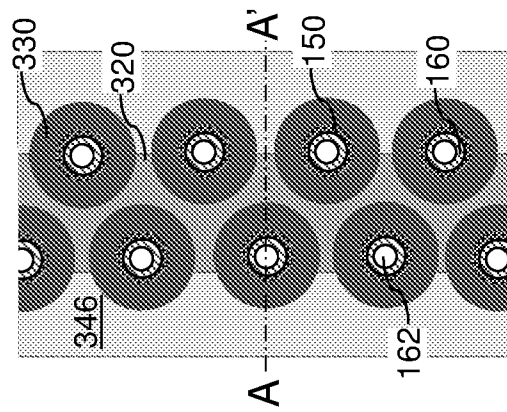


FIG. 27B

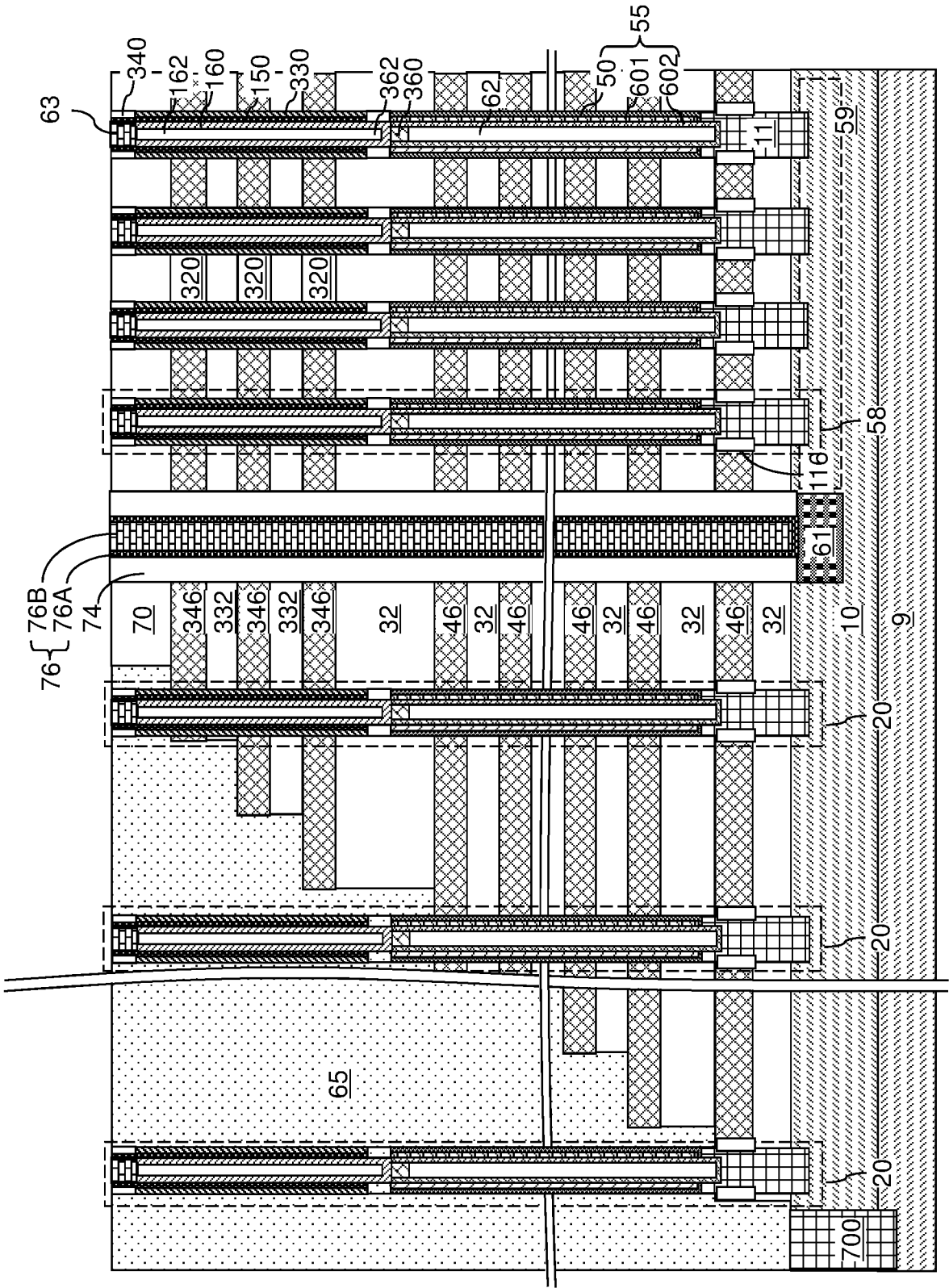


FIG. 28A

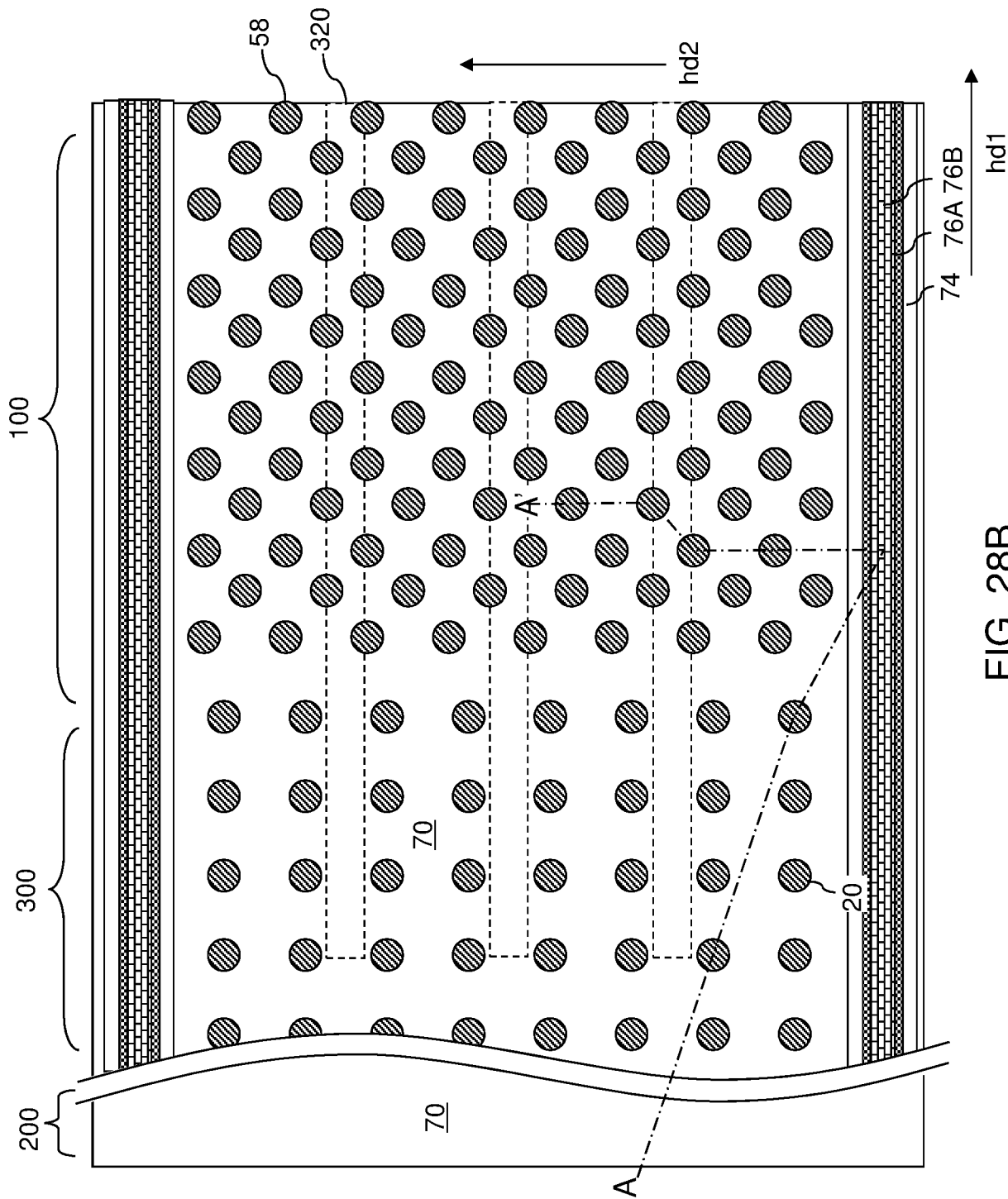


FIG. 28B

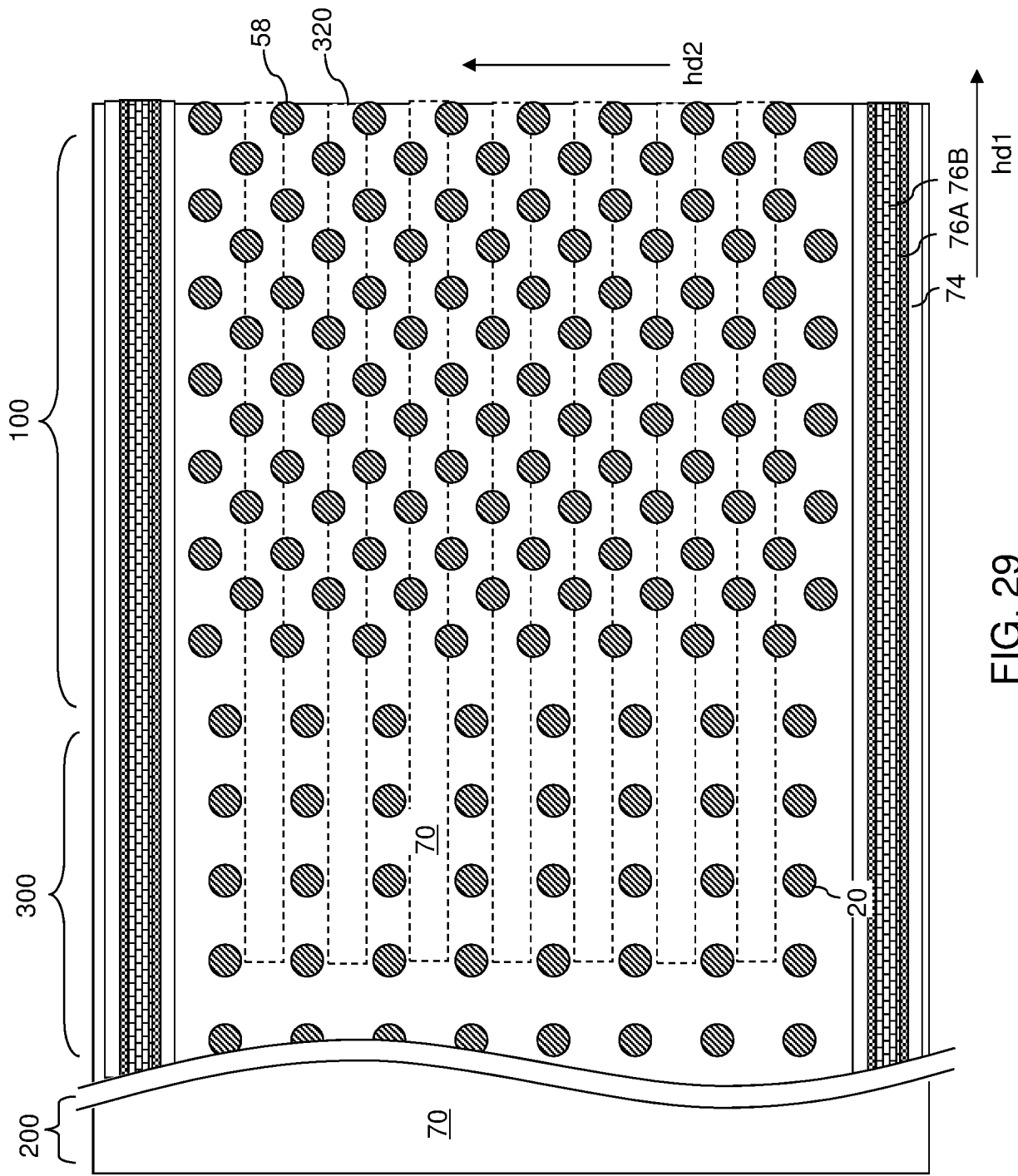


FIG. 29

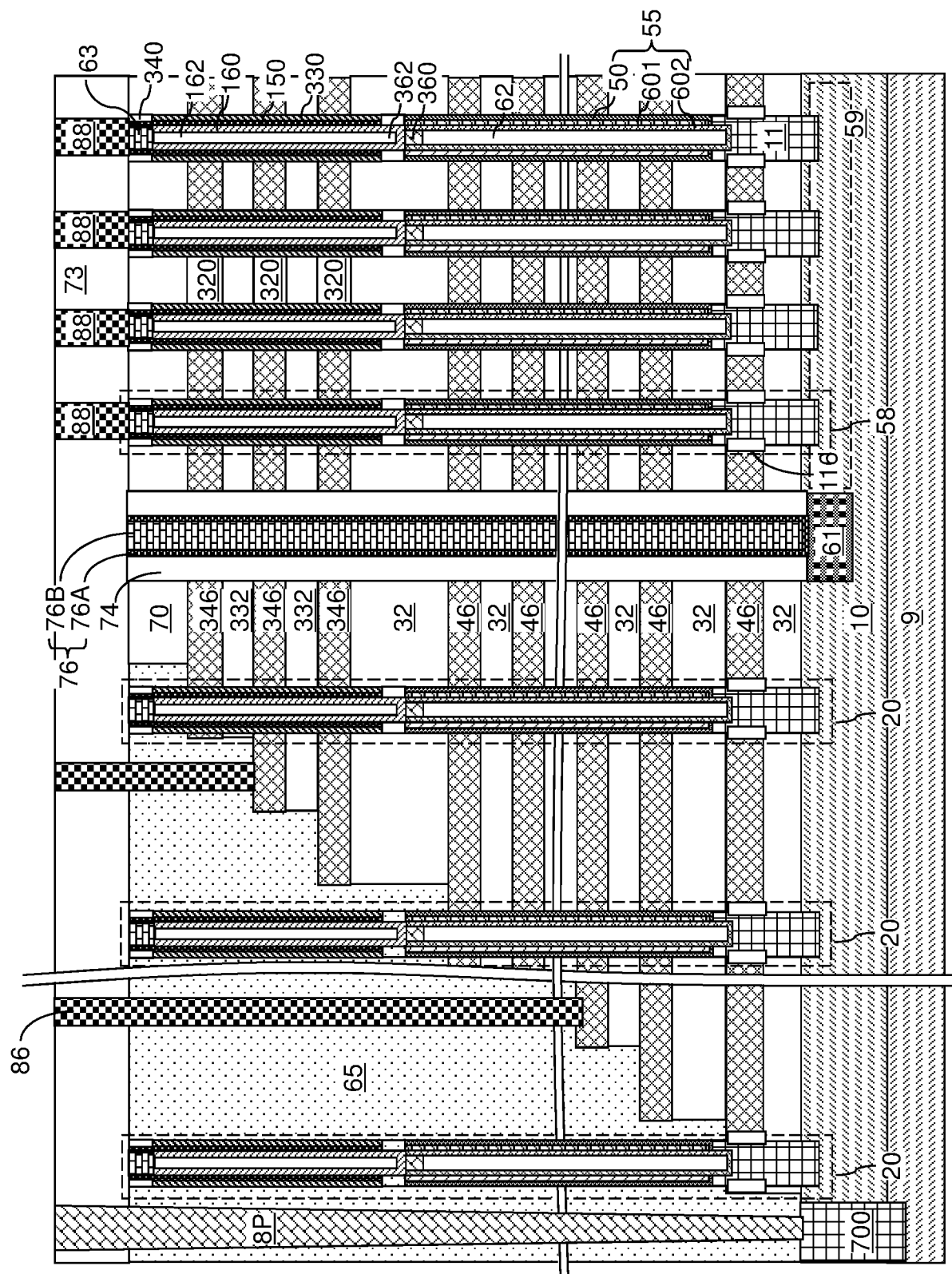


FIG. 30A

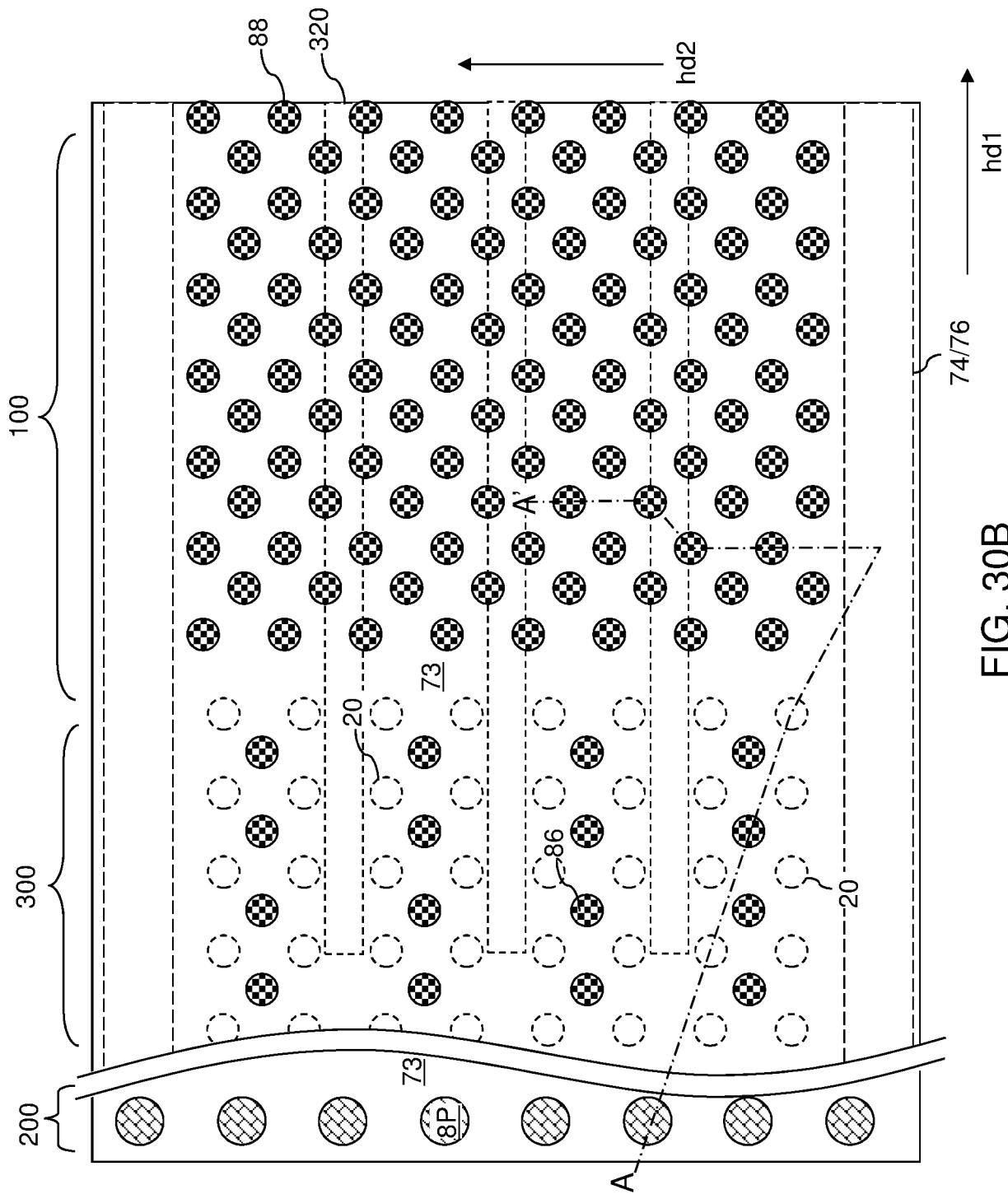


FIG. 30B

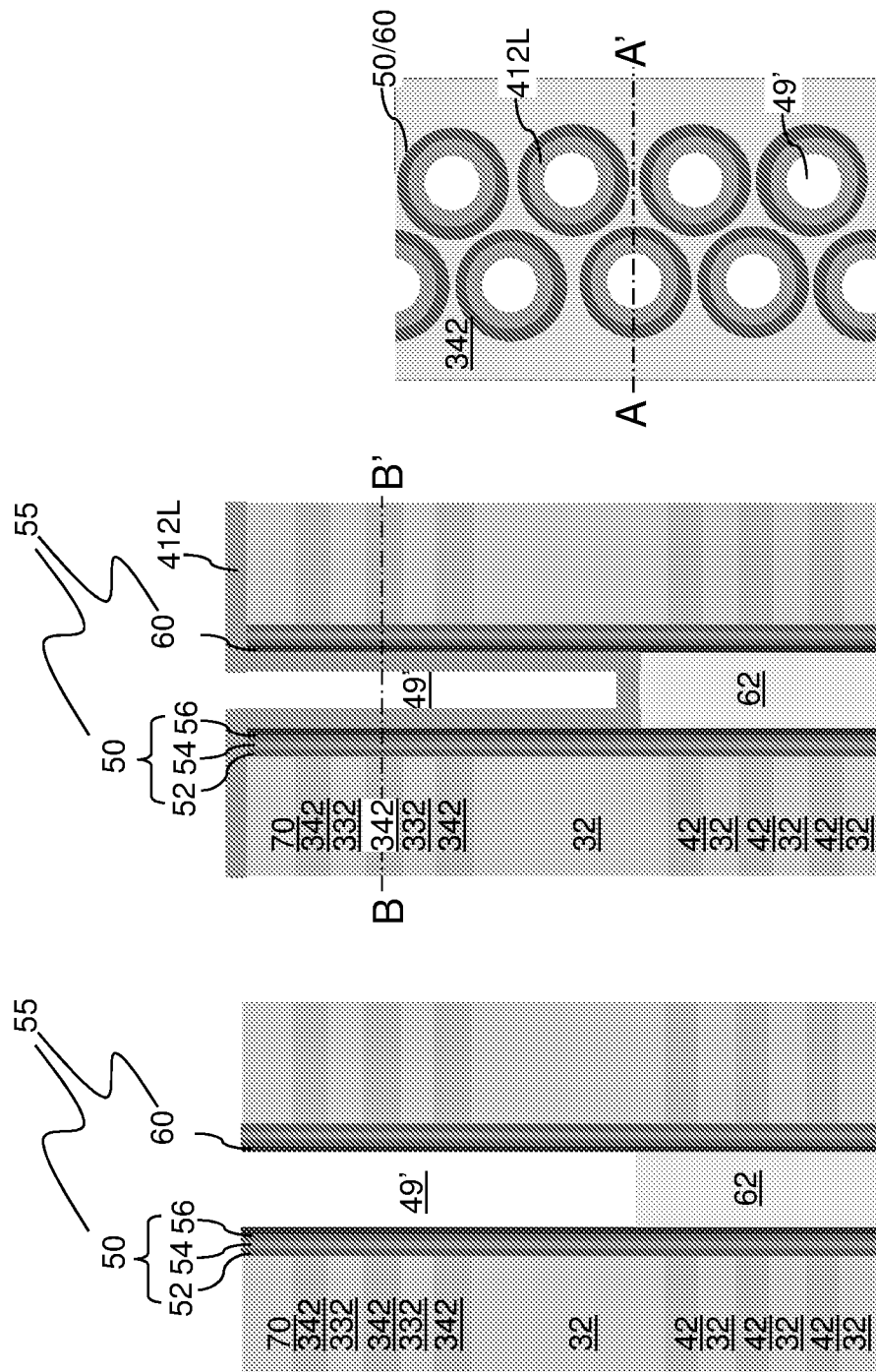


FIG. 32B

FIG. 32A

FIG. 31

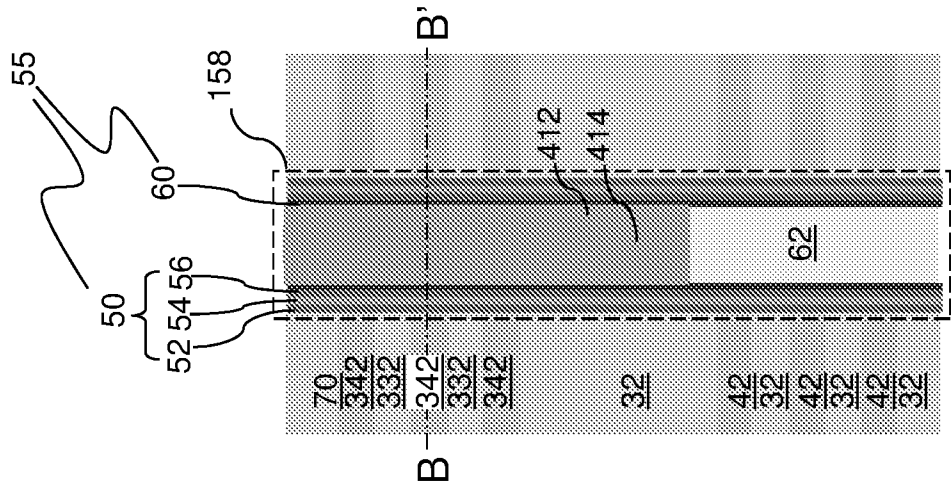


FIG. 33A

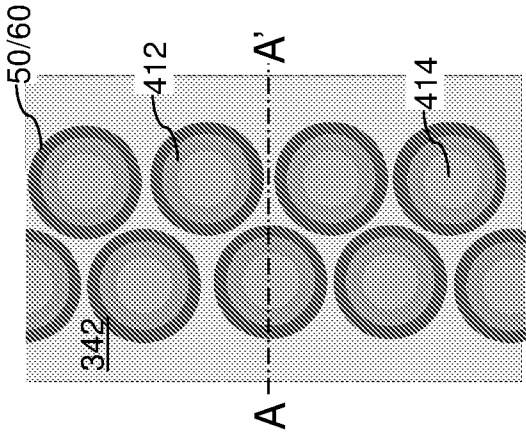


FIG. 33B

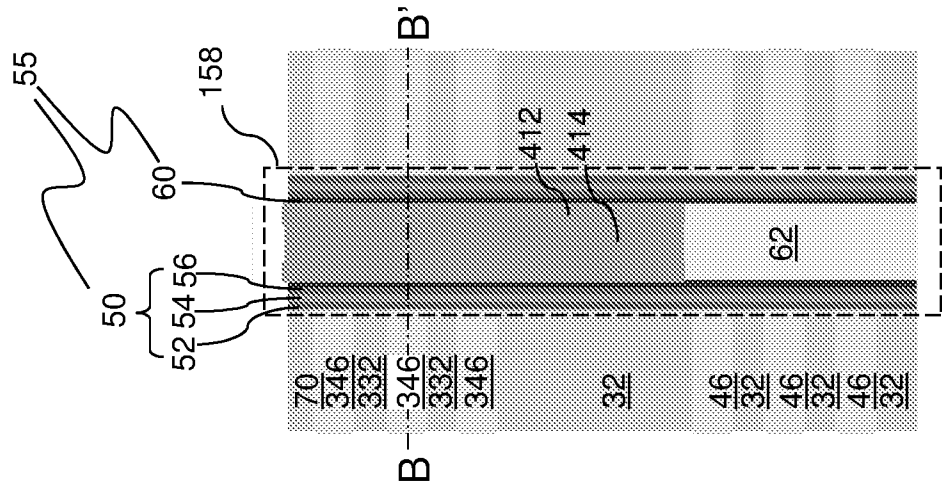


FIG. 34A

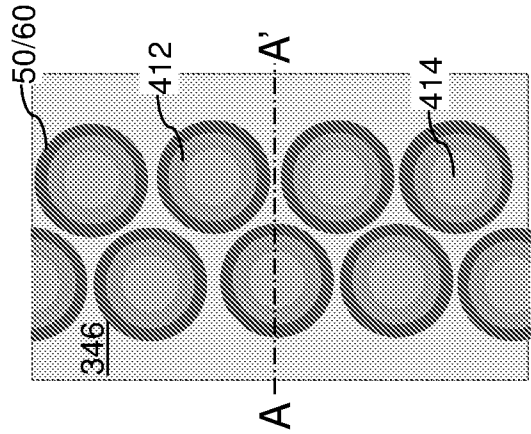


FIG. 34B

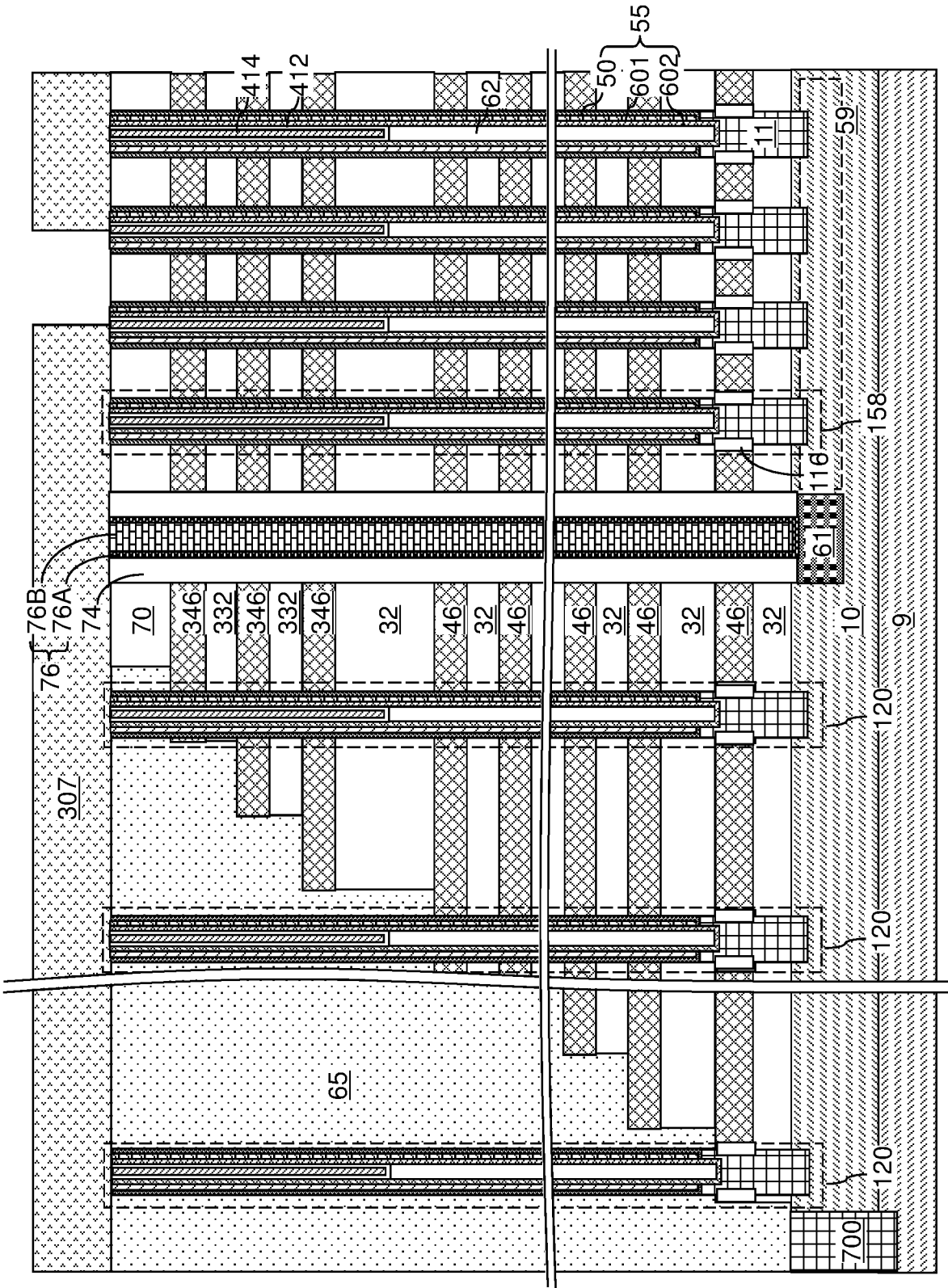


FIG. 35A

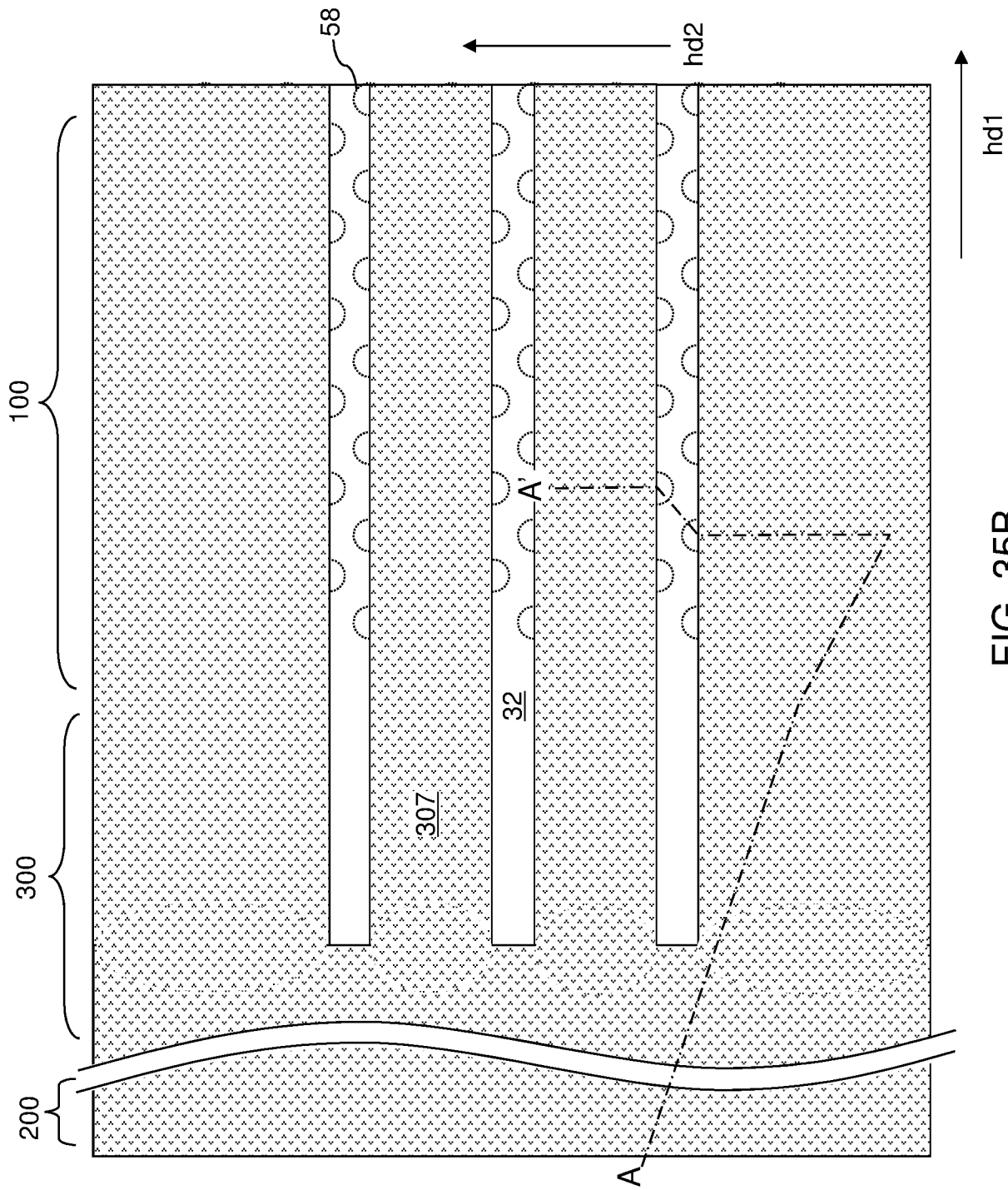


FIG. 35B

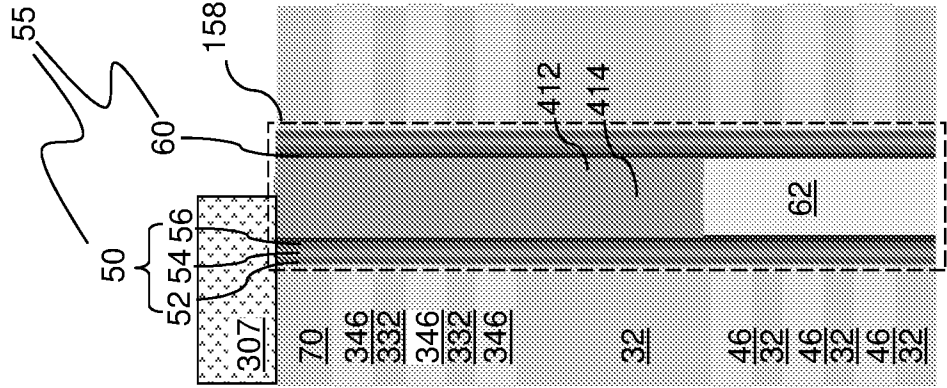


FIG. 36A

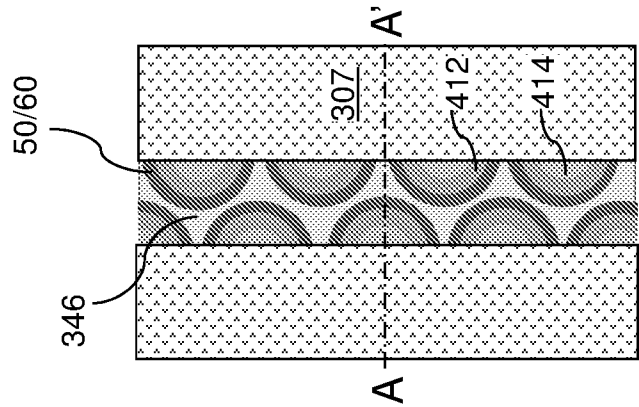


FIG. 36B

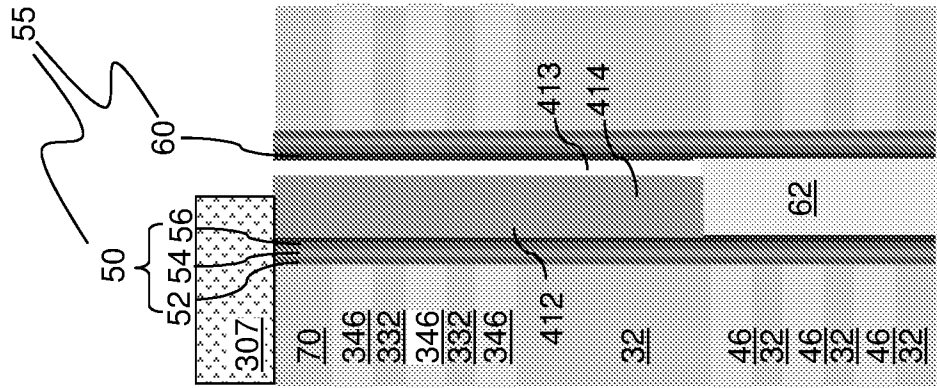


FIG. 37A

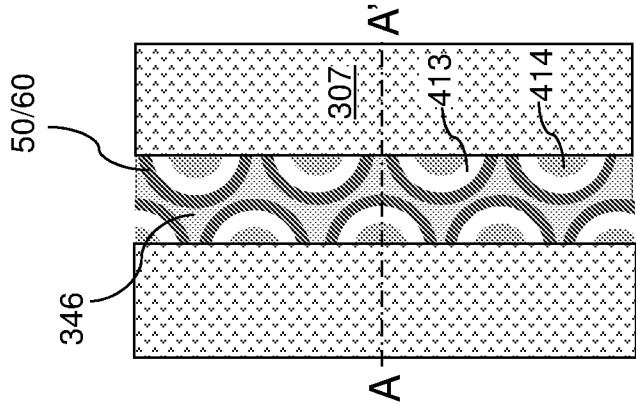


FIG. 37B

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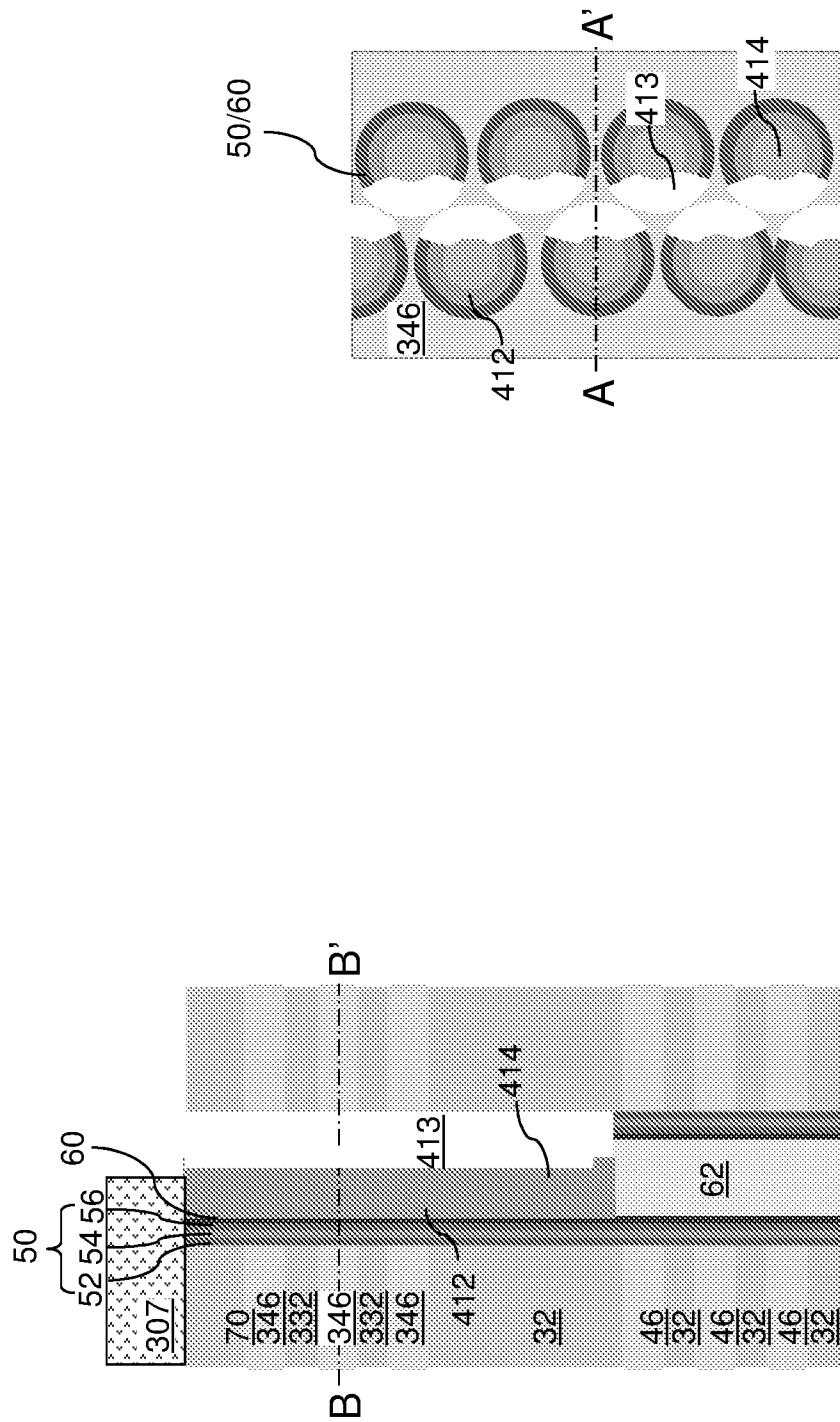


FIG. 38B

FIG. 38A

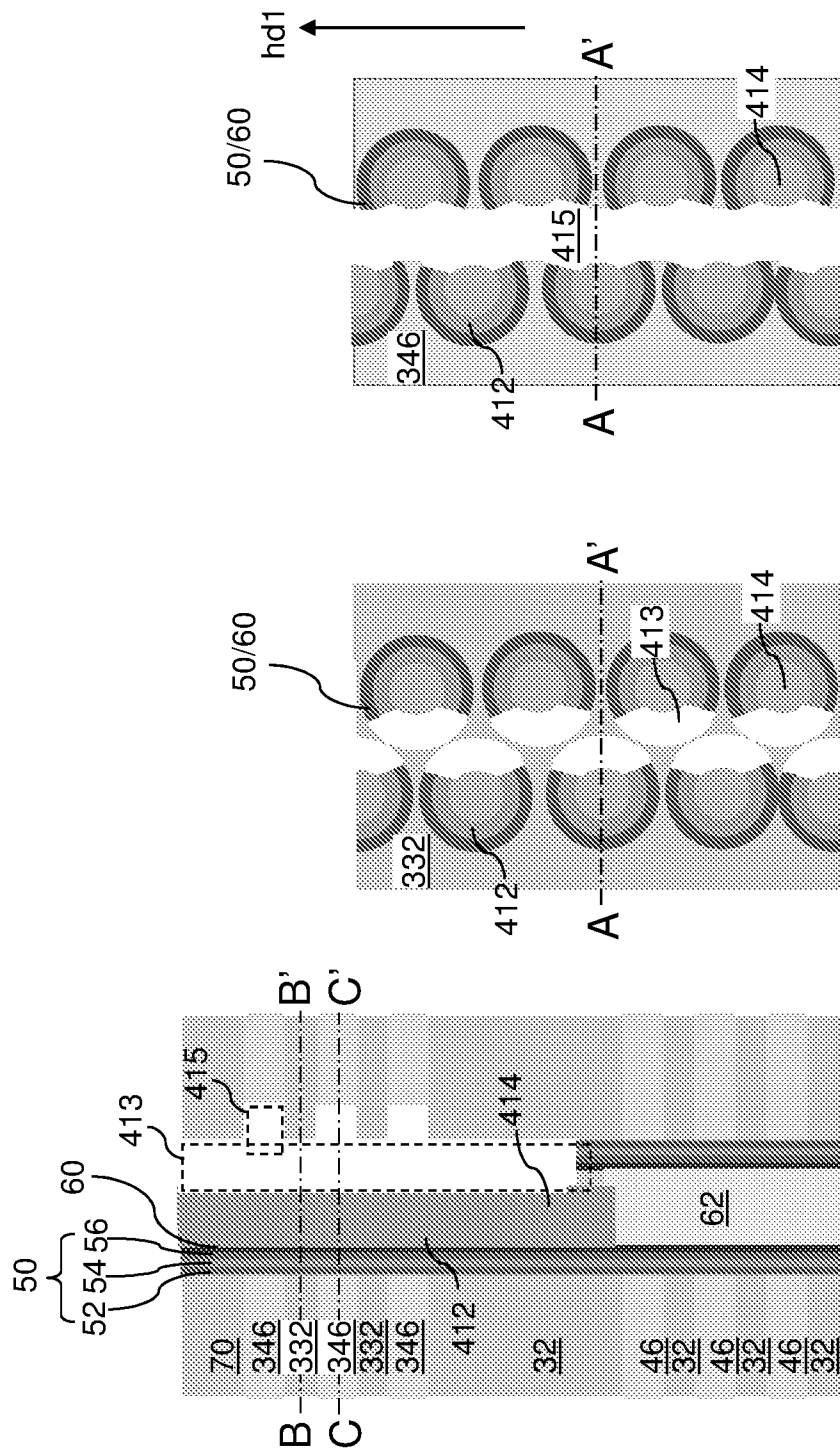


FIG. 39A

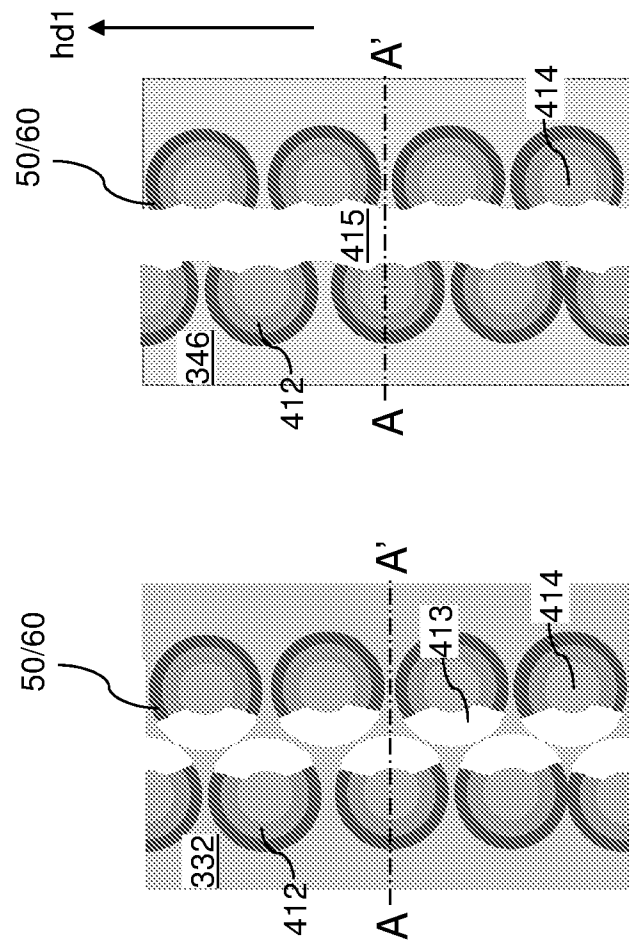


FIG. 39B

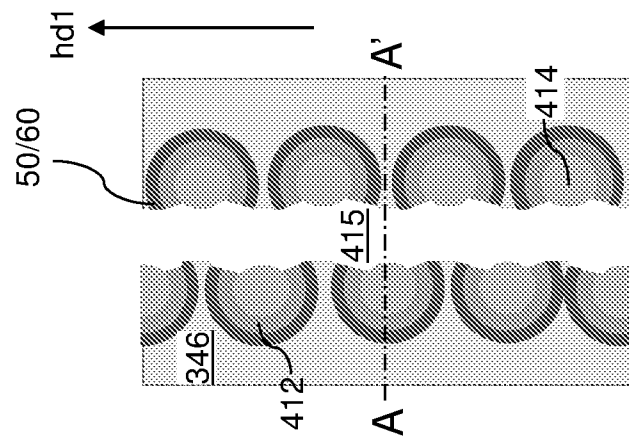


FIG. 39C

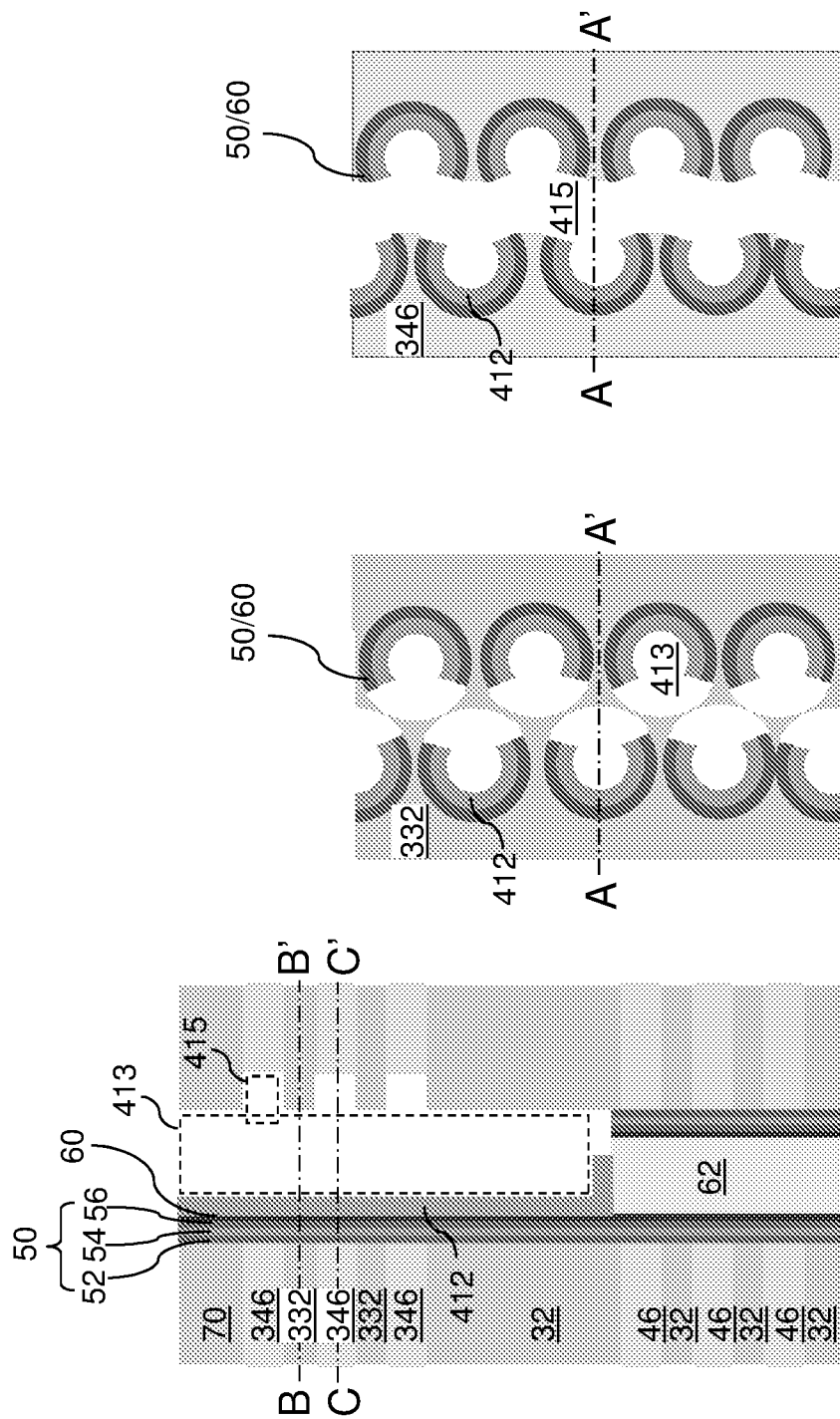


FIG. 40A

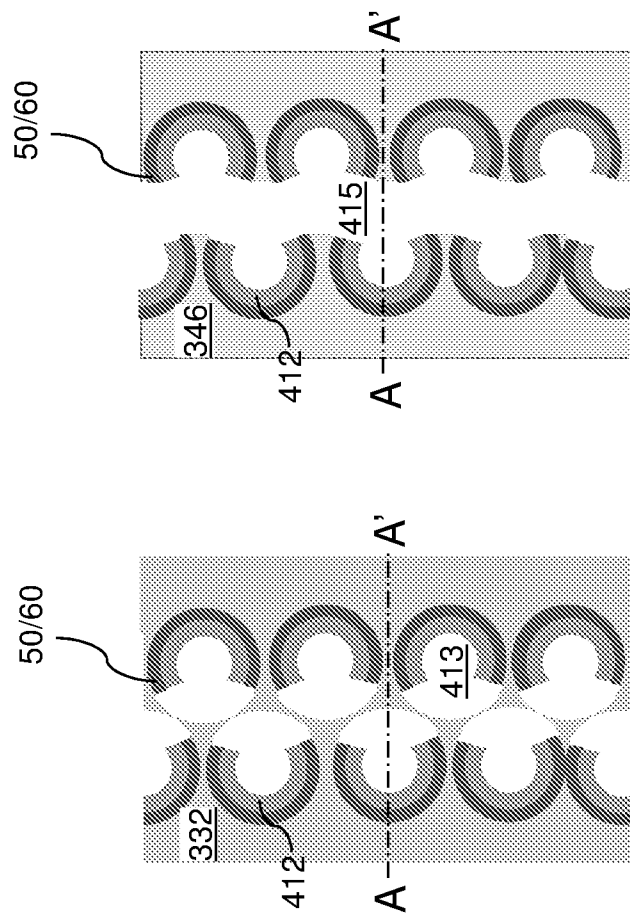


FIG. 40B

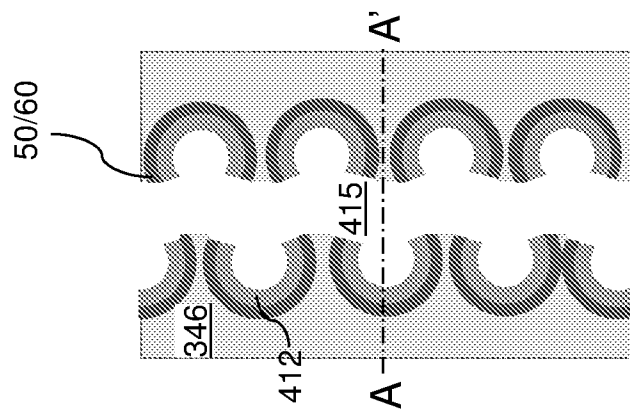


FIG. 40C

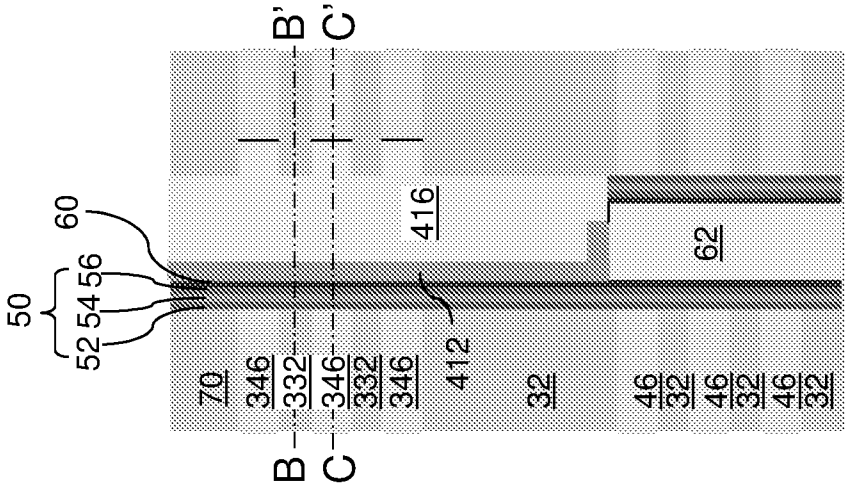


FIG. 41A

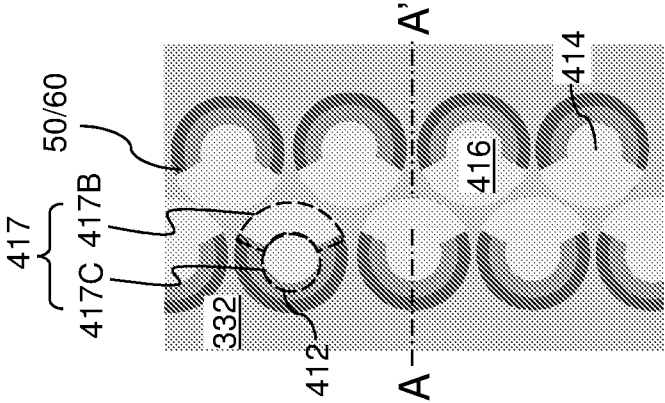


FIG. 41B

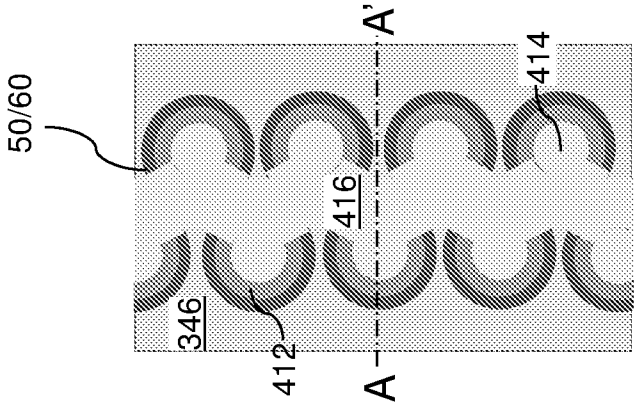


FIG. 41C

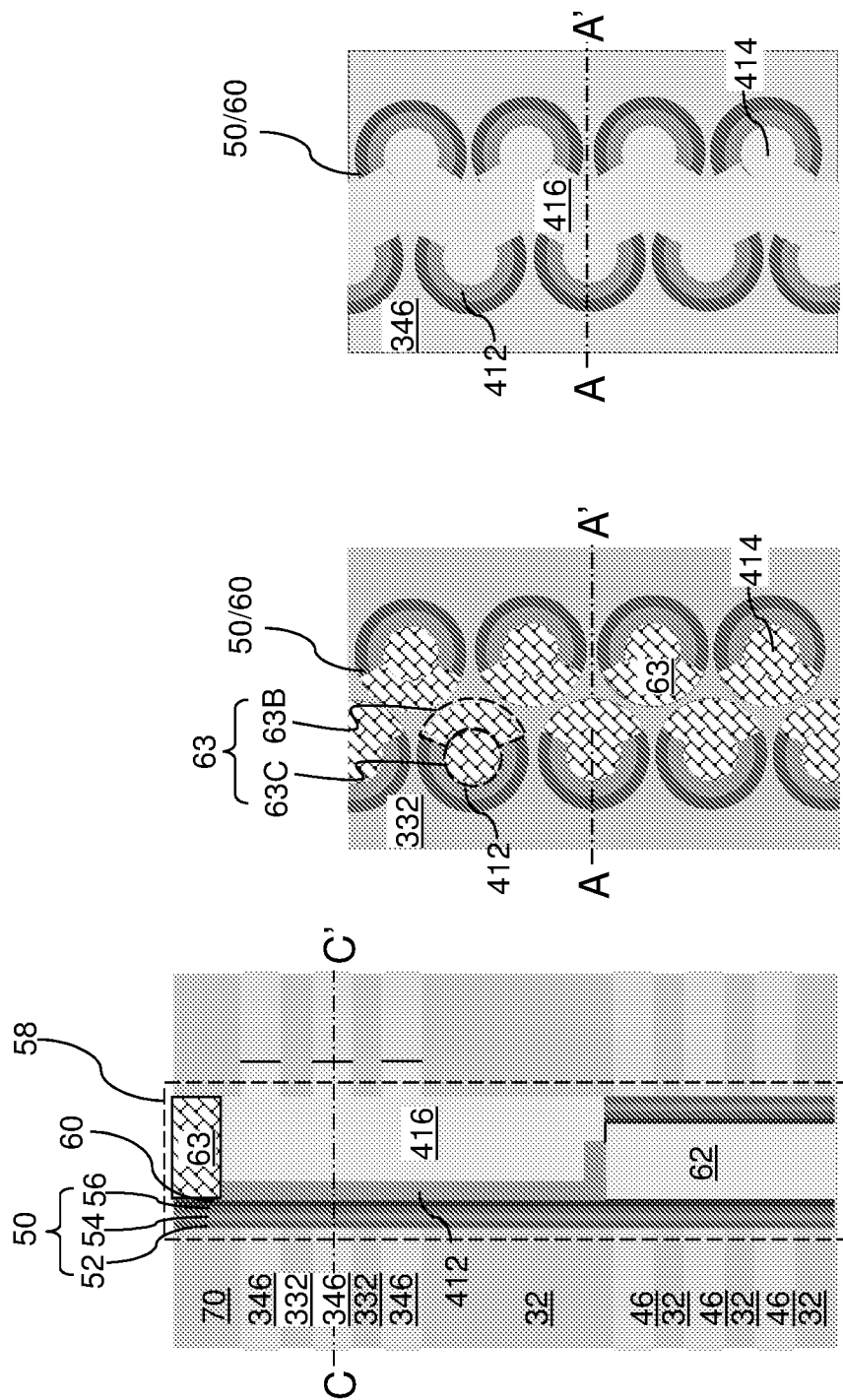


FIG. 42C

FIG. 42B

FIG. 42A

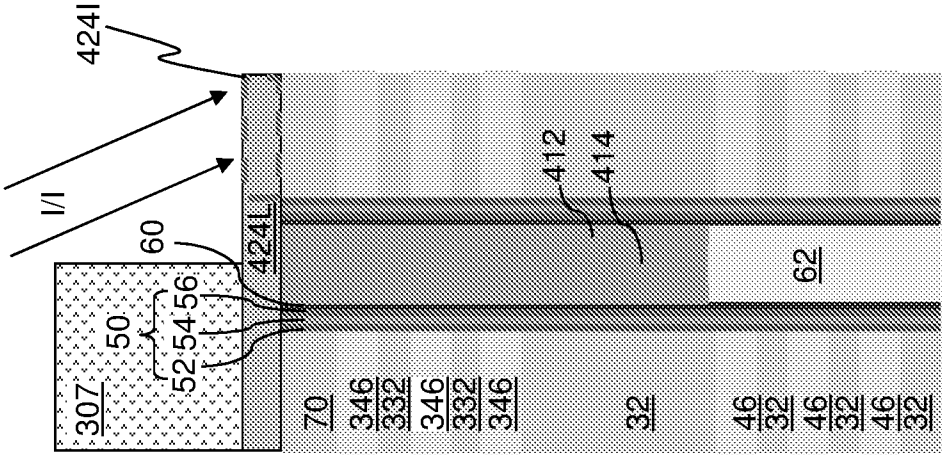


FIG. 43

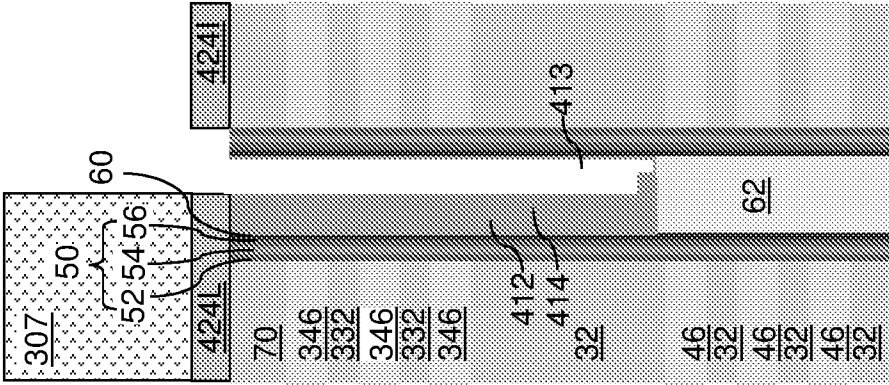


FIG. 44

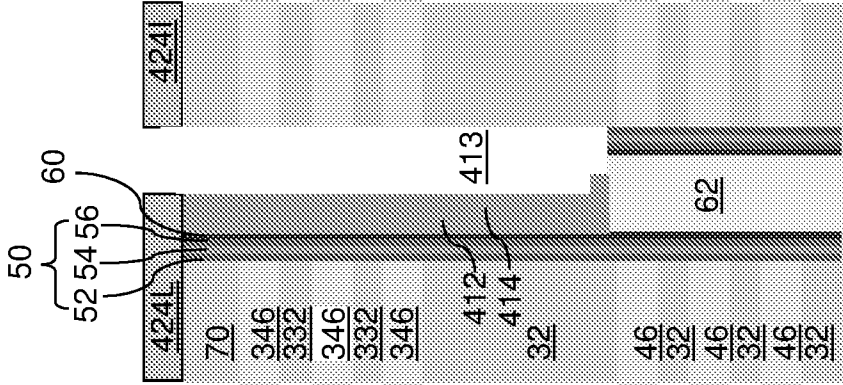


FIG. 45

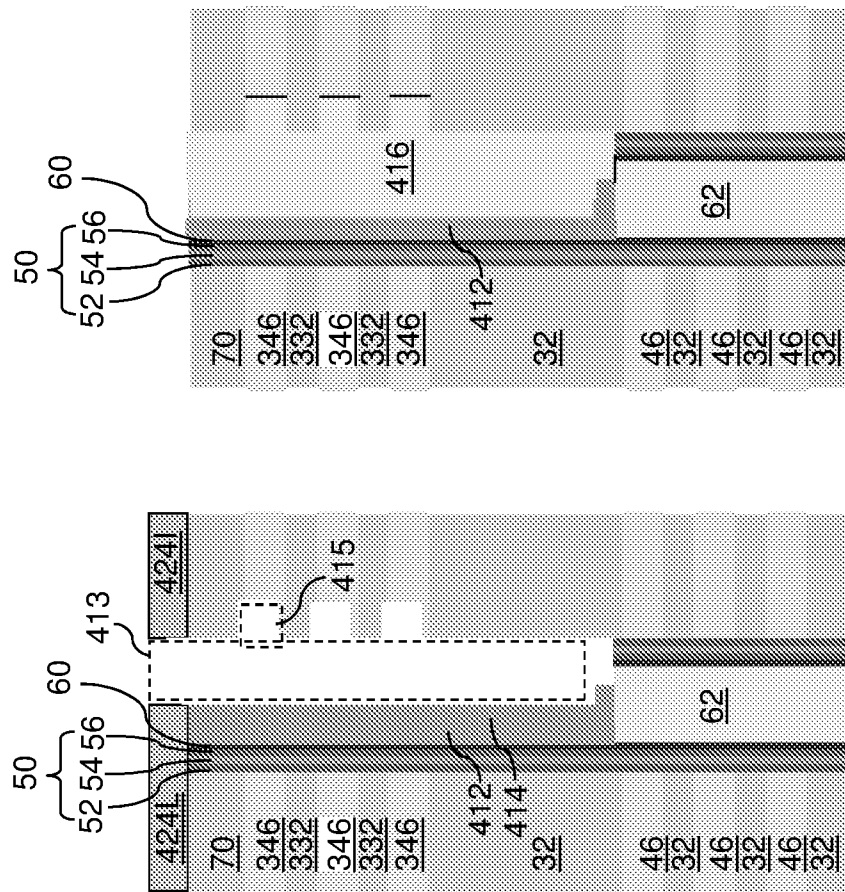


FIG. 47

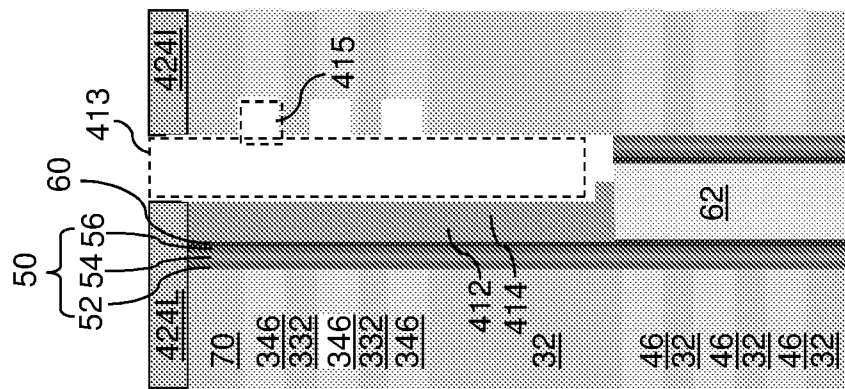
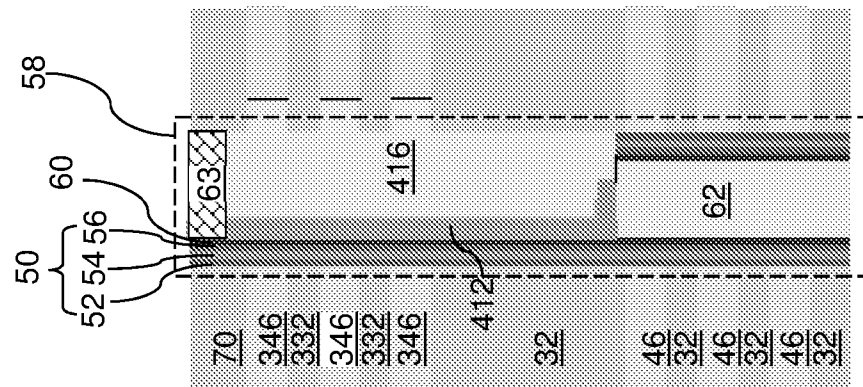
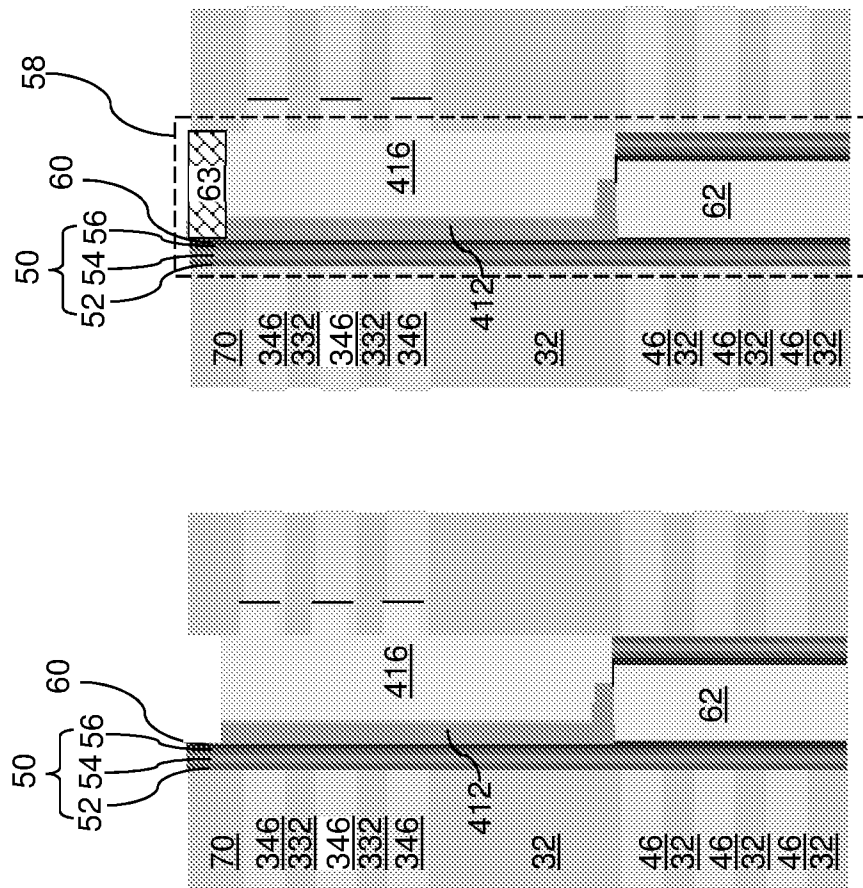


FIG. 46



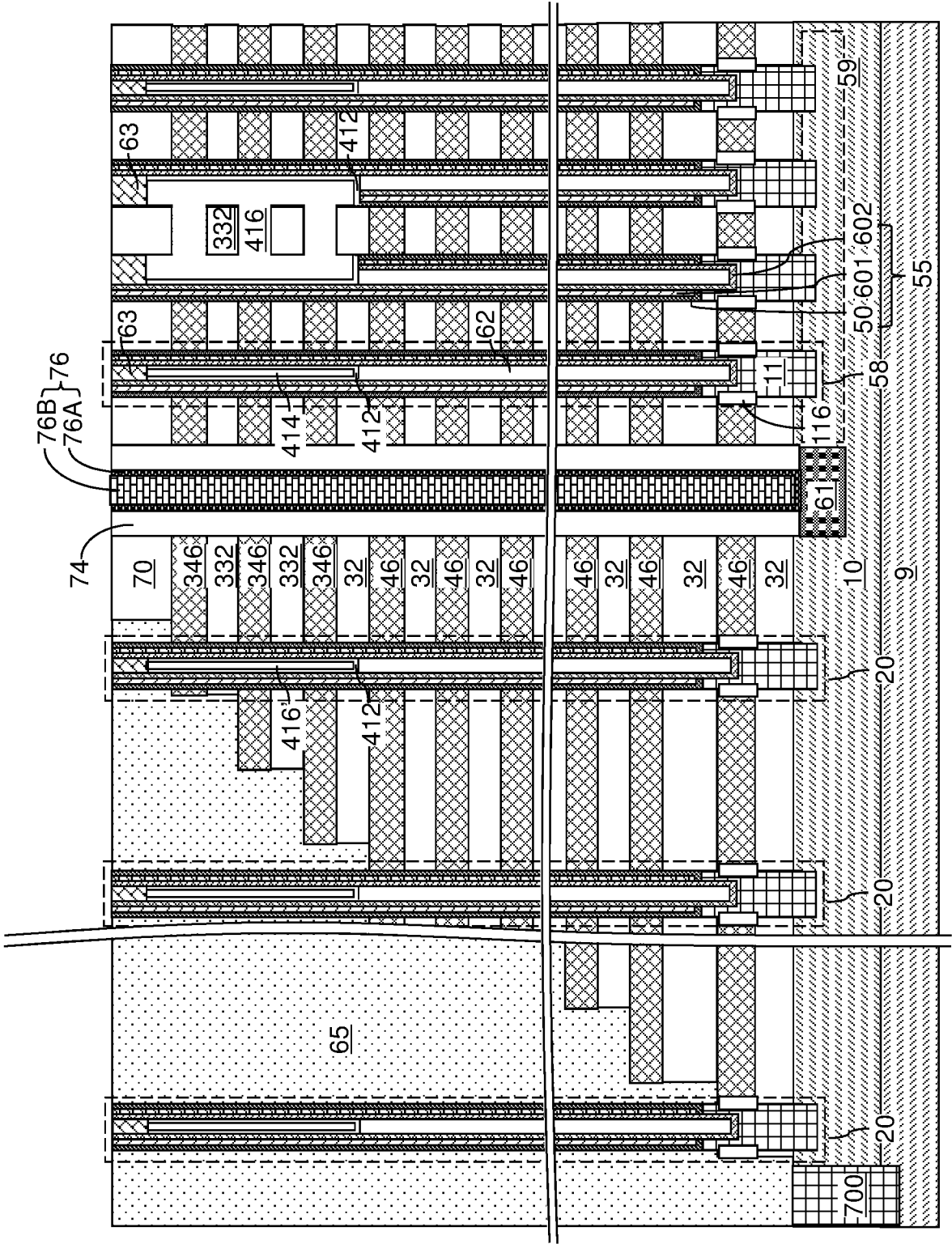


FIG. 50A

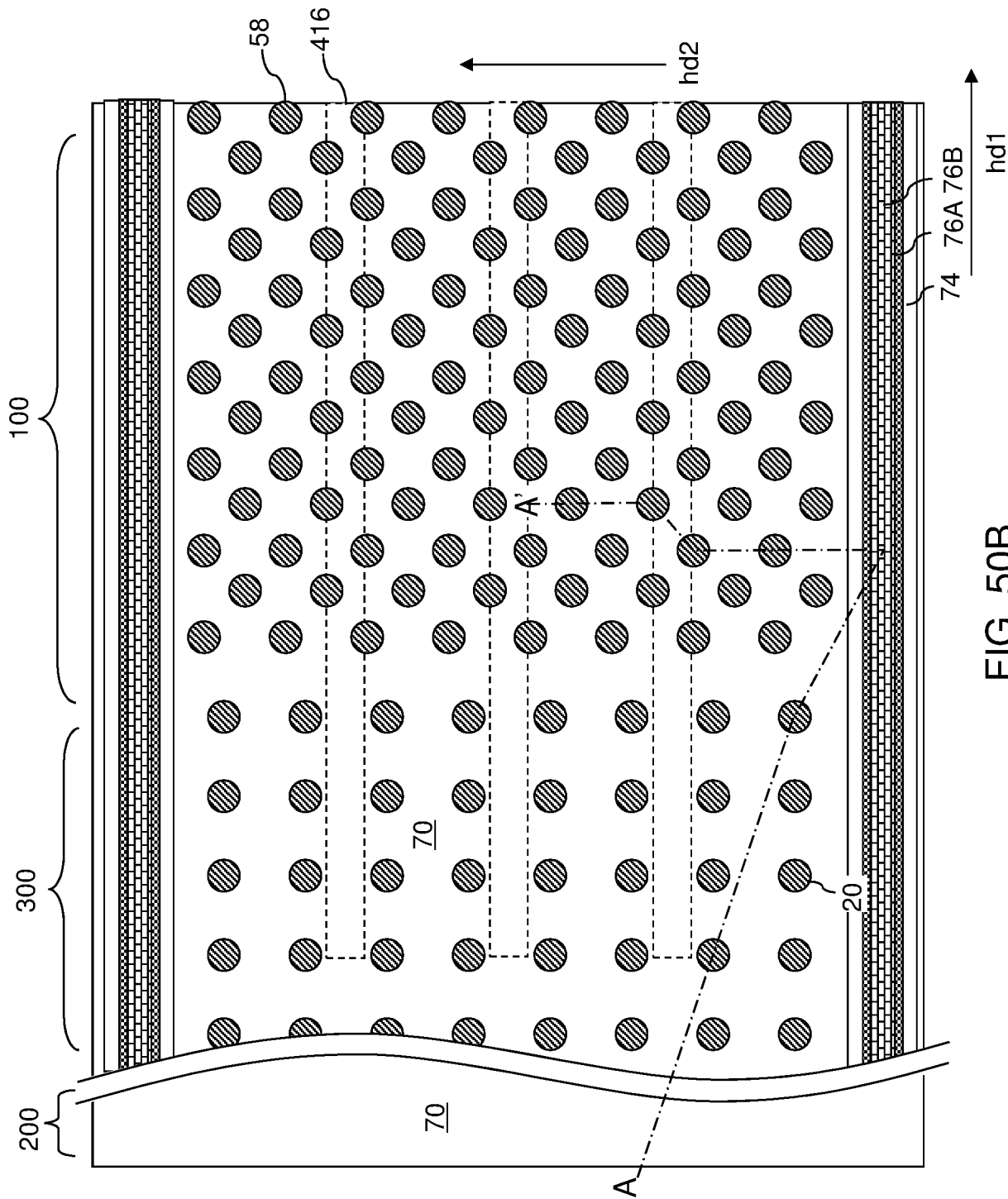


FIG. 50B

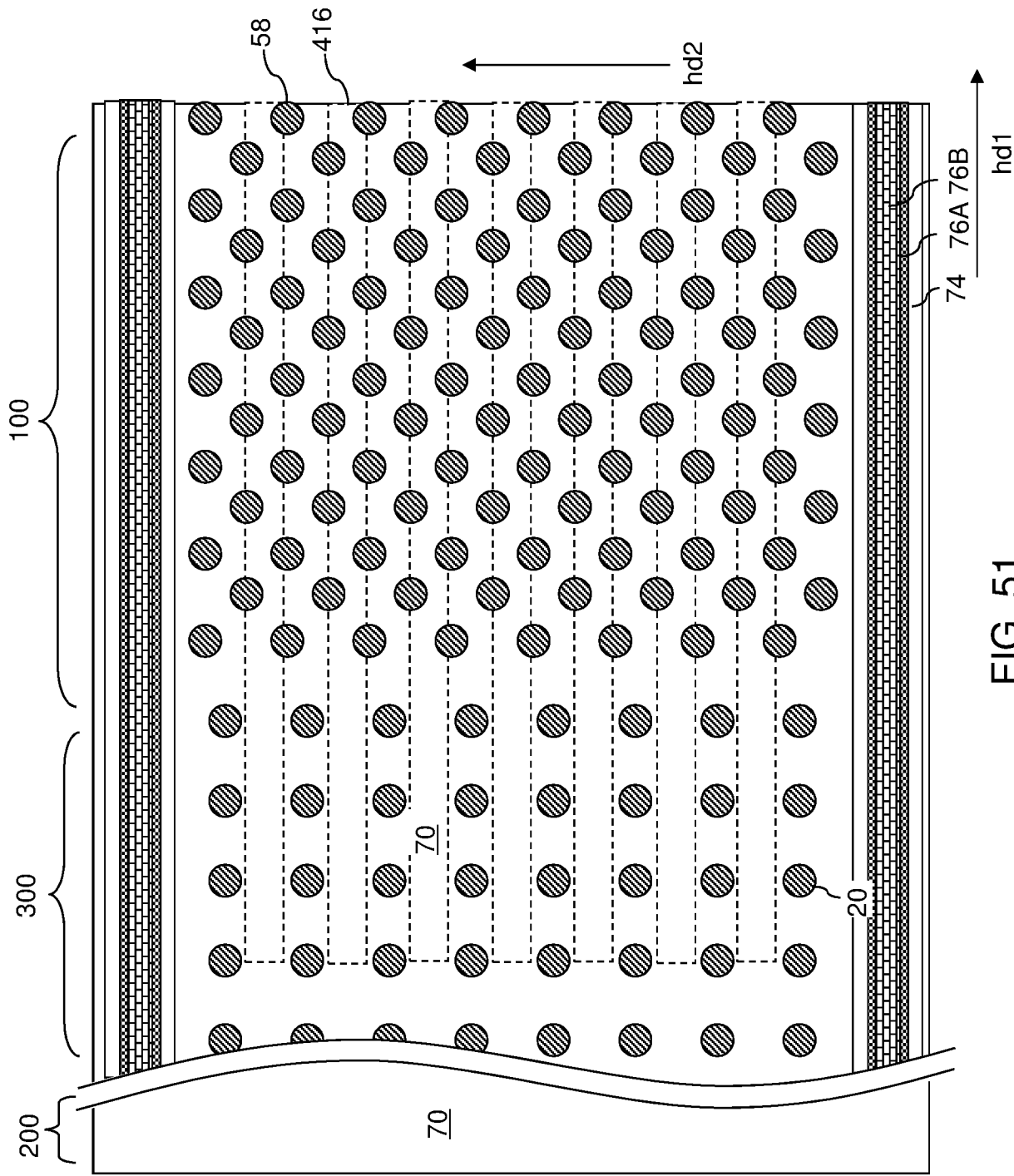


FIG. 51

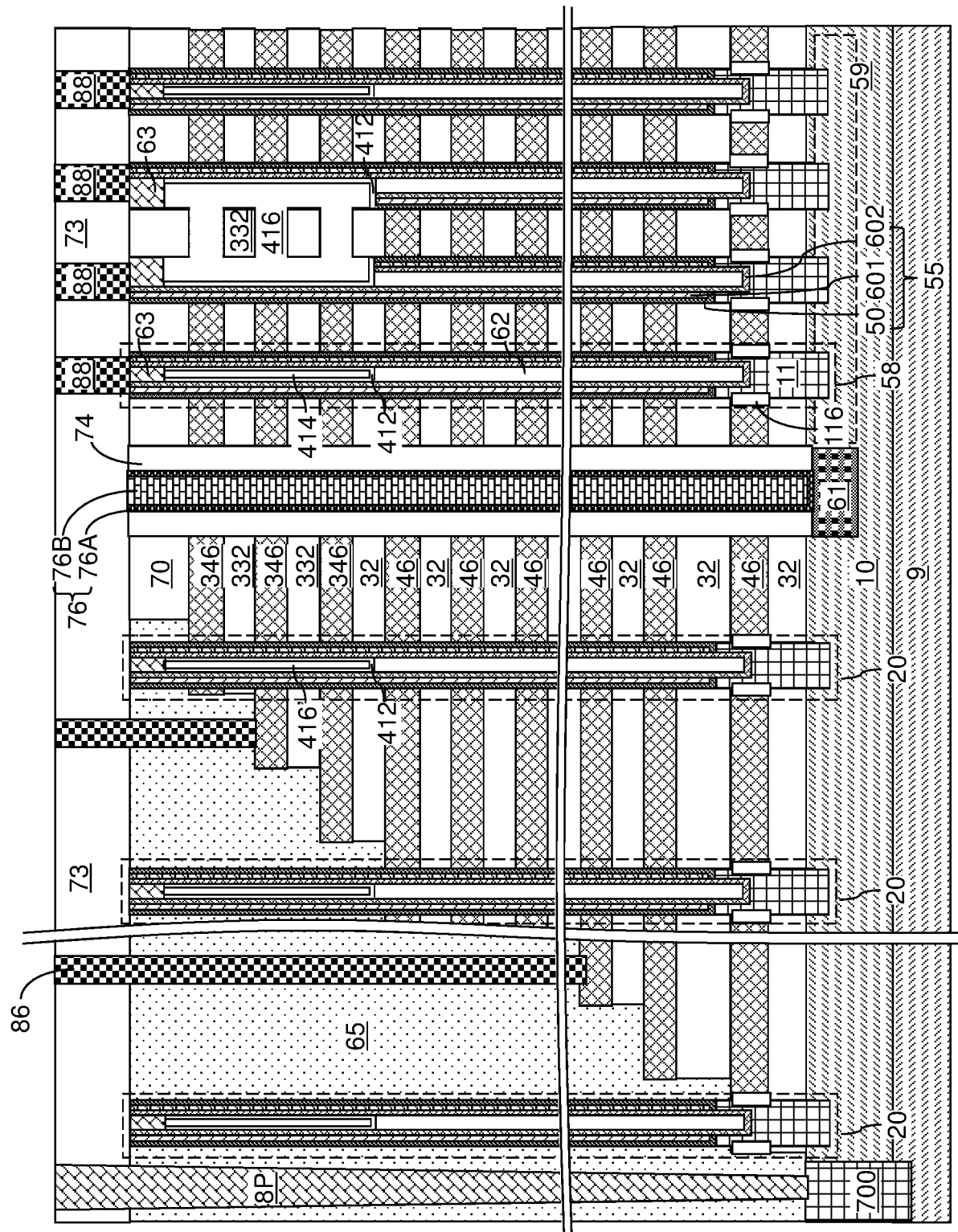
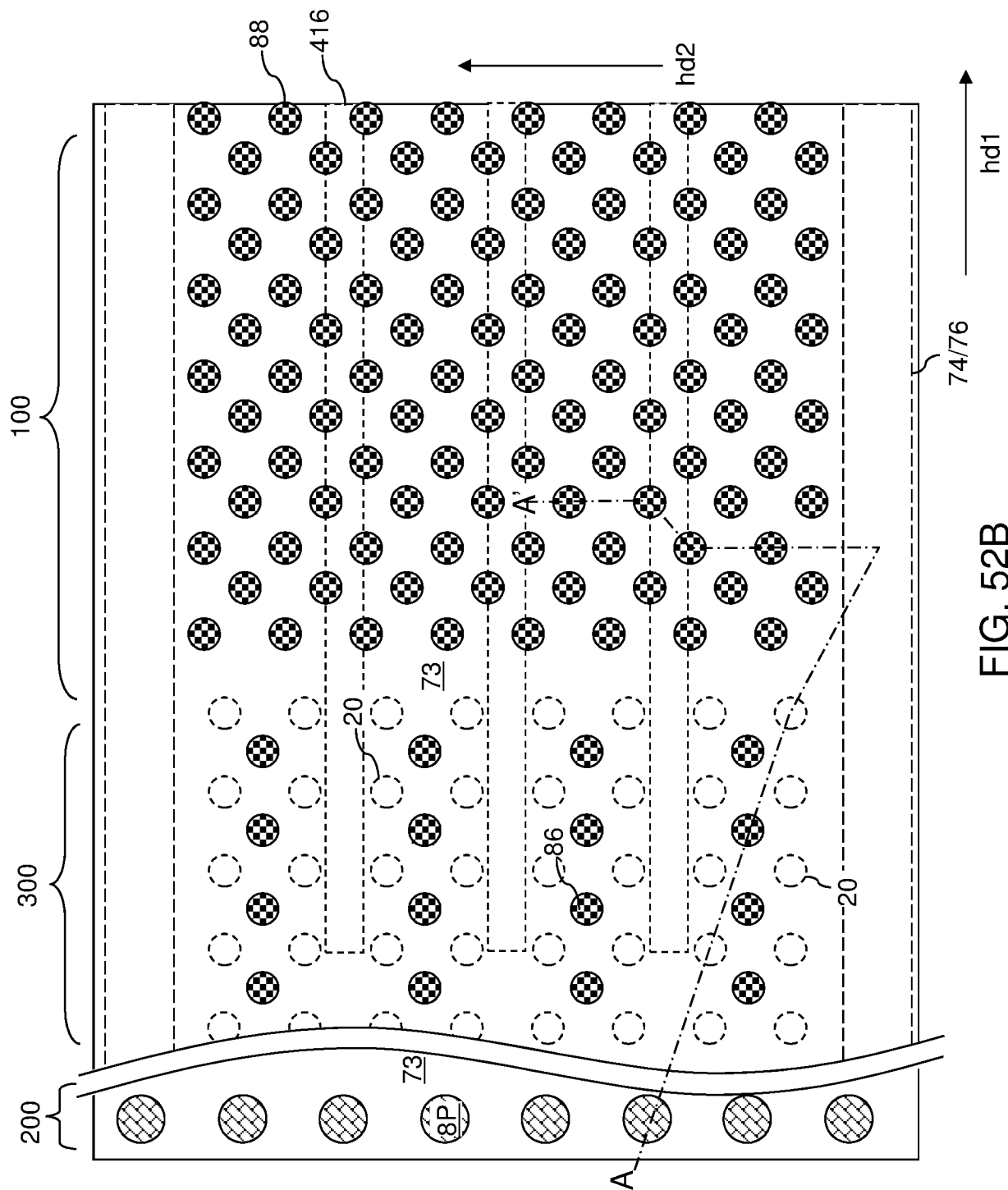


FIG. 52A



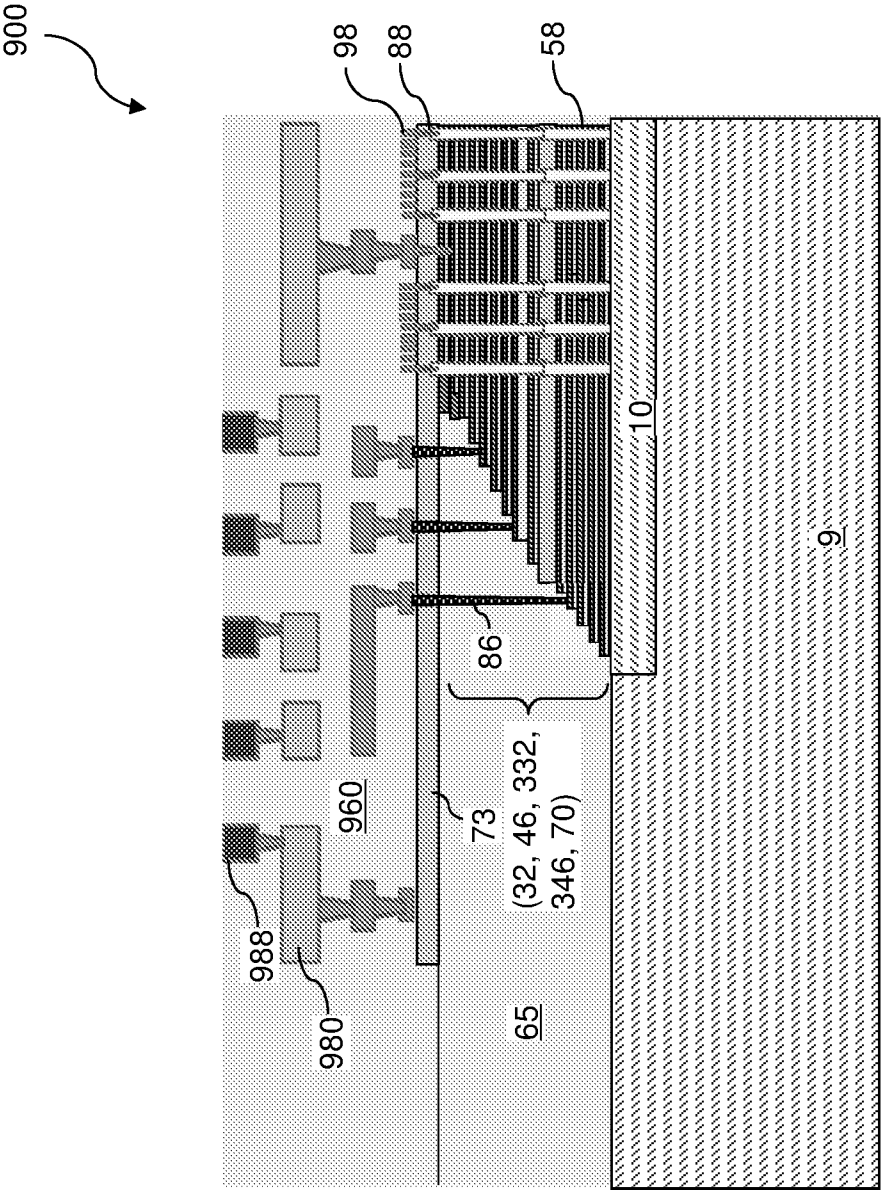


FIG. 53

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2019/063162

A. CLASSIFICATION OF SUBJECT MATTER IPC (20200101) H01L 27/11578, H01L 27/1157, H01L 27/11517, H01L 21/02 CPC (20170101) H01L 27/11578, H01L 27/1157, H01L 27/11517, H01L 21/02488 According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) IPC (20200101) H01L 27/11578, H01L 27/1157, H01L 27/11517, H01L 21/02 CPC (20170101) H01L 27/11578, H01L 27/1157, H01L 27/11517, H01L 21/02488 Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) Databases consulted: Google Patents, Google Scholar, Orbit Search terms used: three dimension memory, film, dielectric, adjoin, PAIR		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2018138189 A1 SANDISK TECHNOLOGIES LLC 17 May 2018 (2018/05/17) The entire document	1-20
P,A	WO 202005335 A1 SANDISK TECHNOLOGIES LLC 02 Jan 2020 (2020/01/02) The entire document	1-20
A	US 2016071860 A1 SanDisk Technologies LLC 10 Mar 2016 (2016/03/10) The entire document	1-20
A	US 8437192 B2 Macronix International Co Ltd 07 May 2013 (2013/05/07) The entire document	1-20
A	WO 2018144957 A1 MONOLITHIC 3D INC. 09 Aug 2018 (2018/08/09) Figures 28-34	1-20
☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.		
* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "D" document cited by the applicant in the international application "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search 20 Feb 2020		Date of mailing of the international search report 25 Feb 2020
Name and mailing address of the ISA: Israel Patent Office Technology Park, Bldg.5, Malcha, Jerusalem, 9695101, Israel Email address: pctoffice@justice.gov.il		Authorized officer ABRAMOVICH Saar Telephone No. 972-73-3927203

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