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(54) Title: INTEGRATED CIRCUIT CONTACT FABRICATION PROCESS

(57) Abstract

A process for fabricating an electrical contact which connects an epitaxial layer (2), well, or substrate with a metallic interconnect layer (62) during the course of creating active integrated circuit devices (16, 17) in a semiconductor wafer. The process forms a self-aligned contact by establishing the contact location (14) coincident with the definition of the active regions in the wafer, at an early step in the wafer fabrication process. Thereafter, a gate silicon dioxide layer (21) and a polycrystalline silicon electrode electrode layer (37) are combined to mask the contact region surface from intermediate process environments, e.g., ion implantation and $POCl_3$ diffusion operations. As the integrated circuit fabrication process approaches conclusion, the contact region (14) is opened by a selective etch of the polycrystalline silicone (37) and the silicon dioxide (21) layers, an enhancement implant into the surface of the contact region, a hydrogen environment annealing operation, and a deposition and patterning of the metallic interconnect layer (62).

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INTEGRATED CIRCUIT CONTACT FABRICATION PROCESS

Technical Field

This invention relates to processes for fabricating, in a semiconductor wafer, an integrated circuit of the kind including: insulated gate field effect devices formed in active regions of said wafer; field oxide regions; an electrical contact between a region in the semiconductor wafer; and a metallic interconnect layer.

Background Art

A process of the kind specified hereinabove is known from published international patent application No. WO 82/01380. In the known process, which is directed to forming a CMOS integrated circuit structure, the formation of the complementary field effect transistors is followed by the provision of a thick oxide layer over the wafer, the opening of contact apertures to the source/drain regions, and the provision of metal contacts to such regions.

Disclosure of the Invention

It is an object of the present invention to provide a process of the kind specified adapted to create a reliable electrical contact between a metallic interconnect layer and a region in a semiconductor wafer.

According to the present invention, there is provided a process of the kind specified, characterized by the steps of: delineating said wafer to define the contact region; forming the field oxide while protecting said contact region; forming a layer of gate dielectric material on said wafer to extend over said contact region; forming a layer of electrode material on said wafer to extend over said contact region; delineating said layer of electrode material to retain the area covering said contact region; delineating an etch mask

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on said wafer to define said contact region after the completion of the field effect devices; sequentially etching through layers of electrode material and dielectric material; and forming a layer of metallic material on said wafer to extend over said contact region.

It will be appreciated that a process according to the invention provides a sequence of steps which create a self-aligned contact structure separated from adjacent active areas by relatively thick silicon dioxide formations (field oxides).

A process according to the invention has a particular application to the provision of reliable contact between a doped epitaxial (epi) layer and a metallic interconnect layer, wherein the process provides for direct masking of the epi contact region during source/drain (S/D) diffusions into the epi layer for field effect devices formed in the epi layer.

In brief summary of a preferred embodiment an epi contact region is defined at an early stage in the wafer process, substantially coincident with the delineation of the active and field oxide regions on the wafer surface. After the formation of the field oxides and gate oxide layer, a first electrode layer of polycrystalline silicon (poly I) is deposited and then photolithographically defined to cover the epi contact region. The poly I covering is oxidized, etched and reoxidized during succeeding process steps while serving to protect the underlying contact region and retaining the initial alignment position. Fabrication of the epi contact concludes with a sequence of selective etches to remove the poly and oxide layers, an enhancement implant of the exposed contact region, a hydrogen environment annealing operation, and a deposition and patterning of the metallic interconnect layer.

Brief Description of the Drawings

One embodiment of the present invention will now be described by way of example with reference to the accompanying drawings, in which:

5 Figs. 1-21 schematically illustrate cross-sections of a semiconductor wafer structure at successive stages during the fabrication of active devices and contacts in an epi layer.

Best Mode for Carrying Out the Invention

10 The composite process to which the present embodiment applies features the use of double level poly and metallic electrodes for fabricating field effect transistors (FETs), silicon-nitride-oxide semiconductor (SNOS) devices, and interconnecting contacts in an
15 electrically isolated epi layer of a semiconductor wafer. The focus of the present embodiment is directed to the formation of reliable electrical contacts between the metallic and epi layer materials without departing significantly from the steps of the aforemen-
20 tioned composite process.

The need for an electrically isolated epi layer arises from the use of relatively high voltages, usually in excess of 20 volts, to "write" or "erase" the SNOS nonvolatile memory devices. The prevailing stan-
25 dard of 5 volts as the nominal supply voltage available to semiconductor chips requires that the higher voltages be generated and controlled on the chip itself. The use of an epi layer allows the isolation of the high voltage from other active devices on the common chip. However,
30 if the threshold shift problems associated with a floating epi are to be suppressed, or control voltages are to be coupled into the epi layer, it is necessary to form an ohmic contact between the epi layer and the metallic interconnect layer.

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To understand how these objectives are accomplished through a unified sequence of process steps, attention is now directed to the cross-sectional schematics beginning with Fig. 1 of the drawings. The unique refinements to the basic SNOS process mentioned hereinbefore will be explicitly noted as they arise during the development of the preferred composite process.

Fabrication of the semiconductor devices begins with an n-type substrate, 1, having a < 100 > cut and a resistivity of 2-3 ohm-cm. A lightly doped p-type epi layer, 2, of 15-20 ohm-cm resistivity is grown on the substrate to a thickness of 15-18 microns. Though the growth process itself is conventional, the presently prescribed thickness has been selected to constrain the current gain in the parasitic npn bipolar device formed by the combination of the shallow n^+ doped source/drain regions in the epi, the p^- doped epi and the n^- doped substrate. Epi layer 2 is itself covered by layer 3, approximately 550 Angstroms of pad silicon dioxide (oxide). The final layer, 4, is a low pressure chemical vapor deposition (LPCVD) of silicon nitride (nitride) having a thickness of approximately 1100 Angstroms. The thickness of the nitride layer includes approximately 400 Angstroms which will eventually be converted to oxynitride and removed during a deglaze operation.

Fig. 2 depicts the wafer cross-section at another stage in the fundamental SNOS process. As depicted, the wafer has undergone a photolithographic pattern definition using a photoresist layer (not shown) defined by mask #1, an etch of nitride layer 4 and oxide layer 3 at locations 6 with appropriate etchants (plasma or wet depending on availability and the size of the geometry sought), a removal of the residual photoresist, a phosphorus-oxygen-trichloride ($POCl_3$) deposition of

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phosphorus, and a deglaze with buffered HF. After the deglaze, the remaining nitride is approximately 700 Angstroms thick. The phosphorus deposition is depicted in Fig. 2 by n^+ doped regions 7 in epi layer 2. Regions 5 7 encircle and thereby define the segment of epi layer 2 which will eventually be electrically isolated.

As illustrated by Fig. 3, the wafer is thereafter subjected to an isolation oxidation step, by which approximately 1,000 Angstroms of oxide 8 is grown at 10 locations 6 from phosphorus doped epi regions 7. The last step ensures that doped epi regions 7 will be adequately protected during the immediately succeeding operations. Oxide 8 prevents the formation of nitride pits which commonly form in the high temperature nitrogen 15 environment utilized to diffuse the phosphorus in region 7 through epi layer 2. Likewise, oxide 8 acts as a mask during the plasma etching of nitride layer 4.

Fig. 4 illustrates the structure of the wafer cross-section at a succeeding step in the fabrication 20 process. As shown, n^+ doped epi regions 7 have been diffused to form regions 9, which extend completely through epi layer 2. This diffusion process creates an electrically isolated region or segment of epi layer 2, hereafter referred to as the isolated epi (iso epi) 11. 25 Given the thickness of epi layer 2, the particular process parameters for accomplishing the isolation drive step are well known by those who routinely practice in the art.

The structure in Fig. 4 also shows the effects 30 of photolithographic processing on photoresist (PR) layer 12 with mask #2, followed in order by a nitride etch operation. The PR patterns the ion implant of boron 13 into the field regions. Again, the process parameters are conventional.

35 It is at this point in the fabrication process that the initial refinements necessary for the practice of the present invention are first introduced. In

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particular, the epi contact location, 14, is delineated in mask #2 as if it were an active region to retain a covering of PR layer 12 and nitride layer 4. Note that the coextensive PR and nitride layers also define two other active regions in the iso epi layer, 11, generally located by reference numerals 16 and 17 in Fig. 4.

Looking to Fig. 5, the cross-section is shown at the conclusion of a group of processing steps, including, a field oxidation, a nitride etch, a pad oxide etch, and a gate oxide growth. In conventional manner, the approximately 18,000 Angstroms of field oxide 18 is grown on exposed substrate silicon not covered by the patterned nitride 4 (Fig. 4). During the growth of the field oxide, the boron impurity implanted previously is driven into the silicon beneath the field oxide regions, as generally designated by reference numeral 19. After the above prescribed nitride and pad oxide etches, the wafer is subjected to a conventional oxidation adequate to grow approximately 775 Angstroms of clean gate oxide 21 in each active region.

Fig. 6 illustrates the enhancement implant with boron, generally 22, into active region 17, after using photolithographically processed mask #3 to pattern PR layer 23. As is well-known, this step adjusts the threshold characteristics of the enhancement mode FET to be formed in active region 17.

Fig. 7 depicts the succeeding implant, 24, a phosphorus impurity into active region 16. The implant pattern is defined by PR layer 26 using process mask #4. In the manner of the immediately preceding implant, the phosphorus impurity adjusts the threshold characteristics of the depletion mode FET to be formed in region 16.

The sequence of the embodying process includes the formation of a poly I contact to the S/D (source/drain) region of the FET to be formed in region 16. Referring to Fig. 8, PR layer 27 is shown after

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photolithographic processing with mask #5 to expose location 28, the position of the proposed poly I-to-S/D contact.

One should not confuse this contact with the metal-to-epi contact formed at location 14. Note that during the formation of the poly I-to-S/D contact, the poly I layer will be doped with n-type impurity, creating a p-n junction with respect to iso epi layer 11.

Proceeding toward the structure in Fig. 9, location 28 is subjected to an oxide etch using PR 27 as a mask. After PR 27 is removed, a poly I layer, 29, of approximately 4,500 Angstroms is deposited. Poly I layer 29 is then implanted with phosphorus to establish a sheet resistance suitable for the proposed poly resistors. Again, such processing is routinely performed by practitioners in the art. The final step, leading to the structure depicted in Fig. 9, involves a photolithographic definition of a pattern in PR layer 31 using mask #6.

It is with mask #6, and the pattern shown in Fig. 9, that the present process proceeds to allow the eventual formation of a low resistivity contact at location 14 to join iso epi layer 11 with a metallic interconnect layer. In particular, mask #6 ensures that PR 31 is retained over the poly I layer at location 14. The contributions of the retained poly will become evident as the process sequence evolves hereinafter.

Fig. 10 illustrates the structure after the combination of an etch of the unmasked portions of poly I, a depletion implant, and a growth of isolation oxide. With greater particularity, the conventional poly I etch step is followed by a removal of PR 31 (Fig. 9) and a conventional blanket implant using phosphorus impurities. The purpose of the implant is to establish the threshold

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characteristics of the depletion FETs having poly II layer gate electrodes. The implant penetrates gate oxide layer 21 (Fig. 9) wherever the gate oxide is not covered by retained areas of poly I, such as poly I electrodes 32, 33, 34 and 36 in Fig. 10. Therefore, the channel characteristics beneath gate electrodes 33, 34 and 36 are not altered. The shielding effect of the poly I layer applies with equal effect to the poly I segment 37, covering the proposed metal-to-epi contact region. The steps leading to the fabrication of the structure in Fig. 10 are concluded with the growth of an isolation oxide, 38, of sufficient thickness to electrically isolate the poly I layer electrodes from the succeeding poly II layer electrodes. As embodied, the thickness of isolation oxide 38 is approximately 2,000 Angstroms over remaining poly I.

Note the direct contact between poly I electrode 32 and iso epi layer 11 at location 39. Succeeding process steps will form the poly-to-S/D contact sought. This structural arrangement is often referred to as a buried contact.

Figs. 11 and 12 depict processing steps particularly directed toward the preparation of an SNOS type nonvolatile (NV) memory device. Fig. 11 shows a PR layer, 41, photolithographically defined with mask #7 to position the SNOS memory FET at location 42, for the memory implant of boron 43 which follows. The boron establishes the threshold voltage of the SNOS memory FET. Thereafter, PR 41 prescribes the mask for etching the oxide layer at memory FET location 42. The oxide etch exposes the monocrystalline silicon surface of iso epi layer 11, as shown in Fig. 12.

The oxide etch step is followed by a PR strip, the formation of the memory dielectric, a deposition of a poly II layer, and a photolithographic definition of

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the composite SNOS type NV memory device. Referring to Fig. 13, formation of the memory dielectric is generally a three step process, which entails the growth of a thin memory oxide, approximately 20 Angstroms thick,
5 followed by the growth of approximately 40 Angstroms of oxynitride and approximately 340 Angstroms of nitride in a single, continuous furnace operation. The outcome is generally depicted in Fig. 13 by memory oxide 43 and oxynitride/nitride composite layer 44. A 3,000 Angstrom
10 deposition of poly II, 46, follows, which layer is itself covered by PR pattern 47 defined by photolithographic mask #8.

Using PR pattern 47, the structure in Fig. 13 is subjected to a sequence of etches in progressing to
15 the cross-section shown in Fig. 14. The objective of the steps is to expose the poly electrodes and the S/D regions in iso epi layer 11 for succeeding diffusion doping operations. Note that the specific sequence of layers and material types establishes a progression of
20 appropriate etchant stops. At the conclusion of the poly II, nitride and oxide etches, the wafer structure appears as shown in Fig. 14.

It is evident from Fig. 14 that poly I layer segment 37, at the location of the metal-to-epi contact,
25 also remains intact at the conclusion of the selected etch sequence, thereby masking gate oxide layer 21 at location 14 from the succeeding oxide etchants.

Care must be exercised in the selection of etchants to ensure that the preferential etch rates are
30 consistent with the progression of materials serving as etchant stops. For purposes of the present embodiment, a suitable choice is a planar plasma using SF_6 followed by C_2ClF_5 (Freon 115) to etch both poly II layer 46 and oxynitride/nitride layer 44. The remaining oxide is
35 then removed with 7:1 buffered HF.

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The structure in Fig. 15 modifies that in Fig. 14 by the operation of two further fabrication steps, a $POCl_3$ deposition of n-type dopant and a second isolation oxidation. Referring to Fig. 15, the $POCl_3$ dopes poly I interconnect electrode 32, poly I mask 37, poly II gate electrode 48, and poly I gate electrodes 33, 34 and 36. Simultaneously, the deposition creates n^+-type S/D diffusions 49 in p^- iso epi layer 11. The buried poly I contact formation at location 51 is now completed, by the diffusion of phosphorus through poly I electrode 32. The second isolation oxide layer, shown at 35 in Fig. 15, is thermally grown to be approximately 350 Angstroms on iso epi layer 11.

Since the features of the composite SNOS type NV memory device at location 17 are secondary to the present contact fabrication process, one seeking a detailed description thereof should consult published International Patent Application No. WO 82/02275.

Note, at this point, that the present metal-to-epi contact fabrication process ensures that no phosphorus dopant is diffused into iso epi layer 11 at contact 14. This occurs by virtue of the blocking effect created when poly I layer 37 is combined with gate oxide layer 21. In such an arrangement, the gate oxide layer is a significantly more efficient barrier against phosphorus diffusion into the surface of iso epi layer 11.

Attention is now directed to Fig. 16 of the drawings. As shown, the structure last depicted in Fig. 15 has been covered by approximately 10,000 Angstroms of low temperature deposited undoped oxide, 52. Oxide 52 is thereafter subjected to a densification step in generally known manner and further covered by photolithographically patterned PR layer 53. Note that the metal-to-epi contact at location 14 remains self-aligned

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from its inception. This permits greater tolerances in the alignment of mask #9, which is used to pattern PR layer 53.

Fig. 17 illustrates the wafer cross-section after the effects of an oxide etch step using the pattern of PR layer 53. As is illustrated, the S/D diffusion at location 54 is exposed by the oxide etch operation, while the metal-to-epi contact at location 14 remains protected from oxide etchants by the masking effect of poly I layer 37. The relatively thick layer of oxide 52 is conveniently removed from location 14 when etching the contact opening at 54, though PR mask 53 could be patterned to defer the etch of location 14 until later in the process. The oxide etch is followed by a $POCl_3$ deposition of phosphorus to enhance the exposed S/D contact regions. The phosphorus impurity diffuses both into iso epi layer 11 and laterally beyond the metal-to-S/D opening at location 54. The lateral diffusion effectively relaxes mask alignment tolerances. The increased depth of the diffusion is visually evident at reference numeral 50 in Fig. 17. Thereafter, the wafer is subjected to a brief deglaze operation, which entails a blanket etch suitable to clean the S/D contact areas at locations such as 54.

To derive the structural cross-section appearing in Fig. 18, the arrangement of Fig. 17 is initially subjected to an oxidation adequate to grow approximately 250 Angstroms of oxide 56 from the exposed S/D region at location 54. This oxide prevents contamination of the S/D by sodium traces common in PR materials, a contaminant material which has been linked to threshold stability problems. Oxide 58, grown from poly I layer 37, is of no consequence. Upon the conclusion of the oxidation step, PR layer 57 is deposited and photolithographically processed with mask #10 to expose the region surrounding the metal-to-epi contact at location 14. Note that the opening in the PR is visibly larger than

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the previous PR openings at location 14, and is significantly larger than the contact region itself. This again illustrates the self-aligning feature of the present process, which feature allows a greater density of active components by increasing the magnitudes of the errors permissible for the mask alignment and fabrication processes.

Using the mask defined by PR layer 57, the wafer in Fig. 18 is taken through an etch sequence. The sequence begins with a wet etch of oxide 58 using 7:1 buffered HF, follows with a conventional wet or plasma etch of poly I layer 37, and is concluded with a wet etch of gate oxide layer 21 using 7:1 buffered HF. Fig. 19 shows the cross-section at the conclusion of the sequence. As was true in previously described sequences, the particular succession of preferential etchants and materials defined serve as self-defining etchant stops, concluding with surface 59 of iso epi layer 11. Though the etching of thick oxide layer 52 could be deferred, as noted hereinbefore, until this sequence, there are no particular benefits while the risks of field oxide damage increase significantly.

To improve the contact between the metallic interconnect layer and the p^- doped iso epi surface, a supplemental boron implant, 61 is effected. The implant removes any possibility of forming a parasitic diode (p-n junction) at surface 59. A preferred implant has an energy of approximately 50 keV and a boron dose of approximately 1×10^{15} atoms per square centimeter. The implant step can be eliminated if the metallic interconnect is formed from a suitable barrier material, i.e. a material that does not form a diode junction when connected to surface 59 of iso epi layer 11. That was not the case with metallic material utilized in the present embodiment.

The formation of the metal-to-epi contact is further enhanced by a hydrogen annealing operation

performed on the wafer after PR layer 57 is stripped. The annealing step, done at approximately 900°C for 30 minutes, removes implantation damage in surface 59 and activates the boron impurities therein. In the context of the complete wafer, the hydrogen annealing cycle also improves the device characteristics of poly I layer resistors and the SNOS type NV memory devices.

Attention is now directed to Fig. 20, where the wafer is shown after metal and PR depositions. To reach this stage of the processing, the annealed wafer is first subjected to a blanket, premetal contact etch in 20:1 buffered HF. The etch removes residual contaminants and thin oxide layer 56 (Fig. 18) at the site of the metal-to-S/D contact, location 54. As shown in Fig. 20, the etched structure is covered by a metal alloy layer, 62, composed of aluminum with approximately 1.2% silicon. The thickness of layer 62 is approximately 10,000 Angstroms. Metallic layer 62 is covered by PR layer 63, which is then patterned photolithographically using mask #11 to define the metal interconnect pattern.

Fig. 21 illustrates the cross-section of the completed device, after the conventional steps of metal etching, metal alloying, deposition of silox 64, and silox etching for chip pad definition. The contact formed between iso epi layer 11 and metal layer 62 at location 14 is immediately apparent. The completed structure in Fig. 21 also illustrates the effective isolation rendered by a segment of field oxide 18, to separate the metal-to-epi contact at 14 from the SNOS device at 17. The self-aligned character of the contact is also evidenced by the structure in Fig. 21, where the opening in oxide layer 52 is visibly wider than actual contact at surface 59 of iso epi layer 11. Moreover, the versatility of the present process is clearly illustrated by way of the whole embodiment, where the contact-making refinements are incorporated into a relatively complex process for simultaneously fabricating

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epitaxially isolated FETs, 16, and SNOS devices, 17, using multiple poly electrode layers and a metallic interconnect layer.

It will no doubt be appreciated that the metal-to-epi contact process described herein has a relatively broad range of potential applications. Therefore, it may be introduced into numerous types of related processes without departing from the fundamental tenets illustrated in the presently preferred embodiment. For instance, the features of the process apply with equal merit to the fabrication of metallic contacts to the substrate itself, to lightly doped wells or to heavily doped diffusions wells formed in a substrate.

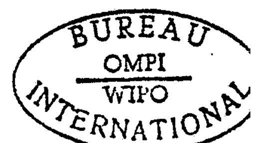
CLAIMS:

1. A process for fabricating, in a semiconductor wafer, an integrated circuit of the kind including: insulated gate field effect devices (16, 17) formed in active regions of said wafer; field oxide regions; an electrical contact between a region in the semiconductor wafer and a metallic interconnect layer (62), characterized by the steps of: delineating said wafer to define the contact region (14); forming the field oxide (18) while protecting said contact region (14); forming a layer of gate dielectric material (21) on said wafer to extend over said contact region (14); forming a layer of electrode material (29) on said wafer to extend over said contact region (14); delineating said layer of electrode material (29) to retain the area (37) covering said contact region (14); delineating an etch mask (57) on said wafer to define said contact region (14) after the completion of the field effect devices (16, 17); sequentially etching through layers of electrode material (37) and dielectric material (21); and forming a layer of metallic material (62) on said wafer to extend over said contact region (14).

2. A process according to claim 1, characterized in that said etch mask (57) exposes a region greater than said contact region (14).

3. A process according to claim 1, characterized by the step of forming a further layer of dielectric material (38) over the electrode material (37) covering said contact region (14).

4. A process according to claim 1, characterized in that said contact region (14) is defined in an epitaxial layer (2) of said wafer.



5. A process according to claim 1, characterized in that said contact region (14) is defined in a lightly doped well of said wafer.

6. A process according to claim 1, characterized in that said contact region (14) is defined in a heavily doped diffusion of said wafer.

7. A process according to claim 4, characterized in that said epitaxial layer (2) is lightly doped with a first impurity type material and said metallic material (62) is an aluminum-silicon composition; and in that said process includes the additional steps of implanting first impurity type ions into said contact region (14) to a concentration adequate to suppress parasitic p-n junctions, and annealing said wafer in a hydrogen environment, following said step of sequentially etching.

8. A process according to claim 7, characterized in that said layer of gate dielectric material (21) and said further layer of dielectric material (38) are formed of silicon dioxide and said electrode material (29) is polycrystalline silicon.

9. A process according to claim 8, characterized in that said sequential etching is performed with etchant materials which are preferential in etching either silicon or silicon dioxide.

10. A process according to claim 8, characterized in that said step of forming a further layer of dielectric material (38) is followed by the additional steps of: forming a further layer of electrode material (46) on said wafer; delineating said further layer of electrode material (46) to define active devices and

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10. (concluded)
interconnects; and forming an additional layer of dielectric material (35) on said wafer.

11. A process according to claim 10, characterized in that said step of delineating said further layer of electrode material (46) is followed by a diffusion of second impurity type dopant into defined
5 electrode and wafer regions.

12. A process according to claim 11, characterized in that said step of delineating said further layer of electrode material (46) is followed by the step of delineating an etching mask (53) over said
5 contact region (14) and over a further contact region (54) for forming a contact to a region doped by diffusion (49), and by the succeeding additional steps of: diffusing a second impurity type dopant into said further contact region (49); forming a relatively thin
10 layer of silicon dioxide material (56) on said further contact region (54); and delinating said etch mask (57) to define said contact region (14).

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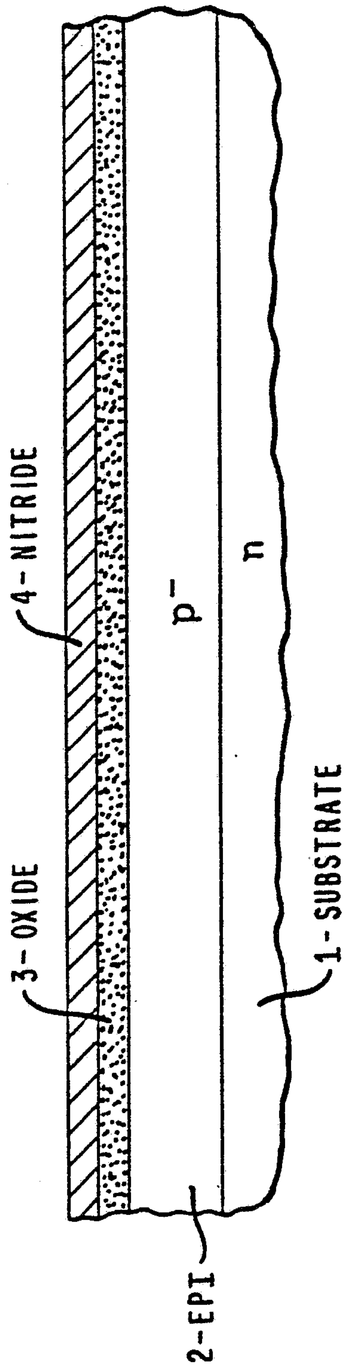

FIG.1

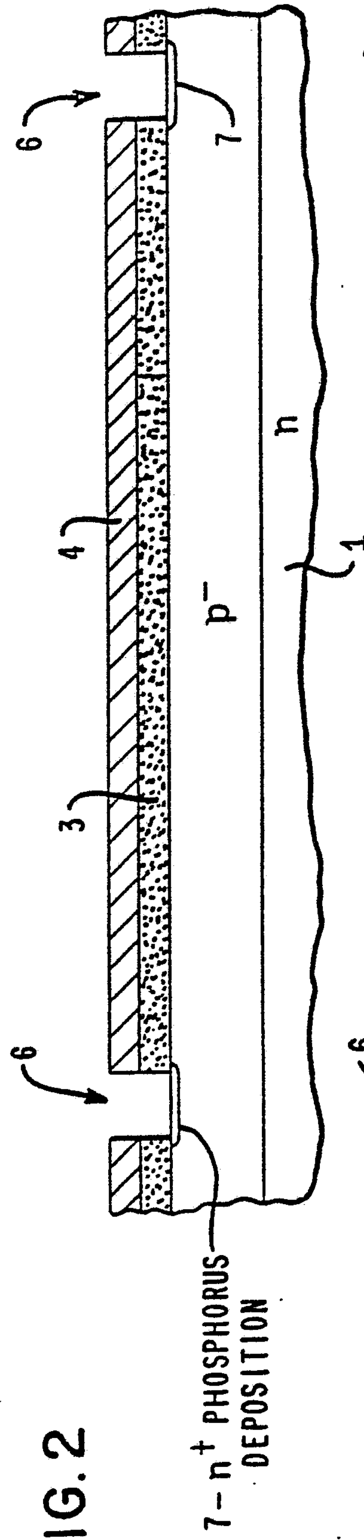

FIG.2

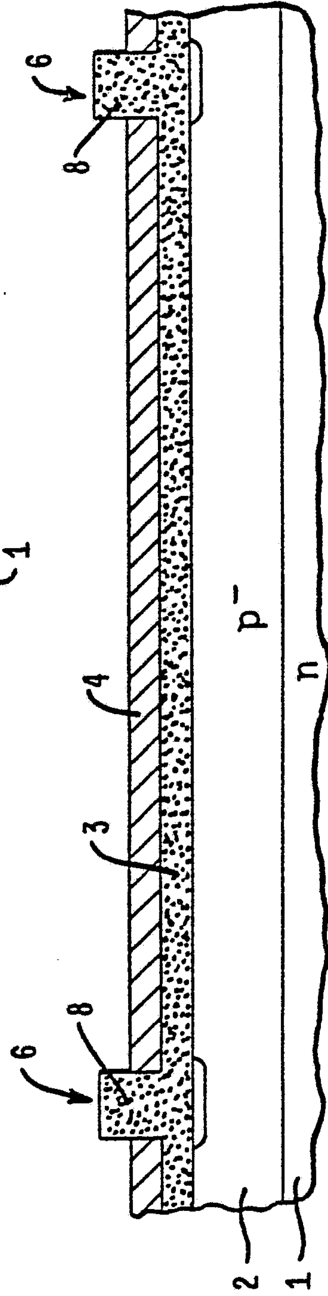

FIG.3

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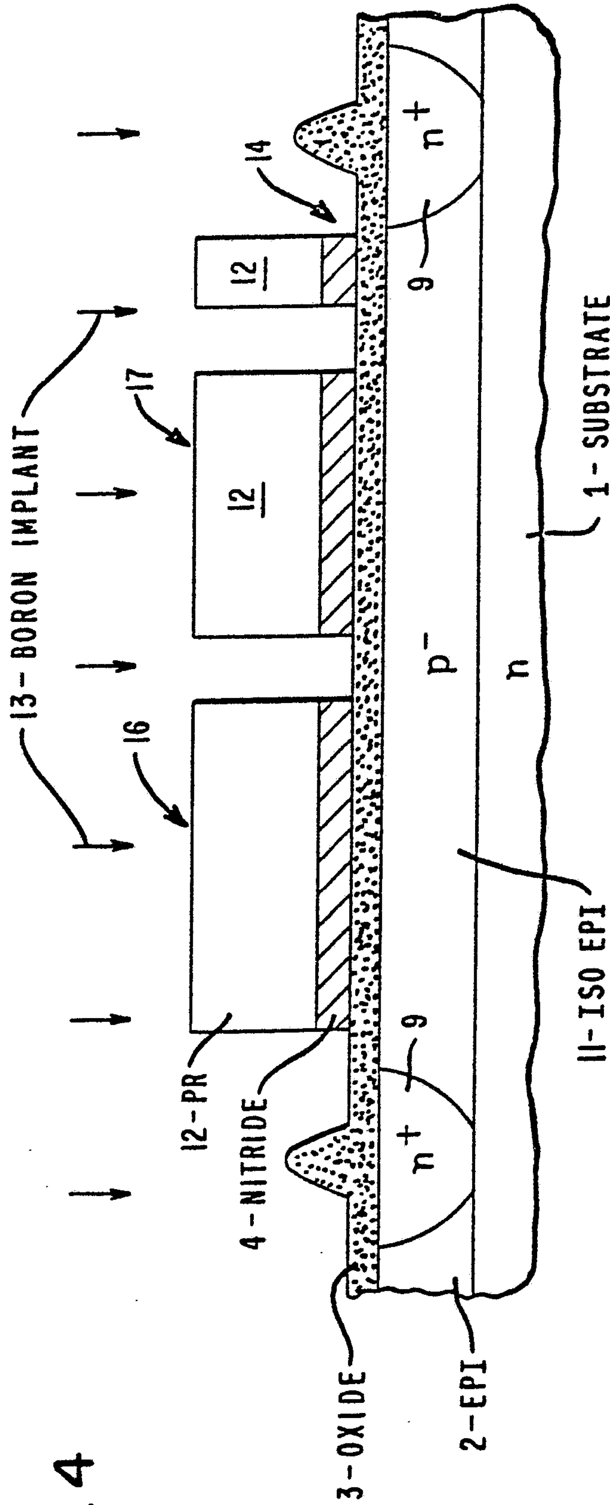

FIG. 4

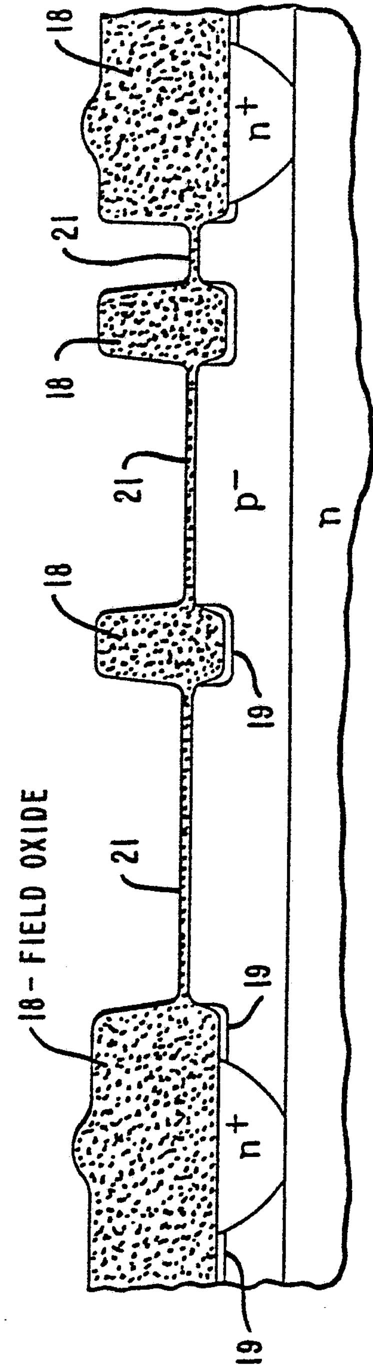

FIG. 5

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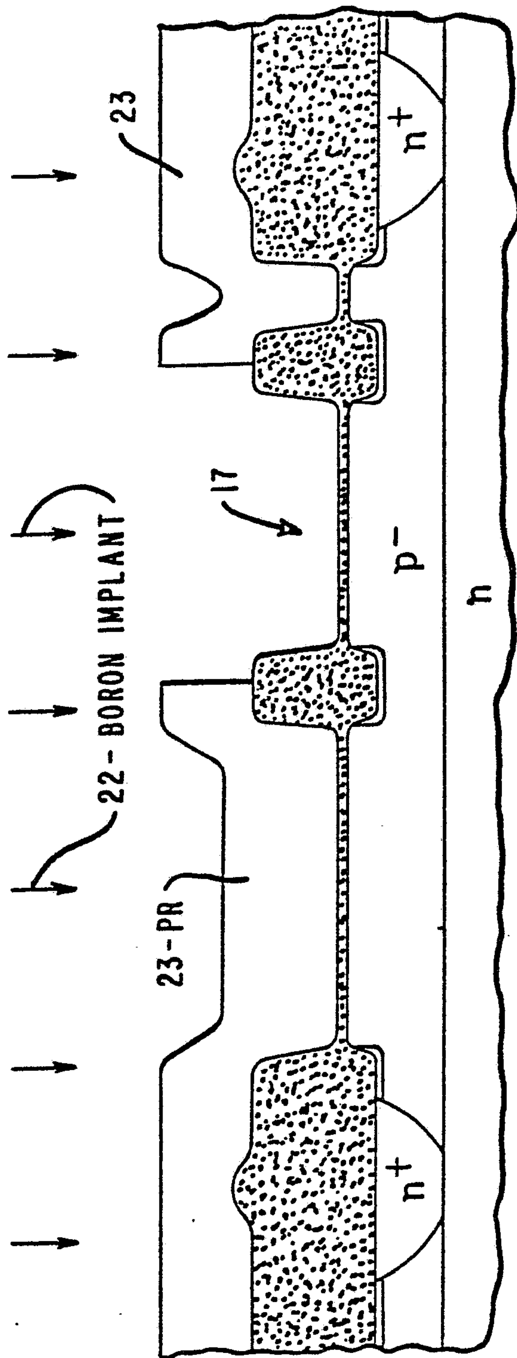

FIG.6

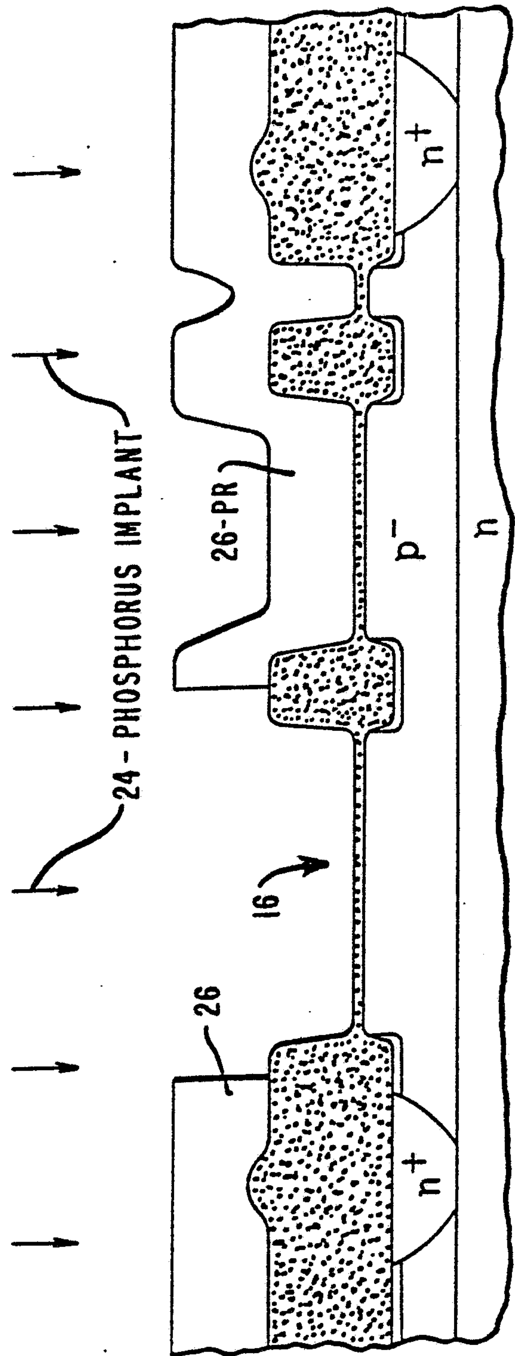

FIG.7

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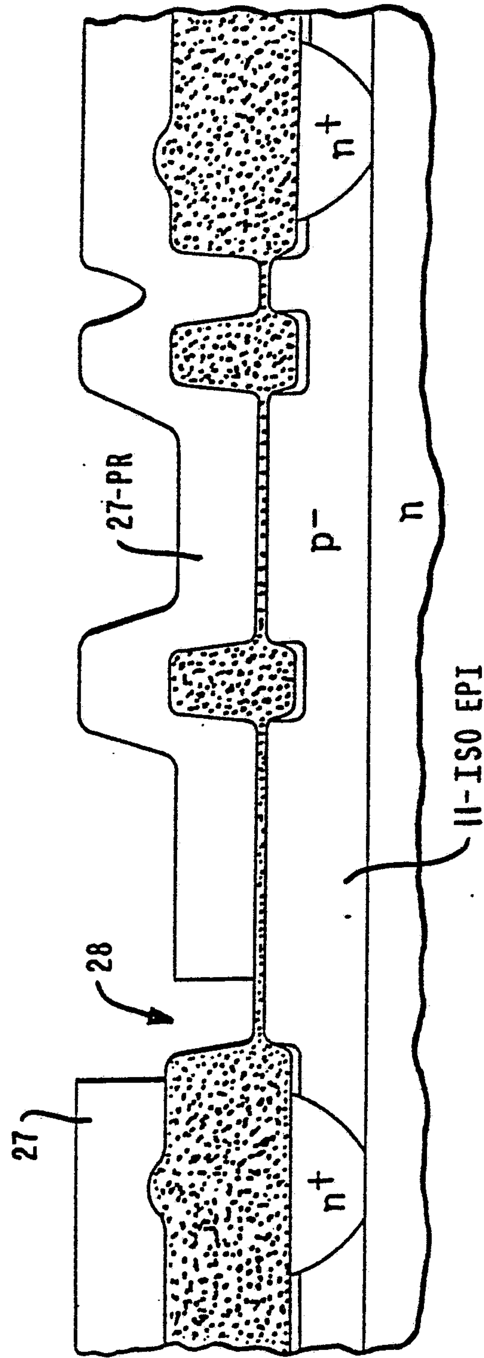

FIG. 8

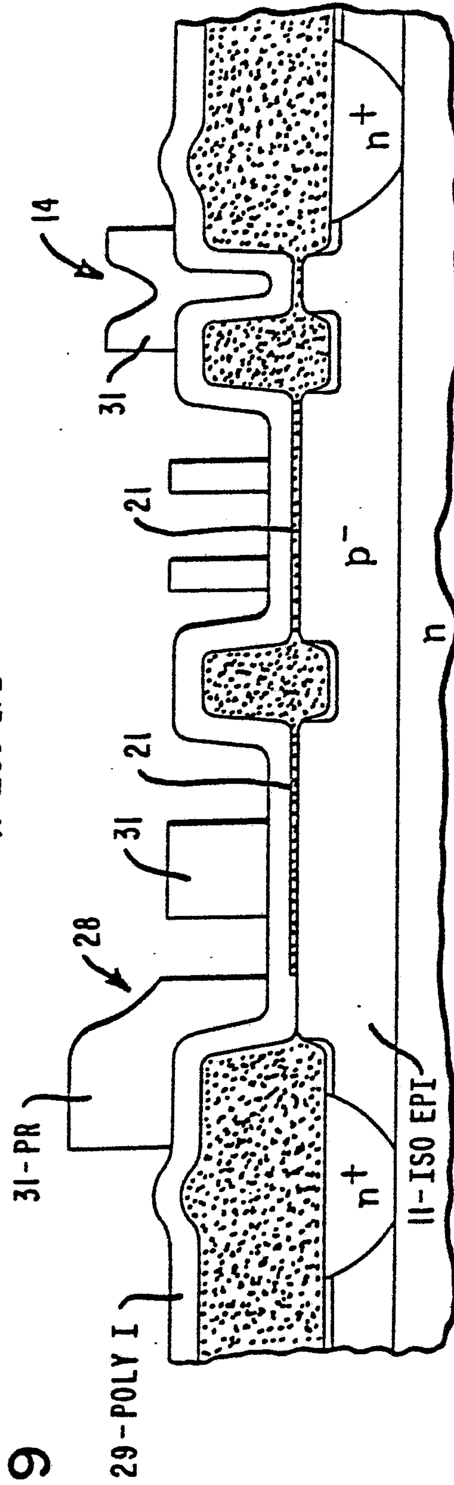

FIG. 9

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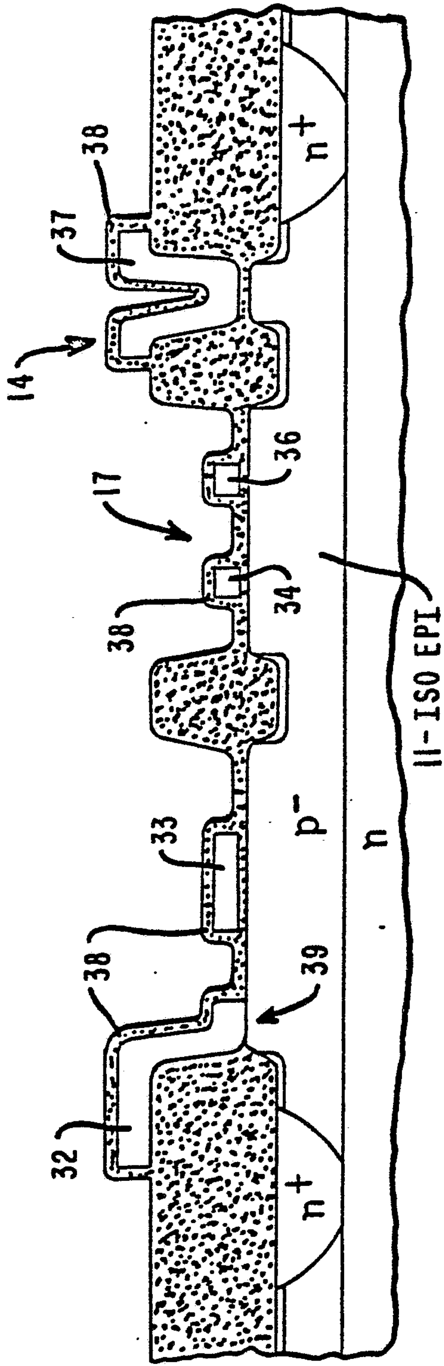

FIG.10

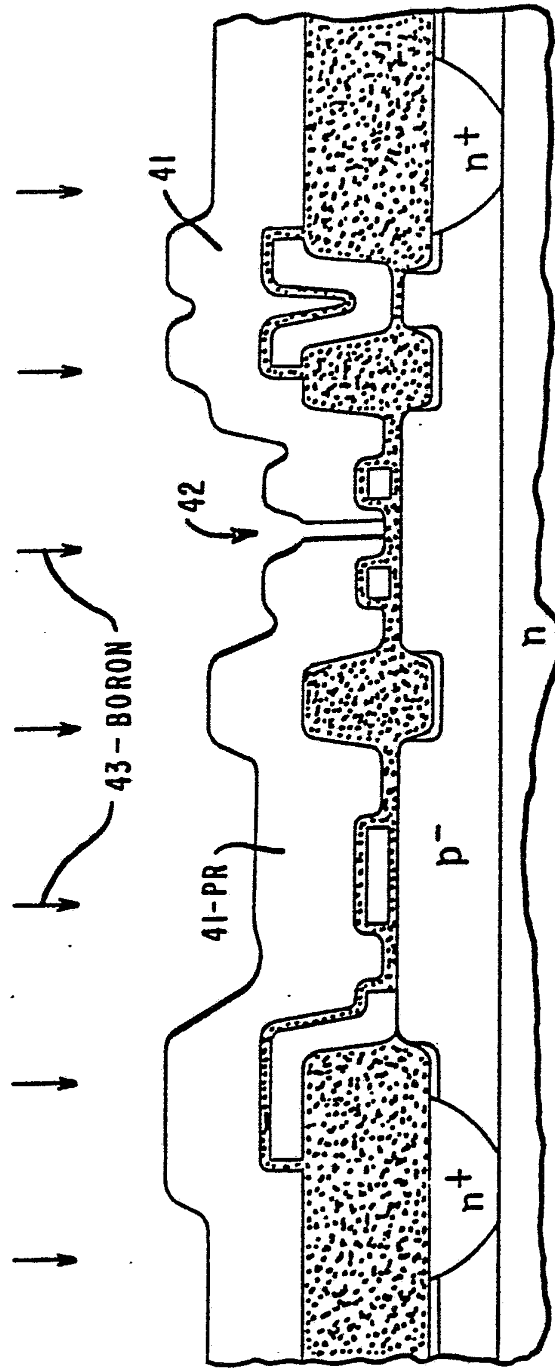

FIG.11

BUREAU OMPI WIPO INTERNATIONAL

FIG.12

41

42

41-PR

p⁻

n

n+

11-ISO EPI

FIG.13

47-PR

43

44-OXYNITRIDE / NITRIDE

46-POLY II

p⁻

n

n+

BUREAU OMPI WIPO INTERNATIONAL

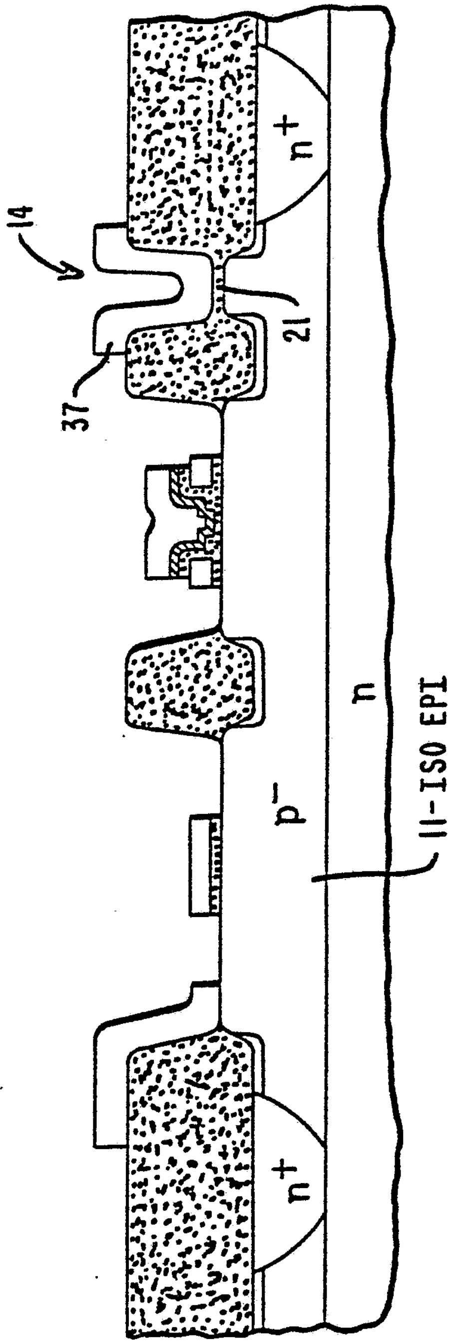

FIG. 14

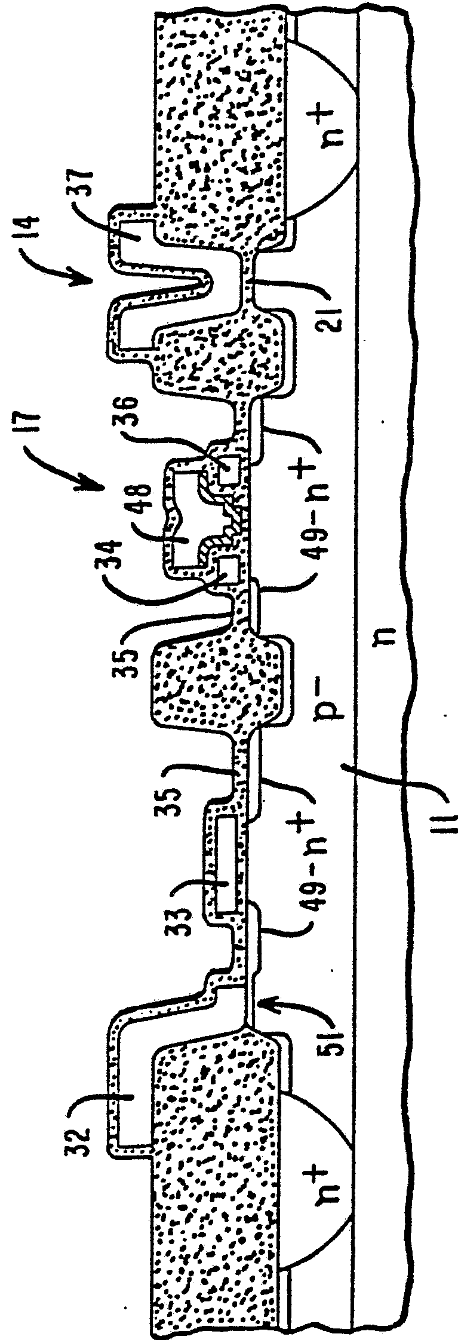

FIG. 15

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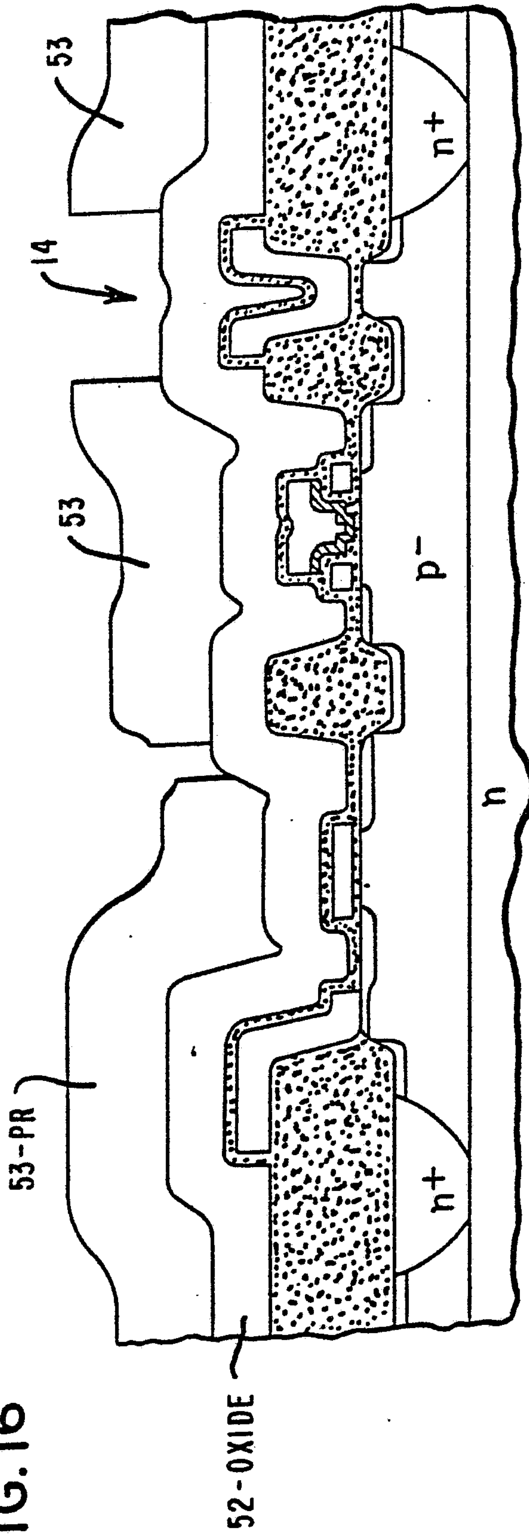

FIG.16

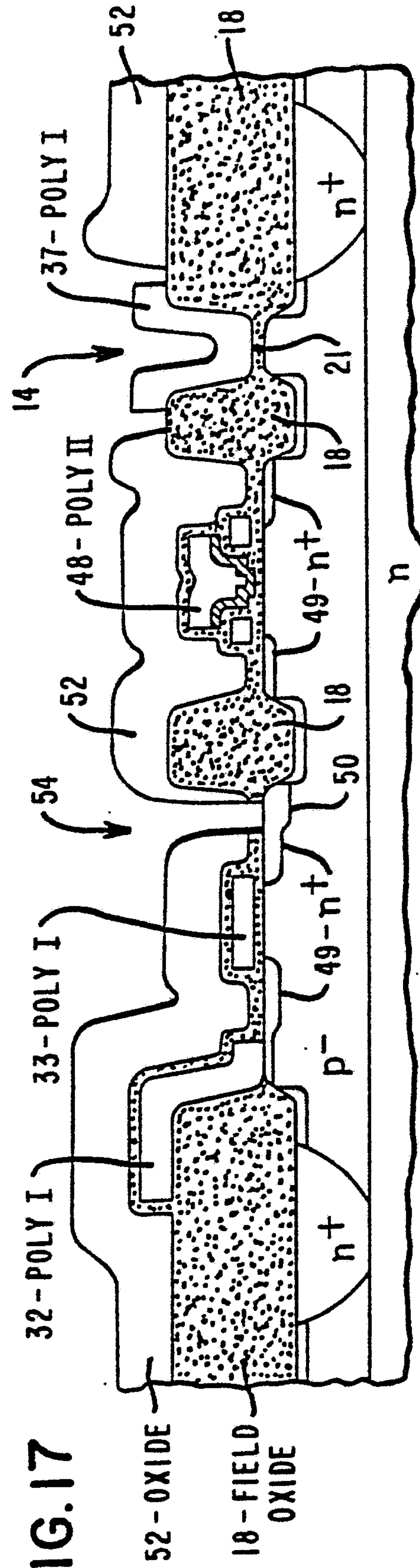

FIG.17

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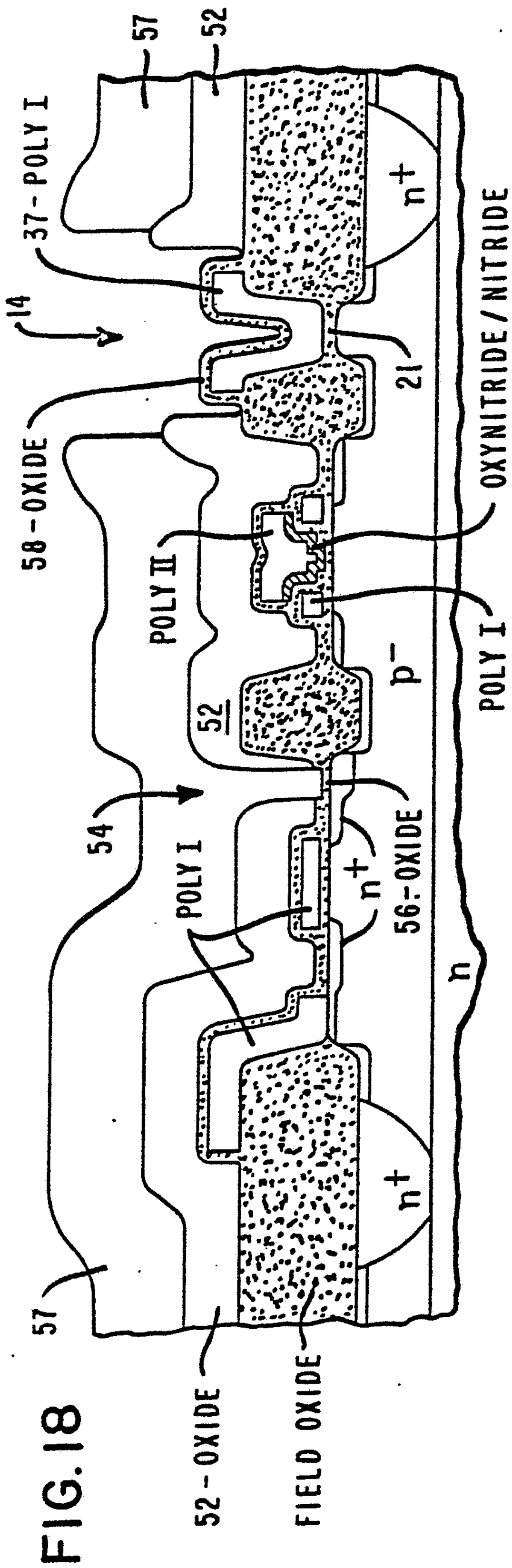

FIG.18

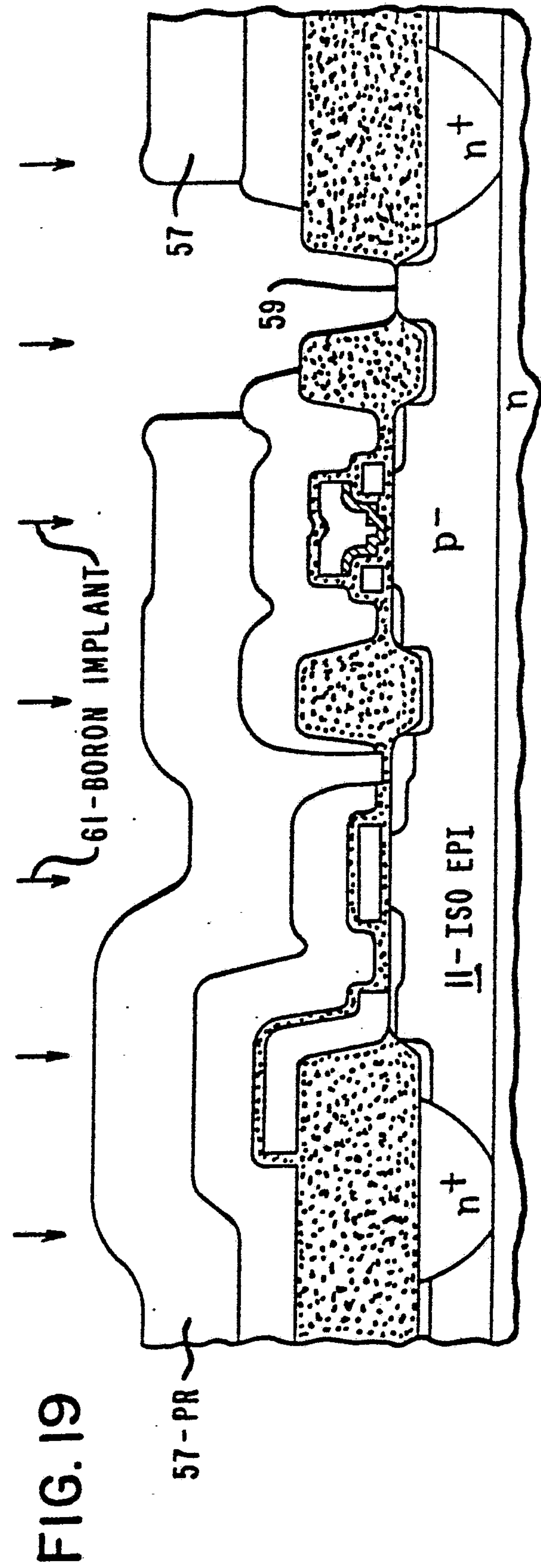

FIG.19

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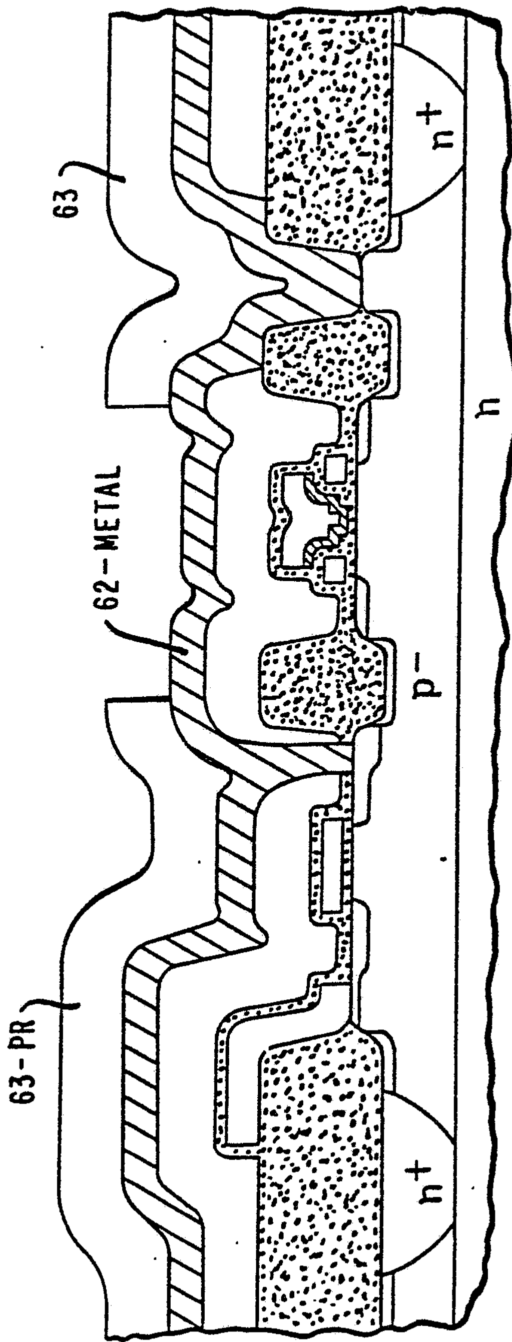

FIG. 20

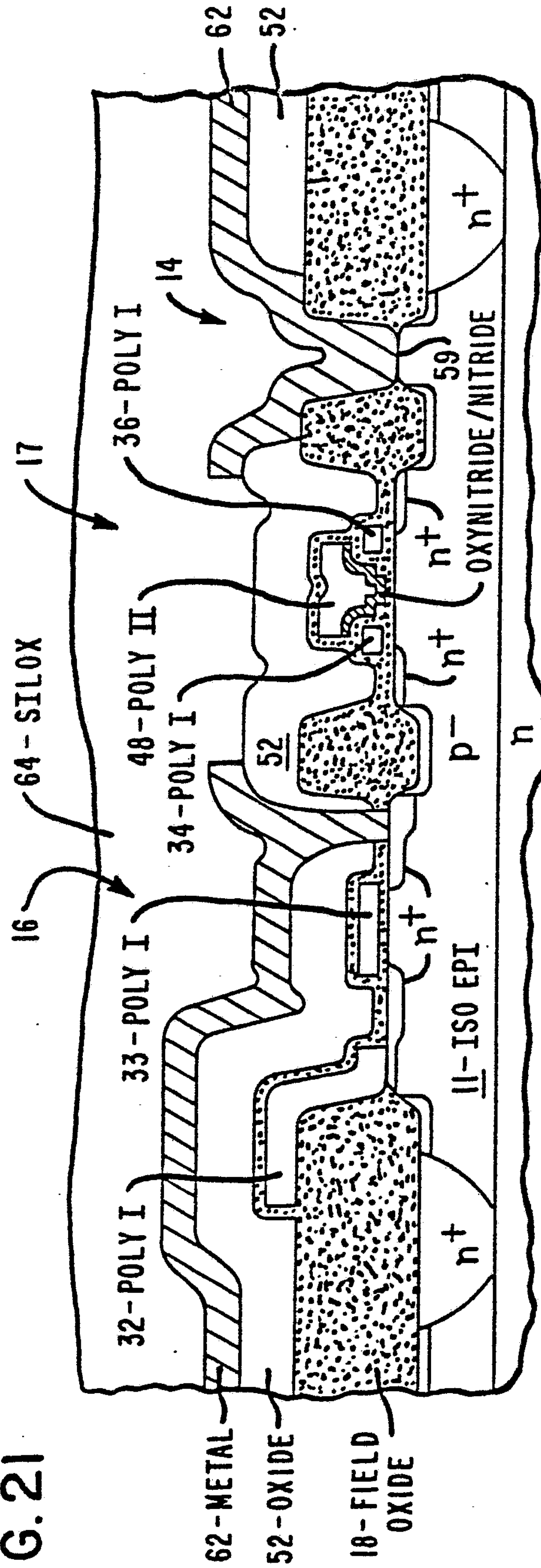

FIG. 21

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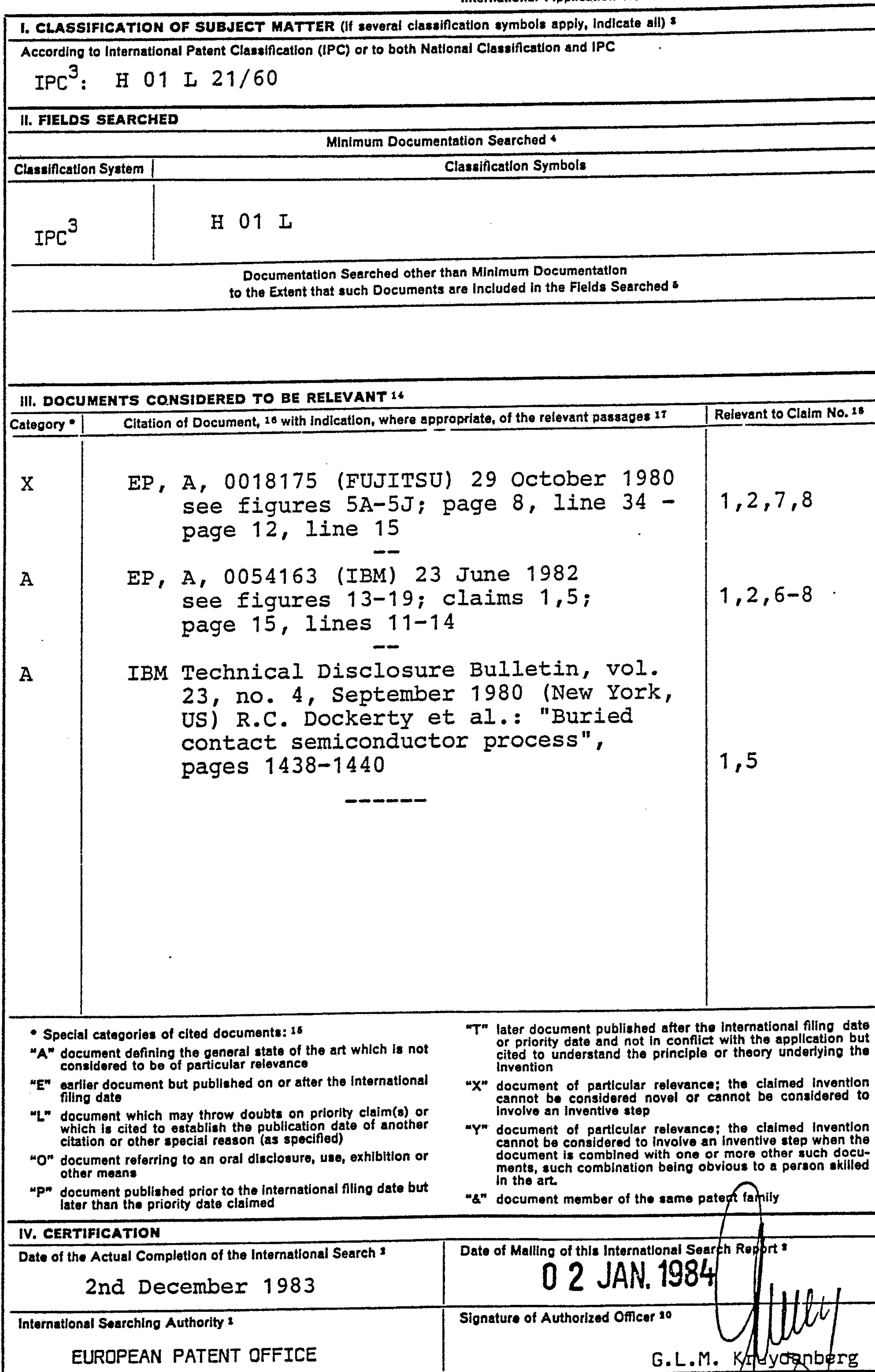

INTERNATIONAL SEARCH REPORT

International Application No PCT/US 83/01288

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC^3: H 01 L 21/60

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
IPC^3	H 01 L

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
X	EP, A, 0018175 (FUJITSU) 29 October 1980 see figures 5A-5J; page 8, line 34 - page 12, line 15	1,2,7,8
A	EP, A, 0054163 (IBM) 23 June 1982 see figures 13-19; claims 1,5; page 15, lines 11-14	1,2,6-8
A	IBM Technical Disclosure Bulletin, vol. 23, no. 4, September 1980 (New York, US) R.C. Dockerty et al.: "Buried contact semiconductor process", pages 1438-1440	1,5

* Special categories of cited documents: [15]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
2nd December 1983	02 JAN. 1984
International Searching Authority [1]	**Signature of Authorized Officer [10]**
EUROPEAN PATENT OFFICE	G.L.M. Kruydenberg

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON

INTERNATIONAL APPLICATION NO. PCT/US 83/01288 (SA 5703)

This Annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 21/12/83

The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP-A- 0018175	29/10/80	JP-A- 55138874 US-A- 4348802	30/10/80 14/09/82
EP-A- 0054163	23/06/82	JP-A- 57097679 US-A- 4341009	17/06/82 27/07/82

For more details about this annex :
see Official Journal of the European Patent Office, No. 12/82