INTEGRATED CIRCUIT BILATERAL CURRENT SOURCE

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ABSTRACT

A bilateral current source is provided for generating equal and opposite sourcing and sinking currents which are useful, for example, in linearly charging and discharging a capacitor. A reference current source utilizes a lateral PNP transistor to provide high output impedance and NPN transistor are interconnected with the lateral PNP transistor to insure that a reference current output is independent of the lateral PNP transistor's β and temperature variations. A pair of diode arrangements connect the reference current source to an opposite current generating circuit and one of the pair of diodes also connect the reference current output to a current output terminal to which a capacitor which is to be charged and discharged is connected. The opposite current generating circuit is coupled by a switch arrangement to a source of reference potential which may be ground and the switching arrangement is driven by a control voltage. When the opposite current generating circuit is floating the constant reference current flows through the one of the diode arrangements and out the current output terminal to charge the capacitor at a linear rate. When the control voltage actuates the switching arrangement, the opposite current generating circuit is grounded and the one of the pair of diode arrangements is reverse biased. The other of the diode arrangements is forward biased so that the reference current flows through the other of the diode arrangements and into the opposite current generating circuit. The opposite current generating circuit thereupon draws a current from the current output terminal which is approximately equal to the reference current so that the capacitor is linearly discharged at approximately the same rate at which it was charged.

18 Claims, 6 Drawing Figures
INTEGRATED CIRCUIT BILATERAL CURRENT SOURCE

BACKGROUND OF THE INVENTION

This invention generally pertains to an integrated circuit bilateral current source and more particularly pertains to such a bilateral current source useful in linearly charging and discharging a capacitor at the same rate.

Many integrated circuits require a bilateral current source. For example, a bilateral current source can be used to generate constant and equal sourcing and sinking currents for linearly charging and discharging a capacitor. The capacitor can be utilized as a voltage reference for a Schmitt Trigger used to drive a voltage-controlled oscillator. The stability and linearity of such an oscillator, of course, depends upon how constant and how "equal" are the sourcing and sinking currents. In order to achieve high output impedance of a current source so that the current is constant, prior art integrated circuits have utilized a lateral PNP transistor which has a high impedance looking into its collector. However, as is well known, lateral PNP transistors have very low values of current gain and are very much affected by temperature variations.

SUMMARY OF THE INVENTION

Accordingly, it is an object of this invention to provide a bilateral current source for generating equal and opposite sourcing and sinking currents.

It is another object of this invention to provide a bilateral current source for generating equal and opposite sourcing and sinking currents which utilizes a single reference current source.

It is another object of this invention to provide a reference current source for use in a bilateral current source.

It is another object of this invention to provide a reference current source for generating a constant current independent of temperature variations.

Briefly, in accordance with one embodiment of the invention, a reference current source is comprised of a lateral PNP transistor interconnected with NPN transistors to provide a reference current source having a high output impedance and producing a constant reference current independent of temperature and current gain variations in the lateral PNP transistor. The reference current output is coupled through diode means to a current output terminal to which a capacitor to be charged and discharged is connected. An opposite current generating circuit is connected to the current output terminal, and through an additional diode means to the reference current. The opposite current generating circuit also has a control input and switching means are provided which are responsive to a control voltage for connecting the control input to a reference potential. When the switching means is not actuated, the opposite current generating circuit is floating and the reference current flows through the diode means and into the capacitor for charging the capacitor. When the switching means is actuated and the opposite current generating circuit is connected to the source of reference potential, the diode means is reverse biased so that the reference current flows through the additional diode means into the opposite current generating circuit. The opposite current generating circuit thereupon draws a current from the current output terminal and hence the capacitor which is approximately equal to the constant reference current so that the capacitor is linearly discharged at a rate approximately equal to the rate at which it was charged.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is an overall circuit diagram of a bilateral current source showing it connected to a capacitor which serves as a reference voltage for a Schmitt Trigger.

FIG. 2 is a schematic circuit diagram of the reference current source of FIG. 1 with the various current relationships labeled.

FIG. 3a and FIGS. 3b, 3c are cross section and top plan views respectively of the lateral PNP transistor integrated circuit structure in the reference current source of FIG. 1 and illustrating collector to base tie back for limiting current gain thereof.

FIG. 4 is a schematic circuit diagram of the opposite current generating circuit and diode means of FIG. 1 with the various current relationships labeled.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The integrated circuit current source in accordance with this invention comprises a reference current source 11 having input terminals 12 and 13 and a reference current output terminal 14. A first source of voltage Vce is provided at a terminal 16 and a second source of voltage Vc is provided at the input terminal 13. A current-setting resistor 17 is connected between the terminal 16 and input terminal 12. The current setting resistor 17 in accordance with one embodiment of the invention is an external resistance which is external to the integrated circuit portions of this invention.

An opposite current generating circuit 18 is provided having a first current terminal 19, a second current terminal 21 and a control input terminal 22. Switching means 23 is provided and is connected between the control input terminal 22 and a source of reference potential at a terminal 24, with the reference potential in this instance being ground. The switching means 23 also has a control voltage terminal 26.

The second current terminal 21 forms a current output terminal to which a capacitor C and a Schmitt trigger 27 are connected. The Schmitt trigger 27 has an output terminal 28 which output is coupled to the control voltage terminal 26 of switching means 23. A first diode means 29 is connected between the reference current output terminal 14 and the first terminal 19 and a second diode means 31 is connected between the reference current output terminal 14 and the second current terminal 21.

In operation, the reference current source 11 has a very high impedance looking from the reference current output terminal 14 back into the reference current source 11 and establishes a constant current at the reference current output terminal 14 which is determined by the value of the voltages Vce, Vc and the value of current setting resistor 17. The constant reference current output is essentially independent of temperature variations. Assuming that the switching means 23 is not actuated so that the opposite current generating circuit 18 is floating, diode means 31 is forward biased and the reference current present at the reference cur-
rent output terminal 14 is conducted through diode means 31 and out the second current terminal 21 for charging the capacitor C. The voltage level on capacitor C controls operation, for example, of the Schmitt trigger 27. When the voltage across capacitor C builds to a predetermined level the voltage controlled oscillator 27 acting through its output on terminal 28 supplies a control voltage to the control voltage terminal 26 of switching means 23. Switching means 23 is responsive to this control voltage for connecting the control input terminal 22 of opposite generating circuit 18 to the terminal 24 and hence the source of reference potential, in this case, ground. With the opposite current generating circuit 18 grounded, diode means 31 is reverse biased and ceases conduction. The diode means 29, however, is forward biased and begins conducting the reference current from reference current output terminal 14 through switching means 23 to ground. The opposite current generating circuit 18 is responsive to the reference current flowing through the first current terminal 19 for generating an equal current from the second current terminal 21. That is, a current is drawn from the second current terminal 21 and hence the capacitor C which is equal to the reference current flowing through the first current terminal 19. Thus the capacitor C is discharged by this current drawn from the second current terminal 21. Since this current drawn from second current terminal 21 and hence the capacitor C is constant and equal in magnitude to the reference current from reference current output terminal 14 with which the capacitor was charged, the capacitor is discharged at the same rate at which it was charged. Since both the charging and discharging current for the capacitor C are constant, the charging and discharging of the capacitor C is linear. The linear variation of voltage across the capacitor C is useful in many applications and in accordance with one embodiment of the invention is used in conjunction with Schmitt trigger 27 for driving a very stable and very linear voltage controlled oscillator.

Turning now to a detailed consideration of the reference current source 11, the reference current source 11 includes transistors Q1, Q2, Q3, and Q4. The transistor Q2 is a lateral PNP transistor which has its emitter connected to the input terminal 12. The transistor Q1 is an NPN transistor having its base connected to the input terminal 13 and its collector connected to the input terminal 12. The emitter of transistor Q1 is connected to the base of transistor Q2. Transistor Q3 is an NPN transistor and has its collector connected to the emitter of transistor Q1. The emitter of transistor Q3 is connected to the reference current output terminal 14. Transistor Q4 is an NPN transistor and has its collector connected to the collector of the lateral PNP transistor Q2 and its emitter connected to the reference current output terminal 14. The base of transistor Q3 and the base of transistor Q4 are both connected to the collector of transistor Q2. A diode D1 is connected between the collector of transistor Q3 and the base of transistor Q1.

Referring now specifically to FIG. 2, there is reproduced the detailed circuitry of the reference current source with the various currents flowing therein labelled. Assuming that transistors Q3 and Q4 are matched so that the emitter current of transistor Q3, \( I_{e3} \), is equal to the emitter current of transistor Q4, \( I_{e4} \), then the output current \( I_o \) which is present at the reference current output terminal 14 is essentially independent of the current gain, \( \beta \), of the lateral PNP transistor Q2 provided that the current gain of transistor Q2 remains above some preset value which in this case is one. Thus because transistors Q3 and Q4 are matched and transistor Q4 is diode connected, \( I_{e4} \) is equal to \( I_{e3} \) since the NPN transistors Q1, Q3, and Q4 have a high current gain. Thus as long as the \( \beta \) of Q2 is greater than one, then the collector current of Q2, \( I_{c2} \), is greater than its base current \( I_{eb} \) and transistor Q1 has an emitter current \( I_{e1} \) which makes up the difference between \( I_{c2} \) and \( I_{eb} \) so as to allow the emitter currents \( I_{e2} \) and \( I_{e4} \) to be equal. The diode D1 is interconnected between the emitter and base of transistor Q1 so as to insure starting current for transistor Q1. The emitter to base voltages of transistors Q1 and Q2 approximately cancel each other. Hence the reference current output \( I_o \) is equal to the current through the current setting resistor 17, \( I_n \), plus the base current of transistor Q1, \( I_{e1} \). If the \( \beta \) of transistor Q1 is high, then its base current \( I_{eb} \) is small and \( I_o \) is given by the following equation:

\[
I_o = I_n = (V_{cc} - V_c) / R_{ext} 
\]  

(1)

The temperature coefficients of the emitter base junctions of transistors Q1 and Q2 should be similar and if \( R_{ext} \) is an external resistor with a low temperature coefficient then \( I_n \) and hence \( I_o \) are insensitive to temperature. The matching of transistors Q3 and Q4 is not critical and serves only to set the lower limit of the current gain \( \beta \) of the PNP transistor Q2. The only criteria which has to be satisfied is that the base current of transistor Q2, \( I_{eb} \), remain less than the emitter current of transistor Q3 \( I_{e3} \). For best operation the current gain \( \beta \) of the PNP transistor Q2 should be low so that transistor Q2 carries most of the current. Then the emitter current of transistor Q1, \( I_{e1} \), is small and hence its base current, \( I_{eb} \), is negligible.

In a more exact analysis of the operation of the reference current source 11 the value of the current \( I_n \) is given by the following:

\[
I_n = (V_{cc} - V_c - V_{ce} - V_{be}) / R_{ext} 
\]  

(2)

Assuming that the transistors Q3 and Q4 are matched the following equation is obtained.

\[
I_{e3} = I_{e1} + I_{e4} 
\]  

(3)

However

\[
I_e = (\beta_e + 1) / \beta_e \quad (I_c) 
\]  

(4)

for a transistor where \( I_e \) is the emitter current, \( \beta_e \) is the current gain of the transistor and \( I_c \) is the collector current. Therefore the following equation is obtained:

\[
\left( \frac{\beta_e + 1}{\beta_e} \right) I_{c1} = I_{c3} 
\]

(5)

\[
\frac{1}{\beta_{e3}} \left( 1 + \frac{1}{\beta_{e3}} \right) = I_{c3} \frac{1 - \frac{1}{\beta_{e3}}}{\beta_{e3}} 
\]

(6)

where \( \beta_{e3} \) is the NPN current gain of the transistors Q1, Q3, and Q4 and \( \beta_{e2} \) is the PNP current gain of the PNP transistor Q2. The following relationship also obtains

\[
(\beta_{e3} + 1) I_{eb} = I_{e3} (\beta_{e2} - 1) / \beta_{e2} 
\]  

(6)

The value of the current \( I_{eb} \) is also given by

\[
I_e = I_{e1} + I_{e4} + I_{eb} 
\]  

(7)
Then equation 3 becomes
\[ I_{C2} = (\beta_b + 1) I_{B1} + (I_{C1})/(\beta_b \cdot 02) \]
from which follows
\[ I_{C1} = (1/(\beta_b)) \]
from which follows
\[ I_{C3} = I_{B1}(\beta_a(\beta_a + 1) \beta_a - 1) \]
Then from Equation 8 there is obtained
\[ I_C = I_{B1}(\beta_a + 1, \beta_a(\beta_a + 1) \beta_a - 1) \]
which reduces to
\[ I_C = I_{B1}(2\beta_a + 1, \beta_a + 1) \beta_a - 1) \]
But remembering that
\[ I_0 = I_C + I_{B1} \]
then
\[ I_0 = I_C(1 + (\beta_a - 1) \beta_a - 1) \]

Thus it can be seen that the reference current output \(I_0\) assuming that the \(\beta\) of the PNP lateral transistor is greater than one but still small and that the current gain \(\beta_b\) of the NPN transistors Q1, Q3 and Q4 is relatively high (say on the order of 100), is approximately independent of variations in the current gain of the lateral PNP transistor Q2. Thus from equation 1 there is obtained
\[ I_0 = \left[ V_{RE} - V_{E} \cdot V_{DRE} + V_{BEE} \right] \left[ 1 + \frac{(\beta_b - 1)}{2\beta_b \beta_a + \beta_a + 1} \right] \]
so that under the normal condition where the NPN transistors are matched so that \(V_{RE}\) is approximately equal to \(V_{BE}\) and the current gain \(\beta_b\) of the NPN transistors is much greater than the current gain \(\beta_a\) of the PNP transistor Q2 then
\[ I_0 = \left( V_{CE} - V_{C1} \right)/(R_{EX}) \]

Thus a constant reference current \(I_0\) is obtained with there being a high impedance because of the lateral PNP transistor when looking back into the current source from the terminal 14 and, as the above analysis has shown, the output reference current \(I_0\) is approximately independent of variations in the current gain of the lateral PNP transistor Q2 due to temperature variations or other causes.

The transistor Q2 is shown in FIG. 2 as having a tie back between its base and collector. By utilizing such a tie back the current variation through transistor Q1 can be more closely controlled and made smaller. This has the effect of minimizing base current necessary to drive Q1 and hence affecting the reference current output \(I_0\).
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The second diode means 31 comprises a diode-connected lateral PNP transistor Q6 having its emitter connected to the reference current output terminal 14 and its base and collector connected to the second current terminal 21.

The opposite current generating circuit 18 comprises three NPN transistors Q7, Q8 and Q9 and two matching resistors R1 and R2. The transistor Q7 has its collector connected to the second current terminal 21 and its base connected to the first current terminal 19. The transistor Q8 has its collector connected to the first current terminal 19 and its base connected to the emitter of transistor Q7. A transistor Q9 has its collector connected to the emitter of transistor Q7 and its base also connected to the emitter of transistor Q7. The emitter of transistor Q8 is connected through matching resistor R1 to the control input terminal 22 and the emitter of transistor Q9 is connected through a matching resistor R2 to the control input terminal 22.

Switching means 23 is adapted upon receipt of a control voltage at its control terminal voltage terminal 26 to connect the control input terminal 22 to a terminal 24 which is at a reference potential, which in this case is ground. Switching means 23 comprises an NPN transistor Q10, a PNP transistor Q11 and an NPN transistor Q12. The transistor Q10 has its collector connected to the control input terminal 22 and its emitter connected to the terminal 24. Transistor Q11 is diode connected having its collector and base electrodes connected to the control input terminal 22 and its emitter connected to the control voltage terminal 26. Transistor Q12 is also diode connected having its base connected to the control voltage terminal 26, its collector connected also to the control voltage terminal 26 and its emitter connected to the base of transistor Q10. A bleeder resistor R3 is connected between the base and emitter of transistor Q10. Transistor Q10 is the switching transistor and is adapted to be turned on for connecting the control input terminal 22 to the terminal 24 upon receipt of a control voltage on control voltage terminal 26. The transistors Q12 and Q11 which are diode connected are provided merely to ensure that the collector of transistor Q10 is held at some voltage slightly above ground in order to prevent saturation of transistor Q10 and provide for rapid switching thereof.

Turning now to a consideration of FIG. 4 there is reproduced the opposite current generating circuit and first and second diode means with various currents labelled thereon for facilitating discussion of the operation of the first and second diode means and the opposite current generating circuit. Assuming first of all that the switching means 26 is not actuated or "on", then the opposite current generating circuit 18 is floating and the reference current Iq from the reference current output terminal 4 is conducted through the diode connected PNP transistor Q6 to terminal 21 and hence to the capacitor C for charging the capacitor C. Since the reference current Iq is constant and independent of temperature variation the capacitor C is linearly charged with the voltage thereon building up in a linear fashion.

Assume now, however, that the switching means 26 has been actuated so that the control input terminal 22 is connected to the terminal 24 at the source of reference potential which in this case is ground. When the switching means 26 is actuated the voltage at the collector of transistor Q5 drops to a relatively low voltage which may be, for example on the order of 2.5 volts while the voltage at the second current terminal 21 due to the charge accumulating on the capacitor C is considerably higher, on the order of 10 volts for example. Thus the diode-connected lateral PNP transistor Q6 is reverse biased. The reason for using a lateral PNP transistor is because it has a much higher reverse voltage breakdown than an NPN emitter base junction and consequently allows operation over a much larger range of supply voltages. A collector-base shorted lateral PNP transistor is used for transistor Q6 rather than the collector-base junction of an NPN transistor in order to minimize current loss to the integrated circuit substrate through parasitic PNP action.

With the diode connected transistor Q6 reverse biased the reference current Iq from the reference current output terminal 14 flows through the diode connected transistor Q5 and the first current terminal 19 into the reverse current generating circuit 18. The opposite current generating circuit 18 includes three transistors, Q7, Q8, and Q9 and may include two matching resistors R1 and R2 which are shown in FIG. 1 but which are omitted for simplicity in FIG. 4. An opposite current generating circuit similar to that is shown in FIGS. 1 and 4 is described in an article entitled "A Monolithic Junction FET-n-p-n Operational Amplifier" by George R. Wilson appearing at pages 339-344 of the IEEE Journal of Solid-State Circuits, Volume SC-3, No. 4, Dec., 1968.

Assuming that the reference current Iq flows from the first current terminal 19, the opposite current generating circuit is adapted to draw a current Iq from the second current terminal 21 and hence the capacitor C which, as will be demonstrated, is very nearly equal to the reference current Iq. In FIG. 4 the currents which are flowing in various parts of the opposite current generating circuit have been labelled with the quantity β referring to the current gain of transistors Q7, Q8 and Q9 which are all assumed to be equal. Thus the base current flowing in the base of transistor Q7 is given by (Iq/β) and the emitter current of transistor Q7 is given by (β+1)(β) (Iq). The collector current of transistor Q8 is given by Iq = (Iq/β). The base current of transistor Q8 is given by (1)(β) (Iq - Iq)(β). The emitter current Iq of transistor Q8 is thus given by

Iq = (Iq/β) + (1)(β) (Iq - Iq)(β).

The emitter current Iq of transistor Q9 is given by

(β+1)(β) Iq - (1)(β) (Iq - Iq)(β).

Since the transistor Q9 is diode connected, then the emitter currents Iq and Iq of transistors Q8 and Q9, respectively, are equal so that

Iq = Iq = (1) - (2)/β + 2

which when rearranged gives

Iq = Iq (1 - (2)/β + 2)
emitter current $I_{em}$ of transistor Q8 is equal to the emitter current $I_{em}$ of the transistor Q9. It can be seen from an inspection of equation 19 that the discharge current $I_{d}$ which is drawn from the second current terminal 21 and hence the capacitor C, is approximately equal to the reference current $I_0$, which it will be recalled was used to charge the capacitor C. Assuming that $\beta$ which is the current gain for transistors Q7, Q8 and Q9, is on the order of 100, then an inspection of equation 19 shows that the currents $I_{em}$ and $I_{d}$ will be very nearly equal. The capacitor C is discharged by the current $I_{d}$ which is very nearly equal to the reference current $I_0$ which was used to charge the capacitor C. Thus the capacitor C is discharged in a linear fashion at approximately the same rate at which it was charged.

The sinking or discharge current $I_{d}$ can be made any proportion of the sourcing or charging current $I_0$ by adjustment of the values of the matching resistors R1 and R2 and the emitter areas of the transistors Q8 and Q9. This happens because the sinking current $I_{d}$ which is generated by the opposite current generating circuit is determined by the reference current $I_0$ and the voltage it sets up on the base of transistor Q9. For example, if matching resistor R2 is one-half the value of matching resistor R1 and the emitter area of transistor Q9 is twice the area of the emitter of transistor Q8, then the emitter current $I_{em}$ of transistor Q9 would be equal to twice the emitter current $I_{em}$ of transistor Q8 since the base voltages of transistors Q8 and Q9 are necessarily equal. Thus it is within the skill of one versed in the integrated circuit art to vary the proportions of the sourcing and sinking current $I_0$ and $I_{d}$, respectively, to provide a ratio between the charging and discharging rate of the capacitor C.

Thus what has been described is a bilateral current source for providing linear and approximately equal sourcing and sinking currents for charging and discharging a capacitor in a linear and equal fashion. An improved constant current source utilizing a lateral connected PNP transistor is provided for generating a reference current source having a high impedance and a reference current output independent of current gain variations in the PNP transistor due to temperature variations by providing inter-connected PNP transistors. The constant reference current output is used to charge a capacitor in a linear fashion. An opposite current generating circuit is provided for generating a sinking current for discharging the capacitor which is very nearly equal to the reference current so that the capacitor is alternately charged and discharged at a linear rate for driving, for example, in conjunction with a Schmitt trigger, a linear and stable voltage controlled oscillator.

What is claimed is:

1. In combination, an integrated circuit bilateral current source for generating approximately equal sourcing and sinking currents for charging and discharging a capacitor in response to a control voltage comprising: a first source of voltage and a second of voltage; a current reference source having first and second input terminals and a reference current output terminal; a current setting resistor connected between said first source of voltage and said first input terminal; connecting means for connecting said second source of voltage to said second input terminal whereby a constant reference current appears on said reference current output terminal; an opposite current generating circuit having a control input terminal and first and second current terminals, said second current terminal also adapted to be connected to the capacitor for charging and discharging the capacitor, first diode means connected between said reference current output terminal and said first current terminal; second diode means connected between said reference current terminal and said second current terminal; a reference potential terminal; and switching means responsive to the control voltage for coupling said control input terminal to said reference potential terminal whereby when the switching means is not actuated the constant reference current flows through said second diode means and said second current terminal for charging the capacitor and whereby when said switching means is actuated said second diode means is reverse biased so that the constant reference current flows through said first diode means and said first current terminal into said opposite current generating circuit which draws a current from said second current terminal for discharging the capacitor which is approximately equal to the constant reference current whereby the capacitor is discharged at the same rate at which it was charged.

2. The combination of claim 1 wherein said reference current source comprises a PNP transistor having its emitter connected to said first input terminal, a first NPN transistor having its collector connected to the collector of said PNP transistor and its emitter connected to said reference current output terminal, a second NPN transistor having its collector connected to the emitter of said PNP transistor and its emitter connected to the base of said NPN transistor, the base of said second NPN transistor being connected to said second source of voltage, a third NPN transistor having its collector connected to the base of said PNP transistor and its emitter connected to said reference current output terminal, the base of both said first and third NPN transistors being connected to the collector of said PNP transistor to cause equal base-emitter voltages to appear across said first and third NPN transistors whereby the emitter currents of said first and third NPN transistors are equal and approximately independent of the current gain of said PNP transistor.

3. The combination of claim 2 wherein said reference current source includes a diode connected between the emitter and base of said second NPN transistor to insure starting current therefore.

4. The combination of claim 2 wherein said PNP transistor is a lateral integrated circuit transistor and wherein said PNP transistor has collector-to-base tie back in order to limit its current gain.

5. The combination of claim 4 wherein said collector to base tie back is in the ratio of 2:1 whereby the PNP transistors current gain will be less than two.

6. The combination of claim 1 wherein said opposite current generating circuit comprises fourth and fifth transistors serially coupled between said second current terminal and said control input terminal, a sixth transistor serially coupled between said first current terminal and said control input terminal, the base of said fourth transistor connected to the collector of said sixth transistor, and the bases of said fifth transistor and said sixth transistor connected to the collector of said
fifth transistor to cause equal base-emitter voltages to appear across said fifth and sixth transistors when said switching means is actuated whereby equal emitter currents flow from said fifth and sixth transistors when said switching means is actuated.

7. The combination of claim 6 wherein said first and second diode means comprise diode-connected transistors.

8. The combination of claim 7 wherein said second diode means comprises a lateral PNP diode-connected transistor able to withstand a relatively high reverse bias voltage.

9. The combination of claim 1 wherein said switching means comprises a seventh transistor serially coupled between said control input terminal and said reference potential terminal and adapted to be turned on by the control voltage to connect said control input terminal to said reference potential terminal.

10. The combination of claim 9 wherein said seventh transistor includes base-collector diode means for holding the collector thereof at a potential higher than the potential of said reference potential terminal to prevent saturation of said seventh transistor.

11. An opposite current generating circuit adapted to be connected to a capacitor for charging and discharging the capacitor at equal rates in accordance with a control voltage comprising: a constant current source having a reference current output terminal into which a constant reference current flows; a control input terminal; a reference potential terminal; switching means responsive to the control voltage for connecting said control input terminal to said reference potential terminal; first and second current terminals, said second current terminal adapted to be connected to the capacitor which is to be charged and discharged; first diode means connected between said reference current output terminal and said reference current terminal; second diode means connected between said reference current output terminal and said second current terminal; a pair of transistors serially coupled between said second current terminal and said control input terminal; an additional transistor serially coupled between said first current terminal and said control input terminal, the base of one of said pair of transistors coupled to the collector of said additional transistor and the base of the other of said pair of transistors and the base of said additional transistor coupled to the collector of said other of the pair of transistors whereby when said switching means is not actuated said second diode means is forward biased and the constant reference current flows therethrough and out through the second current terminal to linearly charge the capacitor, and whereby when said switching means is then actuated said second diode means is reverse biased and said first diode means is forward biased so that the constant reference current flows through said first diode means and said additional transistor and out the emitter thereof so that said other of said pair of transistors which has a base-emitter voltage equal to the base-emitter voltage of said additional transistor has an emitter current approximately equal to the emitter current of said additional transistor with said emitter current of said other of the pair of transistors being drawn from the capacitor through the second current terminal and said one of the pair of transistors so that the capacitor is linearly discharged at approximately the same rate it was charged.

12. An opposite current generating circuit in accordance with claim 11 wherein said second diode means comprises an integrated circuit lateral PNP diode-connected transistor able to withstand a relatively high reverse bias voltage.

13. An opposite current generating circuit in accordance with claim 11 wherein said switching means comprises a switching transistor connected between said reference potential and said control input terminal and responsive to the control voltage for connecting said reference potential terminal to said control input terminal.

14. An opposite current generating circuit in accordance with claim 13 wherein said switching transistor includes base-diode means for holding the collector thereof at a potential higher than the potential of said reference potential terminal to prevent saturation of said switching transistor.

15. A reference current source for producing a constant, temperature-independent current at an output terminal and exhibiting a high impedance looking from the output terminal in the reference current source comprising: a first source of voltage and a second source of voltage; first and second input terminals; a current-setting resistor connected between said first source of voltage and said first input terminal; connecting means for connecting said second source of voltage to said second input terminal; a PNP transistor having its emitter connected to said first input terminal, a first NPN transistor having its collector connected to the collector of said PNP transistor and its emitter connected to said reference output terminal, a second NPN transistor having its collector connected to the emitter of said PNP transistor and its emitter connected to the base of said PNP transistor, the base of said second NPN transistor being connected to said second source of voltage, a third NPN transistor having its collector connected to the base of said PNP transistor and its emitter connected to the output terminal, the base of both said first and third NPN transistors being connected to the collector of said PNP transistor to cause equal emitter voltages to appear across said first and third NPN transistors whereby the emitter currents of said first and third NPN transistors are equal and approximately independent of the current gain of said PNP transistor.

16. A reference current source in accordance with claim 15 including a diode connected between the emitter and base of said second NPN transistor to insure starting current therefore.

17. A reference current source in accordance with claim 15 wherein said PNP transistor is a lateral integrated circuit transistor and wherein said PNP transistor has collector-to-base tie back in order to limit its current gain.

18. A reference current source in accordance with claim 17 wherein said collector to base tie back is in the ratio of 2:1 whereby the PNP transistors current gain will be less than two.