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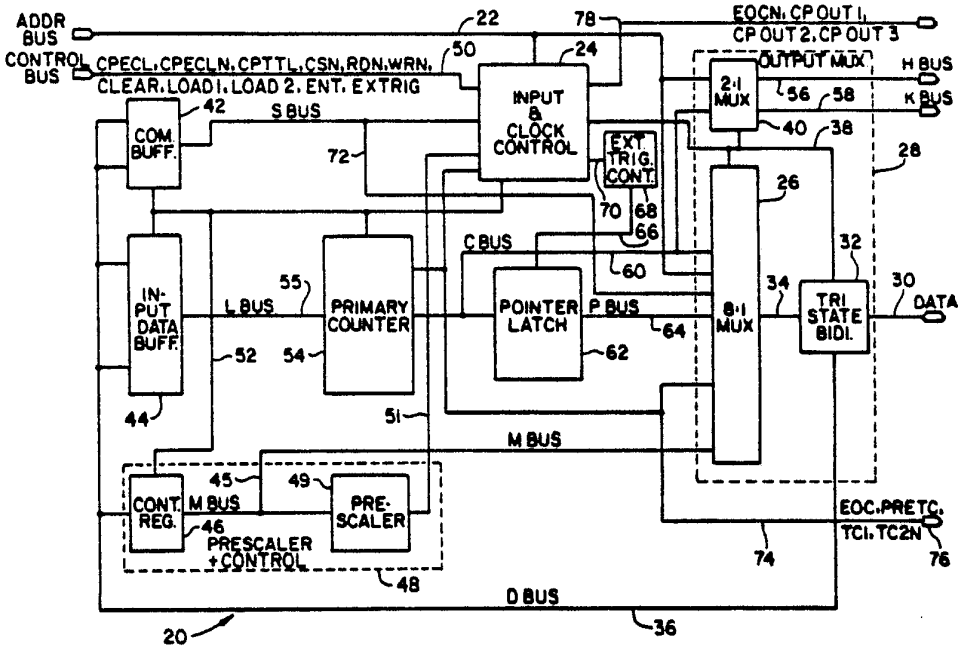

(57) Abstract

Universal programmable modules provide timing and/or address register functions for a broad family of test instruments: such as counter timers, arbitrary function generators, and real time digitizers. The computer programmable apparatus (20) can be used as an accumulator, a time base generator or a memory address register. A clock input (50) receives a clock input signal. A computer input (32), which may include a bidirectional data bus (30), receives inputs from a computer. A processor (24) processes at least one of the clock input signal and the input from the computer to produce at least one output (56, 58, 78). A control circuit (50) controls the processor in accordance with further input from the computer to determine the output produced. An output selector (28), which may include a multiplexer (40) for directly addressing memory, selects at least one output to be used externally of the apparatus.

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UNIVERSAL PROGRAMMABLE COUNTER/TIMER AND ADDRESS REGISTER MODULE

The present invention relates to universal programmable modules for providing timing and/or address register functions for a broad family of test instruments. More particularly, the invention relates to a microcomputer programmable time base generator for counter timers, arbitrary function generators, real time digitizers, and pin electronics stimulus response generators; and to an address register module useful for regulating the flow of data into and out of an instrument memory.

Electronic instruments designed for use in automatic test equipment must have precise and accurate time base generators and accumulators. Further in order to assure some degree of flexibility in test procedures such time base generators must be programmable in a variety of modes so as to be useful in instruments such as counter timers, arbitrary function generators and real time digitizers. In addition, it is necessary for such instruments to interact with a computer or microcomputer which directs instrument operation and acquires data generated by the instrument.

Conventional instrument time base generators and computer memory interfaces require extensive logic circuits to perform the complex functions required for the instrument to operate and to be properly interfaced to the microcomputer. Such logic circuits generally require the use of many integrated circuits. Design costs are high for each specialized circuit. Hardware costs are also high. A great deal of circuit board area is required for such circuits, further increasing costs. Power consumption tends to be high, thus generating excessive heat levels. Reliability is often not as high as would be desirable and trouble shooting is difficult and time consuming.

In accordance with the invention, a programmable apparatus useful as a counter/timer, time base generator, and memory address control or register is provided. The apparatus includes a clock input means for receiving a clock input signal and a computer input means for providing input from a computer. A processing means processes at least one of the clock input signal and the input from the computer to produce at least one output. A control means controls the processing means in accordance with further input from the computer to determine the output produced. An output selecting means selects at least one output to be provided for use externally of the apparatus.

The output selecting means, which includes at least one multiplexer, selects at least one output in response to additional input from the computer. The multiplexer has circuits useful for directly addressing a memory.

The processing means includes a counter responsive to the clock input signal. Means for preloading the counter in accordance with the input from the computer are also provided. A register stores the count in the counter.

The computer input means includes a bidirectional data means for receiving and transmitting data. It also includes an input data buffer for storing data to be loaded into the counter. In addition, the computer input means includes a command buffer or register for storing the further input from the computer.

The registers and the counter provide outputs to the output selecting means.

If the frequency of the clock is high, a programmable prescaler may be provided to divide the frequency to one suitable for use by the counter. The prescaler is programmable in accordance with input from the computer.

In order that the invention may be readily carried into effect, it will now be described with reference to the accompanying drawings, wherein FIG. 1 is a block diagram of a universal programmable counter/timer an address register module according to the invention; FIG. 2A is a schematic diagram of a portion of the output multiplexer of FIG. 1; FIG. 2B is a schematic diagram of an additional portion of the output multiplexer of FIG. 1; FIG. 2C is a schematic diagram of yet another portion of the output multiplexer of FIG. 1; FIG. 2D is a schematic diagram of the remaining portion of the output multiplexer of FIG. 1; FIG. 3 is a schematic diagram of the command buffer of FIG. 1; FIG. 4 is a schematic diagram of the input data buffer of FIG. 1; FIG. 5 is a schematic diagram of the primary counter of FIG. 1; FIG. 6 is a schematic diagram of the pointer latch and external trigger countrol of FIG. 1; FIG. 7A is a schematic diagram of a portion of the prescaler and control of FIG. 1; FIG. 7B is a schematic diagram of the remainder of the prescaler and control of FIG. 1; FIG. 8 is a schematic diagram of the input controls portion of the input and clock control of FIG. 1; FIG. 9 is a schematic diagram of the clock controls portion of the input and clock control of FIG. 1; FIG. 10 is a block diagram of a counter utilizing

three of the modules of FIG. 1; FIG. 11 is a block diagram of an arbitrary function generator utilizing three of the modules of FIG. 1; FIG. 12 is a block diagram of a real time digitizer utilizing three of the modules of FIG. 1; and FIG. 13 is a block diagram of a digital word generator utilizing two the modules of FIG. 1.

The apparatus of the present invention is preferably constructed by depositing two layers of metallization on a gate array of the type commonly available from semiconductor manufacturers such as Applied Micro Circuits Corporation of San Diego, California. The resulting semiconductor chip may be packaged as a 100 pin grid array. While occupying an area of only 1.25 inches by 1.25 inches on a circuit board and having a height of approximately 0.2 inches, such design and packaging permits the module of the present invention, in applications where the circuitry thereon is fully utilized, to replace approximately 60 to 70 conventional SSI/MSI integrated circuits.

As an aid to understanding the drawings, it is noted that inputs or outputs of circuits having pin designation symbols in the form of a five sided figure are shown in bold print if lead out externally of apparatus 20 and are not in bold print when used internally.

As a further aid to understanding FIGS. 1 to 9, the following table designates the symbols used to represent the various buses of the apparatus of the invention.

BUS	DESIGNATION
address bus 22	ADDR
internal data bus 36	DBUS
programming bus 45	MBUS

load bus 55	LBUS
count bus 60	CBUS
latch bus 64	PBUS
status bus 72	SBUS

The following symbols used in FIGS. 1 to 9 and their meanings are set forth below:

E/E	ECL to ECL operation
T/E	TTL to ECL operation
S	Output cell
FF	flip flop
H	high speed gate
1.2, 1.3, etc.	nsec delay of gate

All references in FIGS. 1 to 9 to ground imply a connection to ECL logic zero.

Referring to the block diagram of FIG. 1, in order for the apparatus 20 of the present invention to be compatible with a microcomputer (not shown), interconnections are provided for various functions. An address function provided by data on a 12 bit address bus 22 permits the microcomputer to designate a certain portion of memory for use with apparatus 20. The data on address bus 22 is provided to input and clock control 24 and to a 8:1 multiplexer 26 of output multiplexer 28 (FIGS. 2A, 2B, 2C and 2D). The three least significant bits (binary 0, 1 and 2) of address bus 22 are used to designate which of three internal registers of apparatus

20 are to be loaded or read, as more fully described below.

Data from the microcomputer memory designated may be supplied to apparatus 20, or data from apparatus 20 may be provided to the memory by means of a bidirectional tristate data bus 30 which may be of a conventional 8 bit type, or of 16 bits or more for greater precision. A tristate bidirectional receiver/driver circuit 32 (FIGS. 2A, 2B, 2C and 2D) terminates the end of bus 30 associated with apparatus 20. Data from the output of multiplexer 26 may be provided to the input of receiver/driver circuit 32 by internal bus 34. This data is then placed on bidirectional data bus 30 to be provided to the microcomputer. Data appearing on bus 30 is routed to the 8 bits of internal data bus 36 to be distributed to selected registers of apparatus 20. The direction of operation of receiver/driver circuit 32 is determined by a control signal from input and clock control 24 provided on bus 38. Bus 38 also provides control signals to 8:1 multiplexer 26 and 2:1 multiplexer 40 (FIGS. 2A, 2B, 2C and 2D) of output multiplexer 28.

Data on internal data bus 36 is provided to command buffer 42, input data buffer 44 and control register 46 of prescaler and control 48 (FIGS. 7A, 7B).

Also necessary for interconnection of apparatus 20 to the microcomputer is a control bus 50 which provides inputs to input and clock control 24 for a chip select

function, a clear function for an unconditional clear for initialization of registers and counters when power is turned on, read and write functions, and other functions as more fully described below. It is also necessary that timing functions on apparatus 20 be synchronized by an external clock (not shown). To this end, an ECL compatible input terminal is provided for a 100 MHz clock signal supplied as an input to prescaler 49 of prescaler and control 48 and a TTL input terminal is provided for lower frequencies as more fully described below. Prescaler 49 is programmed to provide various time bases by signals on a programming bus 45 from control register 46 in accordance with command signals from input and clock control 24 appearing on bus 52. Bus 52 also supplies command signals from input and clock control 24 to command buffer 42, input data buffer 44, and a primary counter 54. Pulses from prescaler 49 are conducted to input and clock control 24 by line 51.

Data from apparatus 20 is provided directly to the memory of the microcomputer (without the need to do a block transfer of data) by means of a 12 bit ECL output bus 56 or a 12 bit TTL output bus 58, with the data thereon provided by outputs of 2:1 multiplexer 40. Multiplexer 40 can provide, on buses 56 and 58, data from a first group of its inputs connected to address bus 22 or from a second group of its inputs connected to a count bus 60 having data thereon corresponding to the count of primary counter 54. Primary counter 54 may be preloaded

with data from input data buffer 44 carried by load bus 55.

Any one of eight different inputs to 8:1 multiplexer 26 can be placed on bidirectional data bus 30 by way of bus 34 to the tristate receiver/driver circuit 32 under the direction of control signals on bus 38. The first two inputs of 8:1 multiplexer 26 are connected to the same buses as the inputs of 2:1 multiplexer 40; that is count bus 60 and address bus 22.

A third input to multiplexer 26 is provided by the output of a pointer latch 62 by way of a latch bus 64. Pointer latch 62 (FIG. 6) stores the count from primary counter 54 provided by count bus 60 when directed to do so by a signal on line 66 from external trigger control 68. This signal on line 66 is synchronized to clock by a clock pulse provided to external trigger control 68 on line 70 from input and clock control 24.

A fourth input to multiplexer 26 is the data on a status bus 72 originating at command buffer 42. The data on status bus 72 is also supplied to input and clock control 24. This data is representative of the state of certain selected signals, some of which are not necessary to the operation of apparatus 20, but serve to facilitate a determination, made by automatic test equipment, as to whether apparatus 20 is functioning properly.

Another input to multiplexer 26 is provided by a counter state bus 74 which originates at primary counter

54 and provides data indicative of the state of counter 54. Counter state bus 74 also provides an input to input and clock control 24. Bus 74 is also lead out externally of apparatus 20 to a series of pins represented by 76 to provide the signals on bus 74 directly.

An additional input to multiplexer 26 is data from programming bus 45 as noted above, and as more fully described below.

A clock pulse output line 78 provides clock pulses and other outputs from input and clock control 24 externally of apparatus 20 as more fully described below.

Reference is made to FIGS. 2A, 2B, 2C and 2D for the details of output multiplexer 28 of FIG. 1. Each bit of address bus 22 is terminated in one of receivers 80A to 80L. The output of each receiver 80A to 80L is supplied to a respective driver 81A to 81L. The output of each driver 81A to 81L is supplied to a respective first input of respective multiplexers 40A to 40L which together constitute 2:1 multiplexer 40 (FIG. 1). The respective second inputs of multiplexers 40A to 40L are connected to corresponding bits of count bus 60. The selector input S of each of multiplexers 40A to 40L is connected to a line corresponding to bit 3A of status bus 72 (SBUS3). Thus, the state of said bit of status bus 72 determines whether the contents of address bus 22 or that of county bus 60 is provided by the collective outputs of multiplexers 40A to 40L.

The inputs of respective ECL drivers 82A to 82L are each provided with the respective output of respective multiplexers 40A to 40L. The outputs of drivers 82A to 82L collectively constitute the bits of ECL output bus 56. The respective inverted outputs of multiplexer 40A to 40L are provided to respective inverters 84A to 84L, which in turn provide inputs for TTL drivers 86A to 86L. The outputs of drivers 86A to 86L collectively constitute the bits of TTL output bus 58.

A respective inverter/driver 88A, 88C (FIG. 2A) and 88E (FIG. 2B) is provided for each of the three least significant bits of address bus 22. The outputs of inverter/drivers 88A, 88C and 88E are designated as IA0 IA1 and IA2. An additional inverter/driver 88E' (FIG. 2B) is connected to the inverted output of input buffer 80E thus providing an output IA2N (or A2; that is, the logical opposite of A2). Outputs IA0, IA1, IA2 and IA2N are used internally for register selection as noted above, and as more fully described below.

A series of 16 4:1 multiplexers 26A to 26H and 26A' to 26H' (FIGS. 2A, 2B, 2C and 2D) collectively constitute 8:1 multiplexer 26 (FIG. 1). Multiplexers 26A to 26H and 26A' to 26H' each have four data inputs I0, I1, I2 and I3. The presence of logic high or low on data select inputs S0 and S1 determines which of the four inputs I0, I1, I2 and I3 is presented at data output Y. Such output is not presented until an appropriate enable signal is present at enable input EN.

Multiplexers 26A to 26H and 26A' to 26H' operate in pairs, thus permitting one of two eight bit bytes to be presented on bidirectional tristate data bus 30. More specifically, the enable inputs of a first group of multiplexers 26A to 26H are connected so as to assume the logic states of IA2. On the other hand, the enable inputs of a second group of multiplexers 26A' to 26H' are connected to IA2N. Thus either the first group is enabled, or the second group is enabled, but never both groups. Further, the data outputs Y of each pair of multiplexers 26A and 26A', 26B and 26B', etc. are connected to a respective OR gate 90A to 90H. It will be noted that OR gates 90A to 90H are simple wire OR gates, thus enhancing speed of operation. The respective outputs of OR gates 90A to 90H are connected to respective inputs of input buffers 92A to 92H of respective receiver/driver 32A to 32H which collectively constitute receiver/driver circuit 32.

The outputs of buffers 92A to 92H are connected to respective drivers 94A to 94H of receiver/drivers 32A to 32H. Drivers 94A to 94H each have a control input. When an output enable signal OUTEN is applied to the control inputs, drivers 94A to 94H present data on bidirection tristate data bus 30.

The outputs of drivers 94A to 94H are also supplied to respective receivers 96A to 96H of receiver/drivers 32. The outputs of receivers 96A to 96H are in turn supplied to the inputs of respective drivers 98A to 98H.

The outputs of drivers 98A to 98H provide the 8 bits of data on internal data bus 36. When drivers 94A to 94H are enabled by OUTEN the data supplied to bidirectional tristate bus 30 and internal data bus 36 is that from OR gates 90A to 90H originating at the output of the first group of multiplexers 26A to 26H or the data originating at the output of the second group of multiplexers 26A' to 26H'. When drivers 94A to 94H are not enabled by OUTEN, the tristate output of drivers 94A to 94H are in an open condition. Data on bidirectional tristate data bus 30 then appears at the inputs of receivers 96A to 96H, and also as the above mentioned 8 bits of data on internal data bus 36.

The outputs of drivers 81A to 81L, which represent the 12 bits of address bus 22, and are applied to the I0 input of one of multiplexers 26A to 26M and 26A' to 26M'. With reference to FIG. 2A, the least significant bit, or zero bit, A0 is applied to the I0 input of multiplexer 26A. The least significant bits of count bus 60, latch bus 64 and status bus 72 are applied to inputs I1, I2 and I3, respectively of multiplexer 26A. The eighth bit, A8 of address bus 22 is applied to input I0 of multiplexer 26A' by driver 81B. The eighth bits of count bus 80, latch bus 64 and status bus 72 are applied to input I1, I2, and I3, respectively, of multiplexer 26A'.

The second least significant bit, or 1 bit, A1 of address register 22 is applied to the I0 input of multi-

plexer 26B by driver 81C. Corresponding bits of count bus 60, latch bus 64 and status bus 72 are applied to inputs I1, I2 and I3, respectively of multiplexer 26B. The ninth bit of address bus 22 is applied to the input of multiplexer 26B' by driver 81D. Corresponding bits of count bus 60, latch bus 64 and status bus 72 are applied to inputs I1, I2 and I3, respectively of multiplexer 26B'.

Select inputs S0 of multiplexer 26A, 26A', 26B and 26B' are connected to the output of driver 81A while select inputs S1 of multiplexer 26A, 26A', 26B and 26B' are connected to the output of driver 81C. Thus, the logic values of bits A0 and A1 of address bus 22 determine which input to multiplexer 26A, 26A', 26B and 26B' is present at the respective Y outputs.

The outputs of multiplexers 26A to 26H and 26A' to 26H' are each determined in accordance with the following table:

Select Inputs		Output
S0	S1	Y
0	0	I0
0	1	I1
1	0	I2
1	1	I3

Thus, the values of bits A0 and A1 select which corresponding bit's logic value of four buses (address bus 20, count bus 60, latch bus 64 or status bus 72) is presented at the output of multiplexers 26A, 26A', 26B

and 26B'. However, logic values of IA2 and IA2N determine which byte the bit is actually selected from. For example, the logic value of either the least significant bit (0 bit) or the eighth bit of the selected bus is presented at the output of driver 94A to become the least significant bit of internal data bus 36 and the least significant bit of bidirectional tristate data bus 30 if OUTEN is at the appropriate logic level. In a similar manner, the logic value of the 1 bit or the 9 bit of the selected bus is presented at the output of driver 94B to become the value of the 1 bit of internal data bus 36 and of tristate data bus 30 if OUTEN is at the appropriate logic level.

Referring to FIG. 2B, bits 2 of the same four buses are supplied as inputs to multiplexer 26C, while the 10 or A bits are supplied as inputs to multiplexer 26C'. The three bits of the same buses are supplied as inputs to multiplexer 26D while the 11 or B bits are supplied to multiplexer 26D'. Select inputs S0 of multiplexers 26C, 26C', 26D and 26D' are controlled by the value of IA0, while select inputs S1 of said multiplexers are controlled by the value of IA1. Thus, the logic value of either the 2 or 10 bit appears as bit 2 of internal data bus 36 (and if required as bit 2 of bus 30). The logic value of either the third bit or the eleventh bit appears as bit 3 of internal data bus 36.

Referring to FIG. 2C, the bit 4 inputs of address bus 22, count bus 60, latch bus 64 and status bus 72 are

supplied to inputs I0, I1, I2 and I3, respectively, of multiplexer 26E. The 0 bit of programming bus 45 is supplied to the I0 input to multiplexer 26E'. The 12 bit or C bit of count bus 60 is supplied to the I1 input of multiplexer 26E'. The output of a trigger flip-flop (FIG. 6) is supplied to the I2 input of multiplexer 26E', while the I3 input is connected to ground.

The bit 5 lines of address bus 22, count bus 60, latch bus 64 and status bus 72 are connected to inputs I0, I2, I2 and I3, respectively, of multiplexer 26F. The 1 bit of programming bus 45 is supplied to the I0 input of multiplexer 26F'. Bit 13 or D of count bus 60 is supplied to the I1 input of multiplexer 26F'. The end of count output of a flip flop associated with primary counter 54 (FIG. 5) is supplied to the I2 input of multiplexer 26F', while the I3 input is connected to ground.

Select inputs S0 of multiplexers 26E, 26E', 26F and 26F' are controlled by the logic value of IA0, while select inputs S1 are controlled by the logic level of IA1. As noted above, logic values of IA2 and IA2N control which output of multiplexers 26E and 2E' appears at the output of driver 94E and which output of multiplexers 26F and 26F' appears at the output of driver 94F.

Referring to FIG. 2D, bit 6 of address bus 22, count bus 60, latch bus 64 and status bus 72 are supplied to the I0, I1, I2 and I3 inputs, respectively, of multiplexer 26G. Bit 2 of programming bus 45 is sup-

plied to the I0 input of multiplexer 26G'. Bit 15 or E of count bus 60 is supplied to the I1 input of multiplexer 26G'. The logical inverse of the top count output of primary counter 54 (FIG. 5) is applied to the I2 input of flip flop 26G', while the I3 input is grounded.

The bit 7 lines of address bus 22, count bus 60, latch bus 64 and status bus 72 are connected to the I0, I1, I2 and I3 inputs, respectively, of multiplexer 26H. Bit 3 of programming bus 45 is connected to input I0 of multiplexer 26H and bit 16 or F of count bus 60 is connected to the I1 input. The I2 input is connected to signal TCNTC1 (FIG. 5) from primary counter 54.

Select lines S0 of multiplexers 26G, 26G', 26H and 26H' are controlled by the logic level of IA0, while select lines S1 are controlled by the logic level of IA1. Operation, based on the values of IA2 and IA2N is as described above.

Referring to FIG. 3, command buffer 42 has a series of flip flops 100A to 100H which each receive respectively, at the D inputs thereof, data from respective bits 0 to 7 of internal data bus 36. Flip flops 100A to 100H are all reset by a signal RESET 4 from input and clock control 24 (FIG. 8) and are clocked by a signal CPMODL from input and clock control 24 (FIG. 8) by way of gates 102A to 102H, respectively. The Q outputs of flip flops 100A to 100H are applied to status bus 72 as bit 0 to bit 7. The QN (i.e. $\overline{Q}$) outputs of flip flops 100A, 100B, 100E, 100F, 100G and 100H are also available

for use throughout apparatus 20'. The QN output of flip flop 100D is provided as an input to OR gate 104. The second and third inputs of gate 104 are grounded. The output of gate 104 is provided to the input of a driver 106 which generates the signal SBUS3B which is logically identical to SBUS3A. Two outputs are provided, instead of one, for additional fan out capability.

Command buffer 42 also has four flip flops 100A' to 100D' which each receive, respectively, at the D input thereof, data from respective bits 0 to 3 of internal data bus 36. Flip flops 100A' to 100H' are all reset by a signal RESET 4 from input and clock control 24 (FIG. 8) and are clocked by a signal CPMODH from input and clock control 24 (FIG. 8) by way of gates 102A' to 102D', respectively. The Q outputs of flip flops 100A' to 100D' are applied to status bus 72 as bit 8 to bit 11. The QN outputs are available as well. The significance of the CPMODL and CPMODH will be discussed below with respect to FIG. 8.

The programming of apparatus 20 is accomplished via status bus 72, because data thereon, used directly, and distributed by internal data bus 36, controls operation of the various blocks of FIG. 1. The following table indicates how the various bits of status bus 72 are utilized.

STATUS BUS BIT UTILIZATION

BIT	FUNCTION	FIG. NO.
0	On active low, load data from computer (in input data buffer 44) into primary counter 54	9
1	Select prescaler terminal count or CPECL (less than 50 MHz) as primary time source	
2	Select time base for CP1, CP2 and CP3. 0 = terminal count of primary counter 54, 1 = prescaler output	9
3	Select which one of the outputs of address bus 22 and count bus 60 appears on the H and K buses	2A-2D
4	Select external load pulse (EXLD) to test counters or use internal terminal count for preset (PE inputs)	5
5	± slope selection	6
6	Select external trigger	6
7	On active low, load data from external source into input data buffer 44 (used in conjunction with bit 4)	9
8	Test counter 54A	5
9	Test counter 54B	5
A	Test counter 54C	5
B	Test counter 54D	5

Referring to FIG. 4, input data buffer 44 is comprised of eight pairs of flip flops 108A, 108A' to 108H, 108H'. Bits 0 to 7 of internal data bus 36 are connected, respectively, to the D inputs of said pairs of flip flops. Flip flops 108A to 108H are reset by a

signal RESET 1, while flip flops 108A' to 108H' are reset by signal RESET 2 from input and clock control 24 (FIG. 8). Flip flops 108A to 108H are clocked by a signal CPDATL (by way of gates 110A to 110H), while flip flops 108A' to 108H' are clocked by a signal CPDATH (by way of gates 110A' to 110H'), which originate in input and clock control 24 (FIG. 8) and are discussed more fully below.

The Q outputs of flip flops 108A to 108H appear as bits 0 to 7 on load bus 55, while the Q outputs of flip flops 108A' to 108H' appear as bits 8 to F of load bus 55.

Referring to FIG. 5, primary counter 54 is comprised of four, four bit up counters 54A to 54D. Bits 0 to 3 of load bus 55 are connected respectively to the D0 to D3 inputs of counter 54A. Bits 4 to 7 are connected to the corresponding inputs of counter 54B, bits 8 to 11 to those of counter 54C and bits 12 to 15 to those of counter 54D. Thus, counter 54 is a 16 bit up counter which can be preload with the data on load bus 55.

The Q0N to Q3N outputs of counter 54A are the source of bits 0 to 3 of count bus 60. The Q0N to Q3N outputs of counter 54B are the source of bits 4 to 7 of count bus 60. The Q0N to Q3N outputs of counter 54C are the source of bits 8 to B, while the corresponding outputs of counter 54D are the source of bits C to F of count bus 60.

Counters 54A and 54B are clocked by signal CPC1, while counters 54C and 54D are clocked by signal CPC2, both from input and clock control 24 (FIG. 9).

An external enable signal ENT (provided by a line of control bus 50), which is active on logic low, is provided to an input of an ECL comparator 112. The output of comparator 112 is provided as an input to driver 114. The output of driver 114 is in turn provided as a first input to NAND gate 116. A second input of NAND gate 116 is connected to the bit 9 line of status bus 72 (SBUS8). A third input of gate 116 is grounded. The output of gate 116 is connected to a first input of OR gate 118. The second input of OR gate 118 is connected to the output of a NAND gate 120. Two inputs of NAND gate 120 are grounded. The third input of gate 120 is connected to the logical opposite of SBUS8, SBUS8N. Thus, when SBUS8N is at logic low, or when SBUS8 and ENT are at logic low the output of gate 118 will be at a high logic level, thus providing an actuating signal to the count enable input CE of counter 54A. Counter 54A then counts upward in response to clock pulses CPC1, allowing independent testing of counter 54A without an interaction with other counters. For example, ENT may cause counter 54A to count CPC1 pulses for a given time, after which a check is made by the microcomputer to determine whether the proper count is contained in counter 54A.

When counter 54A has a count of 15, the top count output TC thereof goes high and the TCN output, which is supplied to an input of NAND gate 122 goes low. A second input of gate 122 is connected to ground. The third input is connected to SBUS9, i.e., bit 10 of status bus 72. The output of NAND gate 122 is connected to one input of OR gate 124. The second input of OR gate 124 is connected to the output of NAND gate 126. Two inputs of NAND gate 126 are grounded, while a third input is connected to SBUS9N. The output of OR gate 124 is connected to the count enable input CE of counter 54B. Thus, counter 54B counts pulses of CPC1 when SBUS9N is at a logic low, or when the TCN output of counter 54A is low, indicating counter 54 is at full count and SBUS9 is low. This permits independent testing of counter 54B or testing in conjunction with counter 54A.

Bit 11 of status bus 72, SBUSA, is connected to one input of a NAND gate 128. The other two inputs are connected, respectively, to the TC outputs of counter 54A and 54B. The output of NAND gate 128 is connected to one input of an OR gate 130. The other input of OR gate 130 is connected to the output of a NAND gate 132. Two inputs of NAND gate 132 are grounded, while the third input is connected to SBUSAN. The output of OR gate 130 is connected to the count enable input of counter 54C. Thus, when SBUSAN is at logic low, or when the TCN outputs of gates 54A and 54B and SBUSA are all at logic

low, counter 54C counts pulses of CPC2, and may be tested.

The TCN outputs of counters 54A and 54B are also supplied to the first two inputs of NOR gate 134. The other two inputs of an EXCLUSIVE NOR gate 134 are grounded. The output of NOR gate 134 is connected to one input of NAND gate 136. A second input of NAND gate 136 is connected to the TCN output of counter 54C. The third input of NAND gate 136 is connected to SBUSB, the bit 12 line of status bus 72. The output of NAND gate 136 is connected to the input of OR gate 138. The other input of OR gate 138 is connected to the output of a NAND gate 140. Two inputs of NAND gate 140 are grounded, while a third input is connected to SBUSN. The output of OR gate 138 is connected to the count enable input CE of counter 54D. Thus, counter 54D counts pulses of CPC2 when SBUSBN is low, or when the TCN output of counters 54A, 54B and 54C and SBUSB are all low. Counter 54D can thus be tested independently, or in conjunction with counters 54A, 54B and 54C.

The testing arrangement described above permits a full test of counter 54 with only 65 clock pulses.

The Q1N, Q2N and Q3N outputs of counter 54A are connected, respectively, to the three inverting inputs of an AND gate 142. The Q0N output of counter 54A is connected to one input of an OR gate 144. The other two inputs of gate 144 are connected to ground. Thus, the non-inverted output of gate 142 is high when counter 54A

has a count therein of 14, or one less than its top count.

The inverted output YN of gate 142 is connected to an input of inverting OR gate 146. The other three inputs of gate 146 are connected to respective TCN outputs of counters 54B, 54C and 54D. The inverted output of TCNTL1 of gate 146 is thus high when counter 54A is at count 14 and counters 54B, 54C and 54D are at count 15. TCNTL1 is an internal pre-top count signal which is used to provide an indication to other components of apparatus 20 that there is only one count to go before counter 54 is at a top count condition. TCNTL1 is connected to one input of OR gate 148. The other input of OR gate 148 is grounded. The outputs of OR gate 148 are connected to the input of an output cell or driver 150, which provides a pre-top count output PRETC, externally of apparatus 20 when TCNTL1 makes a transition from low to high.

The TCN outputs of counters 54A to 54D are provided to respective inputs of inverting OR gates 152 and 154. The inverted output of gate 152, which is high only when all of counters 54A to 54D are at a top count of 15, is connected to an input of OR gate 156. The other input of OR gate 156 is grounded. The output of gate 156 is connected to a driver 158 which provides an output TC1 externally of apparatus 20. The output of gate 152 is also connected to one input of OR gate 160. The other input of OR gate 160 is connected to ground. The in-

verted output of OR gate 160 is connected to the input of driver 162 which provides a low output at TC2N when counter 54 is at top count.

The output of gate 152 is also available as a signal TCNT for use elsewhere in apparatus 20. Further, said output is applied as an output I0 to a 2:1 multiplexer 164. The output of multiplexer 164 is connected to the D input of a flip flop 166. The Q output of flip flop 166 is connected to the I1 and select input S1 of multiplexer 164. The clock input of flip flop 166 is connected to the output of an OR gate 168. One input of OR gate 168 is grounded, while another input is connected to CPC2. The Q output of flip flop 166 is high when reset, which causes multiplexer 166 to provide a logic high signal to input D of flip flop 166.

A clock pulse applied by gate 168 which would tend to cause a change in state of output Q of flip flop 166, results in another logic high signal being supplied to the D input of flip flop 166 by way of multiplexer 164 whenever the output of gate 152 is high. It is only when the output of gate 152 is low, that a logic low signal is provided to the D input of flip flop 166 by way of multiplexer 164 upon application of a clock pulse CPC2 to gate 168. This causes the Q output of flip flop 166 to assume a low state, thus providing an end of count output EOCFF on the first clock pulse CPC2 after top count has been reached.

The output of flip flop 166 is also connected to one input of an OR gate 170. The other input of OR gate 170 is connected to ground. The inverted output of OR gate 170 is connected to an output cell or driver 172. When the Q output of flip flop 166 goes from high to low, an output EOC is provided externally of apparatus 20 when the end of count condition has occurred.

The output of OR gate 154 is connected to one input of a NAND gate 174. Another input of NAND gate 174 is connected to ground. The third input of NAND gate 174 is connected to the bit 5 line SBUS4 of status bus 72. The output of NAND gate 174 is connected to one input of an OR gate 176. The other input or OR gate 176 is connected to the output of a NAND gate 178. A first input of NAND gate 178 is grounded and a second input is connected to SBUS4N. The third input of NAND gate 178 is connected to a line EXLD originating in input and control 24 (FIG. 9).

The output of OR gate 176 is connected to the preload enable input of counters 54A to 54D. This output assumes a high state when counter 54 is at top count and SBUS4 is low, or when SBUS4N and EXLD are both at logic low. When either of these two enabling sets of conditions occur, data on load bus 55 is loaded into counters 54A to 54D. Appropriate clock pulses then cause counter 54 to count up from that count.

An input signal RESET 8 serves to reset counters 54A and 54B. Another input signal RESET 9 serves to

reset counters 54C and 54D. These signals originate within input and clock control 24 (FIG. 8).

Referring to FIG. 6, data from counter 54 corresponding to bits 0 to B of count bus 60 is provided to the D inputs of a series of flip flops 180A to 180L of pointer latch 62. The Q outputs of flip flops 180A to 180L are connected to bits 0 to B of latch bus 64.

An external trigger is supplied by a line of control bus 50 to an ECL comparator 182 of external trigger control 68 (FIG. 6). The output of comparator 182 is in turn connected to a driver 184. The non-inverted output of driver 184 is connected to a first input of a NAND gate 186. A second input of NAND gate 186 is connected to SBUS5N. The third input of NAND gate 186 is connected to SBUS6N which serves as an external trigger enable signal.

The outputs of NAND gate 186 is connected to one input of an OR gate 188. The other input of OR gate 188 is connected to the output of a NAND gate 190. A first input of NAND gate 190 is connected to the inverted output of driver 184, a second input to SBUS5, and the third input to SBUS6N. The output of OR gate 188 goes high when SBUS6N, the non-inverted output of driver 184 and SBUS5N are all low. These conditions are indicative of triggering on the negative slope of the signal applied to comparator 182. The output of OR gate 188 is also high when SBUS6N, SBUS5 and the inverted output of ECL comparator 184 are all low. These conditions are

indicative of triggering on the positive slope of the signal applied to comparator 182.

The output of OR gate 188 is supplied to one input of OR gate 192. The other input thereof is grounded. The output of OR gate 192 clocks flip flop 194. The D input of flip flop 194 is connected to SBUS6. Thus when SBUS6N provides an enable external trigger signal by being at logic low, SBUS6 provides a logic high signal which is asynchronously clocked to the Q output of flip flop 194 when the external signal applied to comparator 182 causes a change in the state thereof.

The Q output of flip flop 194 is applied to the D input of flip flop 196. The clock input of flip flop 196 is connected to the output of an OR gate 198. A first input of OR gate 198 is grounded and the second input is connected by line 70 (FIG. 1) to CPC1, the clock used by primary counter 54 and originating in input and clock control 24 (FIG. 9). Flip flop 196 is thus synchronously clocked, on the pulse of CPC1 occurring after the Q output of flip flop 194 goes high. The state of the Q output TRIGFF of flip flop 196 is thus indicative of an external trigger of selected slope having occurred and been synchronized to the pulse of CPC1 immediately after the occurrence of said external trigger.

The QN output of flip flop 196 is connected to an input of an OR gate 198. The other two inputs of gate 198 are grounded. The output of gate 198 is connected

to the input of a driver 200. Driver 200 has sufficient fan out capability so that the inverted output thereof, transmitted over line 66 (FIG. 1), can drive the first input of each of a series of OR gates 202A to 202L. The second input of each of OR gates 202A to 202L is grounded. Thus outputs of OR gates 202A to 202L clock data on count bus 60 to latch bus 64, as noted above.

A reset signal RESET 3 from input and clock control 24 (FIG. 8) resets flip flops 180A to 180L.

It is difficult and often impossible to obtain performance characteristic which would provide a presettable 16 bit counter capable of counting at 100 MHz with certain gate arrays. The use of prescaler 49, programmed by control register 46, avoids this difficulty. Primary counter 54 may operate at a lower count rate, while prescaler 49 operates at 100 MHz.

Referring to FIG. 7A and FIG. 7B, control register 46 is comprised of four flip flops 204A to 204D having D inputs which are connected to bits 3 to 0, respectively, of internal data bus 36. Flip flops 204A to 204D are reset by a signal RESET 1 and are clocked by a signal CPPRE from input and control 24 (FIG. 8) by way of OR gates 206A to 206B. The Q outputs of flip flops 204A to 204D are the origin of bits 3 to 0, respectively, of programming bus 45. The QN outputs of flip flops 204A to 204D are provided, respectively, to the inputs of inverted OR gates 208A to 208D of prescaler 49. A four bit presettable binary counter, of a type well known in

the art, is comprised of inverted OR gates 208A to 208D, 210A to 210D, 212A to 212C, 214A, 214B, wire OR gates 216A to 216D, and flip flops 218A to 218D. This arrangement is designed for high speed counting. Flip flops 218A to 218D are clocked by the 100 MHz system clock CP100 (FIG. 9) by way of OR gates 220A to 220D, respectively. The QN outputs of flip flops 204A to 204D of control register 46 provide preset inputs for flip flops 218A to 218D. Thus, prescaler 49 can generate time bases of predetermined width depending on the binary number loaded into control register 46. Prescaler 49 functions as a divide by N counter, where N is the one's compliment of the binary number in control register 46.

The QN outputs of flip flops 218C and 218D, designated as CNT1N and CNTØN (FIG. 7B) are each provided as an input to inverted OR gates 222 and 224 (FIG. 7A). The QN outputs of flip flops 218A and 218B are also each provided as an input to inverted OR gates 222 and 224. When the QN outputs of flip flops 218A to 218D are all low, prescaler 49 is at top count, and the inverted output of gate 222 is high, providing a signal COUNTN. The non-inverted output of gate 224 is low, providing a signal LOADN (FIG. 7A). COUNTN is supplied to one input of gate 210C and to one input of gate 210D. LOADN is supplied to a second input of gate 210C and an input of gate 208D (FIG. 7B). COUNTN or LOADN are the outputs of prescaler 49 used as a time base or clock. The occurrence of COUNTN may be the event which causes loading of

the number stored in control register 46 into prescaler 49.

Flip flops 218A to 218D are reset by a signal RESET 6 from input and clock control 24 (FIG. 8).

On the basis of a 100 MHz clock, prescaler 49 can produce pulses having time bases of 10 to 160 nsec in increments of 10 nsec. Time bases of 170, 180 and 190 nsec are not produced. However, the output of prescaler 49 may be provided to the input of primary counter 54 to produce time bases of from 20 to at least 20 milliseconds (2^{16} x 160 ns) in increments of 20 nsec, as described below.

The input control section of input and clock control 24 is shown in FIG 8. A base address specifying which of several input or output ports is to be operatively associated with the microcomputer at a given time is decoded therein, in a manner well known in the art. When the apparatus 20 of the present invention is selected, the microcomputer provides a logic low level by way of control bus 50 to external chip select input CSN. A receiver 226 converts from TTL to ECL and has an output connected to the input of a driver 228. The non-inverted output of driver 228 is connected to one input of an OR gate 230. The output of OR gate 230 is connected to the input of a tri-state enable driver 232. Driver 232 provides at its output the output enable signal OUTEN used to enable drivers 94A to 94H (FIG. 2A, 2B, 2C and 2D).

Control bus 50 also provides a read signal RDN to receiver 234 which in turn drives a driver 236. The output of driver 236 is connected to the second input of OR gate 230. Thus, when RDN is at logic high, OUTEN will be high, and drivers 94A to 94H will be inhibited, as required for a write operation; that is writing data on bidirectional tristate data bus 30 from the microcomputer into a register of apparatus 20 by way of internal data bus 36.

In a read operation; that is providing data to the microcomputer from one of the registers of apparatus 20, RDN is at logic low, but a signal WRN, supplied by the microcomputer to a receiver 238 by a line of control bus 50, is at logic high. The output of receiver 238 is connected to the input of a driver 240. The output of driver 240 is connected to one input of each of gates 242 and 244, which are both the logical equivalents of AND gates with inverting inputs and non-inverted and inverted outputs, respectively. The output of driver 228 is connected to a second input of each of gates 242 and 244. A third input of each of gates 242 and 244 is connected to ground. The fourth input of gate 242 is connected to internal address line IA2N. The fourth input of gate 242 is connected to internal address line IA2N. The non-inverted output of gate 242 is connected to the inverting enable input of a decoder 246. The inverted output of gate 244 is connected to the enable input of decoder 248. Which output of each of decoders

246 and 248 assumes a logic high state is determined by internal address signals IA0 and IA1 which are connected to the A and B inputs, respectively, of both of decoders 246 and 248.

Assuming that chip select input CSN is at logic low, WRN is at logic low, and RDN is at logic high, the above described arrangement of gates 242 and 244 and decoders 246 and 248 produces outputs in accordance with supplied inputs to perform the operation as shown below. These operations are deemed write operations:

WRITE OPERATION

INPUTS A2	A1	A0	OUTPUT PRODUCED DECODER	PIN	TITLE	OPERATION	USED FOR
0	0	0	246	Y1	CPDATL	LOAD LOW BYTE	DATA BUFFER 44
0	0	1	246	Y0	CPDATH	LOAD HIGH BYTE	DATA BUFFER 44
0	1	0	246	Y2	CPMODH	LOAD HIGH BYTE	COMMAND BUFFER 42
0	1	1	246	Y3	CPMODL	LOAD LOW BYTE	COMMAND BUFFER 42
1	0	0	248	Y0	CPPRE	LOAD BITS	CONTROL REG. 46
1	0	1	248	Y1	CPBIT	SOFTWARE ORDERING 1 SELF TEST CLOCK PULSE	FIG. 9
1	1	0	248	Y2	-	RESET	ALL REGISTERS
1	1	1	248	Y3	-	RESET	ALL NON-PROGRAMMABLE REGISTERS

A microcomputer software ordered reset of all registers is accomplished, as noted above, when the Y2 output of decoder 248 is applied to a first input of each of OR gates 250A to 250H. The output of each of OR gates 250A to 250H is connected to the input of a respective driver 252A to 252H which produce, at the respective outputs thereof, RESET 1 to RESET 6, RESET 8 and RESET 9.

A microcomputer software ordered reset of all non-programmable registers is accomplished, as noted above, when the Y3 output of decoder 248 is applied to a second input of each of OR gates 250C, 250F, 250G and 250H. The corresponding input of OR gates 250A, 250B, 250D and 250E are grounded. Thus only RESET 3, RESET 6, RESET 8 and RESET 9 are driven to logic high, resetting, respectively, only pointer latch 62, prescaler 49 and primary counter 54. The registers having loaded values, i.e., input data buffer 44, control register 46, and command buffer 42 are not disturbed, and the values loaded therein are retained for use in subsequent operations.

Assuming that CSN is at logic low, RDN is at logic low and WRN is at logic high, address bits A0, A1 and A2, also used internally as IA0, I1 and IA2, control multiplexer 26 to load data from address bus 22, count bus 60, latch bus 64 and status bus 72 on to internal data bus 36. These operations, shown below, are deemed to be read operations.

READ OPERATIONS

INPUTS TO MULTIPLEXER 26			DATA TO INTERNAL DATA BUS 36	
A2	A1	A0	BUS	BYTE
0	0	0	ADDRESS BUS 22	LOW
0	0	1	COUNT BUS 60	LOW
0	1	0	LATCH BUS 64	LOW
0	1	1	STATUS BUS 72	LOW
1	0	0	ADDRESS BUS 22	HIGH
1	0	1	COUNT BUS 60	HIGH
1	1	0	LATCH BUS 64	HIGH
1	1	1	STATUS BUS 72	HIGH

It is desirable to clear all registers when power is initially applied to apparatus 20, or the microcomputer associated therewith. An external clear input CLEAR is provided, on a line of control bus 50, to a receiver 254. The output of receiver 254 is connected to a driver 256. The inverted output of driver 256 is connected to the third input of OR gates 250A to 250H, thus providing a reset of all registers when CLEAR is at logic low.

Referring to FIG. 9, an ECL clock CPECL or its logical opposite CPECLN are supplied to the clock control portion of input and clock control 24 by lines of control bus 50. A receiver 258 processes CPECL and supplies an output to the non-inverting input of a driver 260. A receiver 262 process CPECLN and supplies a signal to the inverting input of driver 260. The inverted

output of driver 260 is connected to the B input of a NAND gate 264. The A input of NAND gate 264 is connected to SBUS1. The output of NAND gate 264 is connected to the input of a driver 266. The 100 MHz ECL clock appears at the output of driver 266 and produces the output CP100 used as an input for prescaler 49 (FIGS. 7A and 7B) only if SBUS1 is at a high logic level.

The output EOCFF of end of count flip flop 166 (FIG. 5) is provided to the A input of an AND gate 268. EOCFF is also provided to a first input of an OR gate 270. The second input of OR gate 270 is grounded. The inverted output of OR gate 270 is connected to the input of an output cell or driver 272, which provides an output EOCN external of apparatus 20.

The B input of AND gate 268 is connected to SBUS4. A logic high output is produced by gate 268 only when counters 54A to 54D of primary counter 54 are at an end of count condition. The output of AND gate 268 is connected to a first input of an AND gate 274 having three inverting inputs. A second input of gate 274 is connected to SBUS1N. The third input of gate 274 is connected to the inverted output of an AND gate 276. Both inputs of AND gate 276 are connected to the top count output COUNTN of prescaler 49. Thus, gate 274 will provide a logic high output to OR gate 278 only when prescaler 49 is not in a top count condition, the output of AND gate 268 is low, and SBUS1N is low. This last con-

dition results in prescaler 49 being used to provide a clock input for primary counter 54.

The second input of OR gate 278 is connected to the output of an AND gate 280 having three inverting inputs. A first input thereof is grounded. A second input is connected to the inverted output of driver 260. The third input is connected to SBUS1.

The output of OR gate 278 is connected to one input of each of OR gates 282 and 284. A second input of each of OR gates 282 and 284 is connected to the output of an OR gate 286. One input of OR gate 286 is driven by a TTL to ECL receiver, which receives a TTL clock pulse CPTTL, of a frequency under 50 MHz, along a line of control bus 50. The third inputs of OR gates 282 and 284 are connected to the CPBIT output of decoder 248 (FIG. 8).

The output of gates 282 and 284 are connected to the inputs of respective drivers 290 and 292, which generate, respectively clock signals CPC1 and CPC2 used by primary counter 54 (FIG. 5).

The inputs to gates 268, 276, 280, 278 and 274 determine whether the input clock goes to primary counter 54 or prescaler 49.

When SBUS1N is low, the top count of prescaler 49 appears as the input for primary counter 54.

Gates 282 and 284 permit a selection of one clock from the group consisting of the clock provided as above, CPTTL or CPBIT.

In applications where it is necessary to generate a time base, the top count TCNT of primary counter 54 may be used. TCNT is provided to the I0 input of a multiplexer 294. The I1 input is connected to CPC1. The select input S1 of multiplexer 294 is connected to SBUS 2. When SBUS2 is low, TCNT appears at the output of multiplexer 294. When SBUS2 is high, the output of prescaler 49 or the 100 MHz clock signal appears at the output of multiplexer 294, the selection being made as previously described. The non-inverted output of multiplexer 294 is converted to an output cell or driver 296. The output of driver 296 is available externally of apparatus 20 as an ECL nominal clock output CPOUT 1.

The inverted output of multiplexer 294 is provided to one input of OR gate 298. The second input of OR gate 298 is grounded. The output of OR gate 298 clocks a flip flop 300. The QN output of flip flop 300 is connected to the D input thereof. Thus flip flop 300 produces a symmetrical output waveform at half the frequency of CPOUT1, which is generally not symmetrical. Flip flop 300 is reset by RESET 8.

The Q output of flip flop 300 is connected to a first input of OR gate 302. The second input thereof is grounded. The inverted output of OR gate 302 is supplied to an output cell or driver 304 which provides an ECL symmetric clock output CPOUT2 externally of apparatus 20.

The QN output of flip flop 300 is connected to a first input of an OR gate 306. The second input thereof is grounded. The output of OR gate 306 drives a TTL output cell 308 which provides TTL symmetric clock output CPOUT 3 externally of apparatus 20.

Control bus 50 has an additional two lines LOAD 1 and LOAD 2 which are used to supply signals directing the preloading of counter 54. LOAD 1 is a TTL signal supplied to a TTL to ECL receiver 310. The output of receiver 310 is supplied to one input of an OR gate 312. The other input of OR gate 312 is grounded. The inverting output of OR gate 312 is supplied to an input of a gate 314 which serves as an AND gate with inverting inputs and an inverted output.

LOAD 2 is an ECL signal which is connected to the input of an ECL comparator 316. The output of comparator 316 is connected to the input of a driver 318. The inverted output of driver 318 is connected to another input of gate 314. The remaining inputs of gate 314 are grounded.

The inverted output of gate 314 is connected to a first input of NAND gate 320. A second input of NAND gate 320 is connected to SBUS7N. The third input thereof is grounded. The output of NAND gate 320 is connected to a first input of OR gate 322. A second input of OR gate 322 is connected to the output of NAND gate 324. Two inputs of NAND gate 324 are grounded, while the

third is connected to SBUS0N. The inverted output EXLD of OR gate 322 is used to cause primary counter 54 to preload data from input data buffer 44 on load bus 55. This occurs when SBUS0N is at logic low, or when one of LOAD 1 or LOAD 2 and SBUS7N are at logic low.

It is thus apparent that apparatus 20 may be programmed by appropriate logic signals from a microcomputer to provide time base signals, to serve as a counter, or to directly address memory. Further, count and address data from apparatus 20 may readily be acquired by the microcomputer.

Referring to Fig. 10, three modules 20A, 20B and 20C constructed according to the invention are used in a counter/timer 326. A 100 MHz clock is provided to module 20A to provide an appropriate time base, when module 20A is programmed by a microcomputer. The time base output of module 20A is connected to a first input of a gate 328. A second input of gate 328 is connected to the output of a conventional selector 330 of the type generally used in a counter/timer. A first input of selector 330 is connected to the output of a comparator 332A which is fed by a driver 334A. A second input of comparator 332A is connected to a first reference voltage VREF1. Comparator 332A should have some hysteresis.

A signal representative of a first event is applied to an input CHA of a microcomputer programmable attenuator 336A. The output of attenuator 336A is connected to the input of driver 334A. The arrangement and opera-

tion of comparator 332A, driver 334A and attenuator 336A, are well known in the art.

A comparator 332B, a driver 334B and an attenuator 336B provide another channel for an input CHB. Comparator 332B is provided with a reference voltage VREF2. The output of comparator 332B is connected to selector 330.

The output of gate 328 is connected to a module 20B constructed according to the invention, which serves as a count accumulator for counts gated through gate 328. If the count will be large enough to fill primary counter 54 and cause an overflow, a second module 20C is provided to count the top count output of module 20B. Count data from modules 20B and 20C is provided to the microcomputer. When modules 20B and 20C are both used, a counter/timer with a 32 bit accumulator is produced.

FIG. 11 illustrates how three modules 20D, 20E and 20F of the present invention can be utilized to provide a microcomputer controlled arbitrary function generator 338. A stable frequency source such as a 100 MHz clock is connected to the input of module 20D which is programmed by the microcomputer to act as a time base generator. The timing output of module 20D is supplied to module 20E which is configured as a burst counter and programmed to provide a signal to module 20D when the required predetermined number of repetitions of the arbitrary function have been generated. The output of module 20D is also supplied to module 20F which is pro-

grammed as a memory address control. Module 20F controls a stimulus memory 340 loaded with computer supplied stimulus data for making up the arbitrary function.

When an external trigger is supplied to module 20F, a base address 342 in stimulus memory 340 is accessed. Base address 342 has a bit which is used to provide a unique indication that base address 342 has been accessed. For example, this bit may be of logic value "1" while the corresponding bits in other addresses in stimulus memory 340 are a logic zero. When this logic one bit is detected, a synchronization signal indicating the start of the arbitrary function is produced by a buffer 344. Module 20F steps through the locations in stimulus memory 340 providing the data in each location sequentially to a digital to analog converter 346 upon successive pulses of the time base generator (module 20D) to the memory address control (module 20F). The output of digital to analog converter 346 is supplied to a buffer 348 which has sufficient output drive capability to provide a signal to be used for test or other purposes. When the function produced by the data in stimulus memory 340 has been repeated the number of times programmed into the burst counter (module 20E), operation ceases until a microcomputer reset has occurred and a new trigger signal is received by module 20F.

FIG. 12 illustrates the manner in which three modules according to the present invention may be intercon-

nected to provide a digitizer 350 for storing a digital representation of an analog signal. A clock, preferably of 100 MHz, is provided to the input of a first module 20G configured as a time base generator. The time base output CPOUT thereof is supplied to a second module 20H used as a memory address control. CPOUT is also supplied to a third module 20I which serves as a samples to go counter.

An input signal to be digitized is provided to an input terminal having a standard 50 ohm terminating resistor 352, connected therefrom to ground. A programmable attenuator 354 adjusts the level of the signal so that it is suitable as an input for a buffer 356. A sample and hold circuit 358 samples the output of buffer 356 and periodically holds the value thereof for conversion by an analog to digital converter 360. The output of analog to digital converter 360 is provided as a digital input to a circular memory file 362.

A synchronization pulse is provided as an input to a buffer 364. The output thereof is provided to a driver 366 having hysteresis so as to prevent undesirable multiple triggering. The output of driver 366 is provided to the memory address control (module 20H) and the samples to go counter (module 20I).

Module 20H is programmed by the microcomputer so that the count bus 60 thereof has data thereon, from primary counter 54, corresponding to the address in memory 362 being accessed by module 20H. When a synchroni-

zation signal is received, this value is stored in pointer latch 62 and provides a reference corresponding to a location in memory 362. The output of driver 366 is also supplied to the ENT input of the samples to go counter (module 20I) to serve as a count enable signal. The samples to go counter (module 20I) is programmed by the microcomputer to count a predetermined number of time base signals from module 20G, corresponding to a like number of locations in memory 362. After the predetermined number has been reached, module 20I provides an end of count EOC pulse to module 20H, preventing additional locations in memory 362 from being addressed, and therefor holding the data desired in digital form in memory 362.

It will be understood that the value programmed into the samples to go counter (module 20I) by the microcomputer can be used to provide storage of the analog signal being digitized for a period of time before or after the occurrence of the synchronization pulse, as circular memory 362 is constantly updated with new data written over the oldest data therein, at a rate determined by the time base provided to module 20H by module 20G.

An additional module (not shown) according to the invention may be used to provide a time delay, after the occurrence of a synchronization pulse, before the external trigger and count enable signals are supplied to modules 20H and 20I, respectively.

Referring to FIG. 13, a digital word generator 368 is constructed using a time base generator module 20J and a memory address control module 20K according to the invention. The output of a stable oscillator, preferably of 100 MHz, is provided to module 20J. In accordance with the output of module 20J, module 20K is used to address a stimulus memory 370, a response memory 372, a tristate control memory 374 and an expected response memory 376.

Stimulus memory 370 may be an N bit by M bit memory, where N is the number of bits or outputs presented at any given time, and M is the number of different outputs to be presented. Upon being accessed by module 20K, the data in one of the M locations of memory 370 is provided to an N bit driver 378 and placed on a bidirectional tristate data bus 380 when an appropriate enable signal is received from tristate control memory 374.

Data bus 380 provides the data thereon to a unit under test (not shown). Data returns from the unit under test on bus 380 (or a separate bus 382, is as appropriate if a switch 384 is open) and is provided to a receiver 386. The output of receiver 386 provides the returning data to response memory 372 which is under the control of module 20K. A digital comparator 388 compares the data being provided to response memory 372 with data from the corresponding address location in expected response memory 376. If the response from the unit under test does not correspond to the expected re-

sponse, comparator 388 provides an output which may be used, for example, to stop the test. Comparator 388 may also be configured with appropriate circuitry for indicating that one of the bits of data returned from the unit under test is neither logic high or logic low, but is at a level somewhere between.

From the above, it is apparent that the apparatus of the present invention has widespread applicability in a broad range of test instruments as a time base generator, an events accumulator, or as a memory address control. Although shown and describe in what is believed to be the most practical and preferred embodiment, it is apparent that departures from the specific design described and shown will suggest themselves to those skilled in the art and may be made without departing from the spirit and scope of the invention. I, therefore, do not wish to restrict myself to the particular constructions described and illustrated, but desire to avail myself of all modifications that may fall within the scope of the appended claims.

WHAT IS CLAIMED IS:

1. A computer programmable apparatus comprising:

a clock input means for receiving a clock input signal;

a computer input means for providing input from said computer;

a processing means for processing at least one of said clock input signal and said input from said computer to produce at least one output;

a control means for controlling said processing means in accordance with further input from said computer to determine the output produced; and

an output selecting means for selecting said at least one output to be used externally of said apparatus.

2. The apparatus of Claim 1, wherein said output selecting means selects said at least one output in response to additional input from said computer.

3. The apparatus of Claims 1 or 2, wherein said processing means comprises:

a counter (54) for counting pulses of said clock input signal; and

means (55) for preloading said counter with a value in accordance with said input from said computer.

4. The apparatus of Claims 1-3, wherein said computer input means includes a bidirectional data means (30) for receiving and transmitting data;

an input data buffer (44) and said processing means includes a counter (54), said input data buffer (44) being for storing data to be loaded into said counter (54); and

a command buffer (42), said command buffer (44) being for storage said further input from said computer.

5. The apparatus of any one of the preceding claims, wherein said output selecting means includes at least one multiplexer, said multiplexer having output circuit means for directly addressing a memory.

6. The apparatus of any one of the preceding claims, wherein said processing means includes a counter (54) responsive to said clock input signal, a register (62) for storing the count in said counter, said register (62) providing an output to said output selecting means, and said counter (54) providing an output to said output selecting means.

7. The apparatus of Claim 6 further comprising external input means (68) for causing said register (62) to store said count in said counter (54) upon application of a signal to said external input means (68).

8. A computer programmable apparatus comprising:

a clock input means for receiving a clock input signal;

a computer input means for providing input from said computer, said computer input means including:

an address input (22) for providing to said apparatus an address supplied by said computer; and

a control input means (50) for providing to said apparatus control inputs supplied by said computer;

a data transmission means (30) for inputting data to said apparatus and outputting data from said apparatus; and

processing means for processing at least one of said clock input signal, said address and said data in accordance with said control inputs to provide at least one output signal.

9. The apparatus of Claim 8, wherein said processing means includes a command buffer (42) for receiving and storing data from said data transmission means, said data being programming data for programming said processing means; and

an input data buffer (44) for receiving and storing data from said data transmission means.

10. The apparatus of Claim 9, wherein said data buffer (44) comprises a first group of flip flops clocked in response to a first control input and a second group of flip flops clocked in response to a second control input.

11. The apparatus of any one of Claims 8-10, wherein said processing means comprises a counter (54) for counting pulses of said clock input signal; said data stored by said input buffer being used to preload said counter; and a latch (62) for storing the value of a count in said counter.

12. The apparatus of any one of Claims 8-11, further comprising an output selector means for selecting one of said at least one output signal produced by said processing means for output by said data transmission means.

13. The apparatus of any one of Claims 8-12, further comprising:

an internal data bus (36) for transmitting internally of said apparatus data being transmitted by said data transmission means; and

loading means for preloading said data stored in said input data buffer into said counter means.

14. The apparatus of Claims 11-13, wherein said counter means comprises a prescaler (49) for receiving and frequency dividing said clock signal to produce a divided clock signal, and a primary counter (54) for counting said divided clock signal.

15. The apparatus of Claims 13 or 14, wherein said loading means pre-loads said primary counter with data in said data buffer.

16. The apparatus of Claims 14 or 15, further comprising a control register (46) for receiving and storing counter control data on said internal data bus (36), additional loading means for supplying said counter control data to said prescaler; and means for supplying said control data as an input to said output selector means for transmission on said data transmission means.

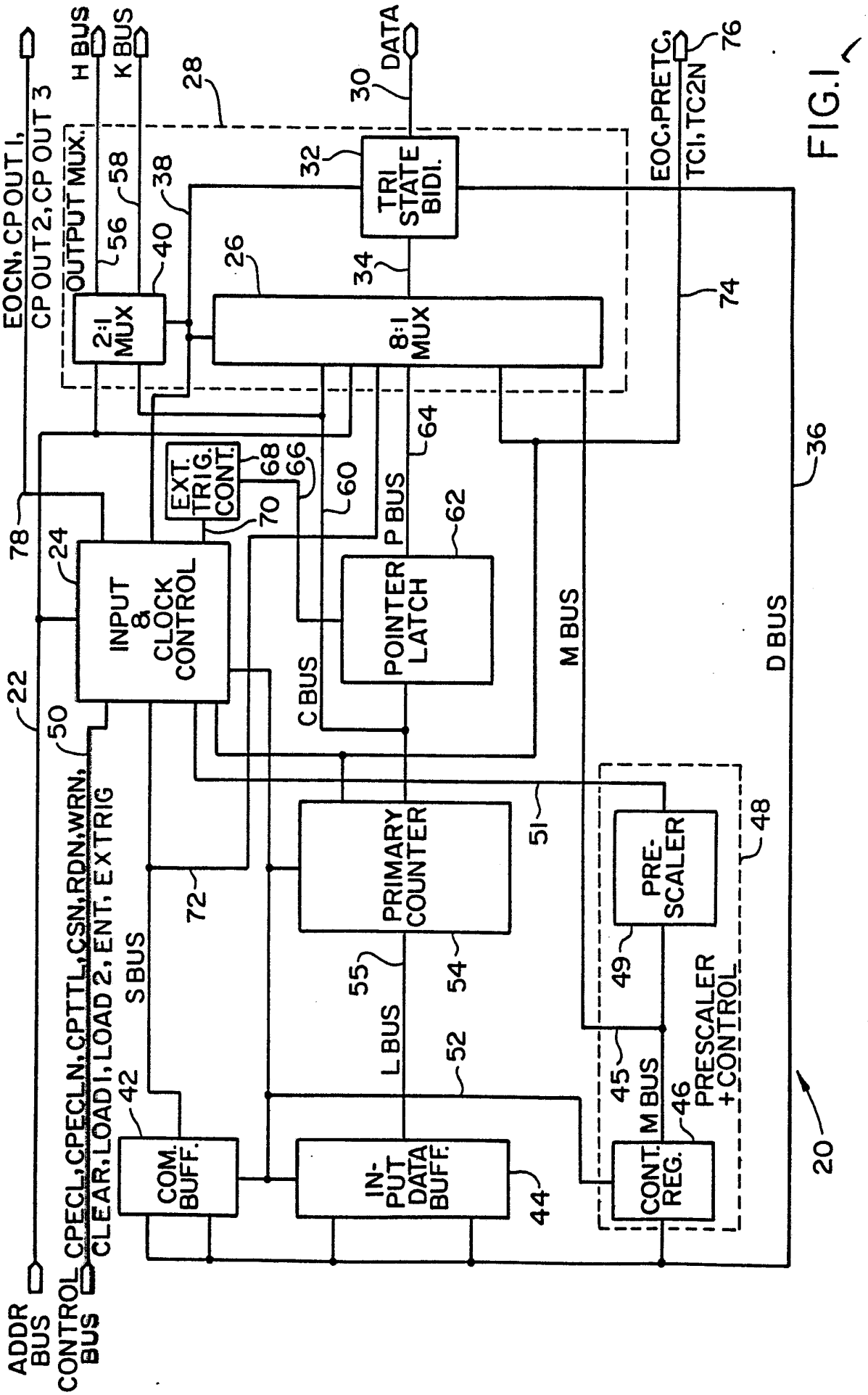


FIG. 1

SUBSTITUTE SHEET

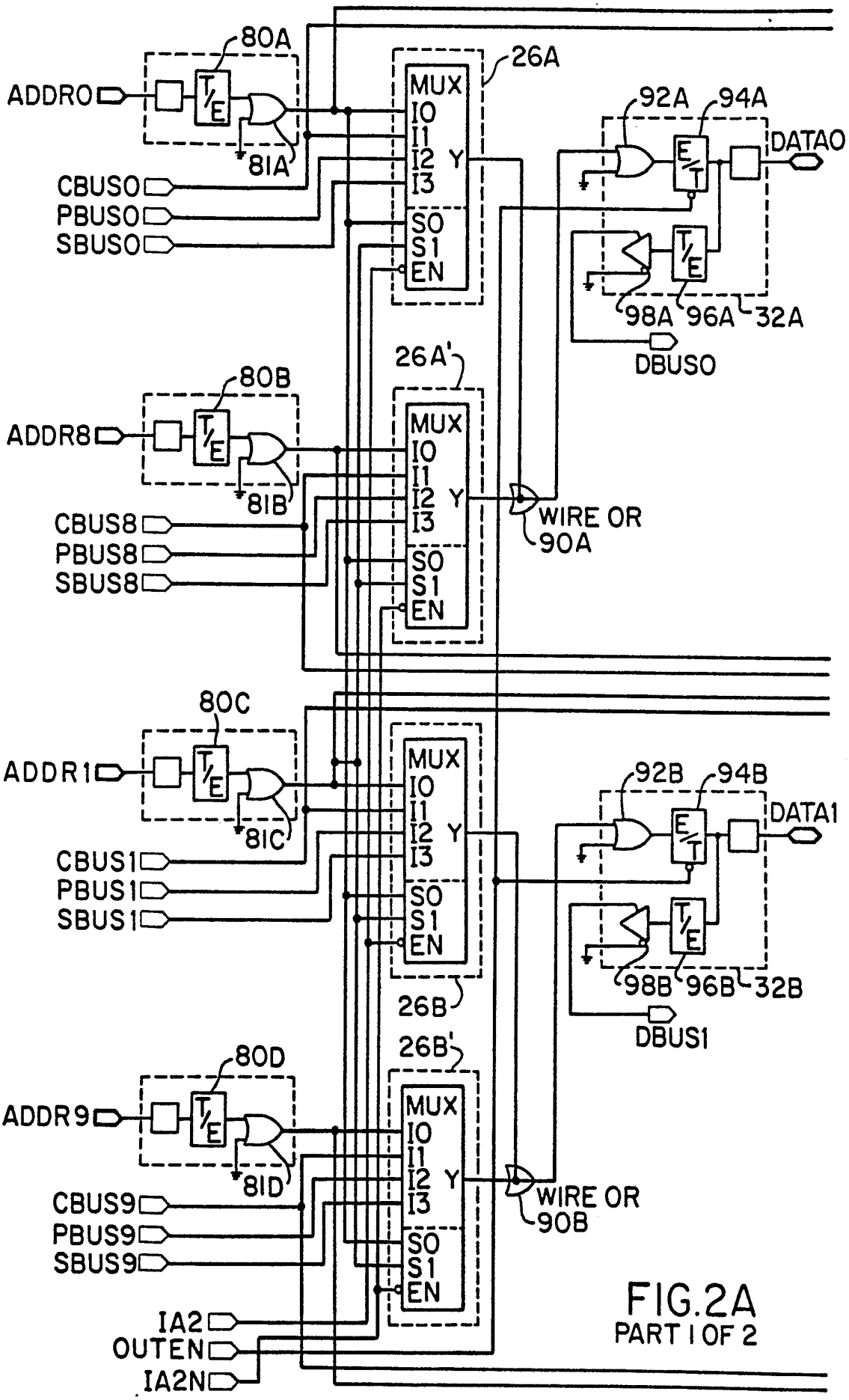


FIG.2A
PART 1 OF 2

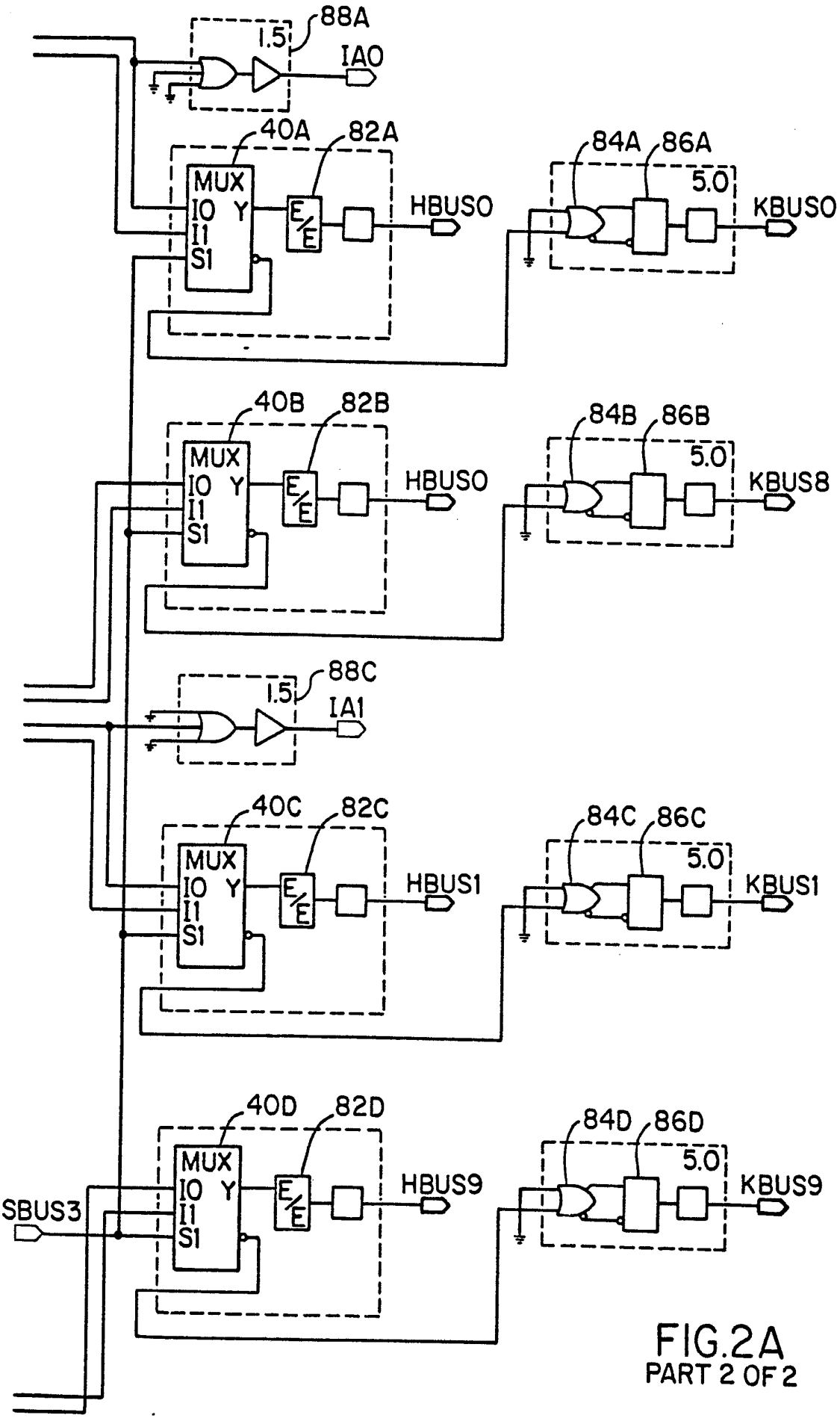


FIG.2A
PART 2 OF 2

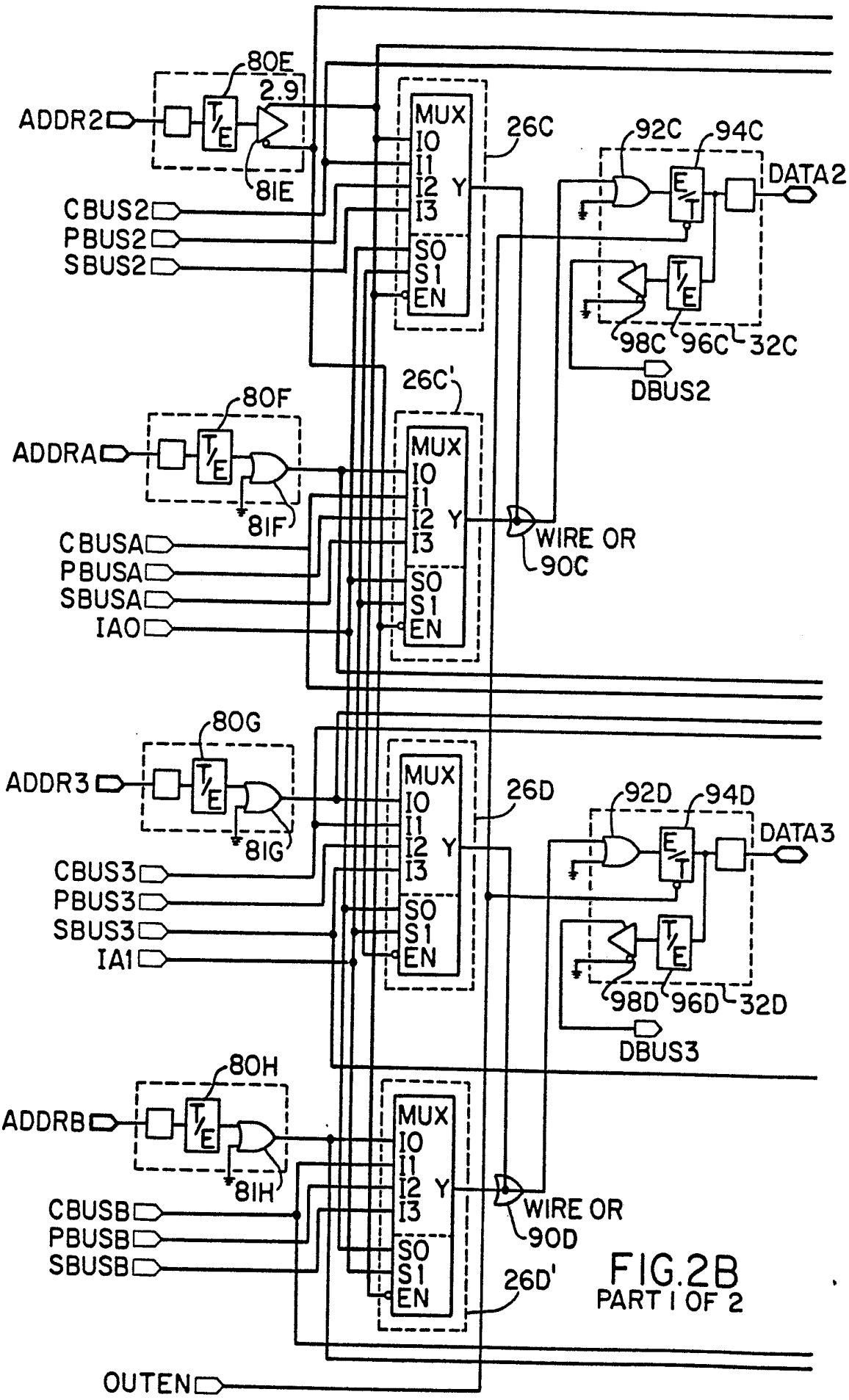


FIG.2B
PART 1 OF 2

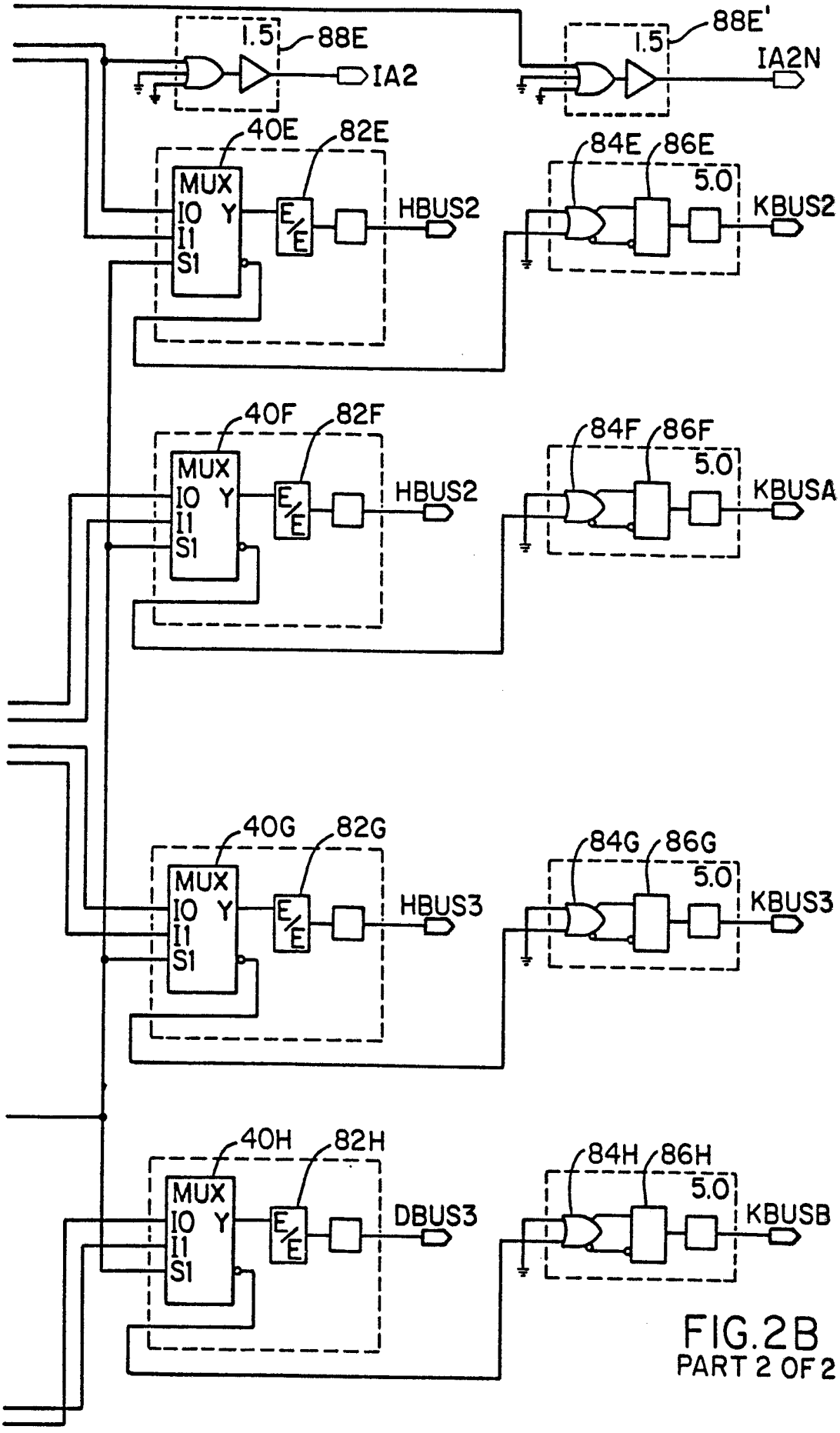


FIG.2B
PART 2 OF 2

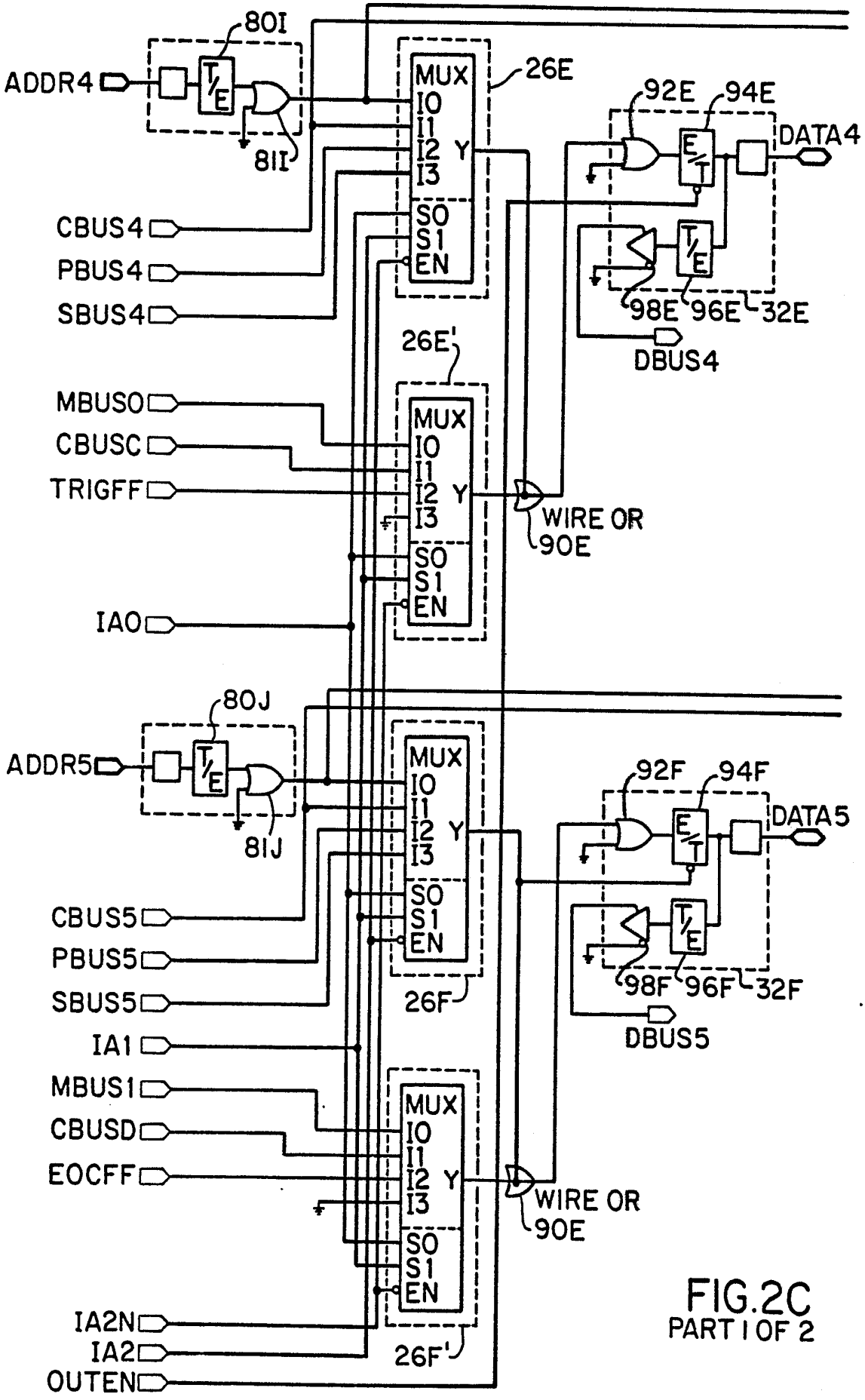


FIG.2C
PART I OF 2

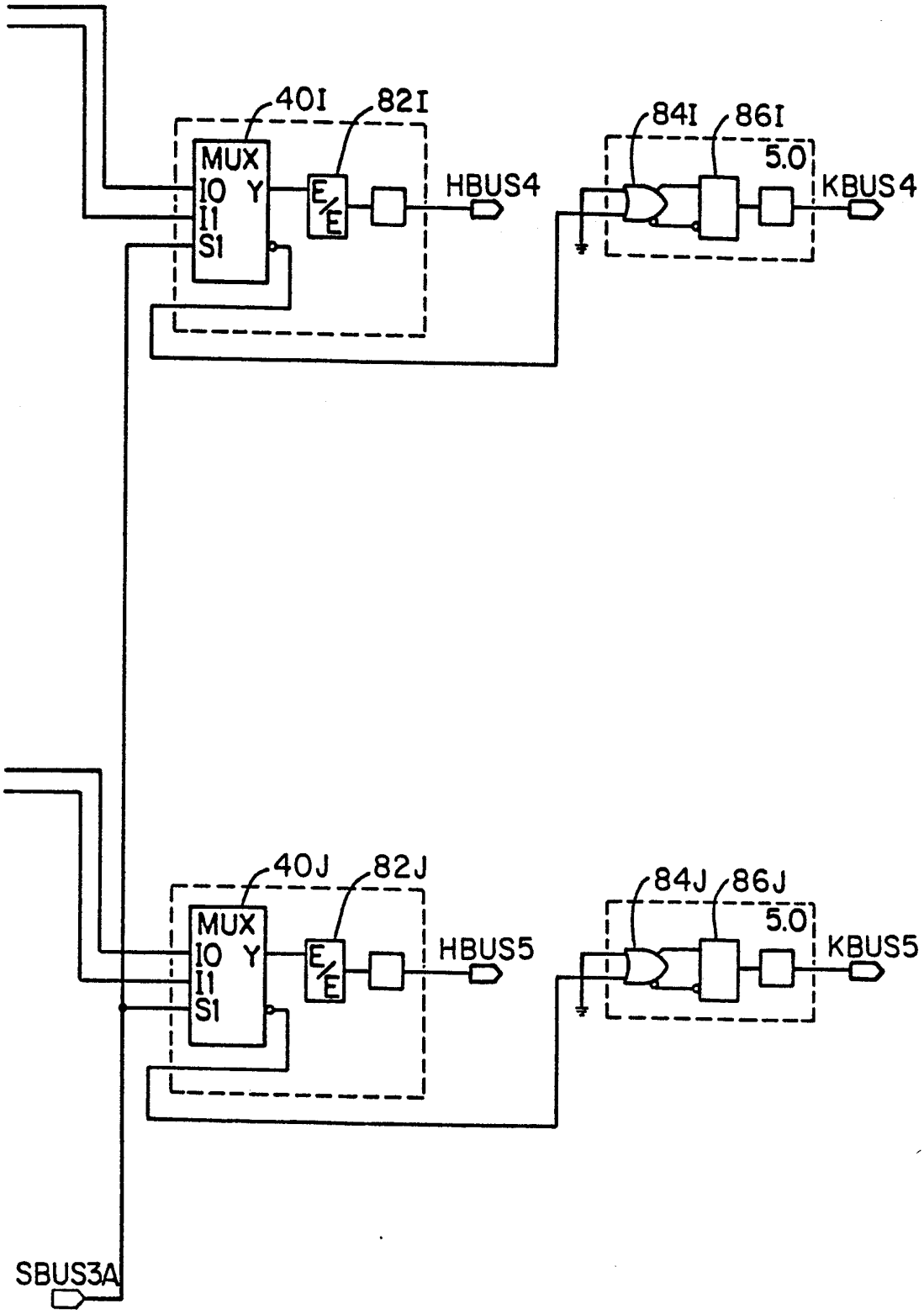


FIG.2C
PART 2 OF 2

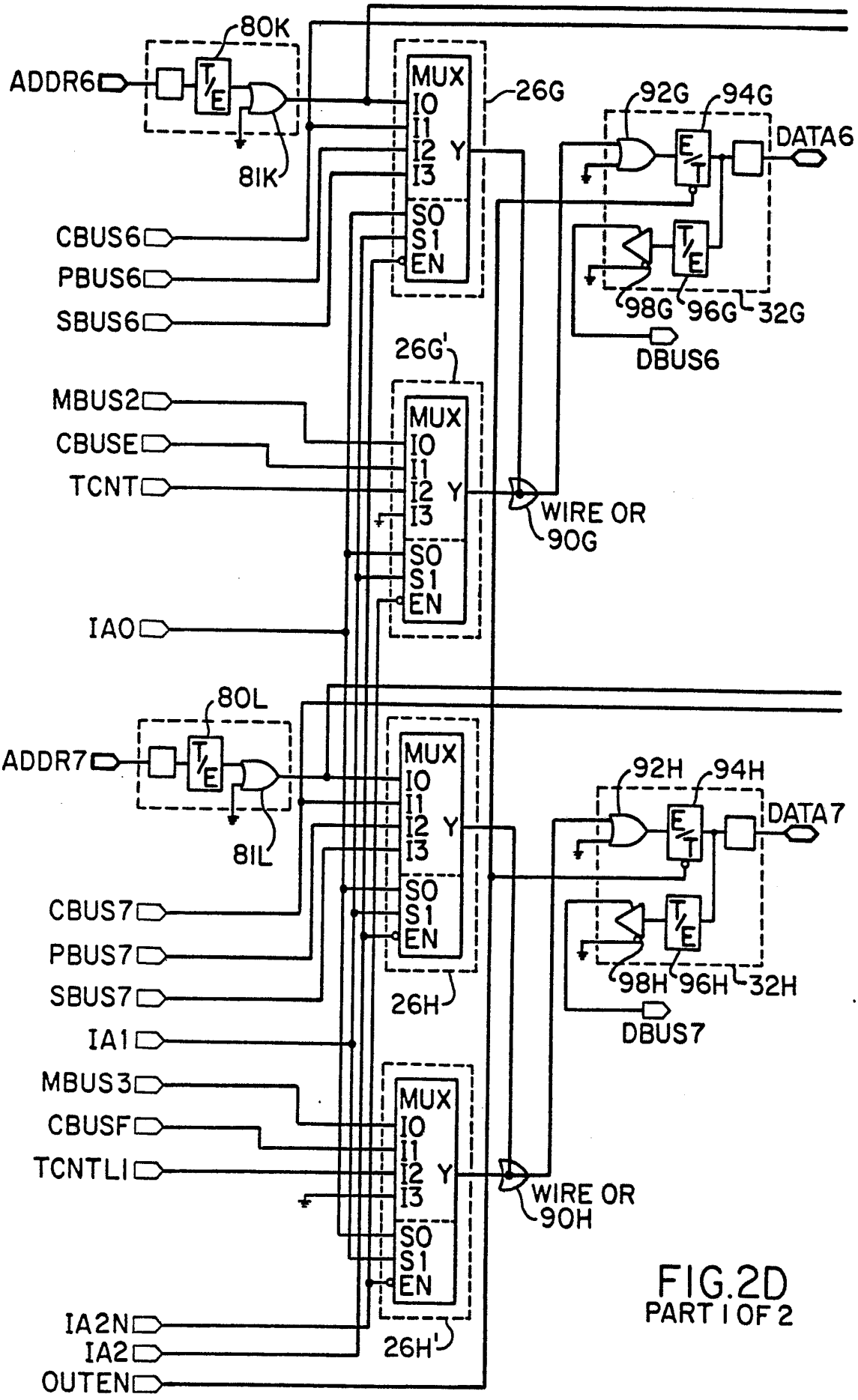


FIG.2D
PART 1 OF 2

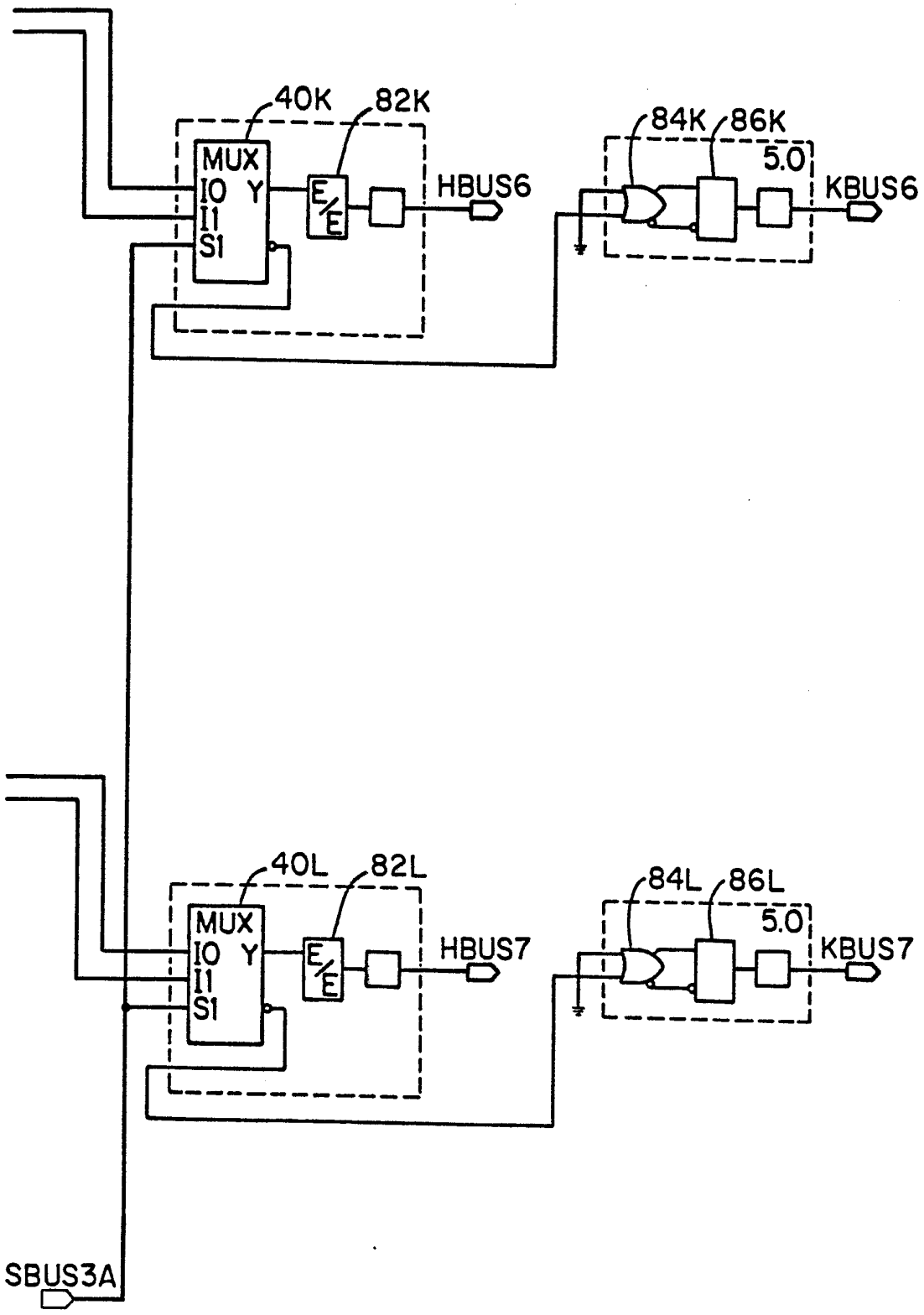


FIG. 2D
PART 2 OF 2

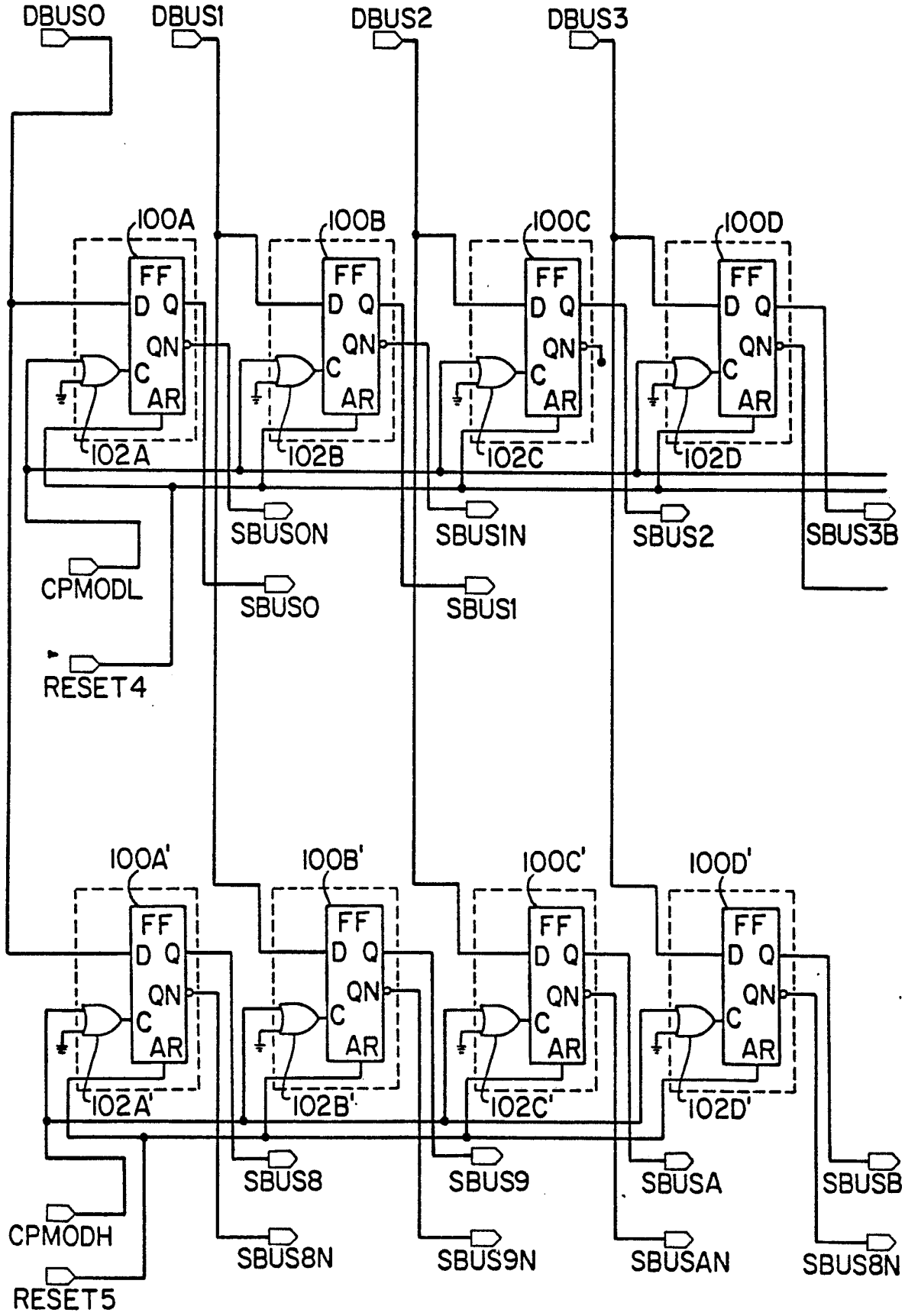


FIG.3
PART 1 OF 2

SUBSTITUTE SHEET

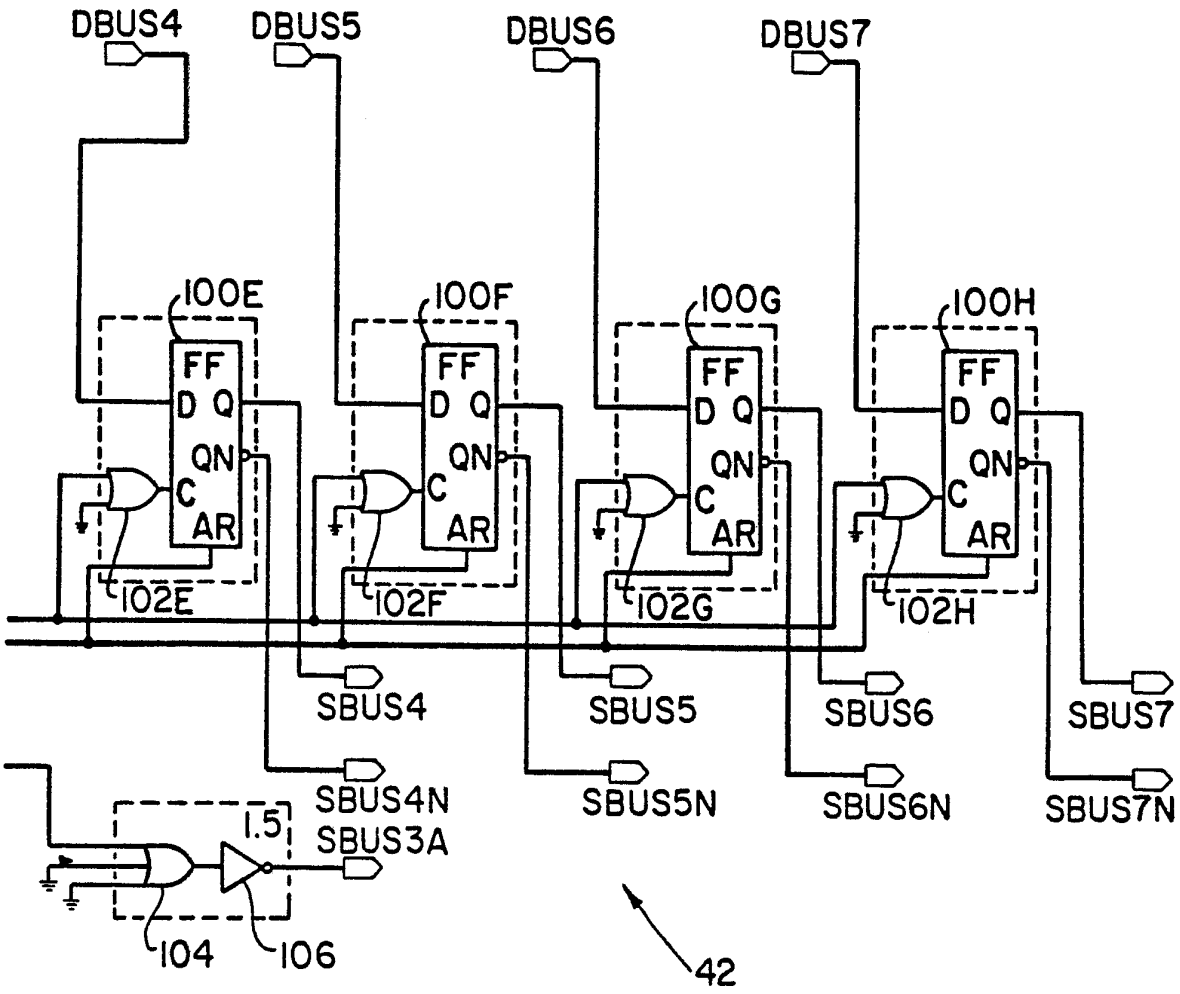


FIG.3
PART 2 OF 2

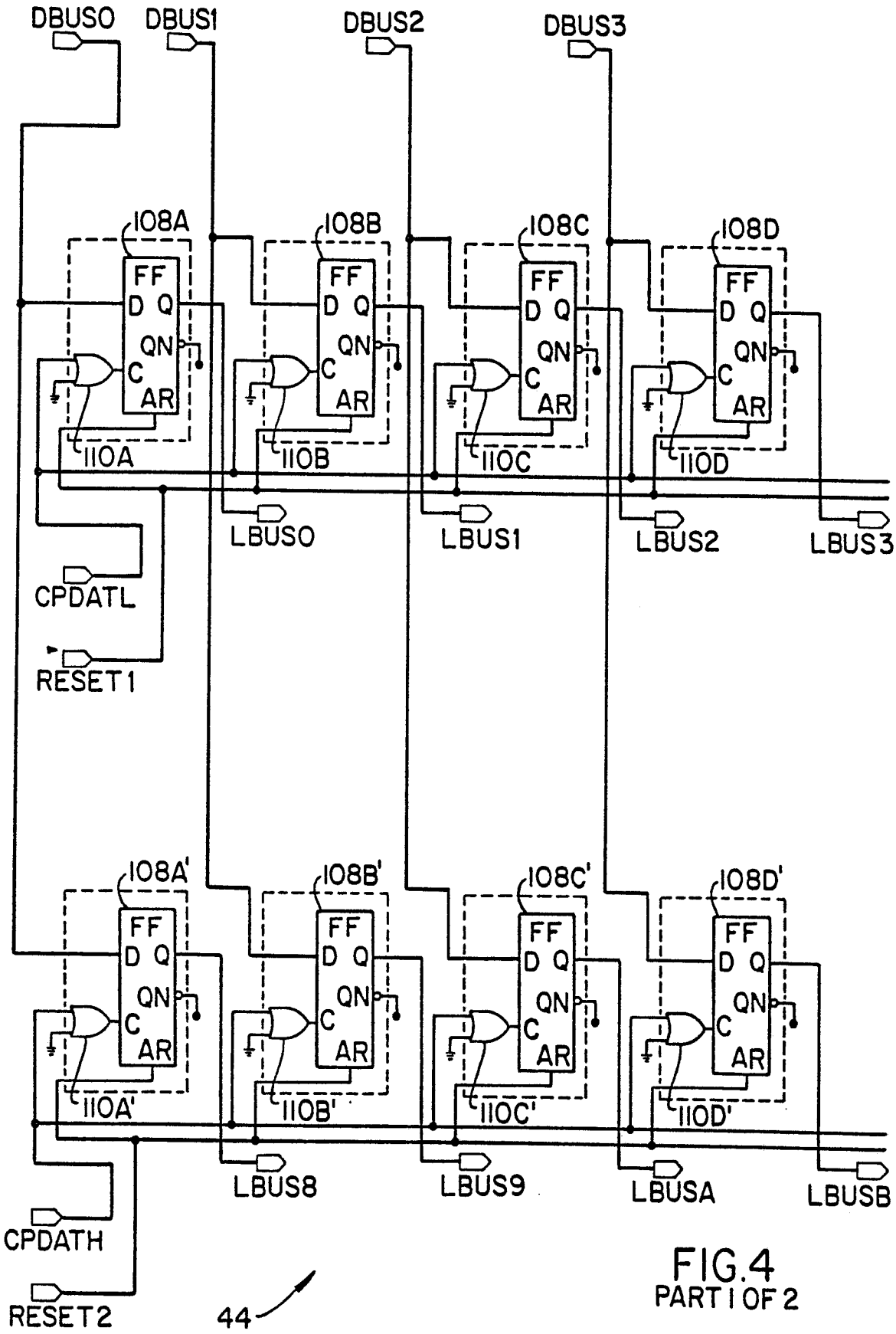


FIG.4
PART 1 OF 2

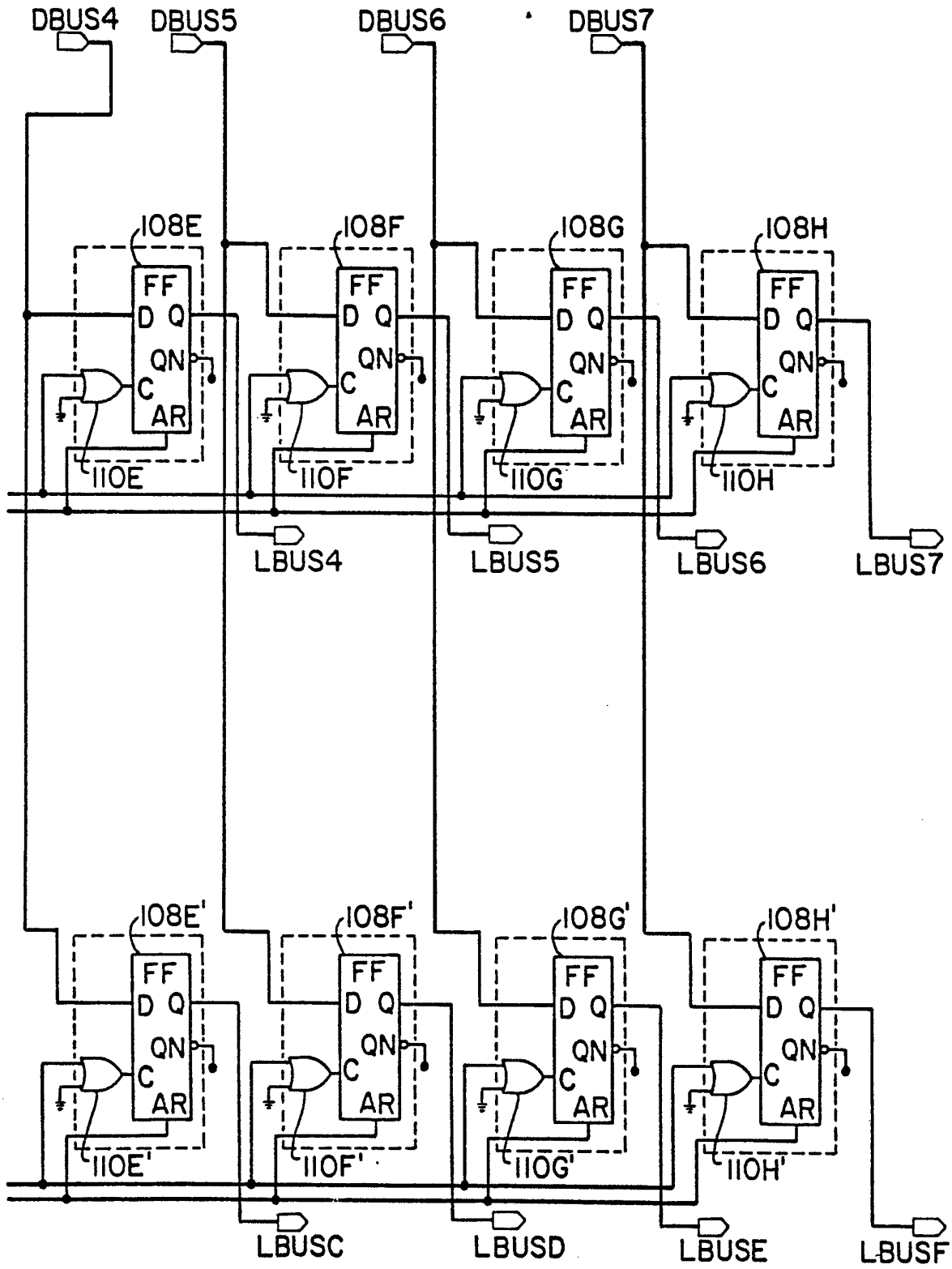


FIG.4
PART 2 OF 2

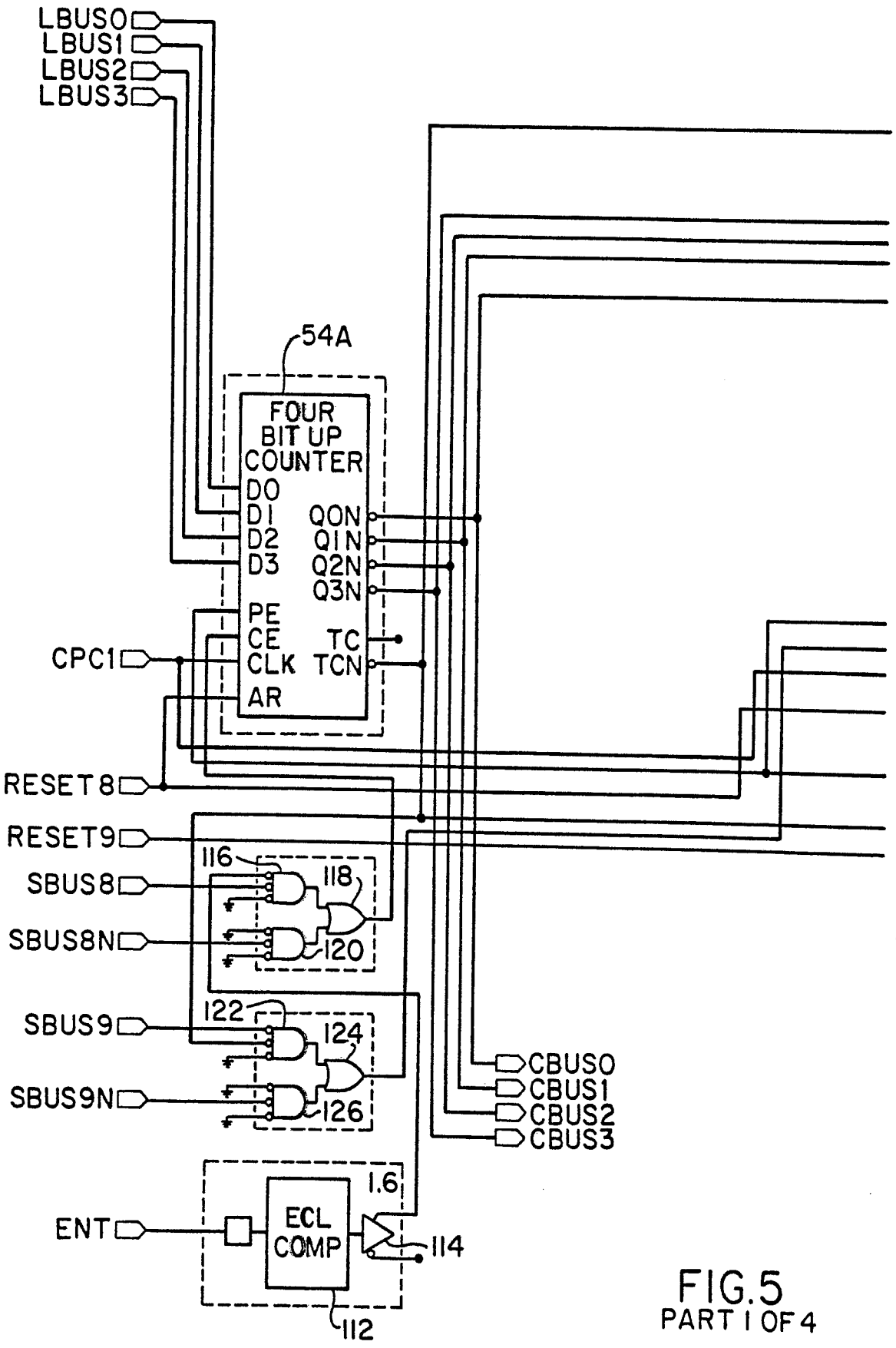


FIG.5
PART 1 OF 4

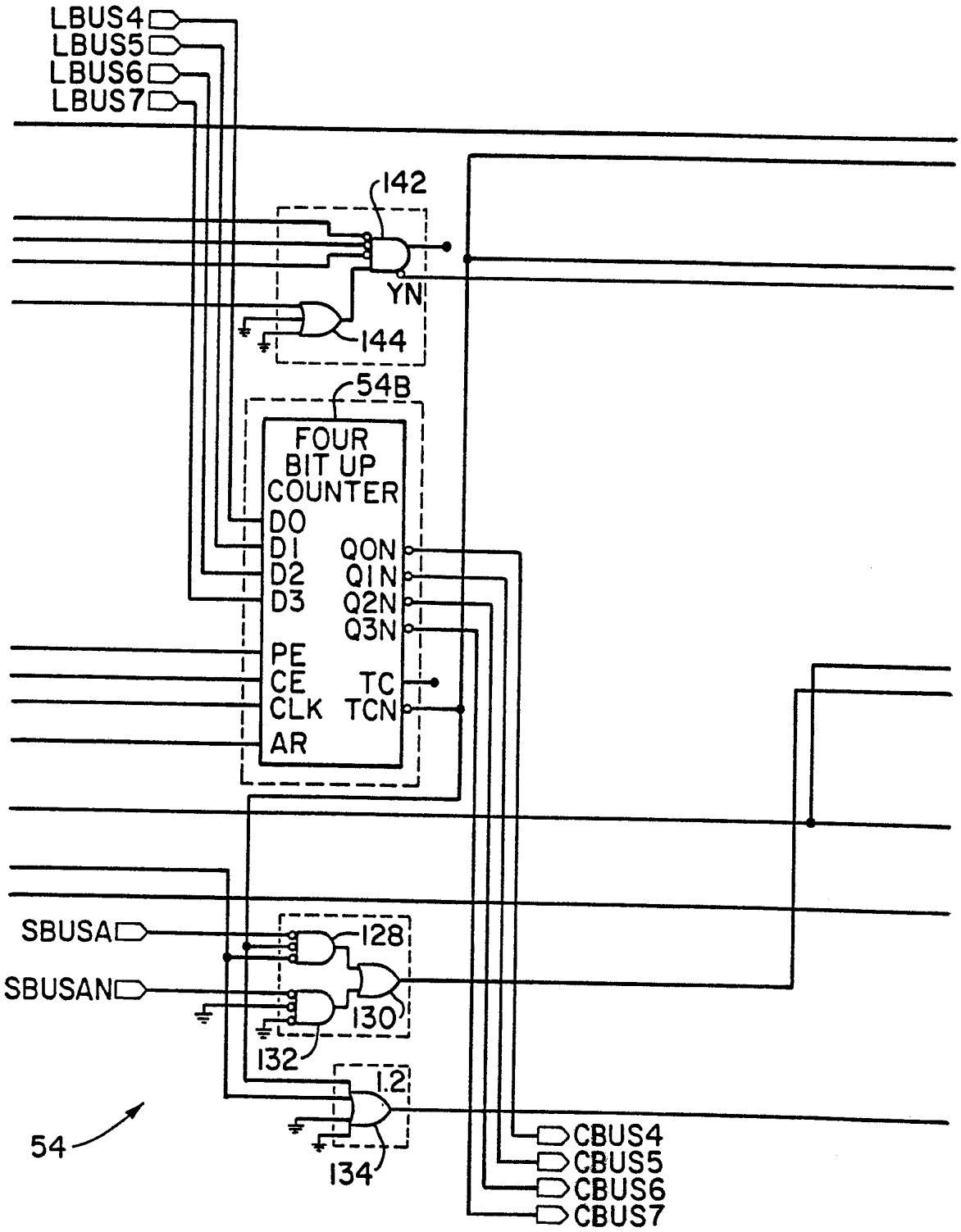


FIG.5
PART 2 OF 4

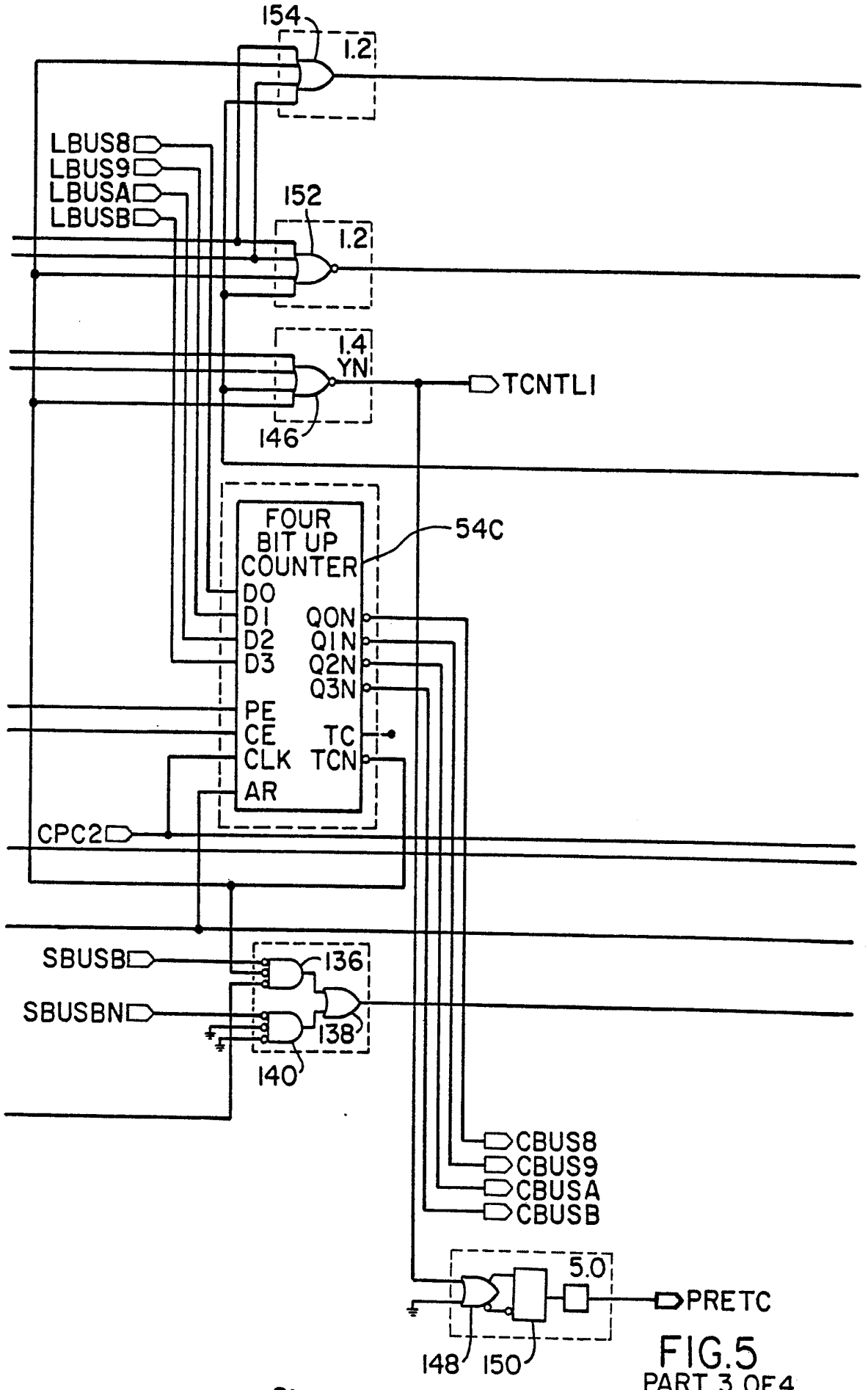


FIG.5
PART 3 OF 4

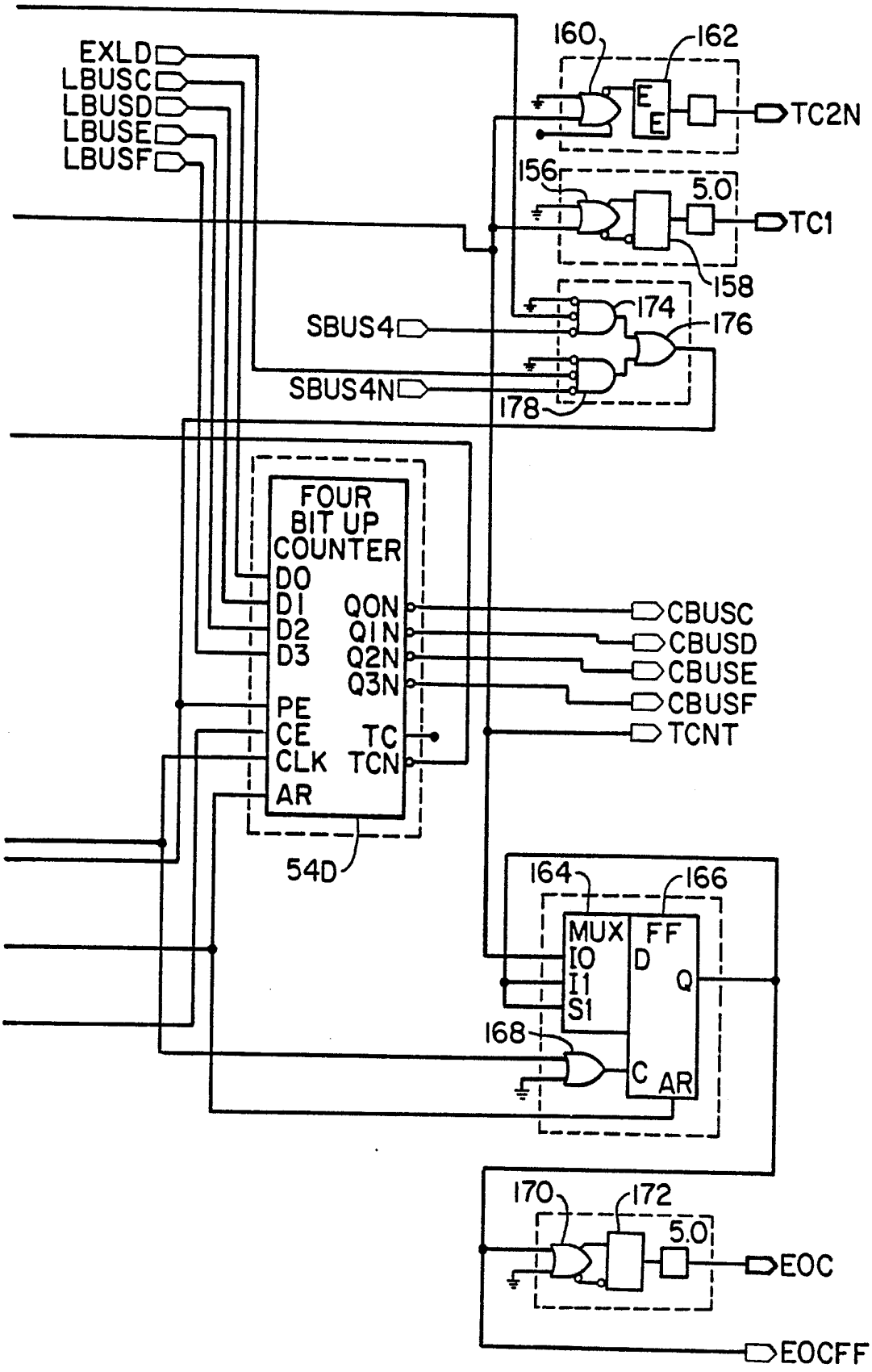
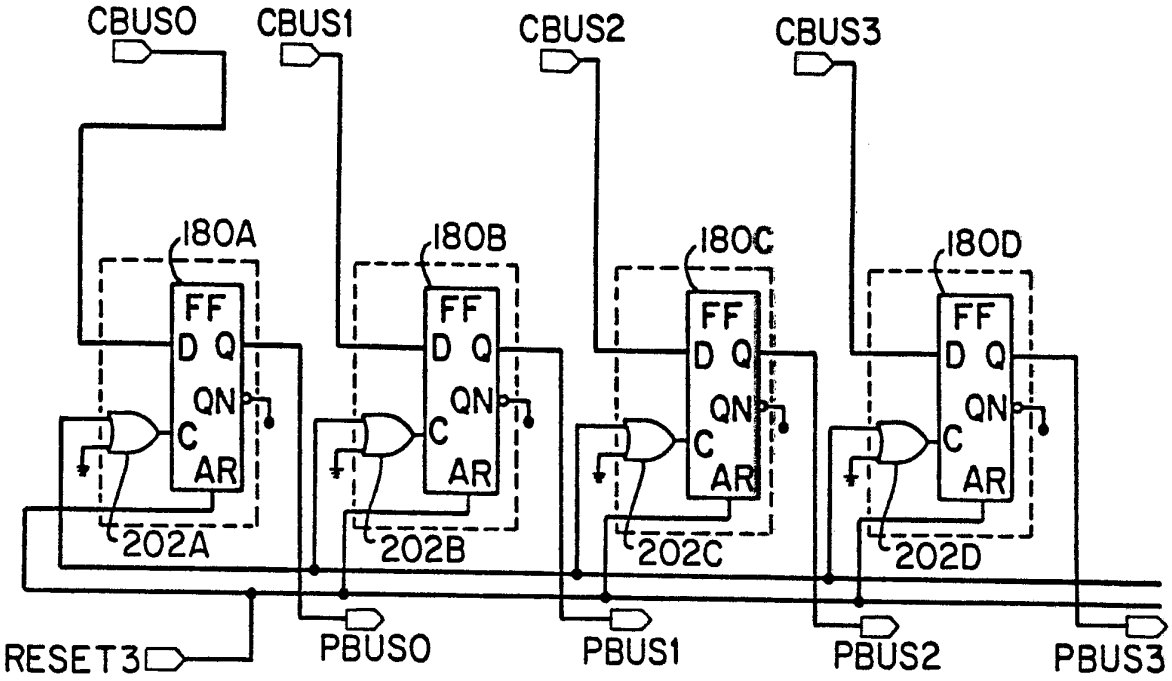


FIG.5
PART 4 OF 4



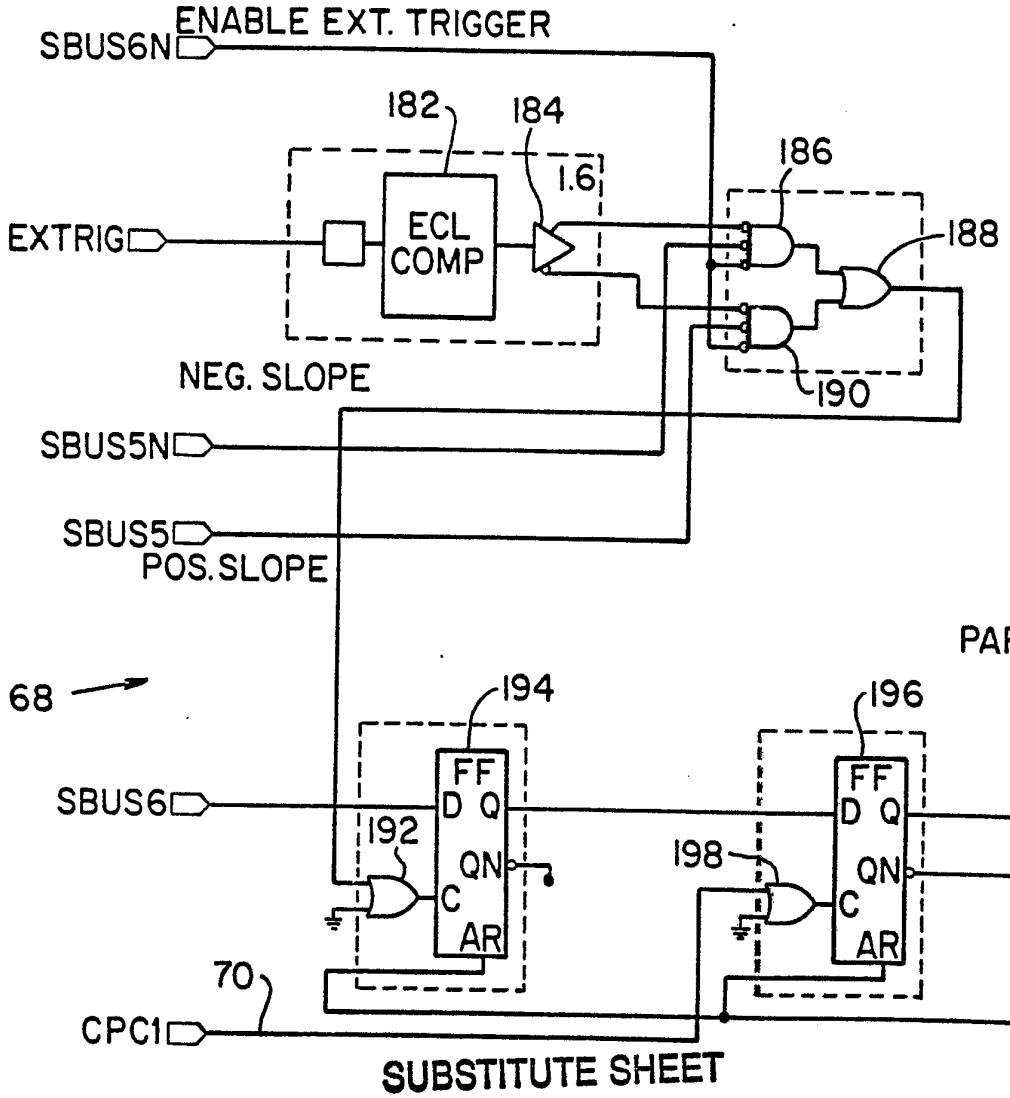


FIG.6
PART 1 OF 2

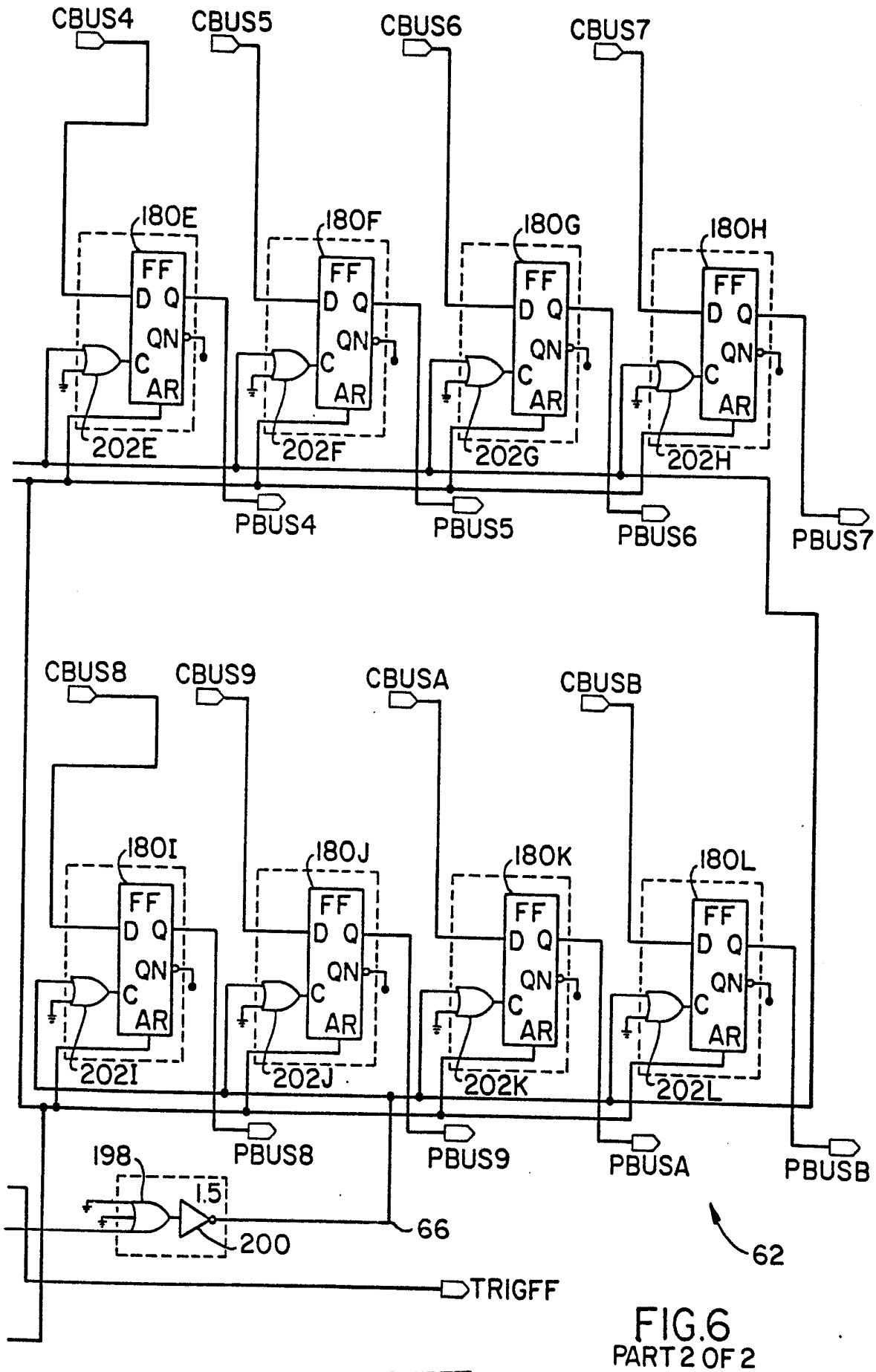


FIG.6
PART 2 OF 2

SUBSTITUTE SHEET

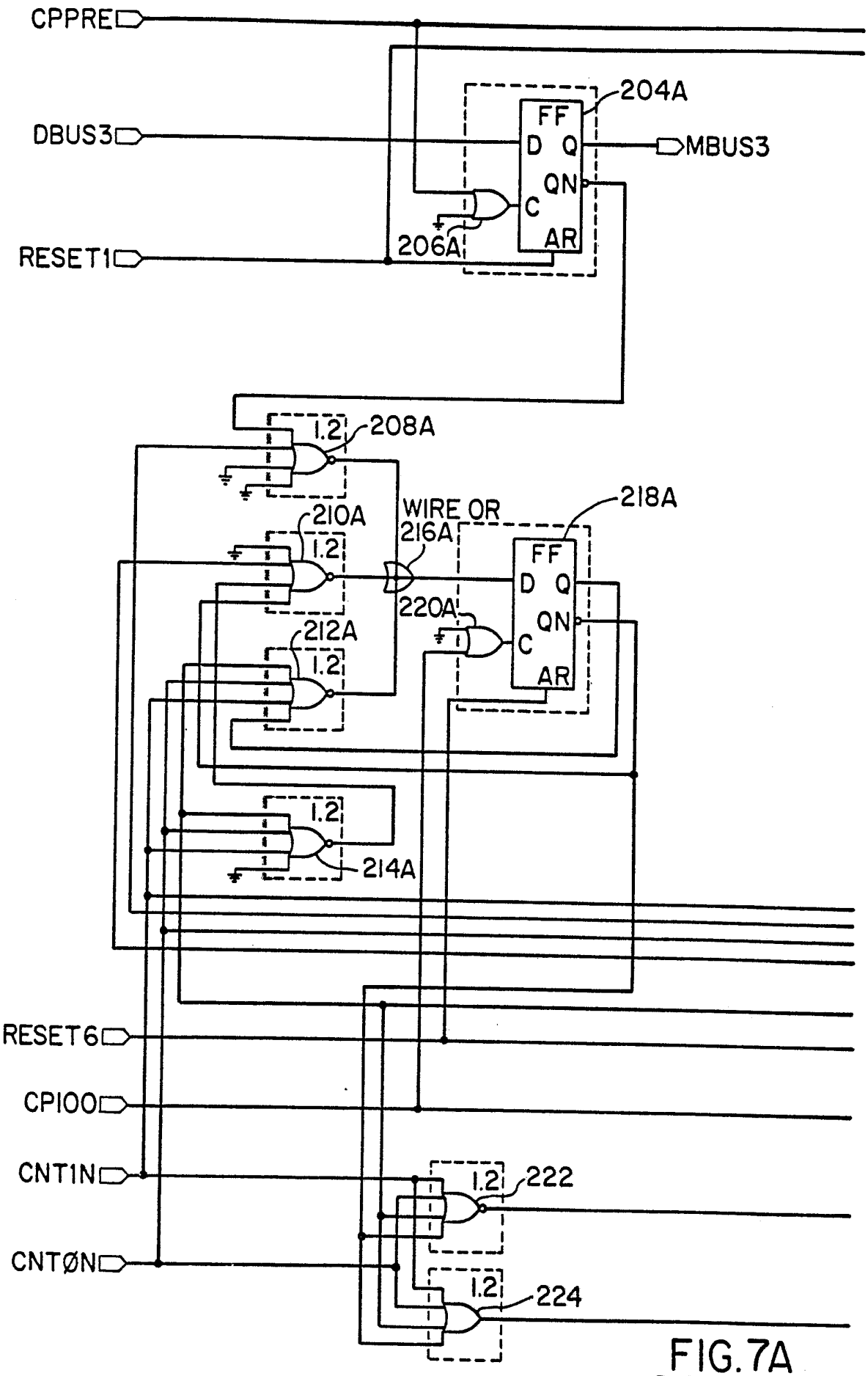


FIG. 7A
PART 1 OF 2

SUBSTITUTE SHEET

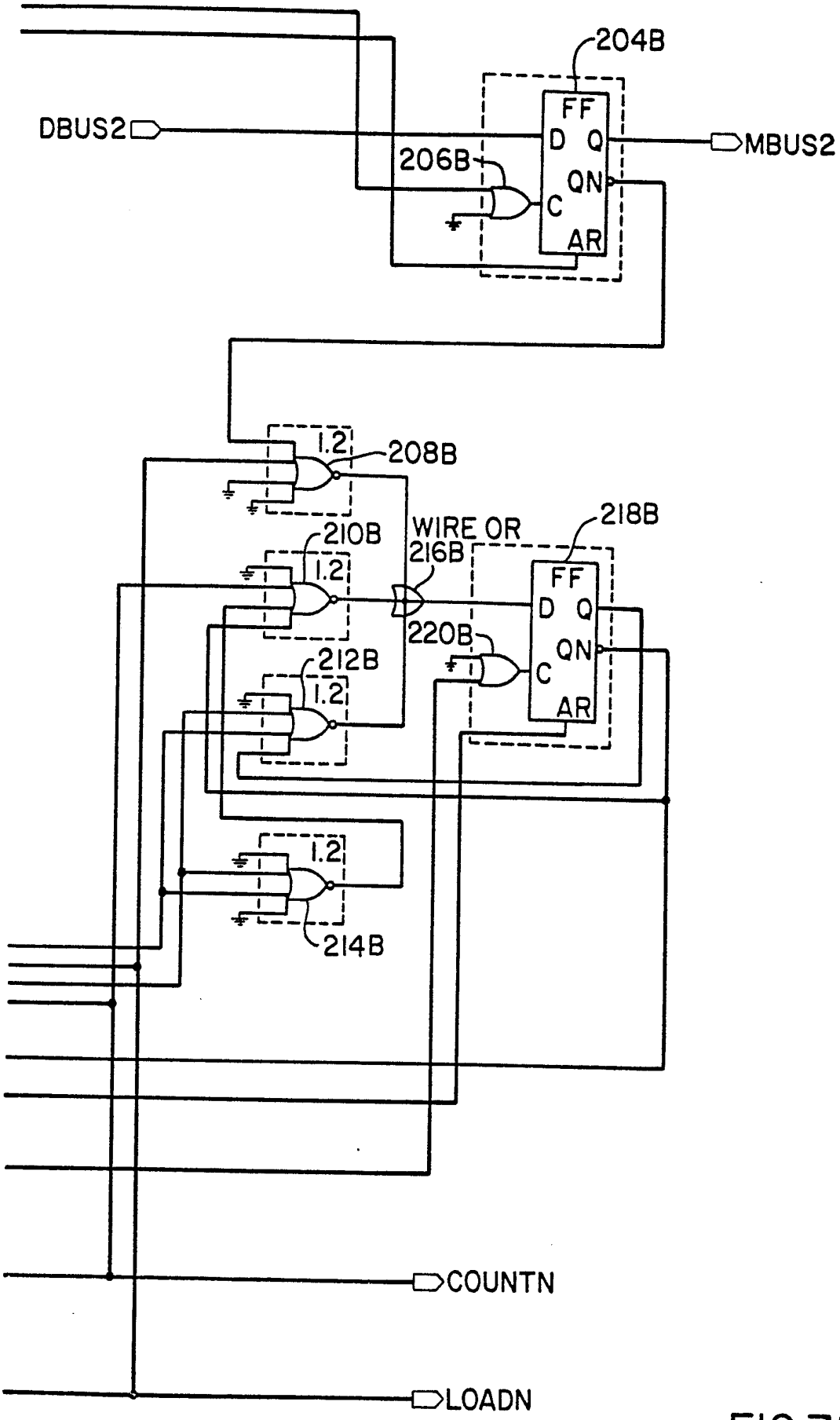


FIG.7A
PART 2 OF 2

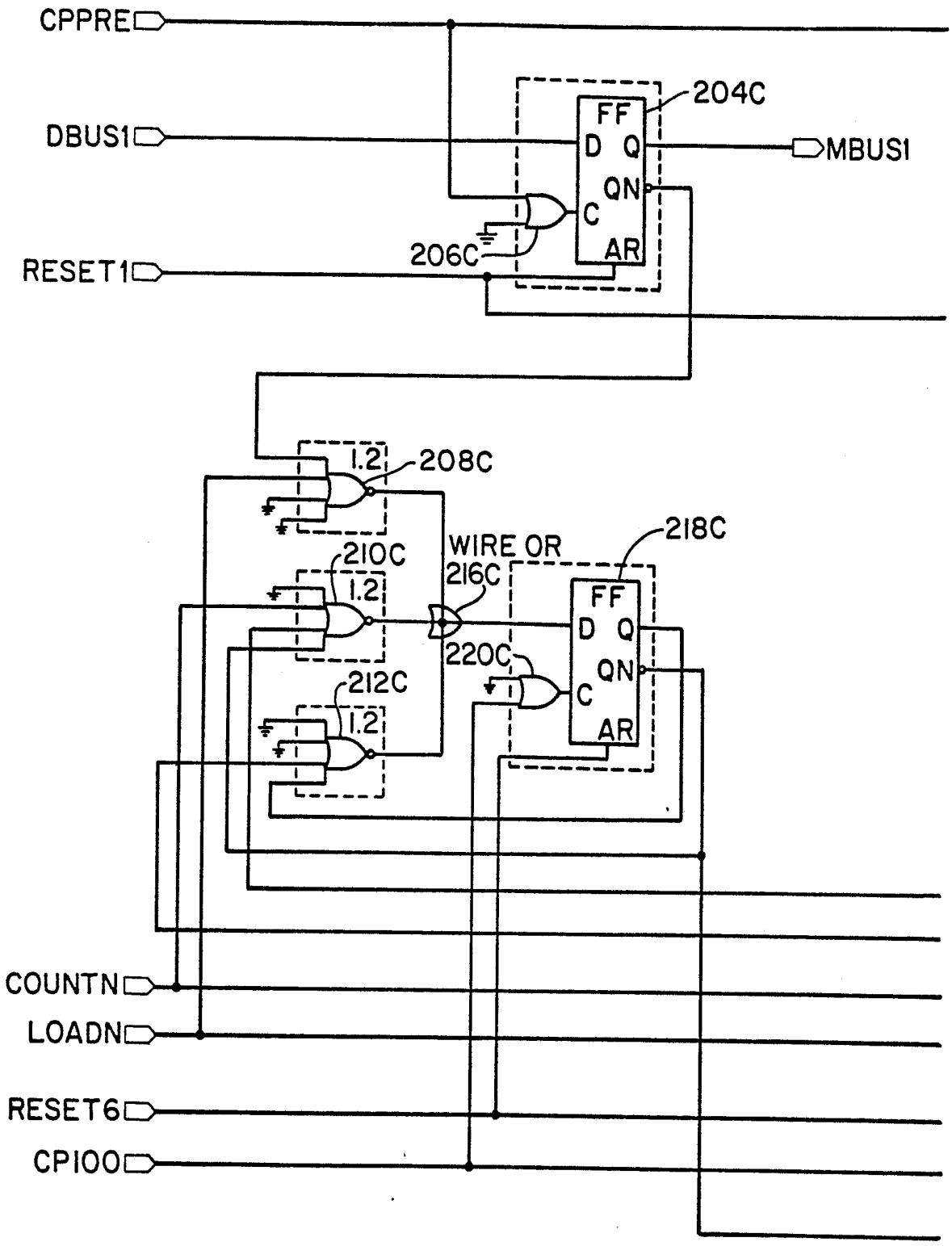


FIG.7B
PART 1 OF 2

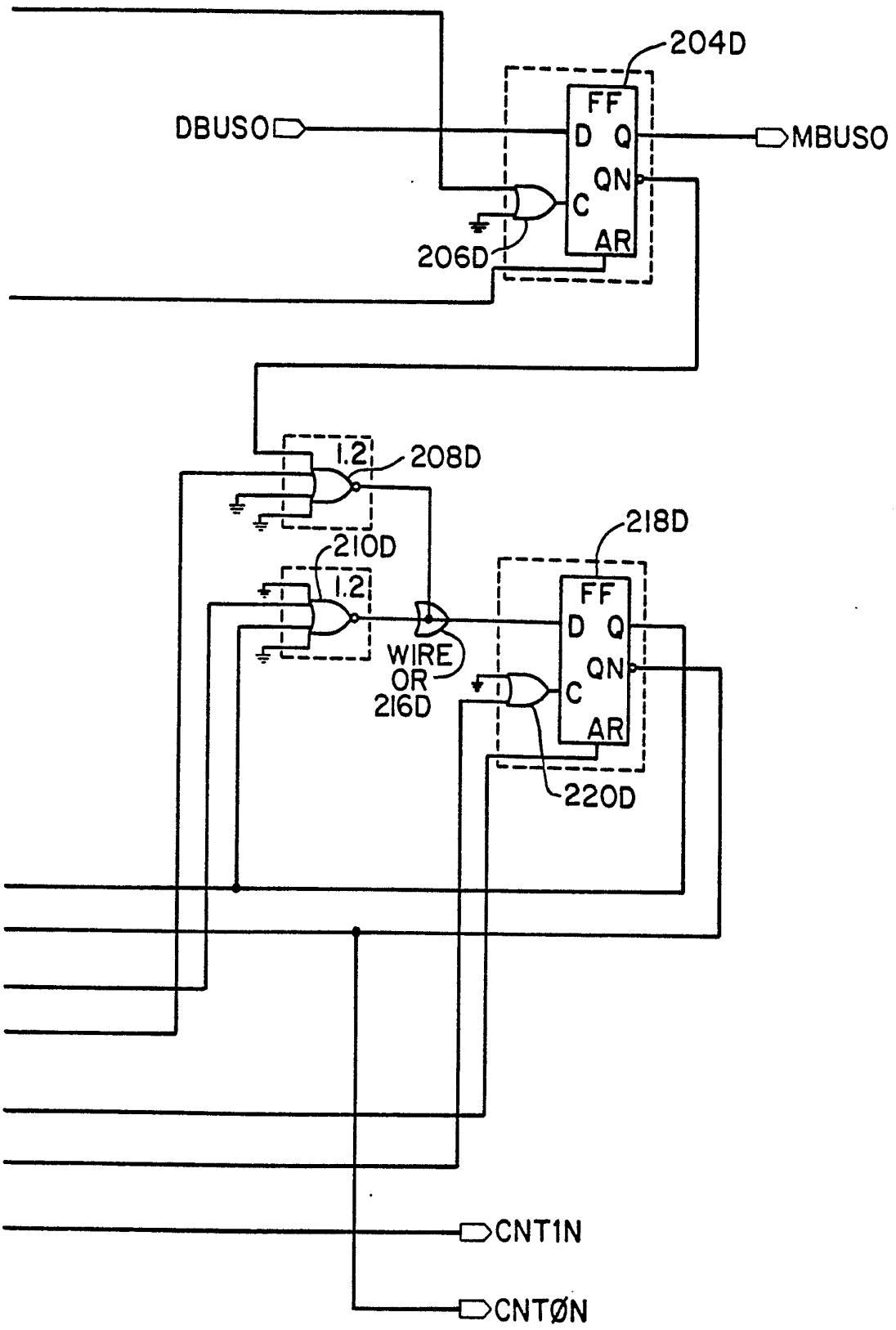


FIG.7B
PART 2 OF 2

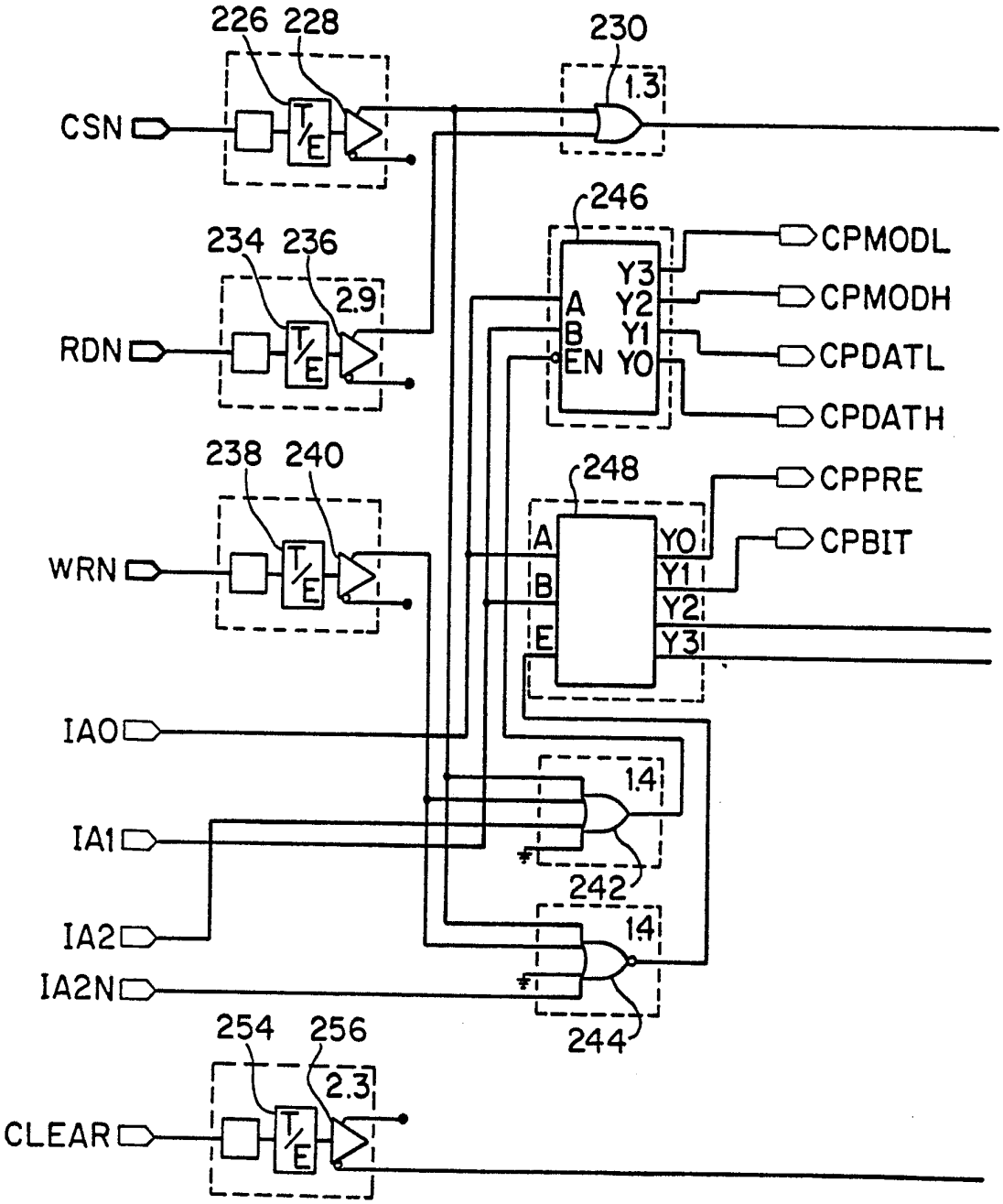


FIG.8
PART 1 OF 2

SUBSTITUTE SHEET

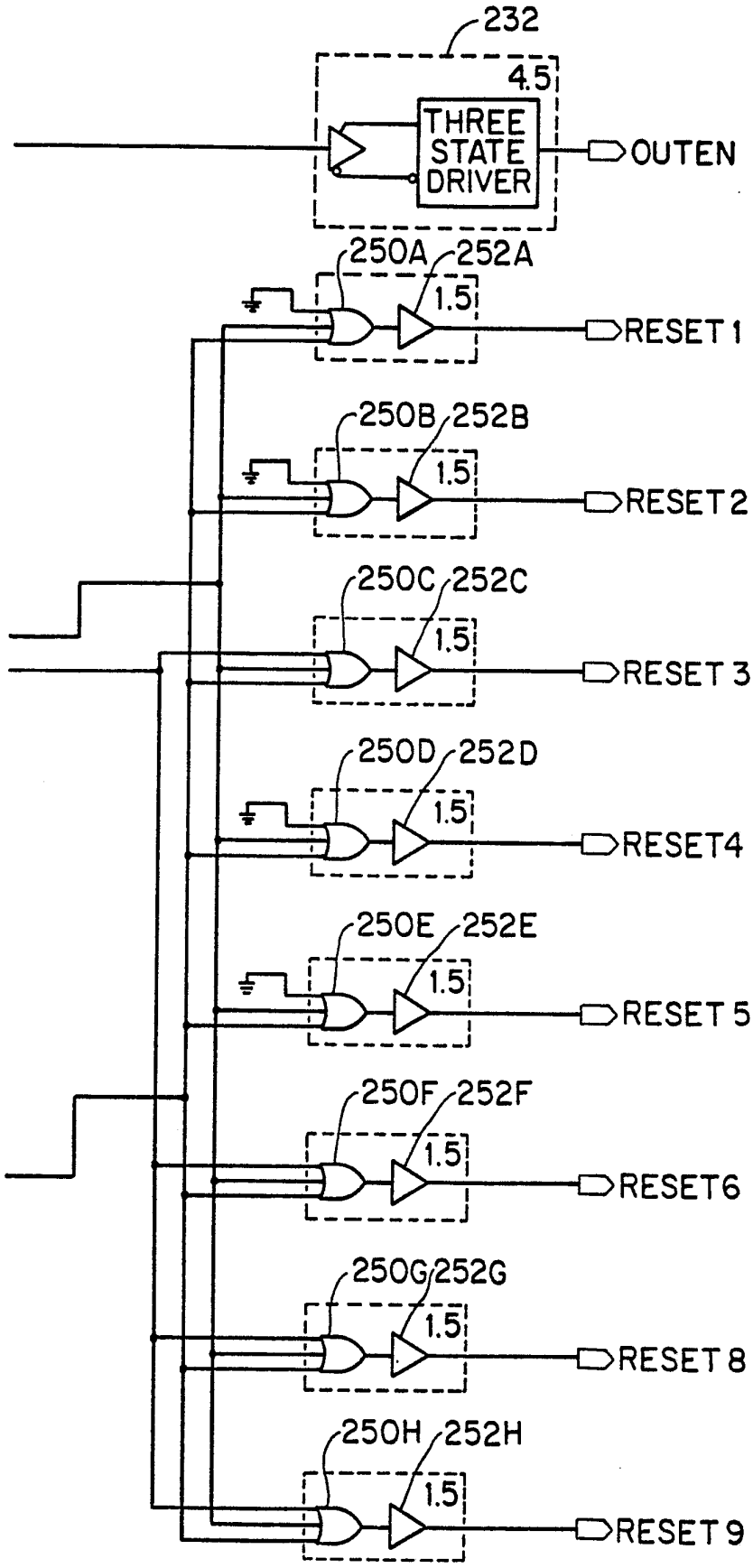


FIG.8
PART 2 OF 2

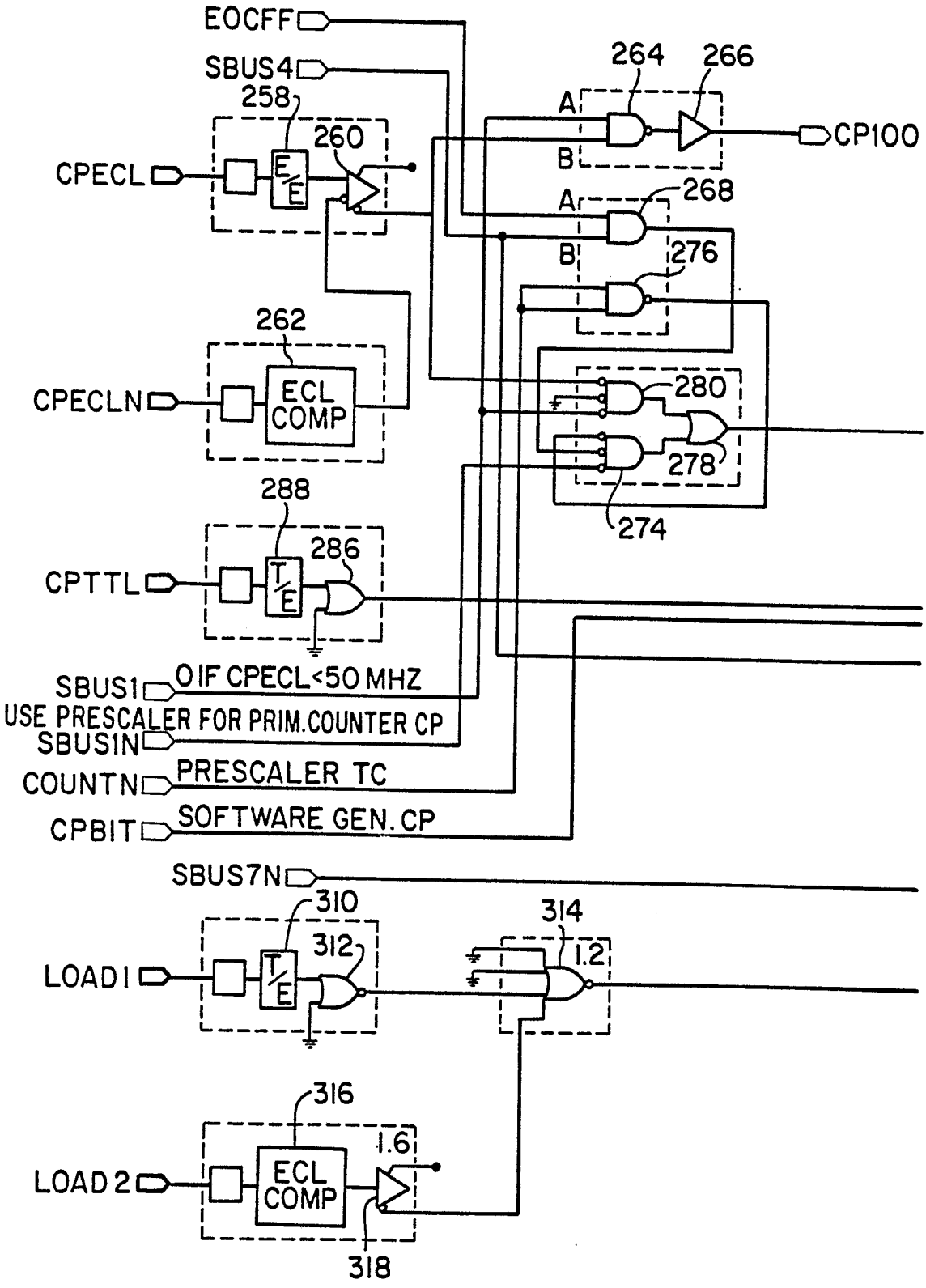


FIG.9
PART 1 OF 2

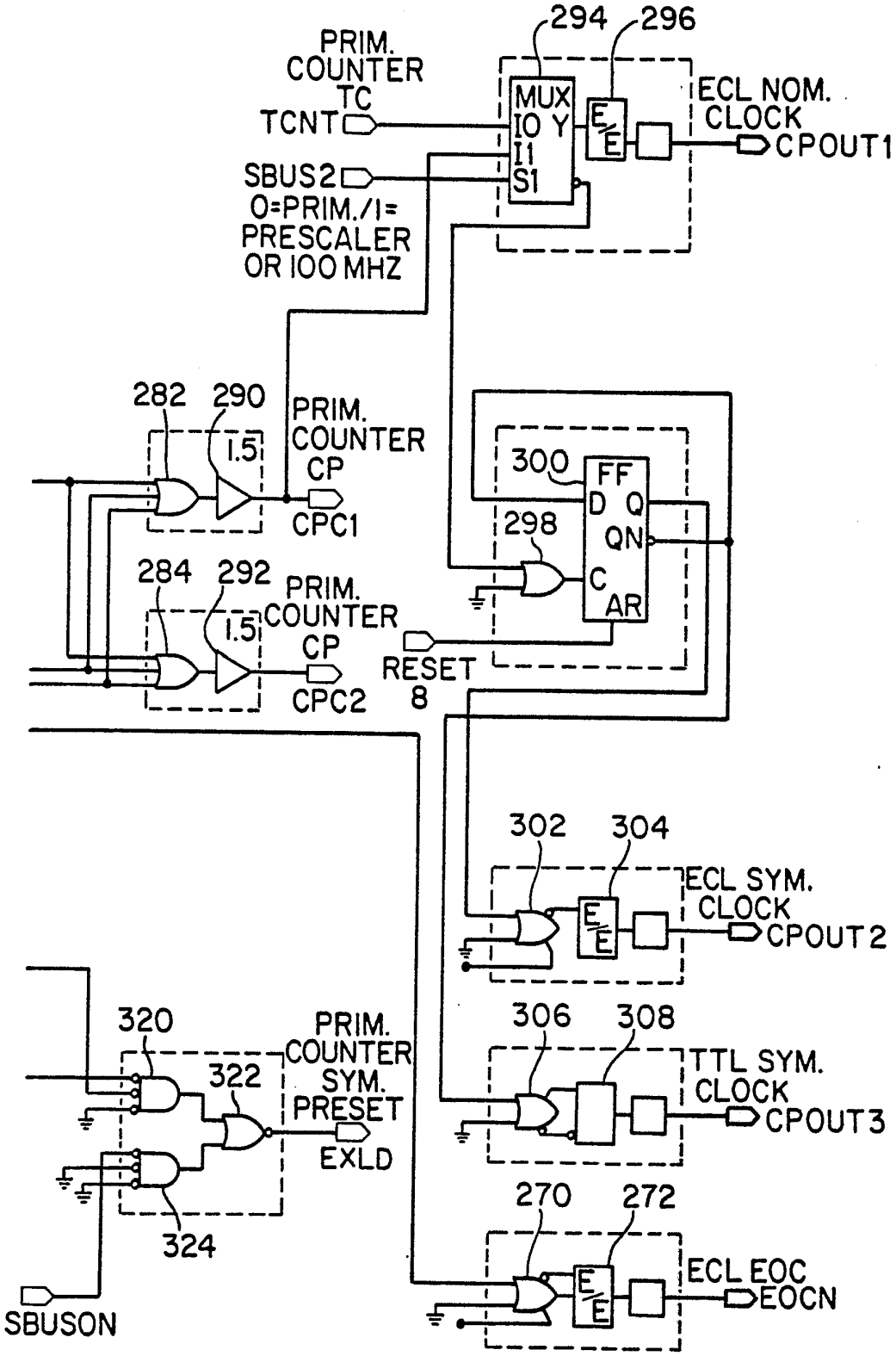


FIG.9
PART 2 OF 2

SUBSTITUTE SHEET

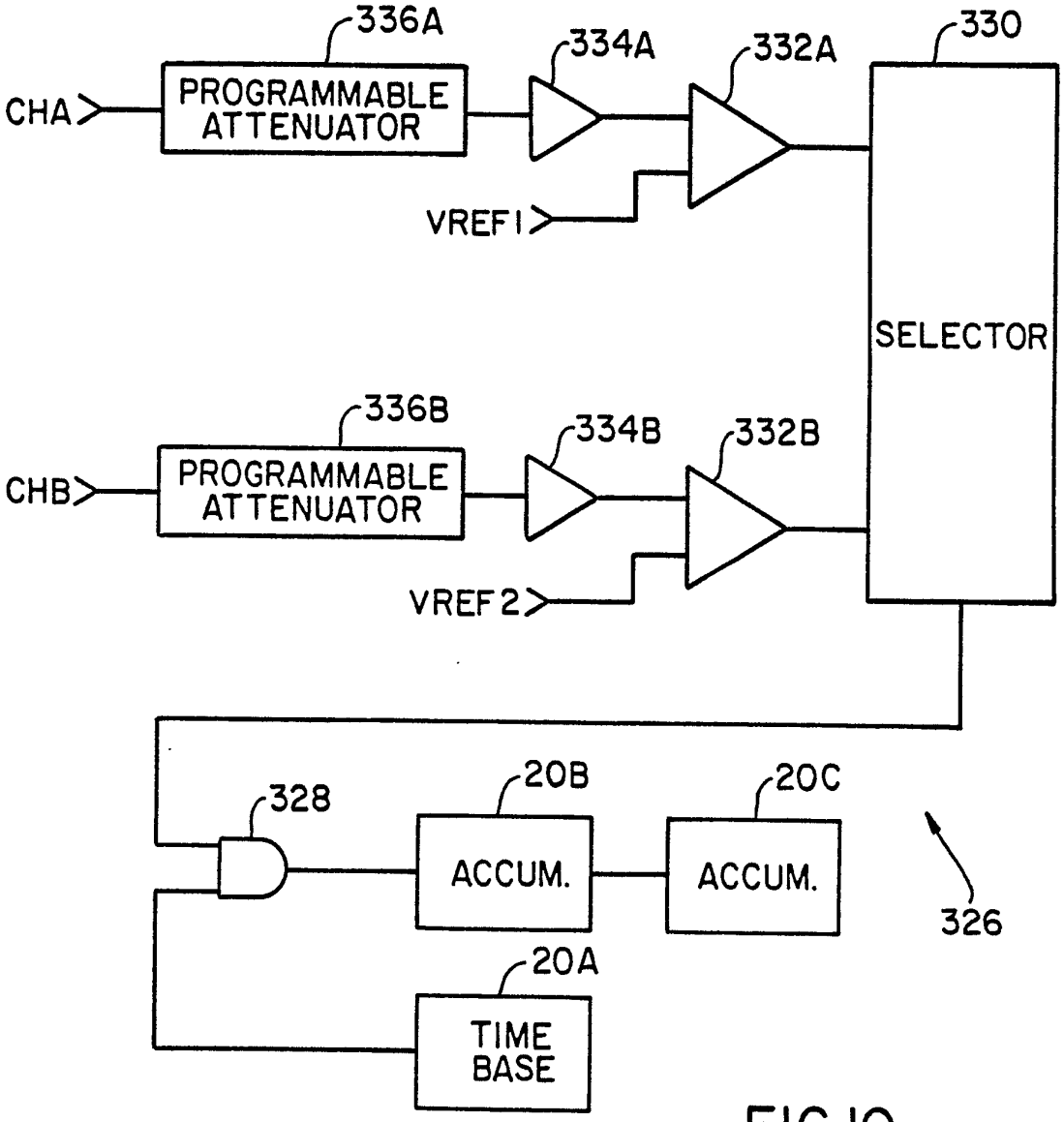

336A
334A
332A
330
CHA
PROGRAMMABLE ATTENUATOR
VREF1
SELECTOR
336B
334B
332B
CHB
PROGRAMMABLE ATTENUATOR
VREF2
328
20B
20C
ACCUM.
ACCUM.
326
20A
TIME BASE

FIG.10

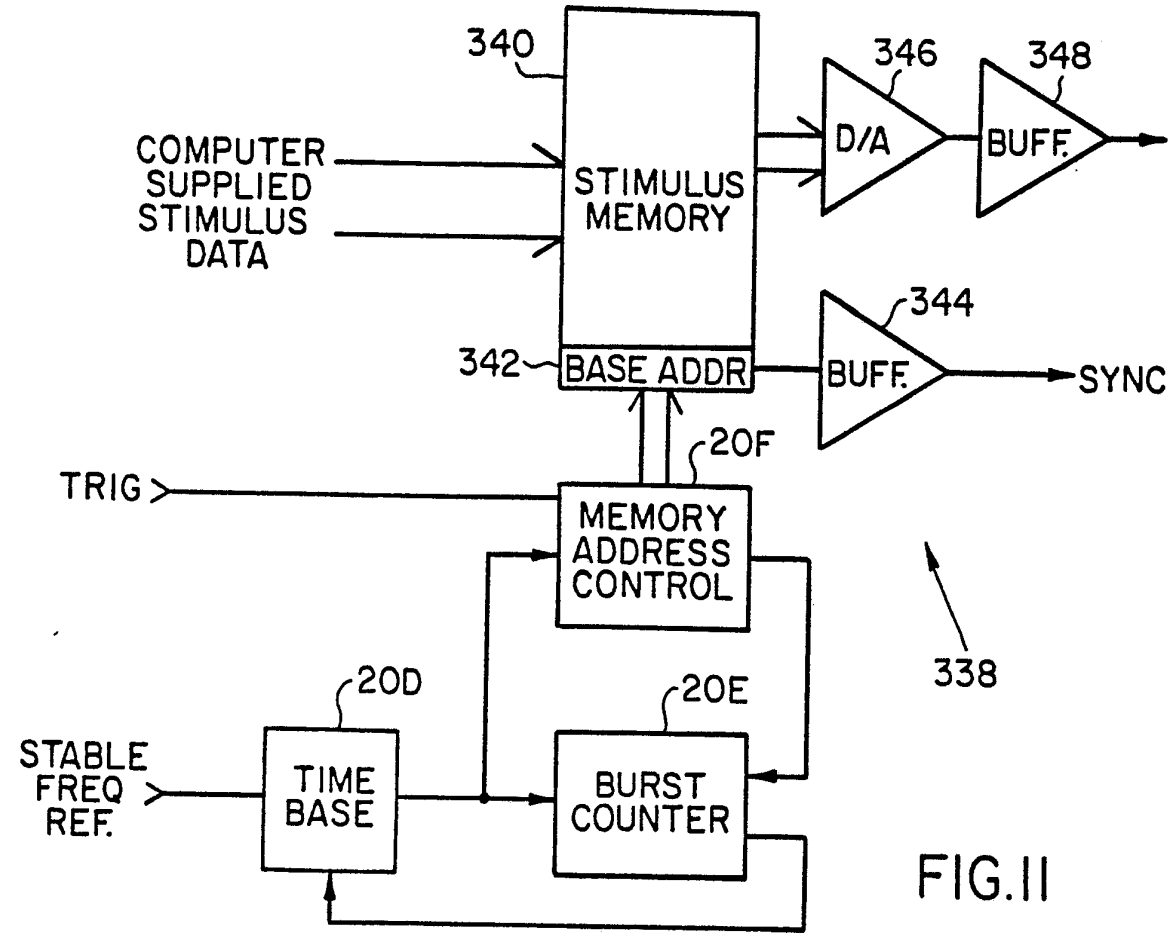

340
346
348
COMPUTER SUPPLIED STIMULUS DATA
STIMULUS MEMORY
D/A
BUFF.
344
342
BASE ADDR
BUFF.
SYNC
20F
TRIG
MEMORY ADDRESS CONTROL
338
20D
20E
STABLE FREQ REF.
TIME BASE
BURST COUNTER

FIG.11

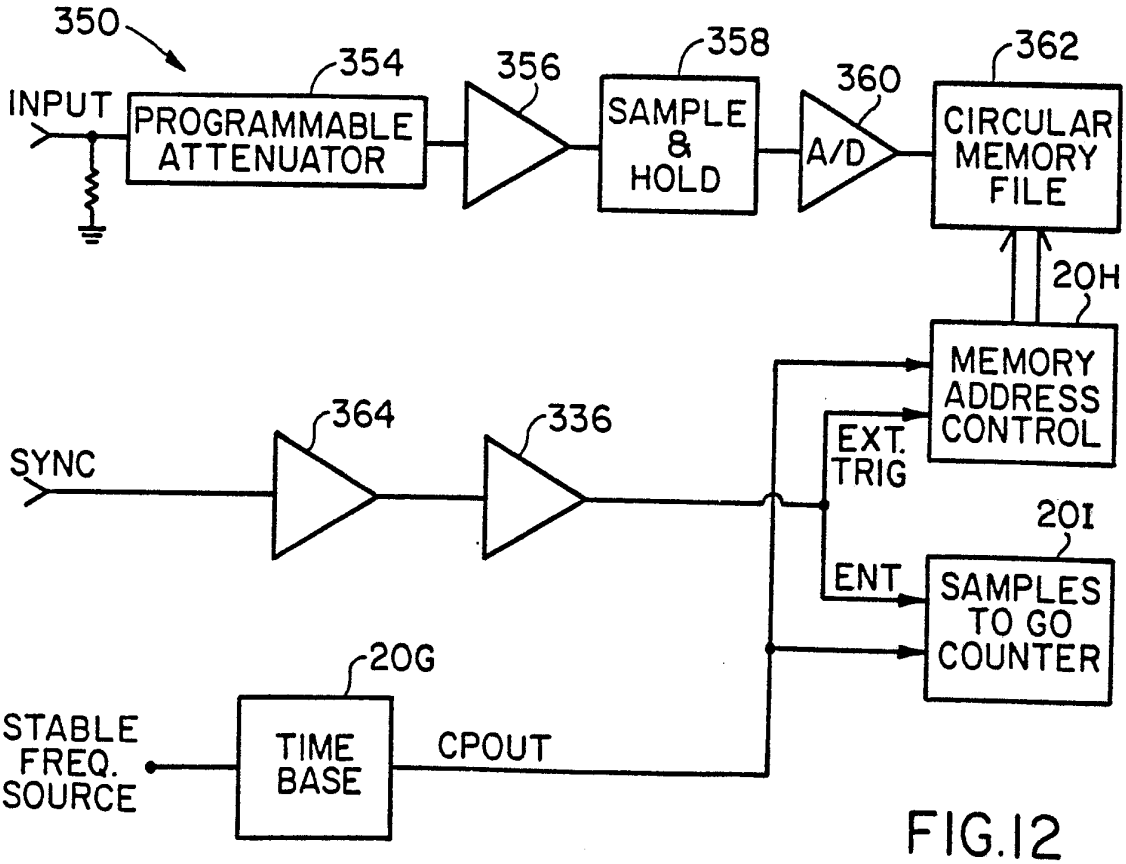

350
354
356
358
360
362
INPUT
PROGRAMMABLE ATTENUATOR
SAMPLE & HOLD
A/D
CIRCULAR MEMORY FILE
20H
MEMORY ADDRESS CONTROL
364
336
SYNC
EXT. TRIG
20I
ENT
SAMPLES TO GO COUNTER
20G
STABLE FREQ. SOURCE
TIME BASE
CPOUT

FIG.12

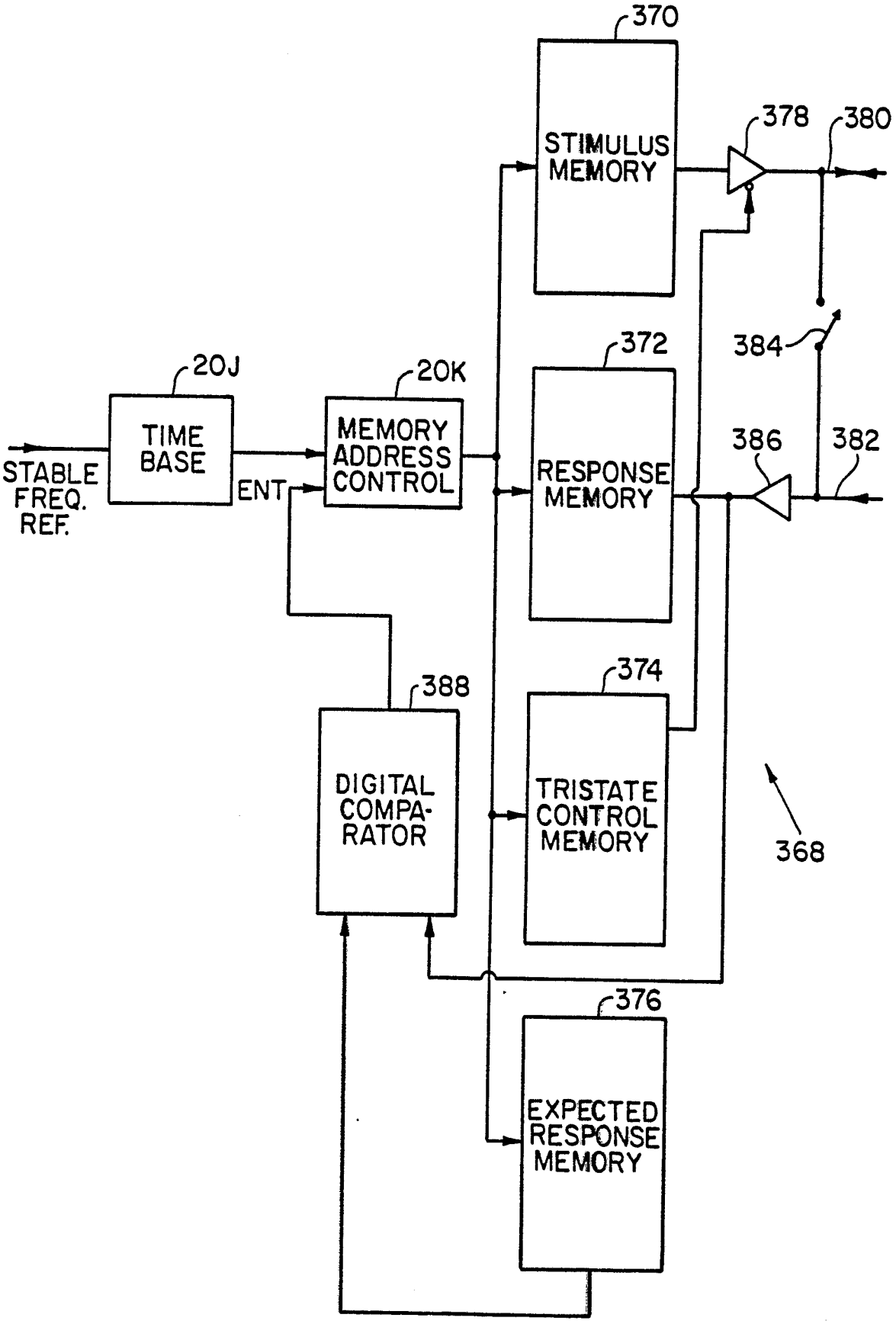

370
STIMULUS MEMORY
378
380
384
372
20J
20K
TIME BASE
MEMORY ADDRESS CONTROL
RESPONSE MEMORY
386
382
STABLE FREQ. REF.
ENT
388
374
DIGITAL COMPA-RATOR
TRISTATE CONTROL MEMORY
368
376
EXPECTED RESPONSE MEMORY

FIG.13

INTERNATIONAL SEARCH REPORT

International Application No PCT/US87/01038

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

INT CL(4) G06F 9/00
US CL 364/900

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
U.S.	364/200, 900.

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
Y	US, A, 4,438,298 (RUBIN) 20 March 1984 See Cols. 6, 7, 28-35, 64-72, 76-82 & 92-77.	1-3 & 8-11
A	US, A, 3,657,658 (KUBO) 18 April 1972 See Col. 1.	
A	US, A, 3,082,374 (BUUCK) 19 March 1963 See Cols. 2 and 3.	
Y	US, A, 4,127,823 (FROST) 28 November 1978 See Cols. 2-4.	1-3
Y	US, A, 4,316,259 (ALBRECHT) 16 February 1982 See Cols. 2-9.	1-3 & 8-11

* Special categories of cited documents: [15]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
23 JULY 1987	04 AUG 1987
International Searching Authority [1]	**Signature of Authorized Officer** [20]
ISA/US	L.E. ANDERSON

FURTHER INFORMATION CONTINUED FROM THE SECOND SHEET

V. ☒ OBSERVATIONS WHERE CERTAIN CLAIMS WERE FOUND UNSEARCHABLE [10]

This international search report has not been established in respect of certain claims under Article 17(2) (a) for the following reasons:

1. ☐ Claim numbers ..... , because they relate to subject matter [12] not required to be searched by this Authority, namely:

4-7 & 12-16

2. ☒ Claim numbers ALL , because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out [13], specifically:

See form 224

VI. ☐ OBSERVATIONS WHERE UNITY OF INVENTION IS LACKING [11]

This International Searching Authority found multiple inventions in this international application as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims of the international application.

2. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims of the international application for which fees were paid, specifically claims:

3. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim numbers:

4. ☐ As all searchable claims could be searched without effort justifying an additional fee, the International Searching Authority did not invite payment of any additional fee.

Remark on Protest

☐ The additional search fees were accompanied by applicant's protest.

☐ No protest accompanied the payment of additional search fees.