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ELECTRONICS, vol. 41, no. 6, 18th March 1968, pages 119-124, New York, US; L.L. BOYSEL: "Adder on a chip: LSI helps reduce cost of small machine"

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Description

The present invention relates to a binary subtracter stage for use in a dedicated binary subtraction circuit.

Binary subtracters are typically realized with binary adder circuits. The minuend is applied to one input port of the binary adder. The subtrahend is complemented and applied to the second input port of the binary adder. The sum output of the adder is the difference between the minuend and subtrahend. The disadvantages of this arrangement are a) the extra circuitry necessary to complement the subtrahends, and b) the complementing function increases the time required to perform a subtraction. A dedicated subtraction circuit may eliminate both of these limitations.

The design of a binary subtracter circuit requires considerations similar to those for binary adder circuits. For example, when subtracting two N-bit binary numbers, time must be provided for the "borrow" indication to propagate from the least significant bit position to the most significant bit position. Secondly, to maximize production yield and thereby to reduce production costs, at least when the circuit is realized in integrated circuit form, a minimum of circuit elements is desired.

Both of these goals are achieved in the design of a relatively fast dedicated binary subtracter stage employing a ripple-borrow generating technique in conjunction with binary subtraction circuitry. Ripple-borrow generation is an adaptation of ripple-carry generation used in binary adders. An example of ripple-carry generation may be found in U.S. Patent No. 4,357,675 entitled "Ripple-Carry Generating Circuit With Carry Regeneration'.

An adder/subtracter performing direct subtraction without operand complementing is disclosed in the publication Electronics, vol. 41, no 6, pages 119-124 published 18 March 1968 titled "Adder on a chip: LSI helps reduce cost of small machine". However, this subtracter is of a different carry generation design.

The present invention as claimed is a dedicated single-bit subtracter stage for subtracting a binary number Y from a binary number X with provision for applying a borrow, Bin, from a lesser significant subtracter stage against the minuend X and generating a borrow output signal Bout. The subtracter stage includes combinatorial logic for exclusive ORing the input numbers X, Y and Bin, the result of which corresponds to the difference X minus Y including a borrow input.

The borrow output signal, Bout, is produced at a borrow out terminal to which is connected the output terminal of a three state circuit. The numbers X and Y are applied to the three state circuit which develops a first logic output state when Y is greater than X, a second logic output state when X is greater than Y and a high impedance output state otherwise. In addition, circuitry responsive to the numbers X and Y selectively applies the Bin signal to the borrow out terminal for X equal to Y.

The invention will now be described by way of example with reference to the drawings in which,

FIGURES 1 and 3 are part logic, part schematic diagrams of alternate single bit subtraction circuits embodying the present invention; and

FIGURE 2 is a block diagram showing the interconnection of a plurality of the FIGURE 1 circuits to form a K+1 bit binary subtraction circuit.

FIGURE 1 is a single bit subtracter stage for determining the difference, Z, between two one-bit binary numbers X and Y. The stage includes a "borrow" input terminal 10 for cascade connection to a subtracter stage of lesser bit significance, and a borrow output terminal 32 for cascade connection to a subtracter stage of greater bit significance.

Binary numbers have only two values, "1" and "0". Therefore, the difference between two binary numbers can only be 1 or 0. Table I illustrates the binary arithmetic difference values for all combinations of X-Y.

TABLE I

X-Y	DIFFERENCE
1-1	0
1-0	1
0-1	1
0-0	0

It will be recognized that the correspondence shown in Table I is identical to a state table for an XOR gate having the values X and Y applied to its input terminals.

In FIGURE 1 the single bit binary numbers X and Y to be subtracted are applied to terminals 14 and 12

respectively. These numbers are coupled to exclusive OR (XOR) gate 18. The output from XOR gate 18 is the difference of X minus Y (without accommodation for a borrow from the next lesser significant digit).

The output of XOR gate 18 is applied to one input terminal of a second XOR gate 20. The borrow input from e.g. a lesser significant bit subtracter stage is applied to the second input terminal of XOR gate 20. The output terminal 34 of XOR gate 20 produces the difference Z of X minus Y including a borrow from the next lesser significant digit.

With respect to XOR gate 20, if the borrow input is a zero, XOR gate 20 passes the differences produced by XOR gate 18 unchanged. Alternatively if the borrow input is a one, XOR gate 20 complements the differences produced by XOR gate 18. Arithmetically, the output of XOR gate 20 corresponds to X reduced by the borrow input minus Y. Table II shows all of the possible combinations of the values of X, Y and the borrow input, Bin.

TABLE II

X	Y	Bin	X-Bin	$Bout_1$	X-Bin-Y	$Bout_2$	X⊛Y	(X⊛Y)⊛Bin
0	0	0	0	0	0	0	0	0
1	0	0	1	0	1	0	1	1
0	1	0	0	0	1	1	1	1
1	1	0	1	0	0	0	0	0
0	0	1	1	1	1	0	0	1
1	0	1	0	0	0	0	1	0
0	1	1	1	1	0	0	1	0
1	1	1	0	0	1	1	0	1

The first, second and third columns of Table II are the values of X, Y and Bin. The column labelled (X-Bin) contains the values of X reduced by the borrow input. The column labelled ($Bout_1$) corresponds to borrow output states resulting from the operation X-Bin. The column labelled (X-Bin-Y) contains the values which result from arithmetically subtracting Y from the values of X reduced by the Bin values. The column labelled ($Bout_2$) lists the borrow output values resulting from the operation (X-Bin-Y). The column labelled (X⊛Y) contains the values output by XOR gate 18 corresponding to the logical function X⊛Y where the symbol ⊛ designates the exclusive OR function. Finally, the column labelled ((X⊛Y)⊛Bin) contains the output values from XOR gate 20 corresponding to the exclusive ORing of (X⊛Y) and Bin.

It is seen that the values in the rightmost column labelled (X⊛Y)⊛Bin) resulting from the exclusive ORing of X, Y and Bin, are equal to the arithmetic differences shown in the column labelled (X-Bin-Y). Thus, the combination of XOR gates 18 and 20 produce the differences Z = X-Y including a borrow input.

The remainder of the FIGURE 1 circuitry generates the borrow out values. The borrow output must be a one whenever either the $Bout_1$ or $Bout_2$ values in Table II are one. A little reflection will convince the reader that a borrow output "one" value should occur whenever the borrow input is greater than X, the subtrahend, Y, is greater than the minuend, X, or Y is equal to X and there is a borrow input. These conditions are all satisfied by the combination of $Bout_1$ and $Bout_2$ values.

In FIGURE 1, the borrow output terminal 32 is coupled to the borrow input terminal 10 by a p-type enhancement mode transistor 22. Transistor 22 couples terminal 32 to terminal 10 when a zero level potential is applied to its gate or control electrode. XOR gate 18 controls transistor 22, and conditions it to pass the value Bin to terminal 32 whenever the input numbers X and Y have the same value, corresponding to the zero values in the column labelled (X⊛Y) of Table II. This occurs in rows 1, 4, 5 and 8 of the table. Note in row 5 a Bin value of one is coupled to terminal 32 to satisfy the one value in row 5 of column $Bout_1$ and a Bin value of one is coupled to terminal 32 to satisfy the one value in row 8 of column $Bout_2$. In rows 1 and 4 transistor 22 couples a borrow in zero to terminal 32 satisfying the $Bout_1$ and $Bout_2$ zero values. Note further that transistor 22 is never "on" when the borrow out is a one and the borrow in is a zero.

The series connection of transistors 24 and 26 between terminal 32 and positive supply potential V_D, and transistors 28 and 30 between terminal 32 and ground develop the remaining borrow output signals. Transistors 24 and 26 are both p-type devices and transistors 28 and 30 are both n-type devices. Complementary transistors 26 and 28, having their gate electrodes coupled together, operate in a complementary mode so that there is never a conducting path between positive supply V_D and ground potential.

A one is coupled to terminal 32 from supply potential V_D whenever transistors 24 and 26 are concurrently "on" or conducting. Transistor 26 has its gate connected to X input terminal 14 and conducts

when X is a zero value. Transistor 24 has its gate coupled to Y input terminal 12 through inverter 16 and conducts when Y is a one value. Thus, transistors 24 and 26 conduct concurrently only in response to the logical AND of $\bar{X}Y$. This occurs for the X and Y values in rows 3 and 7 of Table II. A one borrow out value is required for both of these rows. It is seen that the pass transistor 22 is turned off for the X, Y states of rows 3 and 7.

A zero is coupled to terminal 32 from ground potential whenever transistors 28 and 30 are both conducting. Transistor 28 has its gate electrode coupled to the X input terminal 14 and conducts when X is a one value. Transistor 30 has its gate electrode coupled to the Y input terminal 12 through inverter 16 and conducts when Y is a zero value. Thus, transistors 28 and 30 conduct concurrently only in response to the logical AND function $X\bar{Y}$. This occurs for the X, Y states of rows 2 and 6 of Table II. In both rows a zero borrow out value is required. Again it will be noted that when transistors 28 and 30 are conducting, pass transistor 22 is in the non-conducting state.

In brief, transistors 24-30 and inverter 16 form a three state logic circuit which outputs a logic one for $X=0$, $Y=1$, a logic zero for $X=1$, $Y=0$ and exhibits a high output impedance otherwise. When the three state circuit is in the high impedance state XOR gate 18 conditions pass transistor 22 to couple the borrow input signal at terminal 10 to the borrow output terminal 32.

FIGURE 2 shows the interconnection of a plurality of FIGURE 1 subtracter stages for subtracting one $K+1$ bit binary number Y from another $K+1$ bit binary number X. The least significant bits (LSB's) X_0 and Y_0 of the two binary numbers X and Y are applied to the rightmost subtracter stage 42 and the most significant bits X_k and Y_k are applied to the leftmost stage 40. The borrow input terminal 44 of stage 42 is coupled to a logic zero potential, and the borrow output terminal 46 produces an indication of polarity of the difference of X minus Y.

The borrow output terminal 45 of subtracter stage 42 is coupled to the borrow input terminal of subtracter stage 41, to which the next least significant bits X_1 and Y_1 of the binary numbers X and Y are coupled. $K+1$ stages are interconnected in this manner. The output terminals Z_k to Z_0 of stages 40-42 provide the binary output (x-y) with Z_k and Z_0 being the MSB and LSB of the difference respectively.

FIGURE 3 illustrates a subtractor stage with an alternate three state borrow generating logic circuit. In this embodiment, a p-type transistor 50 and an n-type transistor 51 are coupled between positive supply and the borrow out terminal 32. A p-type transistor 52 and an n-type transistor 53 are serially connected between the borrow out terminal 32 and ground potential. The gates of transistors 50 and 53 are connected to input terminal 14. Transistor 50 conducts when X is a zero value and transistor 53 conducts when X is a one value. The gates of transistors 51 and 52 are connected to input terminal 12. Transistor 51 conducts when Y is a one value and transistor 52 conducts when Y is a zero value. Transistors 50 and 51 conduct concurrently for X equal to zero and Y equal to one. Thus a logic one is applied to terminal 32 by transistors 50 and 51 for the combination of X, Y values defined logically by $\bar{X}Y$. Transistors 52 and 53 conduct concurrently and apply a logic zero to terminal 32 for the combination of logic values defined by $X\bar{Y}$.

The FIGURE 3 three state circuit performs the same logic function as the FIGURE 1 three state circuit. However, the FIGURE 3 circuit does not require an inverter circuit to control two of the serially connected transistors resulting in a subtracter stage with fewer devices.

Claims

1. A binary subtracter stage for subtracting a first single bit binary number Y from a second single bit binary number X comprising:

   first and second binary input terminals (14,12) for applying binary numbers X and Y respectively;

   a borrow output terminal;

   a borrow input terminal for applying a borrow input signal Bin;

   exclusive OR circuitry (18,20) having input terminals coupled to said first and second binary input terminals and said borrow input terminal for producing a signal corresponding to difference values X-Y at an output terminal thereof, according to the logic function $X \oplus Y \oplus Bin$; characterized by coupling means (22) coupled to said exclusive or circuitry for selectively coupling the borrow output terminal to the borrow input terminal exclusively when the numbers X and Y are equal; and

   a three state logic circuit (24-30) having first and second input terminals coupled to said first and second binary input terminals, and having an output terminal coupled to said borrow output terminal, said three state logic circuit generating a first logic output state for the value of Y greater than X, generating a second logic output state for the value of X greater than Y and generating a high impedance output state otherwise.

2. The subtracter stage set forth in claim 1 characterized in that the three state logic circuit comprises: first (26) and second (24) transistors of a first type having primary conduction paths serially coupled between said borrow output terminal and a point of potential corresponding to said first logic level, and having respective control electrodes;

third (30) and fourth (28) transistors of a second type complementary to said first type, having primary conduction paths serially coupled between said borrow output terminal and a point of potential corresponding to said second logic level, and having respective control electrodes;

the control electrodes of said first (26) and fourth (28) transistors being coupled to said first binary input terminal (14);

an inverter circuit (16) having an input terminal connected to said second binary input terminal (12) and an output terminal connected to the control electrodes of said second (24) and third (30) transistors.

3. The subtraction circuit set forth in claim 1 characterized in that the three state logic circuit comprises: first (50) and second (51) transistors of first and second complementary types respectively, having principal conduction paths serially coupled between said borrow output terminal and a point of potential corresponding to said first logic level, and having respective control electrodes connected to said first (14) and second (12) binary input terminals respectively;

third (52) and fourth (53) transistors of said first and second complementary types respectively, having principal conduction paths serially coupled between said borrow output terminal and a point of potential corresponding to said second logic level, and having respective control electrodes coupled to the second (12) and first (14) binary input terminals respectively.

4. The binary subtracter stage according to claim 1, 2 or 3, characterized in that:
said exclusive OR circuitry comprises

a first XOR gate (18) having first (14) and second (12) input terminals coupled to said first and second binary input terminals respectively, and having an output terminal, and

a second XOR gate (20) having first and second input terminals coupled respectively to said borrow input terminal and the output terminal of said first XOR gate, and having an output terminal (34) for producing an output signal corresponding to the difference X minus Y;
said coupling means comprises:

a pass transistor (22) having a primary conduction path coupled between said borrow input (10) and borrow output (32) terminals, and having a control electrode coupled to the output terminal of said first XOR gate (18); and the said three state logic circuit generates a logic one for said first logic output level according to the logic function $\overline{X}Y$, a logic zero for said second logic output level according to the logic function $X\overline{Y}$ and said high impedance output state otherwise, where the terms $\overline{X}$ and $\overline{Y}$ connote the logic complement of the binary values of X and Y respectively.

Revendications

1. Etage de soustraction binaire pour soustraire un premier nombre binaire à bit unique Y d'un second nombre binaire à bit unique X comprenant :

des premières et secondes bornes d'entrée binaires (14, 12) pour appliquer respectivement des nombres binaires X et Y ;

une borne de sortie de retenue ;

une borne d'entrée de retenue pour appliquer un signal d'entrée de retenue Bin ;

un circuit OU exclusif (18,20) ayant des bornes d'entrée couplées auxdites premières et secondes bornes d'entrée binaires et à ladite borne d'entrée de retenue afin de produire un signal correspondant aux valeurs de la différence X-Y à une borne de sortie du circuit, selon la fonction logique $X \oplus Y \oplus Bin$; caractérisé par

des moyens de couplage (22) couplés audit circuit OU exclusif pour coupler sélectivement la borne de sortie de retenue à la borne d'entrée de retenue exclusivement lorsque les nombres X et Y sont égaux et,

un circuit logique à trois états (24-30) ayant des premières et secondes bornes d'entrée couplées auxdites premières et secondes bornes d'entrée binaires et comportant une borne de sortie couplée à ladite borne de sortie de retenue, ledit circuit logique à trois états générant un premier état de sortie logique pour la valeur de Y plus grande que X, générant un second état de sortie logique pour la valeur de X supérieure à Y en générant autrement un état de sortie à impédance élevée.

2. Etage de soustraction selon la revendication 1 caractérisé en ce que le circuit logique à trois états comprend :

des premier (26) et second (24) transistors d'un premier type ayant des trajets de conduction primaire couplés en série entre ladite borne de sortie de retenue et un point de potentiel correspondant audit premier niveau logique et comportant des électrodes de commande respectives ;

des troisième (30) et quatrième (28) transistors d'un second type complémentaire dudit premier type, comportant des trajets de conduction primaire couplés en série entre ladite borne de sortie de retenue et un point de potentiel correspondant audit second niveau logique et comportant des électrodes de commande respectives ;

les électrodes de commande desdits premier (26) et quatrième (28) transistors étant couplés à ladite première borne d'entrée binaire (14)

un circuit inverseur (16) comprenant une borne d'entrée connectée à ladite seconde borne d'entrée binaire (12) et une borne de sortie connectée aux électrodes de commandes desdits second (24) et troisième (30) transistors.

3. Circuit de soustraction selon la revendication 1 caractérisé en ce que le circuit logique à trois états comprend :

des premier (50) et second (51) transistors respectivement d'un premier et d'un second type complémentaire, ayant des trajets de conduction principale couplés en série entre ladite borne de sortie de retenue et un point de potentiel correspondant audit premier niveau logique et ayant des électrodes de commandes respectives connectées respectivement auxdits première (14) et seconde (12) bornes d'entrée binaires ;

des troisième (52) et quatrième (53) transistors respectivement dudit premier et dudit second type complémentaire, ayant des trajets de conduction principale couplés en série entre ladite borne de sortie de retenue et un point de potentiel correspondant audit second niveau logique et comportant des électrodes de commande respectives couplées respectivement aux seconde (12) et première (14) bornes d'entrée binaires.

4. Circuit de soustraction binaire selon la revendication 1.2 ou 3 caractérisé en ce que ledit circuit OU exclusif comprend :

une première porte X OU (18) comportant des première (14) et seconde (12) bornes d'entrée couplées respectivement auxdites première et seconde bornes d'entrée binaires et présentant une borne de sortie et,

une seconde porte X OU (20) ayant des première et seconde bornes d'entrée couplées respectivement à ladite borne d'entrée de retenue et à la borne de sortie de ladite première porte X OU et ayant une borne de sortie (34) pour produire un signal de sortie correspondant à la différence X moins Y ; lesdits moyens de couplage comprennent un transistor de défilement (22) ayant un trajet de conduction primaire couplé entre lesdites bornes d'entrée de retenue (10) et de sortie de retenue (32) et ayant une électrode de commande couplée à la borne de sortie de la première porte X OU (18), et ledit circuit logique à trois états génère un un logique pour ledit premier niveau de sortie logique selon la fonction logique $\overline{X}Y$, un zéro logique pour ledit second niveau de sortie logique selon la fonction logique $X\overline{Y}$ et autrement ledit état de sortie à impédance élevée, $\overline{X}$ et $\overline{Y}$ désignant le complément logique respectivement des valeurs binaires de X et Y.

Patentansprüche

1. Binäre Subtrahierstufe zum Subtrahieren einer ersten einzel-Bit binären Zahl Y von einer zweiten einzel-Bit binären Zahl X mit:

ersten und zweiten binären Eingangsanschlüssen (14, 12) zum Zuführen binärer Zahlen X beziehungsweise Y;

einem Borgübertrags-Ausgangsanschluß;

einem Borgübertrags-Eingangsanschluß zum Zuführen eines Borgübertrags-Eingangssignals Bin;

einer Exklusiv-ODER-Schaltung (18, 20), deren Eingangsanschlüsse mit den ersten und zweiten binären Eingangsanschlüssen und dem Borgübertrags-Eingangsanschluß verbunden sind, die an einem ihrer Ausgänge ein den Differenzwerten X-Y entsprechendes Signal erzeugt, entsprechend der Logikfunktion XOYOBin; gekennzeichnet durch

mit der Exklusiv-ODER-Schaltung verbundene Verbindungsmittel (22) zum selektiven verbinden des Borgübertrags-Ausgangsanschlusses mit dem Borgübertrags-Eingangsanschluß, ausschließlich wenn die Zahlen X und Y gleich sind; und

einer Dreipunkt-(drei-Zustände-)Logikschaltung (24 bis 30), deren erste und zweite Eingangsanschlüssen mit den ersten und zweiten binären Eingangsanschlüssen verbunden sind und deren Ausgangsanschluß mit dem Borgübertrags-Ausgangsanschluß verbunden ist, wobei die Dreipunktlogikschaltung einen ersten logischen Ausgangszustand erzeugt, wenn der Wert von Y größer als X ist, einen zweiten logischen Ausgangszustand, wenn der Wert von X größer als Y ist, und anderenfalls einen Hochimpedanz-Ausgangszustand erzeugt.

2. Subtrahierstufe gemäß Anspruch 1, dadurch gekennzeichnet, daß die Dreipunkt-Logikschaltung das folgende umfaßt: erste (26) und zweite (24) Transistoren eines ersten Typs, deren Primärleitungsstrekken in Reihe zwischen den Borgübertrags-Ausgangsanschluß und einen dem ersten logischen Pegel entsprechenden Potentialpunkt geschaltet sind und die entsprechende Steuerelektroden aufweisen;

dritte (30) und vierte (28) Transistoren eines zweiten, dem ersten Typ gegenüber komplementären Typs, deren Primärleitungsstrecken in Reihe zwischen den Borgübertrags-Ausgangsanschluß und einen dem zweiten logischen Pegel entsprechenden Potentialpunkt geschaltet sind und die entsprechende Steuerelektroden aufweisen;

wobei die Steuerelektroden der ersten (26) und vierten (28) Transistoren mit dem ersten binären Eingangsanschluß (14) verbunden sind;

eine Inverterschaltung (16), deren Eingangsanschluß mit dem zweiten binären Eingangsanschluß (12) und deren Ausgangsanschluß mit den Steuerelektroden der zweiten (24) und dritten (30) Transistoren verbunden ist.

3. Subtrahierstufe gemäß Anspruch 1, dadurch gekennzeichnet, daß die Dreipunkt-Logikschaltung das folgende umfaßt: erste (50) und zweite (51) Transistoren eines ersten beziehungsweise zweiten, komplementären Typs, deren Primärleitungsstrecken in Reihe zwischen den Borgübertrags-Ausgangsanschluß und einen dem ersten logischen Pegel entsprechenden Potentialpunkt geschaltet sind und deren entsprechende Steuerelektroden mit den ersten (14) beziehungsweise zweiten (12) binären Eingangsanschlüssen verbunden sind;

dritte (52) und vierte (53) Transistoren des ersten beziehungsweise zweiten, komplementären Typs, deren Primärleitungsstrecken in Reihe zwischen den Borgübertrags-Ausgangsanschluß und einen dem zweiten logischen Pegel entsprechenden Potentialpunkt geschaltet sind und deren entsprechende Steuerelektroden mit den zweiten (12) beziehungsweise ersten (14) binären Eingangsanschlüssen verbunden sind.

4. Binäre Subtrahierstufe gemäß Anspruch 1, 2 oder 3, dadurch gekennzeichnet, daß die Exklusiv-ODER-Schaltung das folgende umfaßt:

ein erstes Exklusiv-ODER-Gatter (18), dessen erster (14) beziehungsweise zweiter (12) Eingangsanschluß mit dem ersten beziehungsweise zweiten binären Eingangsanschluß verbunden sind und welches einen Ausgangsanschluß aufweist, und

ein zweites Exklusiv-ODER-Gatter (20), dessen erster beziehungsweise zweiter Eingangsanschluß mit dem Borgübertrags-Eingangsanschluß beziehungsweise dem Ausgangsanschluß des ersten Exklusiv-ODER-Gatters verbunden ist und welches einen Ausgangsanschluß (34) aufweist, zum Erzeugen eines der Differenz X minus Y enstprechenden Ausgangssignals;

wobei die Verbindungsmittel das folgende umfassen:

einen Durchschalttransistor (22), dessen Primärleitungsstrecke zwischen den Borgübertrags-Eingangs- (10) und den Borgübertrags-Ausgangsanschluß (32) geschaltet ist und dessen Steuerelektrode mit dem Ausgangsanschluß des ersten Exklusiv-ODER-Gatters (18) geschaltet ist; und wobei die Dreipunkt-Logikschaltung eine logische Eins für den ersten logischen Ausgangspegel gemäß der Logikfunktion $\overline{X}Y$ erzeugt, eine logische Null für den zweiten logischen Ausgangspegel gemäß der Logikfunktion $X\overline{Y}$ und anderenfalls den Hochimpedanz-Ausgangszustand erzeugt, wobei die Terme $\overline{X}$ beziehungsweise $\overline{Y}$ für das logische Komplement der Binärwerte von X beziehungsweise Y stehen.

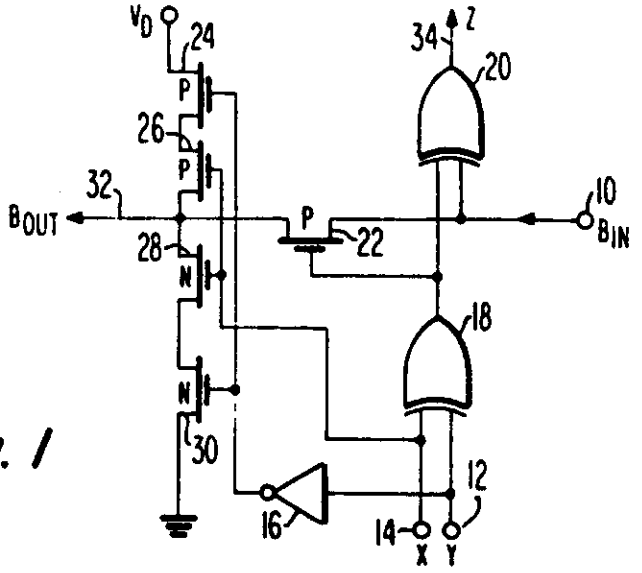

Fig. 1

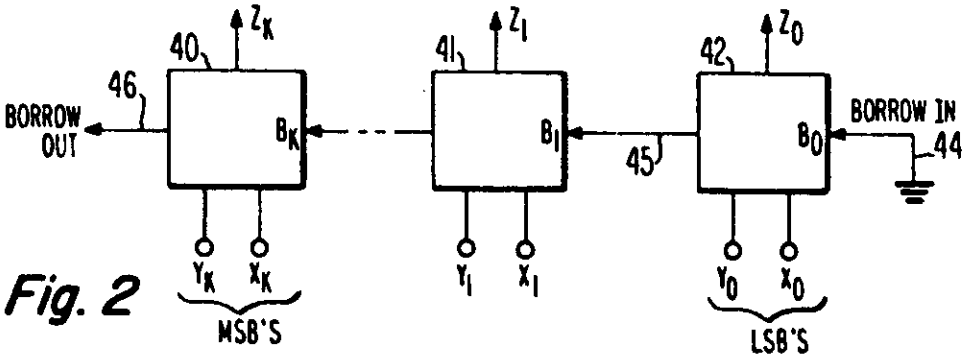

Fig. 2

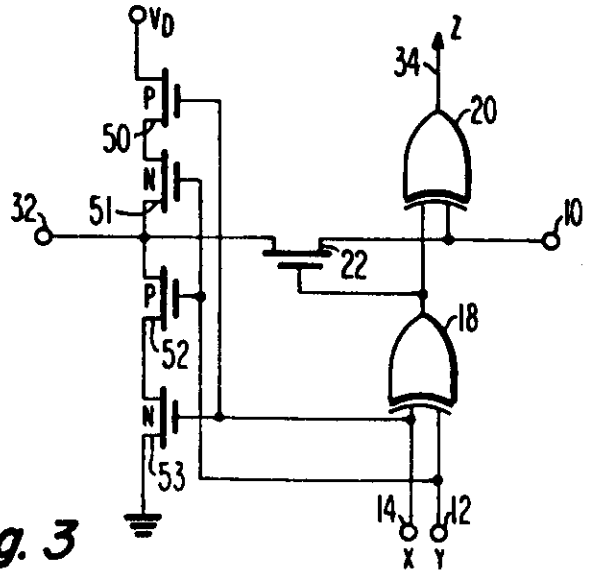

Fig. 3

REGISTER ENTRY FOR EP0185504

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Title A BINARY SUBTRACTION CIRCUIT

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G06F

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