

(51) International Patent Classification:
H03B 5/12 (2006.01)(21) International Application Number:
PCT/US20 12/052464(22) International Filing Date:
27 August 2012 (27.08.2012)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
13/3 14,825 8 December 2011 (08.12.2011) US(71) Applicant (for all designated States except US): **APPLE INC.** [US/US]; 1 Infinite Loop, Cupertino, CA 95014 (US).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **CHOU, Catherine S.** [US/US]; 11701 Southshore Court, Cupertino, California 95014 (US). **ATHAS, William C.** [US/US]; 801 Clintonia Avenue, San Jose, CA 95125 (US). **SULLENS, Heather R.** [US/US]; 33 Haight Street, Apt. 1, San Francisco, California 94102 (US).(74) Agent: **SAHASRABUDDHE, Laxman;** Park, Vaughan, Fleming & Dowler LLP 2820 Fifth Street, Davis, California 95618 (US).

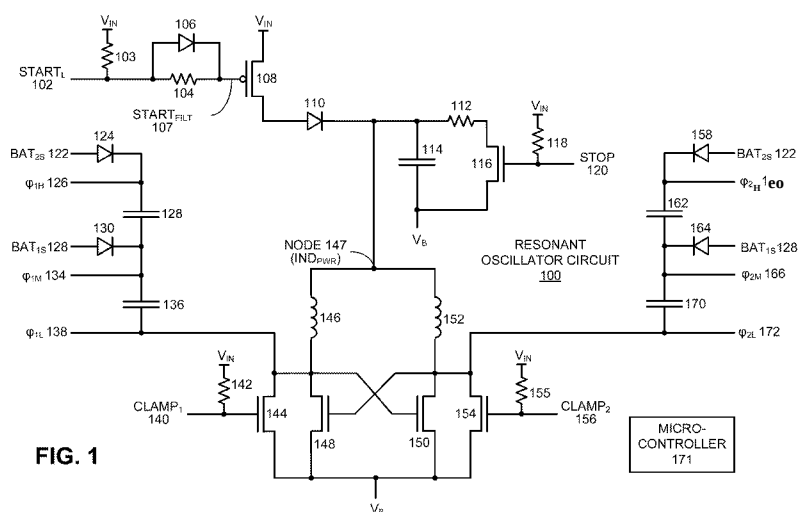
(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— without international search report and to be republished upon receipt of that report (Rule 48.2(g))

(54) Title: RESONANT OSCILLATOR WITH START UP AND SHUT DOWN CIRCUITRY

**FIG. 1**

(57) Abstract: The disclosed embodiments provide a system which starts up and shuts down a resonant oscillator circuit. During the start up process, a driving circuit uses a first clock signal to control a first phase output of the resonant oscillator circuit. At the same time, the driving circuit uses a second clock signal to control a second phase output of the resonant oscillator circuit, wherein the first and second clock signals have opposite phases. While the first and second phase outputs are being controlled, the system ramps up an input voltage, which is used to power the resonant oscillator circuit, wherein the ramping takes place across multiple initial oscillation periods. During the shut down process, the system shuts down the resonant oscillator circuit by ramping down the input voltage. After the input voltage has been ramped down, the system clamps the first and second phase outputs to a fixed voltage.

RESONANT OSCILLATOR WITH START UP AND SHUT DOWN CIRCUITRY

Inventors: Catherine S. Chou, William C. Athas and Heather R. Sullens

BACKGROUND

Field

[0001] The disclosed embodiments generally relate to oscillator circuits. More specifically, the disclosed embodiments relate to a method and an apparatus for starting up a resonant oscillator circuit in a manner which mitigates overshooting problems and protects associated circuitry.

Related Art

[0002] Oscillator circuits are commonly used to generate clock signals in electrical systems. However, commonly used oscillator circuits can consume a significant amount of power, which is a disadvantage for systems that need to conserve power, such as portable computing devices. To solve this problem, "resonant oscillator circuits," which transfer energy back and forth between inductive and capacitive circuit elements, can be used to generate clock pulses without dissipating a significant amount of power. (For example, see U.S. Patent No. 5,559,478, entitled "Highly Efficient, Complementary, Resonant Pulse Generation," by inventor William C. Athas, filed 17 July 1995.)

[0003] Unfortunately, existing designs for resonant oscillator circuits are not well suited for certain applications. For example, in one application a resonant oscillator circuit is used to clock the two phases of a switched capacitor block (SCB) in a voltage conversion system. (See Patent Application No. 12/535,974, entitled "High-Efficiency Switched-Capacitor Power Conversion," filed on 05 July 2009 by inventors William C. Athas and P. Jeffrey Ungar (Attorney Docket No. APL-P7723US1) which is hereby incorporated herein by reference. In this application, if the clock signals are first turned on, so that power field-effect transistors (FETs) in the SCBs are at or near their minimum on-resistance and the capacitors of the SCBs are well below their normal operating voltage levels, the resulting inrush current can damage the FETs. Hence, it is desirable to first clock the SCBs with a low voltage swing, so that the power FETs in

the SCBs have a high on-resistance, and then gradually decrease the on-resistance by increasing the amplitude of the clock signals.

[0004] Another problem is the uncontrolled and unpredictable way in which oscillations commence in a resonant oscillator during power up. As power is applied to the basic two-FET and two-inductor implementation disclosed in U.S. Patent Application No. 12/535,974 (cited above), current more or less equally divides between the two inductor branches. Asymmetries in the component values and the layout will eventually cause the two branch currents to become unequal which allows the oscillations to commence. However, the circuit may exist in a balanced, metastable state for an indeterminate period of time. Meanwhile, current builds up in each inductor in proportion to the duration of the metastable state. Consequently, when the circuit eventually exits the metastable state, the initial output pulses can be almost unbounded in magnitude, and may damage downstream components, such as the SCBs, or even the components of the resonant oscillator circuit itself.

[0005] Hence, what is needed is a resonant oscillator circuit, which does not suffer from the above-described problems.

SUMMARY

[0006] The disclosed embodiments provide a system which starts up a resonant oscillator circuit. During operation, this system operates a driving circuit, which is external to the resonant oscillator circuit, wherein the driving circuit uses a first clock signal to control a first phase output of the resonant oscillator circuit. At the same time, the driving circuit uses a second clock signal to control a second phase output of the resonant oscillator circuit, wherein the first and second clock signals have opposite phases. While the first and second phase outputs are being controlled, the system ramps up an input voltage, which is used to power the resonant oscillator circuit, wherein the ramping takes place across multiple initial oscillation periods.

[0007] In some embodiments, using the first and second clock signals to control the first and second phase outputs involves driving the first clock signal onto a first N-FET gate which clamps the output of the resonant oscillator circuit to a desired frequency, and driving the second clock signal onto a second N-FET gate which clamps the output of the resonant oscillator circuit to the desired frequency.

[0008] In some embodiments, the system discontinues the controlling of the first and second phase outputs after the multiple initial oscillation periods complete.

[0009] In some embodiments, the driving circuit includes a programmable microcontroller.

[0010] In some embodiments, ramping up the input voltage involves using an RC filter to ramp up the input voltage at a controlled rate.

[0011] In some embodiments, the system shuts down the resonant oscillator circuit by ramping down the input voltage. After the input voltage has been ramped down, the system
5 clamps the first and second phase outputs to a fixed voltage.

[0012] In some embodiments, ramping down the input voltage involves disconnecting a power source from the input voltage, and draining charge from a capacitor having a first terminal coupled to the input voltage and a second terminal coupled to a base voltage, wherein draining the charge involves coupling the first terminal of the capacitor to the base voltage through a
10 resistor.

[0013] In some embodiments, the resonant oscillator circuit is an LC oscillator circuit which includes at least two inductors and at least two capacitances.

[0014] In some embodiments, in addition to the first phase and second phase outputs, the resonant oscillator circuit includes a first inductor with a first terminal coupled to an input
15 voltage and a second terminal coupled to the first phase output, and a second inductor with a first terminal coupled to the input voltage and a second terminal coupled to the second phase output. It also includes a first N-type transistor with a source terminal coupled to a base voltage, a drain terminal coupled to the first phase output, and a gate terminal coupled to the second phase output. It also includes a second N-type transistor with a source terminal coupled to the base voltage, a
20 drain terminal coupled to the second phase output, and a gate terminal coupled to the first phase output.

In some embodiments, the resonant oscillator circuit additionally comprises a first capacitance and a second capacitance, which operate in concert with the first inductor and the second inductor to produce resonant oscillations, wherein the first capacitance includes
25 capacitive components from a load on the first phase output and the gate terminal of the second N-type transistor, and the second capacitance includes capacitive components from a load on the second phase output and the gate terminal of the first N-type transistor.

BRIEF DESCRIPTION OF THE FIGURES

[0015] FIG. 1 illustrates a resonant oscillator circuit in accordance with the disclosed
30 embodiments.

[0016] FIG. 2 presents a timing diagram illustrating signal levels during start up and shut down processes for the resonant oscillator circuit in accordance with the disclosed embodiments.

[0017] FIG. 3 presents a flow chart illustrating the start up process in accordance with the

[0018] FIG. 4 presents a flow chart illustrating the shut down process in accordance with the disclosed embodiments.

DETAILED DESCRIPTION

[0019] The following description is presented to enable any person skilled in the art to make and use the disclosed embodiments, and is provided in the context of a particular application and its requirements. Various modifications to the disclosed embodiments will be readily apparent to those skilled in the art, and the general principles defined herein may be applied to other embodiments and applications without departing from the spirit and scope of the disclosed embodiments. Thus, the disclosed embodiments are not limited to the embodiments shown, but are to be accorded the widest scope consistent with the principles and features disclosed herein.

[0020] The data structures and code described in this detailed description are typically stored on a non-transitory computer-readable storage medium, which may be any device or medium that can store code and/or data for use by a computer system. The non-transitory computer-readable storage medium includes, but is not limited to, volatile memory, non-volatile memory, magnetic and optical storage devices such as disk drives, magnetic tape, CDs (compact discs), DVDs (digital versatile discs or digital video discs), or other media capable of storing code and/or data now known or later developed.

[0021] The methods and processes described in the detailed description section can be embodied as code and/or data, which can be stored in a non-transitory computer-readable storage medium as described above. When a computer system reads and executes the code and/or data stored on the non-transitory computer-readable storage medium, the computer system performs the methods and processes embodied as data structures and code and stored within the non-transitory computer-readable storage medium. Furthermore, the methods and processes described below can be included in hardware modules. For example, the hardware modules can include, but are not limited to, application-specific integrated circuit (ASIC) chips, field-programmable gate arrays (FPGAs), and other programmable-logic devices now known or later developed. When the hardware modules are activated, the hardware modules perform the methods and processes included within the hardware modules.

Resonant Oscillator Circuit

[0022] FIG. 1 illustrates a resonant oscillator circuit 100 in accordance with the disclosed embodiments. Referring to the bottom portion of FIG. 1, the core of the resonant oscillator circuit includes two complementary circuit sections that produce opposing clock phases. The

phase output ϕ_{iL} 138. The second complementary circuit section includes inductor 152 and FET 150 and produces phase output ϕ_{2L} 172, wherein phase outputs ϕ_{iL} 138 and ϕ_{2L} 172 provide opposite clock phases. Note that FETs 148 and 150 are cross-coupled so that the control input for each of FETs 148 and 150 is taken from the output from the complementary circuit section.

Also note that the gate capacitance for each FET 148 and 150 is lumped in with the output-load capacitance for the opposing clock phase.

[0023] During operation of resonant oscillator circuit 100, energy oscillates back and forth between inductive and capacitive circuit elements without a significant conductive or switching loss. More specifically, in the first circuit section, energy oscillates between inductor 146 and the load capacitance for phase output ϕ_{iL} 138, which is lumped in with the gate capacitance for the opposing FET 150. Similarly, in the second circuit section, energy oscillates between inductor 152 and the load capacitance for phase output ϕ_{2L} 172, which is lumped in with the gate capacitance for the opposing FET 148.

[0024] The right-hand side of FIG. 1 illustrates circuitry that uses phase output ϕ_{2L} 172 to generate boosted phase outputs ϕ_{2M} 166 and ϕ_{2H} 160. These boosted phase outputs are useful for driving FETs which are sourced at higher voltages. The voltages on boosted phase outputs ϕ_{2M} 166 and ϕ_{2H} 160 track the voltage on phase output ϕ_{2L} 172, but are biased to be at higher voltage levels. This is accomplished by using two bootstrap capacitors 170 and 162, and two diodes 158 and 164. More specifically, diode 164 clamps phase output ϕ_{2M} 166 to BAT_{1S} 128 during one phase and then follows phase output ϕ_{2L} 172 with a positive offset from BAT_{1S} 128 during the other phase. Similarly, diode 158 clamps phase output ϕ_{2H} 160 to BAT_{2S} 122 during one phase and then follows phase output ϕ_{2L} 172 with a positive offset from BAT_{2S} 122 during the other phase. (BAT_{1S} 128 and BAT_{2S} 122 are voltages taken from a battery pack comprised of multiple battery cells coupled together in series. In particular, BAT_{1S} 128 is a voltage across one bank of battery cells, whereas BAT_{2S} 122 is a voltage across two banks of battery cells which are coupled together in series.) Similar circuitry on the left-hand side of FIG. 1 generates boosted phase outputs ϕ_{iM} 134 and ϕ_{iH} 126 from output ϕ_{iL} 138 by using bootstrap capacitors 136 and 128, and diodes 130 and 124.

[0025] The resonant oscillator illustrated in FIG. 1 also includes circuitry to clamp phase output signals ϕ_{iL} 138 and ϕ_{2L} 172. More specifically, the drain of FET 144 is coupled to phase output signal ϕ_{iL} 138 and the source of FET 144 is coupled to V_B . Moreover, CLAMP_i signal 140 is coupled to the gate of FET 144 and is also coupled to V_N through resistor 142. When CLAMP_i signal 140 is asserted, FET 144 causes phase output signal ϕ_{iL} 138 to be clamped to V_B . Similarly, the drain of FET 154 is coupled to phase output signal ϕ_{2L} 172 and the source of

also coupled to V_{IN} through resistor 155. When $CLAMP_2$ signal 156 is asserted, FET 154 causes phase output signal ϕ_{2L} 172 to be clamped to V_B . This clamping circuitry is also activated to initiate oscillations as is described in more detail below with reference to FIG. 2.

[0026] The resonant oscillator illustrated in FIG. 1 also includes circuitry to "ramp up" and "ramp down" a voltage IND_{PWR} on node 147, which is applied to inductors 146 and 152. This circuitry includes P-type field-effect transistor (PFET) 108, which couples V_{IN} to node 147 through diode 110. The gate of PFET 108 is coupled to $START_L$ signal 102 through resistor 104 and diode 106, and is also coupled to V_{IN} through resistors 103 and 104, and diode 106. The circuitry also includes a capacitor 114 with a first terminal and a second terminal. The first terminal is coupled to node 147 and is also coupled through resistor 112 and FET 116 to V_B . The second terminal of capacitor 114 is coupled to V_B . The gate of FET 116 is coupled to STOP signal 120, and is also coupled to V_{IN} through resistor 118.

[0027] The sequences of operations which take place during the start up and shut down processes are described in more detail below with reference to the timing diagrams which appear in FIG. 2. In one embodiment, control signals $START_L$ 102, STOP 120, $CLAMP_i$ 140 and $CLAMP_2$ 156 are all supplied by a programmable controller 171, which sequences the operations involved in the start up and shut down processes. Controller 171 can generally be any type of programmable computational engine, such as a device controller, a microcontroller, a service processor or any microprocessor-based controller.

Timing Diagram

[0028] FIG. 2 presents a timing diagram illustrating signal levels during start up and shut down processes for resonant oscillator circuit 100 illustrated in FIG. 1 in accordance with the disclosed embodiments.

[0029] During the start up process, the system starts clocking the oscillator's clamp FETs 144 and 154 and then applies power to inductors 146 and 152 slowly by ramping up IND_{PWR} on node 147. The inductors with their capacitive loads produce the oscillating phase outputs ϕ_{iL} 138 and ϕ_{2L} 172. Once the amplitude of phase outputs ϕ_{iL} 138 and ϕ_{2L} 172 becomes large enough, the clocking can stop.

[0030] Referring FIG. 2, during the start up process, controller 171 lowers STOP signal 120 which turns off FET 116 and releases node 147. (Otherwise, when STOP signal 120 is asserted, FET 116 ties node 147 to V_B .) At the same time, controller 171 applies clock signals to $CLAMP_i$ 140 and $CLAMP_2$ 156, wherein the clock signals are square waves having opposite phases and having a clock frequency that approximates the resonant frequency of the oscillator

comprised of resistor 104 and the gate capacitance of PFET 108 to produce $START_{FILT}$ signal 107 which turns on PFET 108 and charges up capacitor 114. Note that this RC filter provides a slowly rising edge for voltage IND_{PWR} on node 147, which slowly energizes inductors 146 and 152.

5 **[0031]** Once the amplitude of phase outputs ϕ_{iL} 138 and ϕ_{2L} 172 becomes large enough, the clock signals stop.

10 **[0032]** To shut down resonant oscillator circuit 100, controller 171 drives $START_L$ signal 102 high, which drives the gate of PFET 108 high through diode 106. This bypasses the RC time constant and immediately turns off PFET 108, which shuts off power to node 147. Controller 171 then sets STOP signal 120 high, which causes FET 116 to drain charge from capacitor 114 through resistor 112 to V_B . After a period of time, controller 171 raises CLAMP_i signal 140 and CLAMP₂ signal 154 to V_{iN} .

Start Up Process

15 **[0033]** FIG. 3 presents a flow chart illustrating the start up process in accordance with the disclosed embodiments. During the start up process, the system uses a first clock signal to control a first phase output of the resonant oscillator circuit (step 302). At the same time, the system uses a second clock signal to control a second phase output of the resonant oscillator circuit, wherein the first and second clock signals have opposite phases (step 304). Note that
20 using the first and second clock signals to control the first and second phase outputs can involve driving the first clock signal onto a first N-FET gate which clamps the output of the resonant oscillator circuit to a desired frequency, and driving the second clock signal onto a second N-FET gate which clamps the output of the resonant oscillator circuit to the desired frequency

25 **[0034]** While the first and second phase outputs are being controlled, the system ramps up an input voltage, which is used to power the resonant oscillator circuit. This ramping process takes place across multiple initial oscillation periods (step 306). Finally, after the multiple oscillation periods complete, the system discontinues the controlling of the first and second phase outputs (step 308).

30 **Shut Down Process**

[0035] FIG. 4 presents a flow chart illustrating the shut down process in accordance with the disclosed embodiments. During the shut down process, the system shuts down the resonant oscillator circuit by ramping down the input voltage (step 402). After the input voltage has been ramped down, the system clamps the first and second phase outputs to a fixed voltage (step 404).

[0036] The foregoing descriptions of embodiments have been presented for purposes of illustration and description only. They are not intended to be exhaustive or to limit the present description to the forms disclosed. Accordingly, many modifications and variations will be apparent to practitioners skilled in the art. Additionally, the above disclosure is not intended to
5 limit the present description. The scope of the present description is defined by the appended claims.

What Is Claimed Is:

1. A method for starting up a resonant oscillator circuit, the method comprising:
operating a driving circuit, which is external to the resonant oscillator circuit, wherein the
5 driving circuit uses a first clock signal to control a first phase output of the resonant oscillator
circuit, and uses a second clock signal to control a second phase output of the resonant oscillator
circuit, wherein the first and second clock signals have opposite phases; and
while the first and second phase outputs are being controlled, ramping up an input
voltage, which is used to power the resonant oscillator circuit, wherein the ramping takes place
10 across multiple initial oscillation periods.
2. The method of claim 1, wherein using the first and second clock signals to control
the first and second phase outputs involves driving the first clock signal onto a first N-FET gate
which clamps the output of the resonant oscillator circuit to a desired frequency, and driving the
second clock signal onto a second N-FET gate which clamps the output of the resonant oscillator
15 circuit to the desired frequency.
3. The method of claim 1, further comprising discontinuing the controlling of the
first and second phase outputs after the multiple initial oscillation periods complete.
4. The method of claim 1, wherein the driving circuit includes a programmable
microcontroller.
- 20 5. The method of claim 1, wherein ramping up the input voltage involves using an
RC filter to ramp up the input voltage at a controlled rate.
6. The method of claim 1, further comprising shutting down the resonant oscillator
circuit by:
ramping down the input voltage; and
25 after the input voltage has been ramped down, clamping the first and second phase
outputs to a fixed voltage.
7. The method of claim 6, wherein ramping down the input voltage involves:
disconnecting a power source from the input voltage; and

draining charge from a capacitor having a first terminal coupled to the input voltage and a second terminal coupled to a base voltage, wherein draining the charge involves coupling the first terminal of the capacitor to the base voltage through a resistor.

8. The system of claim 1, wherein the resonant oscillator circuit is an LC oscillator
5 circuit which includes at least two inductors and at least two capacitances.

9. The method of claim 8, wherein the resonant oscillator circuit comprises:
the first phase output;
the second phase output;
a first inductor with a first terminal coupled to an input voltage and a second terminal
10 coupled to the first phase output;
a second inductor with a first terminal coupled to the input voltage and a second terminal
coupled to the second phase output;
a first N-type transistor with a source terminal coupled to a base voltage, a drain terminal
coupled to the first phase output, and a gate terminal coupled to the second phase output; and
15 a second N-type transistor with a source terminal coupled to the base voltage, a drain
terminal coupled to the second phase output, and a gate terminal coupled to the first phase output.

10. The method of claim 9,
wherein the resonant oscillator circuit additionally comprises a first capacitance and a
second capacitance, which operate in concert with the first inductor and the second inductor to
20 produce resonant oscillations;
wherein the first capacitance includes capacitive components from a load on the first
phase output and the gate terminal of the second N-type transistor; and
wherein the second capacitance includes capacitive components from a load on the
second phase output and the gate terminal of the first N-type transistor.

25 11. A resonant oscillator circuit, comprising:
a first phase output;
a second phase output;
a first inductor;
a second inductor;
30 a first capacitance;

wherein the first and second inductors are configured to operate with the first and second capacitances to produce resonant oscillations which appear at the first phase output and the second phase output;

5 a driving circuit configured to use a first clock signal to control the first phase output, and to use a second clock signal to control the second phase output, wherein the first and second clock signals have opposite phases; and

a ramping circuit configured to ramp up an input voltage, which is used to power the resonant oscillator circuit, wherein the ramping takes place across multiple initial oscillation periods.

10 12. The resonant oscillator circuit of claim 11, wherein while using the first and second clock signals to control the first and second phase outputs, the driving circuit is configured to drive the first clock signal onto a first N-FET gate which clamps the output of the resonant oscillator circuit to a desired frequency, and to drive the second clock signal onto a second N-FET gate which clamps the output of the resonant oscillator circuit to the desired
15 frequency.

13. The resonant oscillator circuit of claim 11, wherein the driving circuit is configured to discontinue the controlling of the first and second phase outputs after the multiple initial oscillation periods complete.

20 14. The resonant oscillator circuit of claim 11, wherein the driving circuit includes a programmable microcontroller.

15. The resonant oscillator circuit of claim 11, wherein the ramping circuit includes an RC filter to facilitate ramping up the input voltage at a controlled rate.

25 16. The resonant oscillator circuit of claim 11, wherein during an oscillator-shut-down operation, the ramping circuit is configured to ramp down the input voltage; and

wherein after the input voltage has been ramped down for a period of time, the driving circuit is configured to clamp the first and second phase outputs to a fixed voltage.

17. The resonant oscillator circuit of claim 16, wherein while ramping down the input

disconnect a power source from the input voltage; and

drain charge from a capacitor having a first terminal coupled to the input voltage and a second terminal coupled to a base voltage, wherein draining the charge involves coupling the first terminal of the capacitor to the base voltage through a resistor.

5 18. The resonant oscillator circuit of claim 11,

wherein the first inductor includes a first terminal coupled to the input voltage and a second terminal coupled to the first phase output;

wherein the second inductor includes a first terminal coupled to the input voltage and a second terminal coupled to the second phase output;

10 wherein the resonant oscillator circuit also includes a first N-type transistor with a source terminal coupled to a base voltage, a drain terminal coupled to the first phase output, and a gate terminal coupled to the second phase output;

wherein the resonant oscillator circuit additionally includes a second N-type transistor with a source terminal coupled to the base voltage, a drain terminal coupled to the second phase output, and a gate terminal coupled to the first phase output;

15 wherein the first capacitance includes capacitive components from a load on the first phase output and the gate terminal of the second N-type transistor; and

wherein the second capacitance includes capacitive components from a load on the second phase output and the gate terminal of the first N-type transistor.

20 19. The resonant oscillator circuit of claim 11,

wherein the first phase output is coupled to a first bootstrapping circuit which adds one or more voltage offsets to the first phase output to produce one or more boosted first phase outputs; and

25 wherein the second phase output is coupled to a second bootstrapping circuit which adds one or more voltage offsets to the second phase output to produce one or more boosted second phase outputs.

20. A resonant oscillator circuit, comprising:

a resonant oscillator with a first phase output and a second phase output, which produce clock signals with substantially opposite clock phases; and

30 a start up circuit for the resonant oscillator which includes,

a ramping circuit configured to ramp up an input voltage, which is used to power the resonant oscillator circuit, wherein the ramping takes place across multiple initial oscillation periods; and

a driving circuit, wherein during the multiple initial oscillation periods, the driving circuit is configured to use a first clock signal to control the first phase output, and a second clock signal to control the second phase output, wherein the first and second clock signals have opposite phases.

21. The resonant oscillator circuit of claim 20, wherein while using the first and second clock signals to control the first and second phase outputs, the driving circuit is configured to drive the first clock signal onto a first N-FET gate which clamps the output of the resonant oscillator circuit to a desired frequency, and to drive the second clock signal onto a second N-FET gate which clamps the output of the resonant oscillator circuit to the desired frequency.

22. The resonant oscillator circuit of claim 20, wherein the driving circuit is configured to discontinue the controlling of the first and second phase outputs after the multiple initial oscillation periods complete.

23. The resonant oscillator circuit of claim 20, wherein during an oscillator-shut-down operation, the ramping circuit is configured to ramp down the input voltage; and wherein after the input voltage has been ramped down, the driving circuit is configured to clamp the first and second phase outputs to a fixed voltage.

24. The resonant oscillator circuit of claim 23, wherein while ramping down the input voltage, the ramping circuit is configured to:

disconnect a power source from the input voltage; and drain charge from a capacitor having a first terminal coupled to the input voltage and a second terminal coupled to a base voltage, wherein draining the charge involves coupling the first terminal of the capacitor to the base voltage through a resistor.

25. The resonant oscillator circuit of claim 20, wherein the resonant oscillator circuit further comprises:

a second inductor;

a first capacitance; and

a second capacitance;

5 wherein the first and second inductors are configured to operate with the first and second capacitances to produce resonant oscillations which appear at the first phase output and the second phase output.

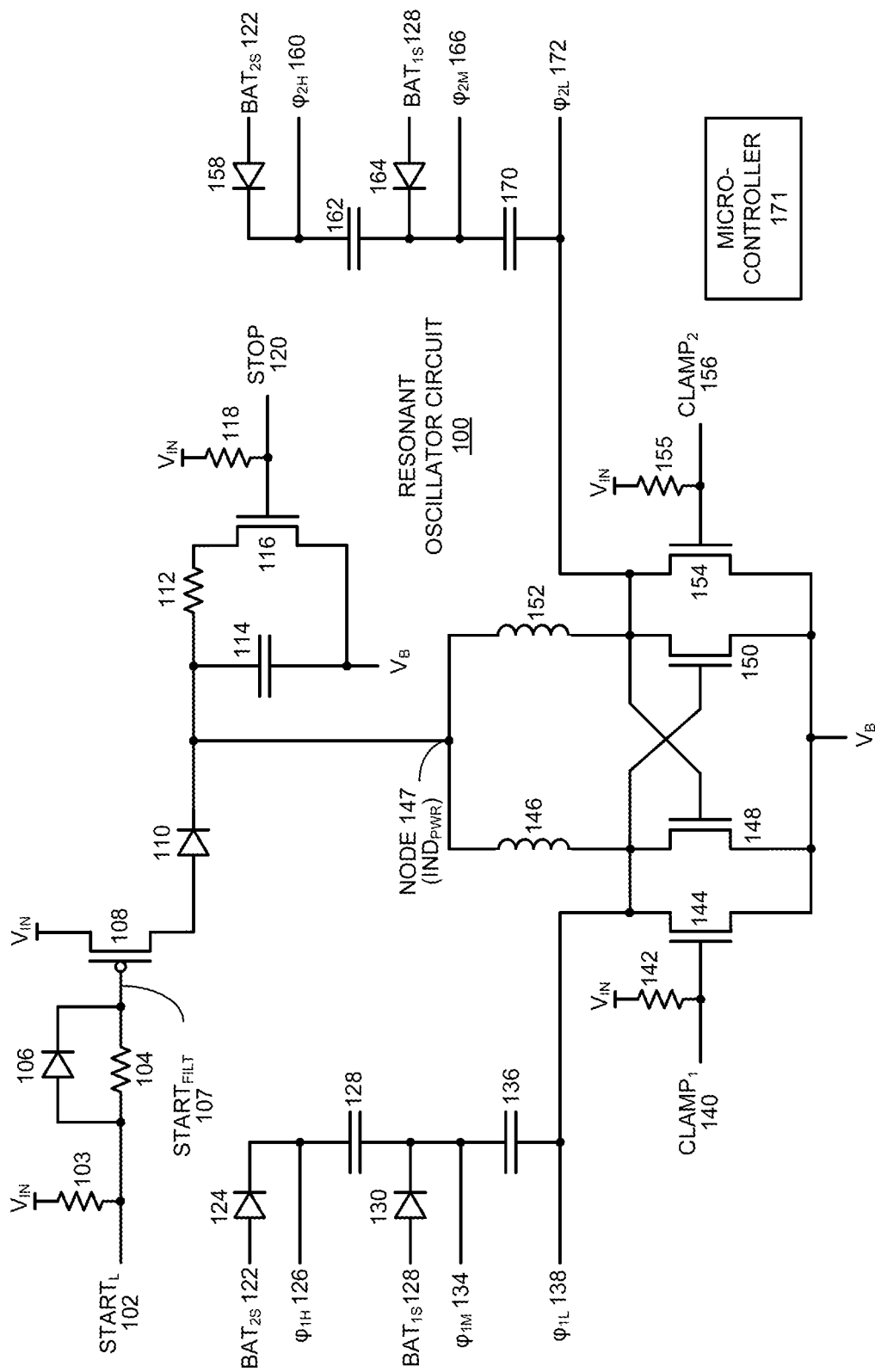


FIG. 1

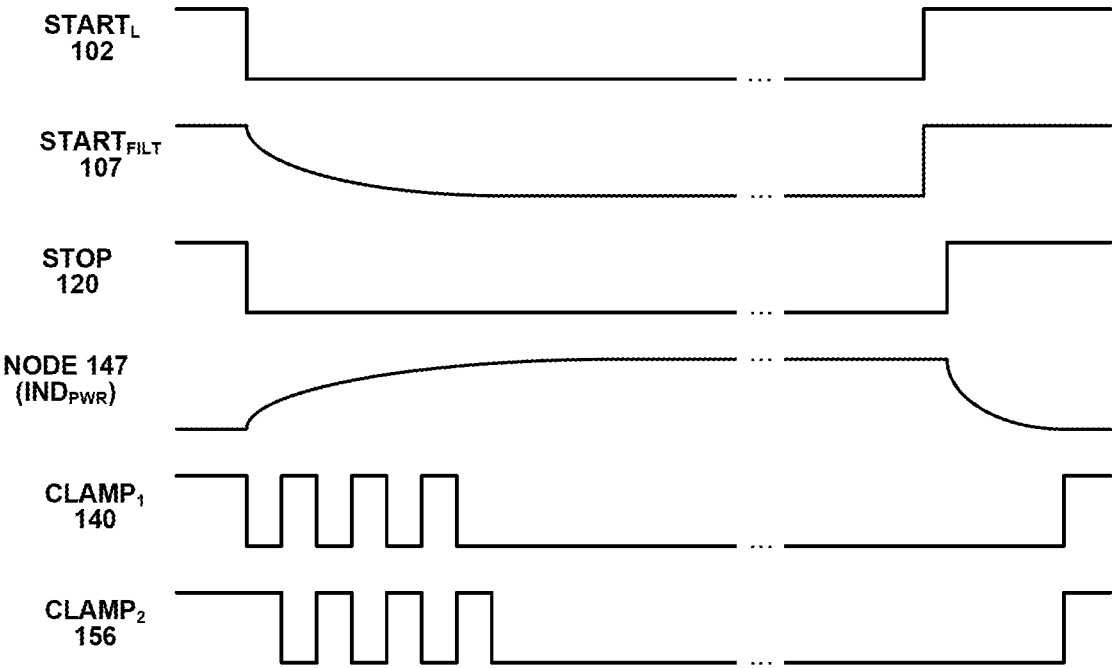
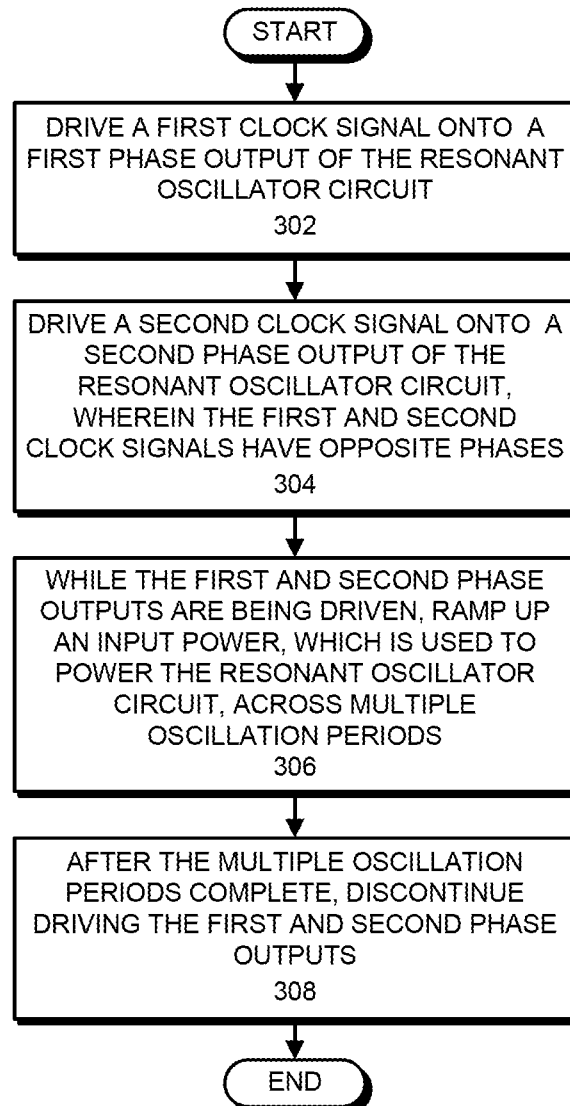
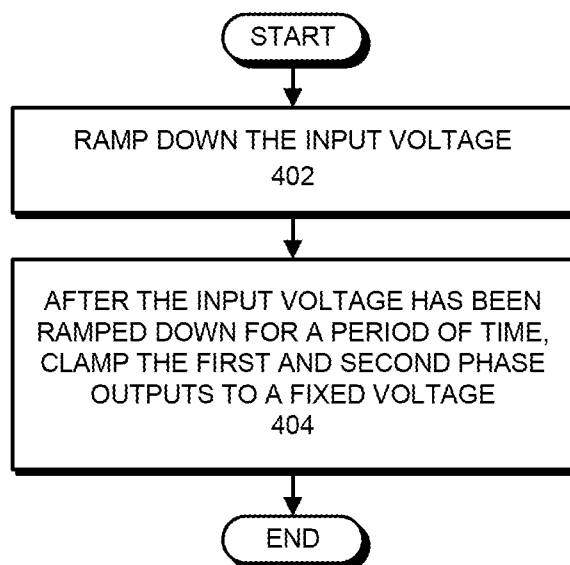


FIG. 2

**FIG. 3**

**FIG. 4**