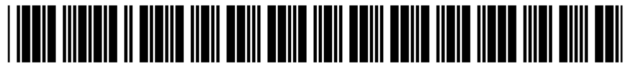

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(54) **SEMICONDUCTOR DEVICE AND FABRICATING METHOD THEREOF**

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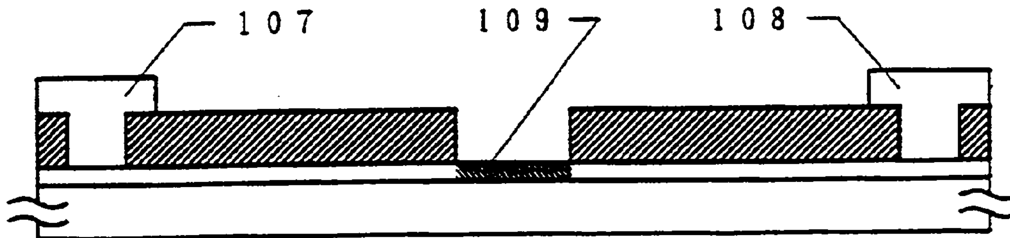
(57) **ABSTRACT**

To effectively crystallize an amorphous semiconductor film comprising silicon by utilizing nickel element and remove nickel element contributed to the crystallization, a mask **103** is provided on an amorphous silicon film **102**, oxide film patterns **107** and **108** including nickel are formed, phosphorus is doped in a region **109**, thereafter, heating is performed, nickel element is diffused via paths **110** and **111** and nickel element diffuses in the amorphous silicon film and gettered by phosphorus at the region **109** by which crystallization of diffusion of nickel and gettering of nickel can be carried out simultaneously.



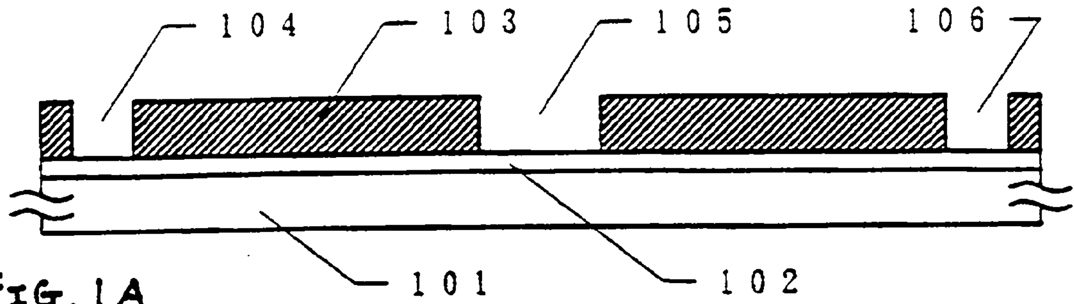


FIG. 1A

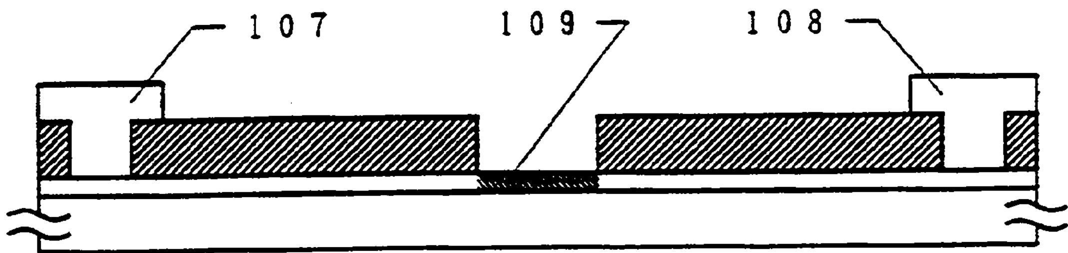


FIG. 1B

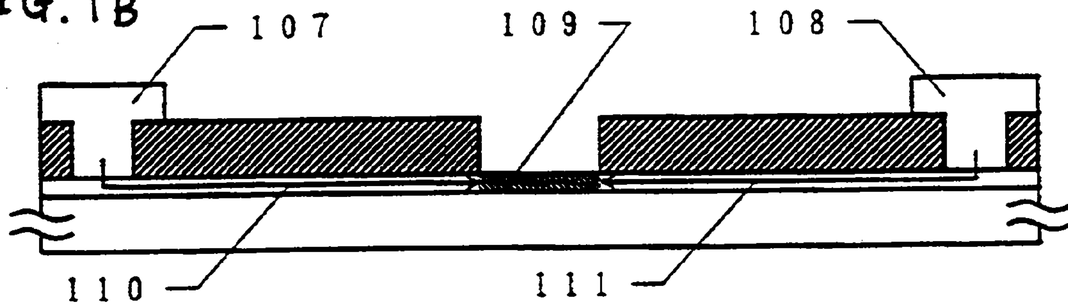


FIG. 1C

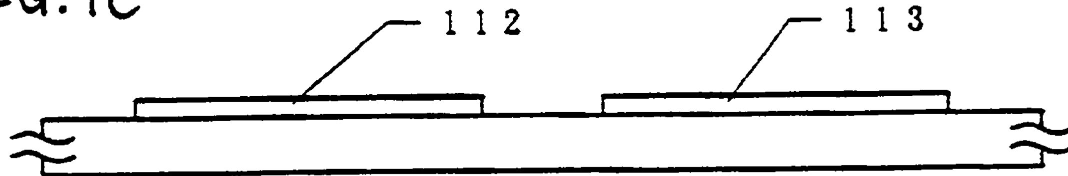


FIG. 1D

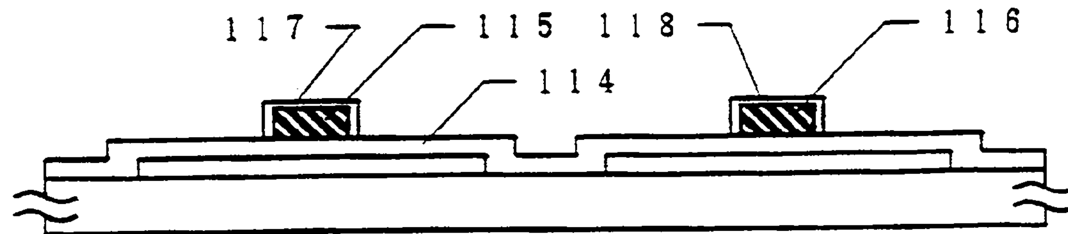


FIG. 1E

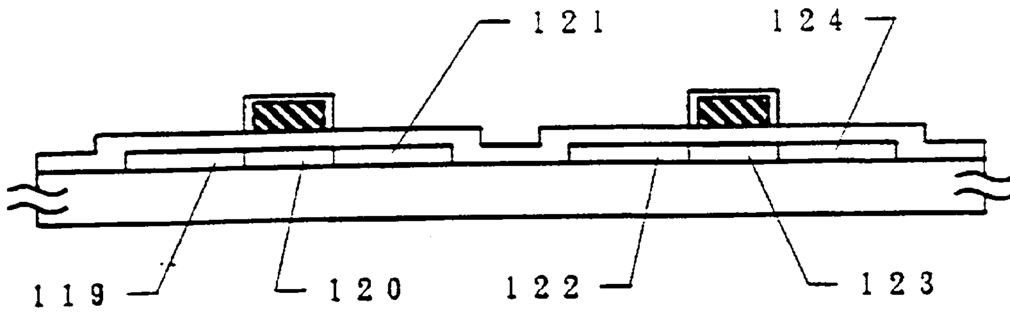


FIG. 2A

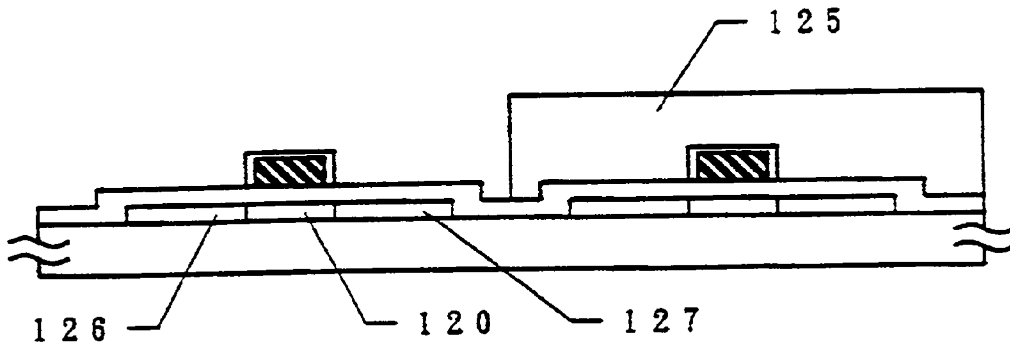


FIG. 2B

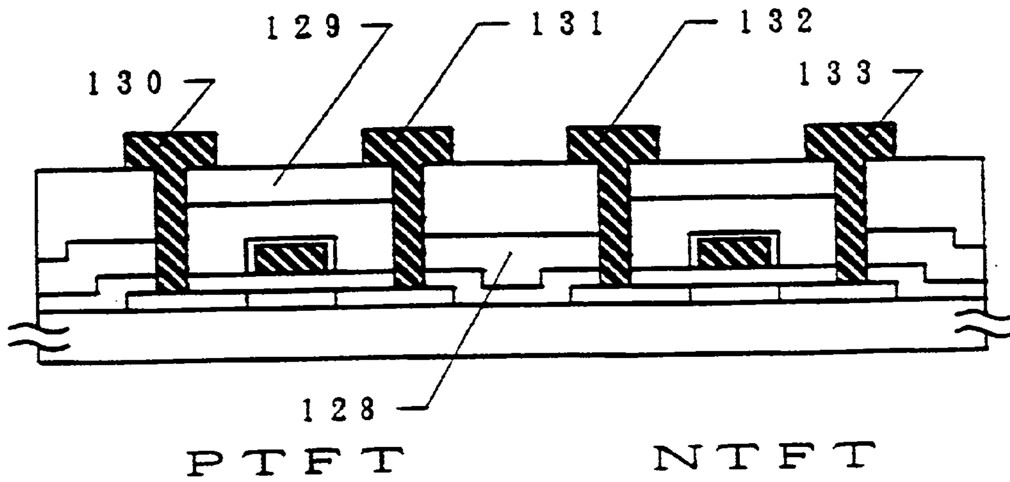


FIG. 2C

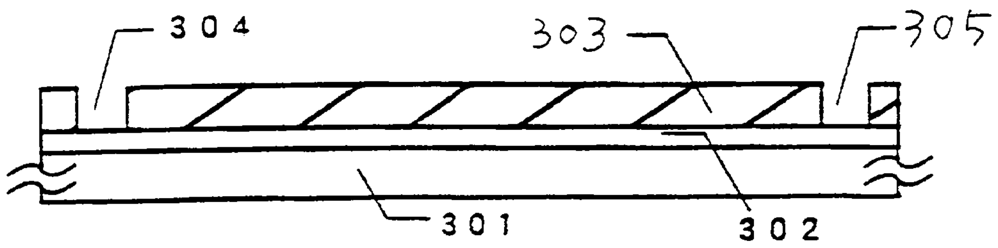


FIG. 3A

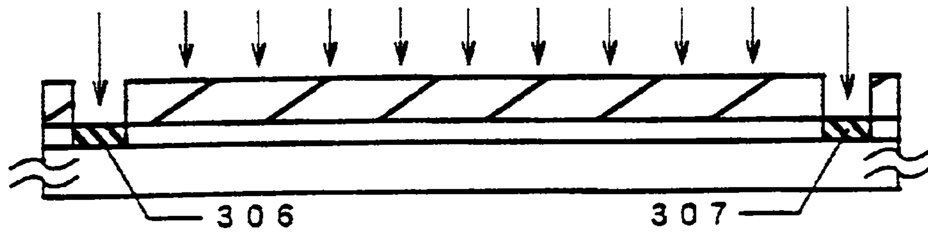


FIG. 3B

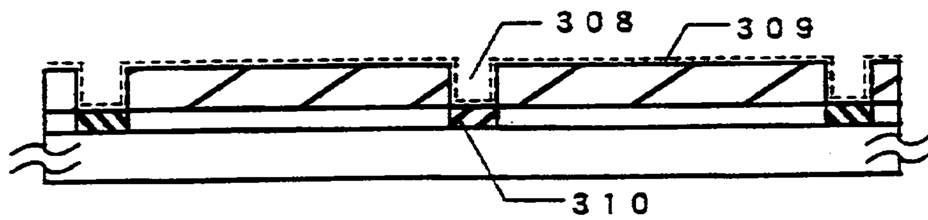


FIG. 3C

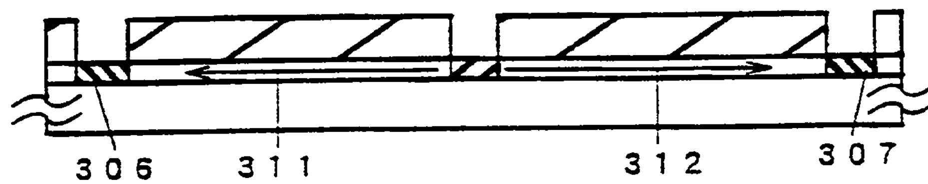


FIG. 3D

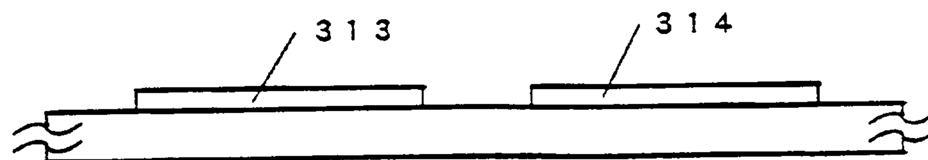


FIG. 3E

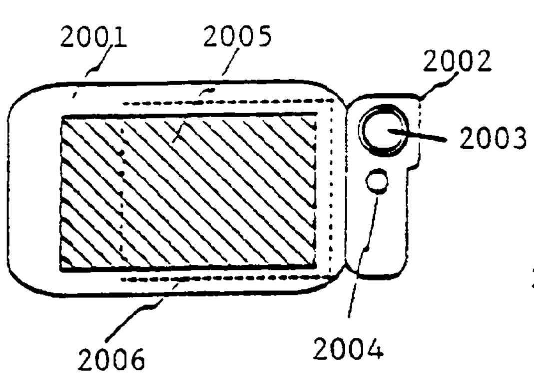


FIG. 4A

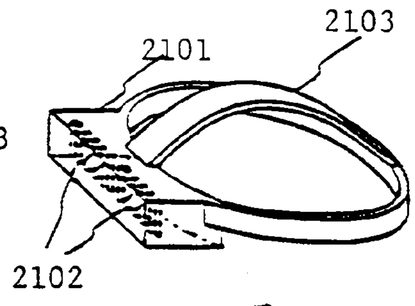


FIG. 4B

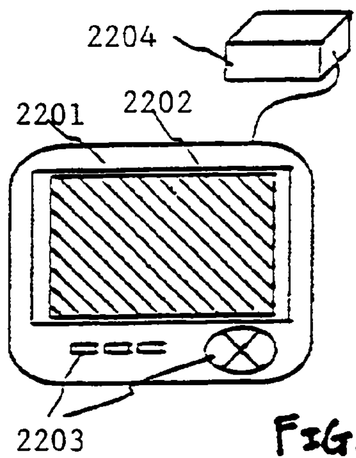


FIG. 4C

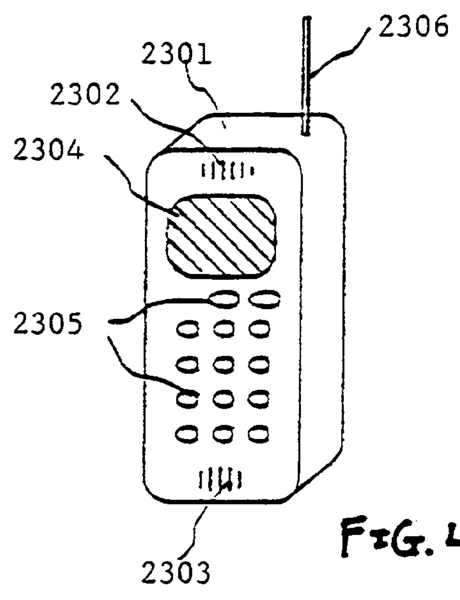


FIG. 4D

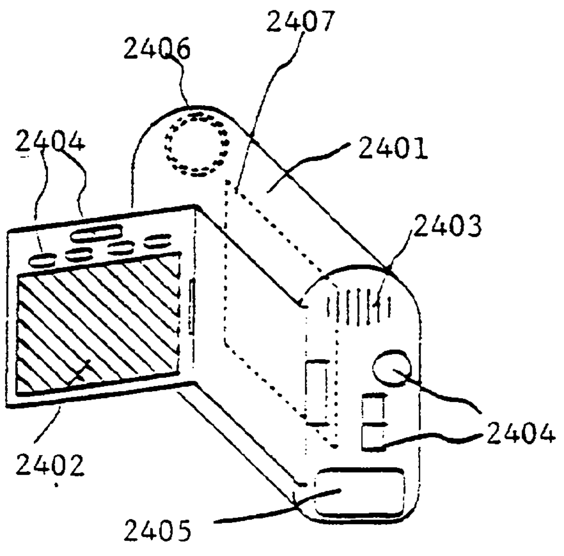


FIG. 4E

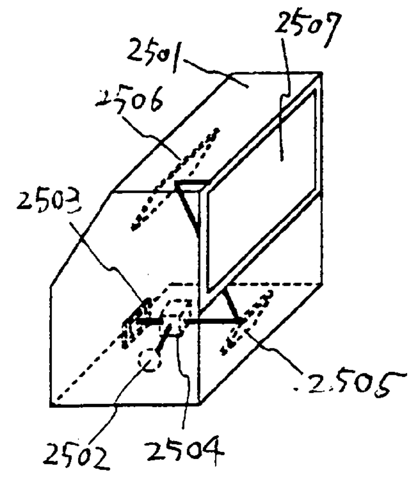
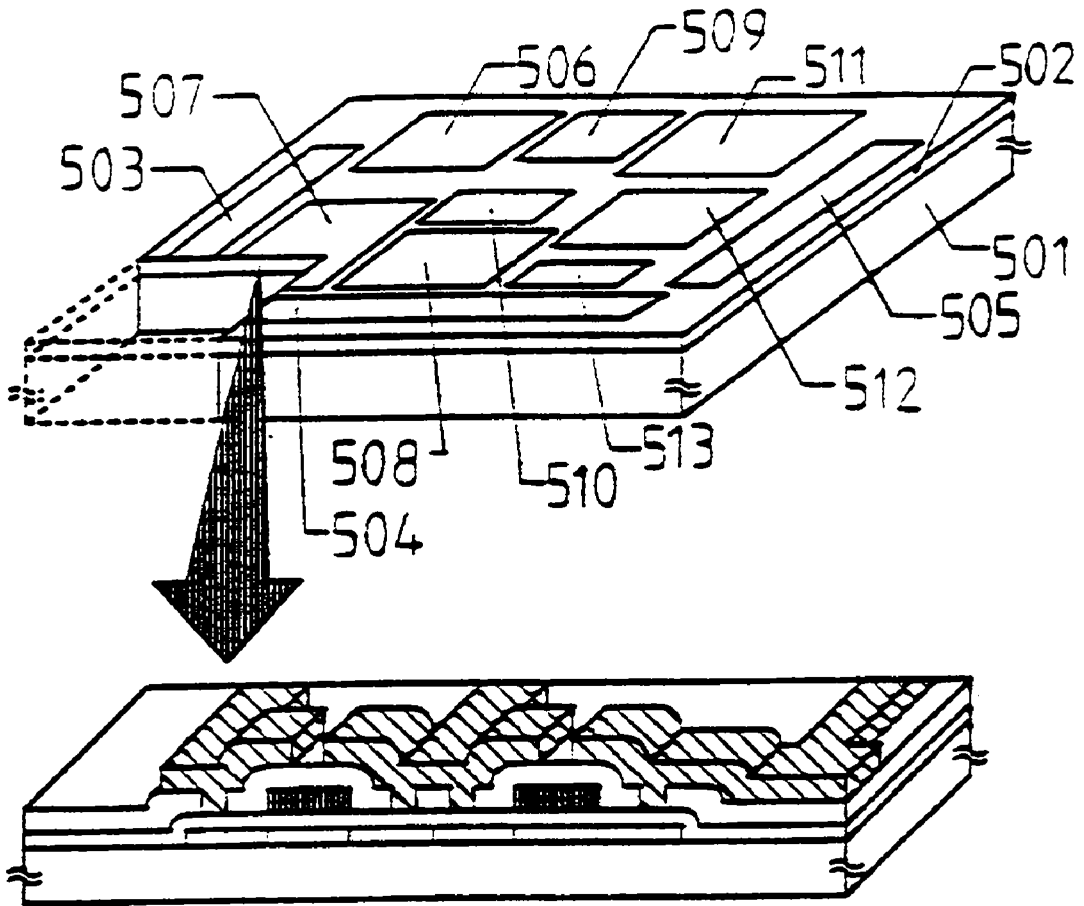


FIG. 4F

FIG. 5



SEMICONDUCTOR DEVICE AND FABRICATING METHOD THEREOF

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention disclosed in the specification relates to a method of fabricating a thin film transistor using a crystalline semiconductor film.

[0003] 2. Description of Related Art

[0004] Conventionally, there has been known a thin film transistor (hereinafter, referred to as TFT) using an amorphous silicon film. The transistor is utilized mainly for constituting an active matrix circuit of a liquid crystal display device of an active matrix type.

[0005] However, according to TFT using an amorphous silicon film, there poses a problem where the operational speed is retarded and a P-channel type one cannot be reduced to practice.

[0006] The transistor cannot be used in a liquid crystal display device of an active matrix type integrated with a peripheral drive circuit and various integrated circuits cannot be constituted by using such TFT because of such a problem.

[0007] There has been known a constitution using a crystalline silicon film as means for resolving the problem.

[0008] As methods of fabricating a crystalline silicon film, there are classified roughly into a method by heating and a method by irradiation of laser beam.

[0009] According to the method by heating, there poses a problem where a glass substrate cannot be utilized since a process at a high temperature as high as 900° C. or higher is needed.

[0010] In consideration of the fact that a major field of application of TFT is a liquid crystal display device, capability of utilizing a glass substrate as a substrate constitutes a problem with priority.

[0011] Meanwhile, according to the method by irradiation of laser beam, although a process in which a substrate does not undergo thermal damage can be realized, the process is not satisfactory in view of uniformity and reproducibility of crystallinity and a degree of crystallinity of the semiconductor film.

[0012] As a means for resolving such a problem, there has been a method of accelerating crystallization by using a predetermined catalyst element which is the invention of the applicant.

[0013] According to the method, a catalyst element represented by nickel is introduced into an amorphous silicon film and a crystalline silicon film is provided later by a heating treatment.

[0014] According to the method, a crystalline silicon film having excellent crystallinity can be provided by a heating treatment at about 600° C. or lower in which a glass substrate can be utilized.

[0015] However, nickel element remains in the crystalline silicon film by which adverse influence is effected on properties of TFT fabricated thereby.

[0016] Specifically, there poses a problem of aging change of the properties, deterioration in reliability or the like.

SUMMARY OF THE INVENTION

[0017] It is an object of the present invention disclosed in the specification to provide a technology in which in respect of TFT fabricated by using a crystalline semiconductor film obtained by utilizing a catalyst element promoting crystallization of semiconductor, adverse influence of the catalyst element is prevented from effecting on properties of TFT.

[0018] According to one aspect of the present invention disclosed in the specification, there is provided a method of fabricating a semiconductor device comprising the steps of making crystals grow from a region at a portion of an amorphous silicon film to other region thereof, the crystals growing in accordance with movement of a catalyst element promoting crystallization of semiconductor, making the catalyst element diffuse from the region of the portion of the amorphous silicon film, and gettering the catalyst element at the other region.

[0019] According to another aspect of the present invention, there is provided a method of fabricating a semiconductor device comprising the steps of making crystals grow from a region of a portion of an amorphous silicon film to other region thereof, the crystals growing in accordance with movement of a catalyst element promoting crystallization of semiconductor, and making the catalyst element diffuse from the region of the portion of the amorphous silicon film and gettering the catalyst element at the other region simultaneously.

[0020] According to another aspect of the present invention, there is provided a method of fabricating a semiconductor device comprising the steps of making crystals grow from a region of a portion of an amorphous silicon film to other region thereof, the crystals growing in accordance with movement of a catalyst element promoting crystallization of semiconductor, an origin of the movement of the catalyst element is formed at the region of the portion of the amorphous silicon film, and a destination of the movement of the catalyst element is formed at the other region.

[0021] It is most preferable to use Ni as the catalyst element in the aspects of the present invention.

[0022] According to another aspect of the present invention, one or a plurality selected from the group consisting of Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu, Au, Ge, Pb and In can be used as the catalyst element.

[0023] In respect of the aspects of the present invention; the catalyst element is selectively added to or held in contact with the region of the portion of amorphous silicon film, and an element selected from the group consisting of P, As and Sb is selectively added to or held in contact with the other region.

[0024] An element selected from P, As and Sb is an element for gettering the catalyst element. As other element for gettering, N can be pointed out. In this signification, as an element for gettering, an element selected from elements of 15 group can be used.

[0025] According to the present invention disclosed in the specification, the highest effect can be achieved when nickel

is selected as the catalyst element and P (phosphorus) is selected as the element for gettering.

[0026] As a method of introducing a catalyst element for promoting crystallization or a method of introducing an element for gettering, there can be used an ion implantation process, a diffusion process using a solution, a diffusion process using a solid, a process of diffusing the element from a film formed by a sputtering process or a CVD (Chemical Vapor Deposition) process, a plasma process, a gas adsorption process and so on.

[0027] Further, combination of these processes may be used. A selection of the processes may be carried out. For example, introduction of a catalyst element may be carried out by a process of using a solution, introduction of an element for gettering may be carried out by using a process by diffusion or the like.

BRIEF DESCRIPTION OF THE DRAWINGS

[0028] **FIGS. 1A through 1E** are views showing steps of fabricating TFT;

[0029] **FIGS. 2A through 2C** are views showing steps of fabricating TFT;

[0030] **FIGS. 3A through 3E** are views showing steps of fabricating TFT;

[0031] **FIGS. 4A through 4F** are views showing outlines of apparatuses using TFTs; and

[0032] **FIG. 5** is a view showing an outline of an integrated circuit using TFTs.

DETALED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0033] A specific example of the present invention is shown in **FIGS. 1A through 1E**.

[0034] According to an aspect of the present invention, there is provided a method of fabricating a semiconductor device comprising the steps of: making crystals grow from a region (region where openings **104** and **106** are formed) of an amorphous semiconductor film **102** to other region **109**; the crystals growing in accordance with movement of a catalyst element promoting crystallization of the semiconductor film; wherein an origin of the movement of the catalyst element is formed at the region of the portion of the amorphous semiconductor film; and wherein a destination of the movement of the catalyst element is formed at the other region.

[0035] The crystal growth is carried out simultaneously with moving nickel element from silicon oxide film patterns **107** and **108** including nickel which are sources for diffusion of nickel to a region **109** doped with phosphorus which is a site for gettering nickel.

[0036] The constitution is featured in that diffusion of nickel and gettering of nickel are simultaneously carried out.

[0037] (Embodiments)

[0038] (Embodiment 1)

[0039] Fabrication steps of the embodiment are shown in **FIGS. 1A through 1E** and **FIGS. 2A through 2C**. First, an amorphous silicon film **102** is formed on a glass substrate **101** of Corning **1737** (strain point; 667° C.) by a low pressure thermal CVD process by a thickness of 50 nm.

[0040] As a method of fabricating the amorphous silicon film, a plasma CVD process can be used other than the low pressure thermal CVD process. However, a concentration of included hydrogen which constitutes a hazard in crystallization is smaller in the case of a film formed by the low pressure thermal CVD process and accordingly, it is preferable to use the low pressure thermal CVD process when further excellent crystallinity or reproducibility is required.

[0041] When the amorphous silicon film **102** is formed, a mask **103** constituted by a silicon nitride film is formed. In this case, a silicon nitride film, not illustrated, is firstly formed by a plasma CVD process by a thickness of 250 nm. Further, a mask designated by numeral **103** is formed by patterning the film.

[0042] The mask **103** is formed with openings designated by numerals **104**, **105** and **106**. In this case, the openings **104** and **106** are for introducing nickel which is catalyst element for promoting crystallization of silicon. On the other hand, the opening **105** is for forming a site for gettering for removing nickel.

[0043] When a state illustrated in **FIG. 1A** is provided by arranging the mask **103**, a silicon oxide film including nickel is successively formed. The silicon oxide film is formed by coating a coating solution for forming a silicon oxide-base film and heating it.

[0044] In this case, as a coating solution for forming a silicon oxide-base film, OCD (Ohka Coat Diffusion-Source) Type-1 (non-doping type) made by Tokyo Ohka Kogyo Co., Ltd. is used. Nickel is included in the OCD solution to constitute a concentration of 100 ppm in conversion of weight.

[0045] A film thickness of the silicon oxide film including nickel is set to 300 nm. When the silicon oxide film including nickel is formed, the film is patterned and patterns **107** and **108** of **FIG. 1B** are formed.

[0046] The patterns **107** and **108** of the silicon oxide film constitute sources for diffusion of nickel. A nickel thin film may directly be formed as sources for diffusion of nickel. Or, implantation of nickel ions may be carried out.

[0047] Next, doping of phosphorus is carried out by using a plasma doping process (or ion implantation process). In this step, phosphorus ions are shielded by the silicon oxide film patterns **107** and **108** and the mask patterns **103** comprising silicon nitride films and selectively doped to a region designated by numeral **109** in the amorphous silicon film **102**. **(FIG. 1B)**

[0048] Although an example of introducing phosphorus by doping is shown in this example, for example, a PSG film or an amorphous silicon film including phosphorus may be formed and phosphorus may be held in contact with the region designated by numeral **109**. As or Sb can be used in place of phosphorus.

[0049] Next, a heating treatment is carried out at 500° C. for 8 hours. In this step, nickel element is diffused from the silicon oxide film patterns **107** and **108** into the amorphous silicon film **102**. Further, crystallization is progressed in accordance with diffusion of nickel.

[**0050**] On the other hand, in the region **109** where phosphorus is doped, nickel which has diffused is coupled with phosphorus and solidified there.

[**0051**] Phosphorus and nickel constitute a variety of coupling states and all of the coupling states are solid. Meanwhile, phosphorus does not diffuse in the silicon film unless at temperatures of 800° C. or higher.

[**0052**] Viewing as a whole, nickel which has diffused via paths designated by numerals **110** and **111** of **FIG. 1C** is coupled with phosphorus at the region **109** and is fixed there.

[**0053**] Further, the amorphous silicon film **102** is crystallized in accordance with the diffusion of nickel. The crystallization is progressed by the paths designated by numerals **110** and **111** in **FIG. 1C**.

[**0054**] It is preferable to select heating temperature in the crystallizing step from a range of 450° C. through 800° C., preferably, 500° C. through 750° C.

[**0055**] When the heating temperature is lower than the temperature range, operation of crystallization in accordance with diffusion of nickel is reduced.

[**0056**] Further, when the heating temperature is higher than the temperature range, in addition to diffusion of nickel, an effect of diffusing phosphorus emerges and the effect of fixing nickel to a specific region is reduced.

[**0057**] The heating treatment in this case may generally be carried out by using a heating furnace having a heater of a resistor heating type. However, the heating may be carried out by irradiating infrared ray.

[**0058**] The crystal growth carried out by the paths designated by numerals **110** and **111** is singular which is carried out in a direction in parallel with the film face. The crystal growth is referred to particularly as lateral growth.

[**0059**] The laterally-grown region can be regarded as a region where crystallization is progressed when nickel is passing.

[**0060**] Further, the region can also be regarded as a region where nickel has passed through.

[**0061**] Almost no nickel remains in the region where the crystal growth has been carried out since nickel which has contributed to crystallization is fixed at the region **109**.

[**0062**] That is, in respect of the region where the crystals have grown laterally, crystallization by diffusion of nickel and removal of nickel are simultaneously carried out.

[**0063**] When the step of crystallization shown in **FIG. 1C** has been finished, the silicon oxide film patterns **107** and **108** are removed. Further, the masks **103** comprising silicon nitride films are removed.

[**0064**] Further, the remaining silicon film is patterned and patterns designated by numerals **112** and **113** of **FIG. 1D** are formed. These patterns are formed by utilizing the regions where lateral growth of crystals has been carried out.

[**0065**] According to the embodiment, a pattern designated by numeral **112** constitutes an activation layer of TFT of P-channel type. Further, a pattern designated by numeral **113** constitutes an activation layer of TFT of an N-channel type.

[**0066**] Next, a silicon oxide film **114** for constituting a gate insulating film is formed by a plasma CVD process by a thickness of 100 nm. **(FIG. 1E)**

[**0067**] Next, an aluminum film, not illustrated, is formed by a thickness of 400 nm and the aluminum film is patterned by which patterns designated by numerals **115** and **116** of **FIG. 1E** are formed.

[**0068**] These aluminum patterns constitute gate electrodes of respective TFTs. Next, by carrying out anodic oxidation with the gate electrode patterns as anodes, anodized films **117** and **118** are formed. The film thickness of the anodized film is set to 70 nm. In this way, a state shown in **FIG. 1E** is provided.

[**0069**] The anodized film achieves an effect of restraining physically formation of projections referred to as hillocks or whiskers.

[**0070**] Next, doping of phosphorus over an entire region is carried out by using a plasma doping process. In this step, as shown in **FIG. 2**A, phosphorus is doped at regions **119**, **121**, **122** and **124** as shown in **FIG. 2A**. Further, doping is not carried out at regions **120** and **123**.

[**0071**] Next, a resist mask **125** is formed as shown in **FIG. 2B**. Further, at this occasion, doping of boron is carried out by a plasma doping process.

[**0072**] According to the step, the doping is carried out under a condition where an amount of dose is made larger than that in previous doping operation of phosphorus. Further, the conductive type of regions **126** and **127** is reverted.

[**0073**] In this way, the regions **122** and **124** of an N-type and the regions **126** and **127** of a P-type are formed.

[**0074**] The region **122** constitutes a drain region of TFT of an N-channel type. Further, the region **124** constitutes a source region of TFT of an N-channel type. Further, the region **123** constitutes a channel region of TFT of an N-channel type.

[**0075**] Further, the region **126** constitutes a source region of TFT of a P-channel type. Further, the region **127** constitutes a drain region of TFT of a P-channel type. Further, the region **120** constitutes a channel region of TFT of a P-channel type.

[**0076**] Next, as shown in **FIG. 2C, a** silicon nitride film **128** is formed as an interlayer insulating film by a plasma CVD process by a thickness of 250 nm. Further, an acrylic resin film **129** is formed as an interlayer insulating film. The film thickness of the acrylic resin film is set to 700 nm at a portion where it is minimized.

[**0077**] Acrylic resin is used since a surface thereof can be flattened. Other than acrylic resin, a material of polyimide, polyamide, polyimide amide, epoxy or the like can be used.

[**0078**] After forming the interlayer insulating films, contact holes are formed and a source electrode **130** and a drain electrode **131** of a P-channel type TFT (PTFT) are formed.

[**0079**] Further, a source electrode **133** and a drain electrode **132** of an N-channel type TFT (NTFT) are formed.

[**0080**] In this way, a P-channel type TFT and an N-channel type TFT can be fabricated by integrating them on the same substrate.

[0081] Although according to the embodiment, an example in the case where aluminum is used as gate electrode has been shown, the gate electrode can be constituted by using titanium or silicon material, or various silicide materials.

[0082] In this embodiment, an example of the case of a top gate type has been shown as the type of TFT. However, the present invention disclosed in the specification can be utilized also in TFT of a bottom gate type where the gate electrode is on the lower side (substrate side) of the activation layer.

[0083] In this case, the fabrication procedure is such that an amorphous film is formed after forming a gate electrode.

[0084] (Embodiment 2)

[0085] This embodiment shows an example where the solution of Embodiment 1 which includes nickel (Ni) as catalyst element for promoting crystallization of an amorphous silicon film is coated by a spin coating process.

[0086] **FIGS. 3A through 3E** show fabrication steps of the embodiment. First, similar to Embodiment 1, an amorphous silicon film **302** is formed on a glass substrate of Corning **1737** (strain point; 667° C.) **301** by a low pressure CVD process by a thickness of 50 nm.

[0087] When the amorphous silicon film **302** has been formed, in this case, a silicon oxide film, not illustrated, is firstly formed by a plasma CVD process by a thickness of 150 nm. Then, the film is patterned by which a silicon oxide film pattern designated by numeral **303** is formed.

[0088] The silicon oxide film pattern **303** is formed with openings designated by numerals **304** and **305**. The openings **304** and **305** are for selecting regions for adding P (phosphorus) to remove nickel.

[0089] When the silicon oxide film pattern **303** has been arranged and a state shown in **FIG. 3A** is provided, addition of phosphorus is successively carried out by using a plasma doping process (or ion implantation process). In this step, phosphorus ions are shielded by the silicon oxide film pattern **303** and are selectively doped to regions designated by numerals **306** and **307** of the amorphous silicon film **302** from the openings **304** and **305** of the silicon oxide film pattern.

[0090] When doping of phosphorus has been carried out, the silicon oxide film pattern **303** is patterned again and an opening **308** is newly formed in addition to the openings **304** and **305**.

[0091] The opening **308** is for introducing nickel which is catalyst element for promoting crystallization of the amorphous silicon film **302**.

[0092] When the silicon oxide film pattern **303** having the openings **304**, **305** and **308** has been arranged and a state shown in **FIG. 3B** is provided, a solution including nickel (10 ppm) is coated by a spin coating process and a layer **310** of a region including Ni is formed (**FIG. 3C**).

[0093] In gettering remaining nickel, it is preferable to set a condition where a concentration of phosphorus element is higher than a concentration of nickel. According to the embodiment, phosphorus element is set to remain with a concentration of about 1×1020 atoms/cm^3 or more at minimum since the concentration of nickel remaining in the amorphous silicon film **302** is 1×10^{19} atoms/cm^3 when the gettering step is not carried out.

[0094] When the step of adding catalyst element has been finished, crystallization of the amorphous silicon film **302** is carried out by performing a heating treatment at temperatures of 450 through 800° C. (representatively, 500 through 700° C.) for 4 through 24 hours in an inert atmosphere, a hydrogen atmosphere or an oxygen atmosphere. According to the embodiment, the heating treatment is carried out at 570° C. for 4 through 8 hours in a nitrogen atmosphere.

[0095] In this step, nickel diffuses from the region **310** into the amorphous silicon film **302**. Further, crystallization is progressed in directions of arrow marks **311** and **312** of **FIG. 3D** in accordance with diffusion of nickel.

[0096] On the other hand, at the regions **306** and **307** where phosphorus is doped, diffused nickel is coupled with phosphorus and is solidified there.

[0097] Phosphorus and nickel are provided with a variety of coupling states and all of the coupling states are solid. When the heating temperature is lower than 450° C., operation of crystallization in accordance with diffusion of nickel is reduced.

[0098] Further, when the heating temperature is higher than 800° C., in addition to diffusion of nickel, an effect of diffusing phosphorus emerges and the effect of solidifying nickel at specific regions is reduced.

[0099] The heating treatment mentioned here may generally be carried out by using a heating furnace having a heater of a resistor heating type. However, the heating may be carried out by irradiating infrared ray.

[0100] According to the crystal growth which is carried out via the paths designated by numerals **311** and **312**, similar to Embodiment 1, crystals are grown laterally.

[0101] Nickel which has contributed to crystallization is solidified concentratingly at the regions **306** and **307** and therefore, almost no nickel remains in the regions where the lateral growth has been carried out.

[0102] That is, in respect of the regions where lateral growth has been carried out, crystallization by diffusion of nickel and removal of nickel are simultaneously performed.

[0103] Therefore, viewing as a whole, nickel which has diffused via the paths designated by numerals **311** and **312** of **FIG.** 3D, is coupled with phosphorus at the regions **306** and **307** and is solidified there.

[0104] Further, by setting a condition where a concentration of adding phosphorus element is higher than a concentration of adding nickel to the amorphous silicon film **302** by one order or more, nickel added to the phosphorus adding regions **306** and **307** in **FIG.** 3D, is gettered in the phosphorus adding regions **306** and **307** without diffusing into the amorphous silicon film **302**.

[0105] When the step of crystallization shown in **FIG. 3D** has been finished, the silicon oxide film pattern **303** is removed and the remaining silicon film is patterned by which patterns designated by numerals **313** and **314** of **FIG. 3E** are formed.

[0106] After patterning the silicon film, TFTs are fabricated in later steps in accordance with Embodiment 1 or other publicly-known process.

[0107] (Embodiment 3)

[0108] According to the embodiment, examples of various apparatuses utilizing TFTs are shown. **FIG. 5** shows an example of a microprocessor of a semiconductor circuit utilizing TFTs and complementary TFT of N-type TFT and P-type TFT by enlarging a portion of the semiconductor circuit.

[0109] An insulating film **502** is formed on a ceramics substrate **501** and the substrate and elements are insulated and separated from each other. Further, there are formed on top thereof I/O ports **503** through **505**, CPU **506**, a cash memory **507**, a cash address array **508**, a multiplier **509**, a circuit **510** including real time clock, serial interface, a timer and so on, a clock control circuit **511**, a cash controller **512** and a bus controller **513**.

[0110] The thin-film transistors disclosed in the specification can be utilized in various flat panel displays, information processing terminals having flat panel displays, a video camera and the like. According to the specification, these apparatuses are generally referred to as semiconductor devices.

[0111] Examples of specific constitutions of various apparatuses will be shown below. **FIGS. 4A through 4F** show examples of various semiconductor devices. These semiconductor devices use TFTs at least portions thereof.

[0112] **FIG. 4A** shows an information processing terminal of a portable type. The information processing terminal is provided with a liquid crystal display of an active matrix type or an EL (Electro-luminescence) display of an active matrix type at a main body **2001** and is provided with a camera unit **2002** for taking information from outside. An integrated circuit **2006** is provided therein.

[0113] The camera unit **2002** is arranged with an image receiving unit **2003** and an operation switch **2004**.

[0114] An information processing terminal is considered to become thinner and lighter in the future to promote the portability.

[0115] According to the constitution, it is preferable to integrate also peripheral drive circuit, operation circuit and memory circuit on a substrate formed with a display **2005** of an active matrix type by TFTs.

[0116] **FIG. 4B** shows a head mount display. The device is provided with a liquid crystal display or an EL display **2102** of an active matrix type at a main body **2101**. Further, the main body **2101** can be mounted on the head by a band **2103**.

[0117] **FIG. 4C** shows a car navigation system. The device is provided with a function of receiving a signal from an artificial satellite by an antenna **2204** and displaying geographical information on a liquid crystal display **2202** of an active matrix type installed to a main body **2201** based on the signal.

[0118] A display device of an EL type can also be adopted as the display **2202**. In any cases, the display is a flat panel display of an active matrix type utilizing TFTs.

[0119] Further, the main body **2201** is provided with operation switches **2203** whereby various operation can be carried out.

[0120] **FIG. 4D** shows a portable telephone. The device is provided with a liquid crystal display device **2304**, operation switches **2305**, a voice input unit **2303**, a voice output unit **2302** and an antenna **2306** at a main body **2301**.

[0121] In recent times, a constitution combining the portable type information processing terminal shown in **FIG.** 4A and the portable telephone shown in **FIG. 4D** is commercialized.

[0122] **FIG. 4E** shows a portable type video camera. The camera is provided with an image receiving unit **2406**, a voice input unit **2403**, operation switches **2404**, a liquid crystal display **2402** of an active matrix type and a battery **2405** at a main body **2401**.

[0123] **FIG. 4F** shows a liquid crystal display device of a rear projection type. The constitution is provided with a structure having a screen for projection at a main body **2501**. In the displaying operation, light from a light source **2502** is separated by a polarized beam splitter **2504**, separated light is optically modulated by a liquid crystal display device **2503** of a reflecting type, and an image which has been optically modulated is reflected by reflectors **2505** and **2506** and is projected on a screen **2507**.

[0124] In this case, an example of using a reflecting type of the liquid crystal display device **2503** has been shown. However, a liquid crystal display device of a transmitting type may be used here. In this case, an optical system may be changed.

[0125] (Embodiment 4)

[0126] The embodiment shows an example in the case where a film comprising Si_xGe_{1-x} $(0.5<X<1)$ is used in place of a silicon film in constitutions of other embodiments.

[0127] According to the present invention disclosed in the specification, a film comprising not only a single body of silicon but also a compound whose major component is silicon can be used. In this case, in the constitution of Embodiment 1, an amorphous film whose major component is silicon may be used in place of the amorphous silicon film mentioned before.

[0128] Further, a film whose major component is silicon is referred to a film including at least a half or more of silicon component.

[0129] For example, in the case of Embodiment 1, the amorphous silicon film **102** can be constituted by a film comprising Si_xGe_{1-x} $(0.5<X<1)$.

[0130] (Embodiment 5)

[0131] The embodiment shows an example in the case where a method of introducing nickel element is devised in the constitution shown in Embodiment 2.

[0132] According to the embodiment, a solution including nickel is held in contact with the surface of amorphous silicon film at the openings **303** and **304** in **FIG. 3A**.

[0133] Specifically, the portions of the openings **303** and **304** are masked by a resist or the like and phosphorus is doped to the region **308**.

[0134] Further, masks at the portions of the openings **303** and **304** are removed and the region of the opening **308** is separately masked by a silicon oxide film or the like.

[0135] Under the state, a solution of nickel acetate is coated. Thereby, a state where nickel is held in contact with the surface of the amorphous silicon film is provided at the openings **303** and **304**.

[0136] Next, by carrying out a heating treatment, crystal growth shown in **FIG. 3D** is carried out.

[0137] Although in this case, an example of using a solution is shown as a method of introducing nickel, otherwise, a method of forming a nickel film or a film including nickel by a sputtering process or a CVD process may be adopted.

[0138] (Embodiment 6)

[0139] The embodiment shows an example in the case where in the fabrication steps shown in Embodiment 1, a step of removing nickel element from the silicon film is further added.

[0140] According to the embodiment, a glass substrate is used as the substrate **101** in the fabrication steps shown in **FIGS. 1A through 1E**.

[0141] Further, after finishing to getter nickel in respect of the region **109** where phosphorus is doped shown in **FIG.** 1C, the heating step is carried out in an atmosphere including **97** volume % of oxygen and 3 volume % of HCl. The heating step is carried out under conditions of 950° C. and 30 minutes. Other than HCl, for example, $POCl_3$ gas can be used.

[0142] In this case, nickel element is vaporized in a state of nickel chloride from the film and is removed to outside.

[0143] In this way, nickel element can be removed from inside of the silicon film to outside. Successively, the silicon film is patterned as shown in **FIG.** 1D and TFTs are fabricated.

[0144] (Embodiment 7)

[0145] The embodiment shows an example in the case where in the fabrication steps shown in Embodiment 1, a thermally oxidizing step is used in the step of fabricating the gate insulating film which is the step shown in **FIG. 1E**.

[0146] In this embodiment, a glass substrate is used as the substrate **101**. Further, in the step shown in **FIG.** 1E, after forming the silicon oxide film **114** by a plasma CVD process, a thermally oxidized film is further formed on the surface of the activation layer pattern by a thermally oxidizing process.

[0147] In this case, after forming the silicon oxide film **114** by a thickness of 30 nm, a heating treatment in an atmosphere including 97 volume % of oxygen and 3 volume % of HCl is carried out under conditions of 950° C. and 30 minutes.

[0148] In this case, the thermally oxidized film grows to a thickness of 30 nm. In this way, the thermally oxidized film having a thickness of 60 nm is formed.

[0149] Thereby, a state of an interface between the activation layer and the gate insulating film can be improved and TFTs having excellent properties can be provided.

[0150] According to the present invention disclosed in the specification, the following constitutions are basically adopted.

[0151] (1) A source for diffusing a catalyst element for promoting crystallization of an amorphous silicon film and a site for gettering the catalyst element are selectively formed in the amorphous silicon film.

[0152] (2) In crystallizing the amorphous silicon film, the crystallization is carried out by moving the catalyst element from the source of diffusion to the side of gettering.

[0153] (3) The source for diffusion and the site for gettering are removed and a region which has been crystallized in accordance with passage of the catalyst element is used as an activation layer.

[0154] In this way, in TFT fabricated by using a crystalline silicon film provided by utilizing a catalyst element promoting crystallization of semiconductor, adverse influence of the catalyst element can be restrained from effecting on properties thereof.

[0155] Further, the present invention disclosed in the specification is featured in that the above-described effects can be achieved in simplified fabrication steps.

What is claimed is:

1. A method of fabricating a semiconductor device comprising the steps of:

making crystals grow from a region at a portion of an amorphous semiconductor film to other region thereof;

making a catalyst element diffuse from the region of the portion of the amorphous semiconductor film, said catalyst element promoting crystallization of said semiconductor film; and

gettering the catalyst element at said other region,

wherein said crystals grow in accordance with movement of said catalyst element in said semiconductor film.

2. A method of fabricating a semiconductor device comprising the steps of:

making crystals grow from a region of a portion of an amorphous semiconductor film to other region thereof; and

making a catalyst element diffuse from the region of the portion of the amorphous semiconductor film and gettering the catalyst element at the other region simultaneously,

wherein said crystals grow in accordance with movement of said catalyst element promoting crystallization of semiconductor.

3. A method of fabricating a semiconductor device comprising the steps of:

making crystals grow from a region of a portion of an amorphous semiconductor film to other region thereof, said crystals growing in accordance with movement of a catalyst element promoting crystallization of semiconductor,

wherein an origin of the movement of the catalyst element is formed at the region of the portion of the amorphous semiconductor film; and

wherein a destination of the movement of the catalyst element is formed at the other region.

4. The method according to claim 1, wherein said catalyst element is nickel.

5. The method according to claim 2, wherein said catalyst element is nickel.

6. The method according to claim 3, wherein said catalyst element is nickel.

7. The method according to claim 1, wherein said catalyst element is one or a plurality selected from the group consisting of Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu, Au, Ge, Pb and In.

8. The method according to claim 2, wherein said catalyst element is one or a plurality selected from the group consisting of Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu, Au, Ge, Pb and In.

9. The method according to claim 3, wherein said catalyst element is one or a plurality selected from the group consisting of Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu, Au, Ge, Pb and In.

10. The method according claim 1 wherein said catalyst element is selectively added to or held in contact with the region of the portion of amorphous semiconductor film, and wherein an element selected from the group consisting of P, As and Sb is selectively added to or held in contact with said other region.

11. The method according claim 2 wherein said catalyst element is selectively added to or held in contact with the region of the portion of amorphous semiconductor film, and wherein an element selected from the group consisting of P, As and Sb is selectively added to or held in contact with said other region.

12. The method according claim 3 wherein said catalyst element is selectively added to or held in contact with the region of the portion of amorphous semiconductor film and an element selected from the group consisting of P, As and Sb is selectively added to or held in contact with said other region.

13. The method according to claim 1, wherein said catalyst element is selectively added to or held in contact with the region of the portion of amorphous semiconductor film and an element selected from elements of 15 group is selectively added to or held in contact with said other region.

14. The method according to claim 2, wherein said catalyst element is selectively added to or held in contact with the region of the portion of amorphous semiconductor film and an element selected from elements of 15 group is selectively added to or held in contact with said other region.

15. The method according to claim 3, wherein said catalyst element is selectively added to or held in contact with the region of the portion of amorphous semiconductor film and an element selected from elements of 15 group is selectively added to or held in contact with said other region.

16. The method according to claim 1, wherein the crystals are made to grow by heating the semiconductor film.

17. The method according to claim 2, wherein the crystals are made to grow by heating the semiconductor film.

18. The method according to claim 3, wherein the crystals are made to grow by heating the semiconductor film.

19. The method according to claim 1, wherein said amorphous semiconductor film comprises silicon as a major component.

20. The method according to claim 2, wherein said amorphous semiconductor film comprises silicon as a major component.

21. The method according to claim 3, wherein said amorphous semiconductor film comprises silicon as a major component.

22. The method according to claim 1 further comprising a step of performing a heating treatment in an atmosphere including a halogen element for moving the catalyst element to outside of the semiconductor film.

23. The method according to claim 2 further comprising a step of performing a heating treatment in an atmosphere including a halogen element for moving the catalyst element to outside of the semiconductor film.

24. The method according to claim 3 further comprising a step of performing a heating treatment in an atmosphere including a halogen element for moving the catalyst element to outside of the semiconductor film.

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