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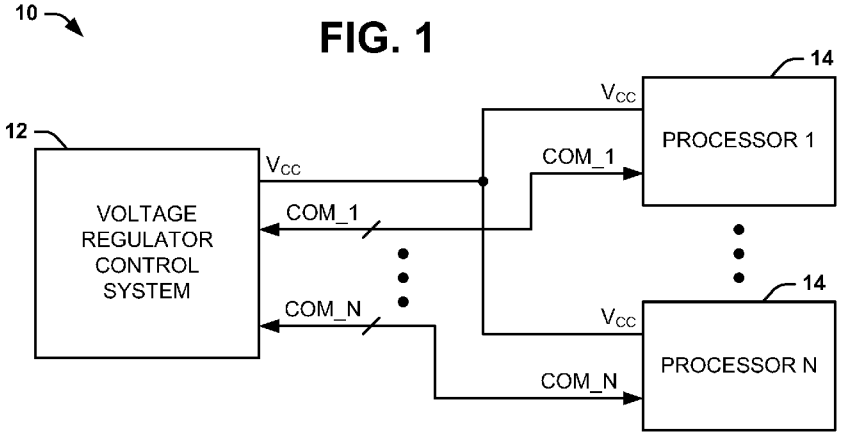
(54) Title: VOLTAGE REGULATOR CONTROL SYSTEM

FIG. 1



(57) Abstract: A processor power management system and method are disclosed. The system includes a voltage regulator control system that is communicatively coupled to each of a plurality of processors. The voltage regulator control system is to generate a processor voltage that is provided to each of the plurality of processors and to control a magnitude of the processor voltage based on receiving power management request signal s that are provided from each of the plurality of processors.

VOLTAGE REGULATOR CONTROL SYSTEM

BACKGROUND

[0001] A high-performance processor, such as one that can be implemented in a variety of computer and portable electronic devices, can receive power from a voltage regulator that generates a processor voltage. The processor can control the voltage regulator that provides its power to optimize for performance and efficiency. For example, when a heavy computational load is required, the processor can send a command to the voltage regulator to increase the processor voltage to substantially meet the needs of the processor. As another example, when the processor does not require a heavy computational load, the processor can issue a command to decrease the processor voltage and to deactivate unnecessary components to conserve power.

BRIEF DESCRIPTION OF THE DRAWINGS

[0002] FIG. 1 illustrates an example of a power management system.

[0003] FIG. 2 illustrates an example of a voltage regulator control system.

[0004] FIG. 3 illustrates another example of a power management system.

[0005] FIG. 4 illustrates an example method for controlling a processor voltage that is provided to each of a plurality of processors.

DETAILED DESCRIPTION

[0006] FIG. 1 illustrates a power management system 10. The power management system 10 includes a voltage regulator control system 12 and a plurality N of processors 14, where N is a positive integer greater than one. As an example, the power management system 10 can be implemented in a variety of computer systems and/or portable electronic devices, such as laptop or tablet computers or in wireless communication devices. The plurality of processors 14 can be configured as low-power processors that are implemented, for example, instead of a single high-performance processor, such that the plurality of processors can provide a substantially more efficient processing system.

[0007] The voltage regulator control system 12 is communicatively coupled to each of the plurality of processors 14 via a respective plurality of signals COM. In the example of FIG. 1, the signals COM are demonstrated respectively as COM_1 through COM_N corresponding to each of the respective N processors. As an example, each of the signals COM_1 through COM_N can be communicated between the voltage regulator control system 12 and the respective processors 14 via a Serial Voltage IDentification (SVID) bus or another type of communication bus. The voltage regulator control system 12 is also configured to generate a processor voltage V_{CC} that is provided to each of the processors 14 to provide power to the processors 14. As an example, the voltage regulator control system 14 can include one or more power supplies, with at least one of the power supplies being configured to generate the processor voltage V_{CC}.

[0008] As an example, the processors 14 can be configured to individually switch between an active mode and a low power mode. The active mode can correspond to a mode in which a respective one of the processors 14 is performing a substantial amount of processing capability (*e.g.*, based on substantially high computational resource requirements). Therefore, the active mode can require a relatively higher magnitude of the processor voltage V_{CC} to support the power requirements of the processing performance of the active mode. Conversely, the low power mode can correspond to a mode in which a respective one of the processors 14 is in an idle mode (*e.g.*, sleep mode) or is performing a nominal processing capability (*e.g.*, based on substantially low computational resource requirements). Therefore, the low power mode does not require the relatively higher magnitude of the processor voltage V_{CC}, and thus can operate based on a relatively low magnitude of the processor voltage V_{CC} to substantially conserve power consumption for more efficient operation of the power management system 10. While it is described herein that the processors 14 operate in either an active mode or a low power mode, it is to be understood that the processors 14 can be configured to operate in a plurality of additional voltage levels, such as based on the respective workloads required by the processor. Therefore, as described herein, switching from the active mode to the low power mode can correspond to any transition of the processor voltage V_{CC} from a relatively higher magnitude to a relatively lower

magnitude, and switching from the low power mode to the active mode can correspond to any transition of the processor voltage V_{CC} from a relatively lower magnitude to a relatively higher magnitude.

[0009] The voltage regulator control system 12 can be configured to adjust the magnitude of the processor voltage V_{CC} based on one or more power management request signals provided via the signals COM from at least one of the processors 14. For example, one of the processors 14 may need to switch from the low power mode to the active mode, such as based on a requested amount of computational resources, while receiving an insufficient magnitude of the processor voltage V_{CC} for operation in the active mode. Thus, the respective processor 14 can generate a voltage increase request signal via the respective signal COM to the voltage regulator control system 12. As an example, the voltage increase request signal can include one or both of the [01h – SetVID-fast] or the [02h – SetVID-slow] commands in a VR12 Specification associated with an SVID bus.

[0010] In response to receiving the voltage increase request signal, the voltage regulator control system 12 can be configured to increase the magnitude of the processor voltage V_{CC}. The voltage regulator control system 12 can also be configured to issue an alert to each of the remaining processors 14, such as to indicate that the processor voltage V_{CC} is about to increase to support operation in the active mode. Therefore, the remaining processors 14 can likewise switch to the active mode, if necessary, based on having a sufficient magnitude of the processor voltage V_{CC} for operating in the active mode. As an example, the remaining processors 14 can thus switch to the active mode without providing a voltage increase request signal. As another example, any of the processors 14 that switch to the active mode can generate an acknowledgement to the voltage regulator control system 12 to indicate the mode in which the respective processors 14 operate.

[0011] As another example, one of the processors 14 may no longer be required to operate in an active mode, and can thus switch to the low power mode in an attempt to conserve power. For example, the processor 14 can revert to an idle mode from the active mode upon substantially completing a given computation or processing operation. Thus, the respective processor 14 can generate a voltage

decrease request signal via the respective signal COM to the voltage regulator control system 12. For instance, in the example of the use of an SVID bus, the voltage increase request signal can include one or all of the [01h – SetVID-fast], the [02h – SetVID-slow], or [03h – SetVID-decay] commands in the VR12 Specification.

[0012] In response to receiving the voltage decrease request signal, the voltage regulator control system 12 can be configured to determine the current operating mode of each of the remaining processors 14. The voltage regulator control system 12 could thus decrease the magnitude of the processor voltage V_{CC} in response to the voltage decrease request signal and a determination that all of the remaining processors 14 are operating in the low power mode. Therefore, a decreased magnitude of the processor voltage V_{CC} is sufficient for all of the processors 14 to function in the low power mode. However, in response to determining that at least one of the processors 14 operates in the active mode, the voltage regulator control system 12 is configured to maintain the magnitude of processor voltage V_{CC}, as opposed to decreasing it in response to the voltage decrease request signal. As a result, the processor 14 operating in the active mode can continue to receive the power sufficient for operation in the active mode based on the relatively greater magnitude of the processor voltage V_{CC}.

[0013] In addition, the voltage regulator control system 12 can also be configured to issue an alert to each of the remaining processors 14, such as to indicate that the processor voltage V_{CC} is about to decrease. Furthermore, in the event that the voltage regulator control system 12 is unable to decrease the processor voltage V_{CC} based on one of the processors 14 operating in the active mode, the voltage regulator control system 12 can issue an alert to the processor 14 that provided the voltage decrease request signal to inform the respective processor 14 that the processor voltage V_{CC} that the request to decrease the processor voltage V_{CC} cannot be satisfied at that time. As a result, the requesting processor 14 can attempt the request again at a later time, such as periodically. Additionally or alternatively, the voltage regulator control system 12 can queue the request until all of the processors 14 are switched the low power mode. Therefore, the voltage regulator control system 12 can eventually satisfy the request at an

appropriate time, and can first provide an alert to all of the processors 14 of an imminent decrease to the processor voltage V_{CC}.

[0014] As a result of the communicative coupling of the plurality of processors 14 with the voltage regulator control system 12, the voltage regulator control system 12 can effect power management of the plurality of processors 14 in a simple, efficient, and cost effective manner. By transmitting alert signals to all of the processors 14 based on a voltage change request issued by one of the processors 14, the power regulator system 10 can be configured as a centralized, system-wide regulator in which the power requirements of the processors 14 are openly communicated with respect to each other. Thus, the more centralized implementation of the power regulator system 10 for controlling the power of the plurality of processors 14 can operate in a manner that takes into account a multitude of factors, such as total system power, thermal requirements, and other load balancing considerations. In addition, as an example, by implementing the single voltage regulator control system 12 instead of a plurality of voltage regulators associated with the respective plurality of processors 14, the power management system 10 can achieve cost savings based on a reduced set of electronic components and can be implemented in a more compact design. As another example, by implementing a single, larger power supply in the voltage regulator control system 12 relative to smaller power supplies associated with the respective processors 14, the voltage regulator control system 12 can be designed in a more power efficient and flexible manner. Therefore, the power management system 10 can be implemented in a variety of electronic device environments for a more efficient, cost effective, and space-saving design.

[0015] FIG. 2 illustrates an example of a voltage regulator control system 50. The voltage regulator control system 50 can correspond to the voltage regulator control system 12 in the example of FIG. 1. Therefore, reference is to be made to the example of FIG. 1 in the following description of the example of FIG. 2. In the example of FIG. 2, the voltage regulator control system 50 can be configured as an integrated circuit (IC), such as an application specific integrated circuit (ASIC).

[0016] The voltage regulator control system 50 includes a plurality X of voltage regulators 52, where X is a positive integer. In the example of FIG. 2, each

of the voltage regulators 52 can be configured to generate a respective voltage V_{CC}, demonstrated in the example of FIG. 2 as V_{CC_1} through V_{CC_X}. As an example, each of the voltage regulators 52 can include at least one power supply to generate the respective voltages V_{CC_1} through V_{CC_X}. One of the voltages V_{CC_1} through V_{CC_X} can correspond to the processor voltage V_{CC} (*e.g.*, the voltage V_{CC_1}) in the example of FIG. 1. Therefore, the voltage regulator control system 50 can provide the remaining voltages (*e.g.*, the voltages V_{CC_2} through V_{CC_X}) to other components in an associated computer system that includes the voltage regulator control system 50. While the example of FIG. 2 demonstrates that the voltage regulator control system 50 includes at least two voltage regulators 52, it is to be understood that X could be equal to one, such that the voltage regulator control system 50 generates only a single processor voltage V_{CC}.

[0017] The voltage regulator control system 50 also includes a processor voltage regulator (VR) controller 54 and a VR memory 56 that are communicatively coupled together. The processor VR controller 54 can be configured as a processor or a logic controller that is communicatively coupled to the processors 14 via the signal COM, which can be configured as one or more buses. The processor VR controller 54 can thus be configured to process requests that are provided from the respective processors 14 and can issue alerts to the respective processors 14 via the signals COM. It is to be understood that the VR memory 56 can be a memory specific to the processor VR controller 54, such that the plurality of processors 14 of the power management system 10 can be communicatively coupled with a separate memory (not shown). Alternatively, the VR memory 56 could be implemented as part of an overall memory system, such as including memory associated with the processors 14.

[0018] As an example, the processor VR controller 54 can be configured to buffer requests that are provided by the processors 14 in the VR memory 56. The processor VR controller 54 can also be configured to store status conditions and parameters associated with regulating the power of each of the respective processors 14 in the VR memory 56. For example, the parameters can include data associated with a maximum current requirement of each of the processors 14, a slew-rate of the current (*i.e.*, di/dt) for each of the processors 14, and a variety of

other parameters associated with power regulation of each of the respective processors 14. Such parameters associated with each of the processors 14 can be different for each of the respective processors 14, and can change over the operation life of the respective processors 14.

[0019] The VR memory 56 can include a set of memory registers that are specific to each of the respective processors 14. Therefore, the processor VR controller 54 can be configured to set address pointers within the VR memory 56 to correspond to a given one of the processors 14 from which a respective message is provided to the voltage regulator control system 50. As an example, the processor VR controller 54 can be configured to designate specific memory registers to each of the respective processors 14, such as during a boot-up operation of the associated computer system in which the voltage regulator control system 50 is included. Thus, the processor VR controller 54 can manage the VR memory 56 with respect to the processors 14. Accordingly, commands communicated between the processor VR controller 54 and the processors 14 can be buffered and/or stored in the specific registers of the VR memory 56 in a manner that is substantially transparent to the processors 14.

[0020] FIG. 3 illustrates another example of a power management system 100. The power management system 100 includes a voltage regulator system 102, a multi-host voltage regulator control system 104, and a plurality N of processors 106, where N is a positive integer greater than one. As an example, the power management system 100 can be implemented in a variety of computer systems and/or portable electronic devices, such as laptop or tablet computers or in wireless communication devices. As an example, the voltage regulator system 102 and the multi-host voltage regulator control system 104 can be implemented as separate systems, such as separate ICs, or can be implemented as a single system, such as in a common IC.

[0021] The multi-host voltage regulator control system 104 is communicatively coupled to each of the plurality of processors 106 via a respective plurality of signals COM_1 through COM_N, in a manner similar to as described in the example of FIG. 1. As an example, each of the signals COM_1 through COM_N can be communicated between the multi-host voltage regulator control system 104 and the

respective processors 106 via a Serial Voltage IDentification (SVID) bus. The multi-host voltage regulator control system 104 is also communicatively coupled to the voltage regulator system 102, demonstrated in the example of FIG. 3 as via a signal VR. The voltage regulator system 102 is configured to generate a processor voltage V_{CC} that is provided to each of the processors 106 to provide power to the processors 106. As an example, the voltage regulator system 106 can include one or more power supplies, with at least one of the power supplies being configured to generate the processor voltage V_{CC}.

[0022] The power management system 100 is therefore configured substantially similar to the power management system 10 in the example of FIG. 1. However, the functionality of the voltage regulator control system 12 in the example of FIG. 1 is distributed between the voltage regulator system 102 and the multi-host voltage regulator control system 104 in the power management system 100 in the example of FIG. 3. Specifically, the multi-host voltage regulator control system 104 can receive and process the power management requests provided from the processors 106, as well as issue alerts to the processors 106, via the signals COM_1 through COM_N. In response to the processing of the requests via the signals COM_1 through COM_N, the multi-host voltage regulator control system 104 can provide commands to the voltage regulator system 102 via the signal VR to increase or decrease the processor voltage V_{CC}. As a result, the voltage regulator system 102 can be configured substantially similar to a conventional voltage regulator system 102 that controls a processor voltage V_{CC} for a single processor, while the multi-host voltage regulator control system 104 includes all of the intelligence for managing the power of all of the processors 106.

[0023] In view of the foregoing structural and functional features described above, an example method will be better appreciated with reference to FIG. 4. While, for purposes of simplicity of explanation, the method of FIG. 4 is shown and described as executing serially, it is to be understood and appreciated that the method is not limited by the illustrated order, as parts of the method could occur in different orders and/or concurrently from that shown and described herein.

[0024] FIG. 4 illustrates an example of a method 150 for controlling a processor voltage that is provided to each of a plurality of processors. At 152, a

voltage increase request signal (*e.g.*, via a signal COM) is generated from a given one of the plurality of processors (*e.g.*, a processor 14) to increase the processor voltage (*e.g.*, the voltage V_{CC}) in response to the given one of the plurality of processors switching from a low power mode to an active mode. At 154, the processor voltage is increased via a voltage regulator control system (*e.g.*, the voltage regulator control system 12) in response to the voltage increase request signal. At 156, a voltage decrease request signal is generated from the given one of the plurality of processors to decrease the processor voltage in response to the given one of the plurality of processors switching from the active mode to the low power mode. At 158, the processor voltage is decreased via a voltage regulator control system in response to the voltage decrease request signal and in response to determining that a remaining plurality of processors are operating in the low power mode.

[0025] What have been described above are examples. It is, of course, not possible to describe every conceivable combination of components or methodologies, but one of ordinary skill in the art will recognize that many further combinations and permutations are possible. Accordingly, the invention is intended to embrace all such alterations, modifications, and variations that fall within the scope of this application, including the appended claims. As used herein, the term “includes” means includes but not limited to, the term “including” means including but not limited to. The term “based on” means based at least in part on. Additionally, where the disclosure or claims recite "a," "an," "a first," or "another" element, or the equivalent thereof, it should be interpreted to include one or more than one such element, neither requiring nor excluding two or more such elements.

CLAIMS

What is claimed is:

1. A voltage regulator control system communicatively coupled to each of a plurality of processors, the voltage regulator control system is to generate a processor voltage that is provided to each of the plurality of processors and to control a magnitude of the processor voltage based on receiving power management request signals that are provided from each of the plurality of processors.

2. The system of claim 1, wherein the voltage regulator control system comprises a plurality of voltage regulators, wherein one of the plurality of voltage regulators is to generate the processor voltage.

3. The system of claim 1, wherein the voltage regulator control system comprises a voltage regulator memory, wherein the voltage regulator control system is to designate respective registers of the voltage regulator that are each individually dedicated to each of the respective plurality of processors.

4. The system of claim 1, wherein the voltage regulator control system is to reduce the processor voltage in response to a power management request signal from one of the plurality of processors in response to each of a remaining plurality of processors operating in a low power mode, such that the processor voltage provides sufficient power to the remaining plurality of processors upon being reduced.

5. The system of claim 1, wherein each of the plurality of processors is to generate a request to the voltage regulator control system to decrease the processor voltage in response to switching from an active mode to a low voltage mode, and wherein the voltage regulator control system is to provide an alert signal to a respective one of the plurality of processors in response to receiving the request and being unable to reduce the processor voltage based on power required by another one of the plurality of processors.

6. The system of claim 1, wherein the voltage regulator control system is to provide an alert signal to each of a remaining plurality of processors in response to one of the plurality of processors issuing a request to the voltage regulator control system to one of increase and decrease the processor voltage.

7. The system of claim 1, wherein the voltage regulator control system comprises:

a multi-host voltage regulator control system that is communicatively coupled to each of the plurality of processors to transmit and receive power management commands to and from the plurality of processors;

a voltage regulator system communicatively coupled to the multi-host voltage regulator control system to generate and control the magnitude of the processor voltage based on receiving commands that are provided from the multi-host voltage control regulator system.

8. The system of claim 1, wherein the voltage regulator control system and the plurality of processors are to communicate via a Serial Voltage IDentification (SVID) bus.

9. An integrated circuit (IC) comprising the voltage regulator control system of claim 1.

10. A method for controlling a processor voltage that is provided to each of a plurality of processors, the method comprising:

generating a voltage increase request signal from a given one of the plurality of processors to increase the processor voltage in response to the given one of the plurality of processors switching from a low power mode to an active mode;

increasing the processor voltage via a voltage regulator control system in response to the voltage increase request signal;

generating a voltage decrease request signal from the given one of the plurality of processors to decrease the processor voltage in response to the given

one of the plurality of processors switching from the active mode to the low power mode; and

decreasing the processor voltage via a voltage regulator control system in response to the voltage decrease request signal and in response to determining that a remaining plurality of processors are operating in the low power mode.

11. The method of claim 10, further comprising providing an alert signal to the remaining plurality of processors in response to receiving each of the voltage increase request signal and the voltage decrease request signal.

12. The method of claim 10, further comprising maintaining a magnitude of the processor voltage in response to the voltage decrease request signal and in response to determining that at least one of the remaining plurality of processors is operating in the active mode.

13. A power management system comprising:

a plurality of processors, each of the plurality of processors being to switch between operation in an active mode and a low power mode;

a voltage regulator control system communicatively coupled to each of a plurality of processors, the voltage regulator control system to generate a processor voltage that is provided to each of the plurality of processors, and is further to increase a magnitude of the processor voltage in response to one of the plurality of processors switching to the active mode and to decrease the magnitude of the processor voltage in response to receiving one of the plurality of processors switching to the low power mode and based on determining that a remaining plurality of processors operates in the low power mode.

14. The system of claim 13, wherein the voltage regulator control system comprises a voltage regulator memory, wherein the voltage regulator control system is to designate respective registers of the voltage regulator memory that are each individually dedicated to each of the respective plurality of processors.

15. The system of claim 13, wherein the voltage regulator control system is to provide an alert signal to each of the remaining plurality of processors in response to the one of the plurality of processors issuing a request to the voltage regulator control system to one of increase and decrease the processor voltage.

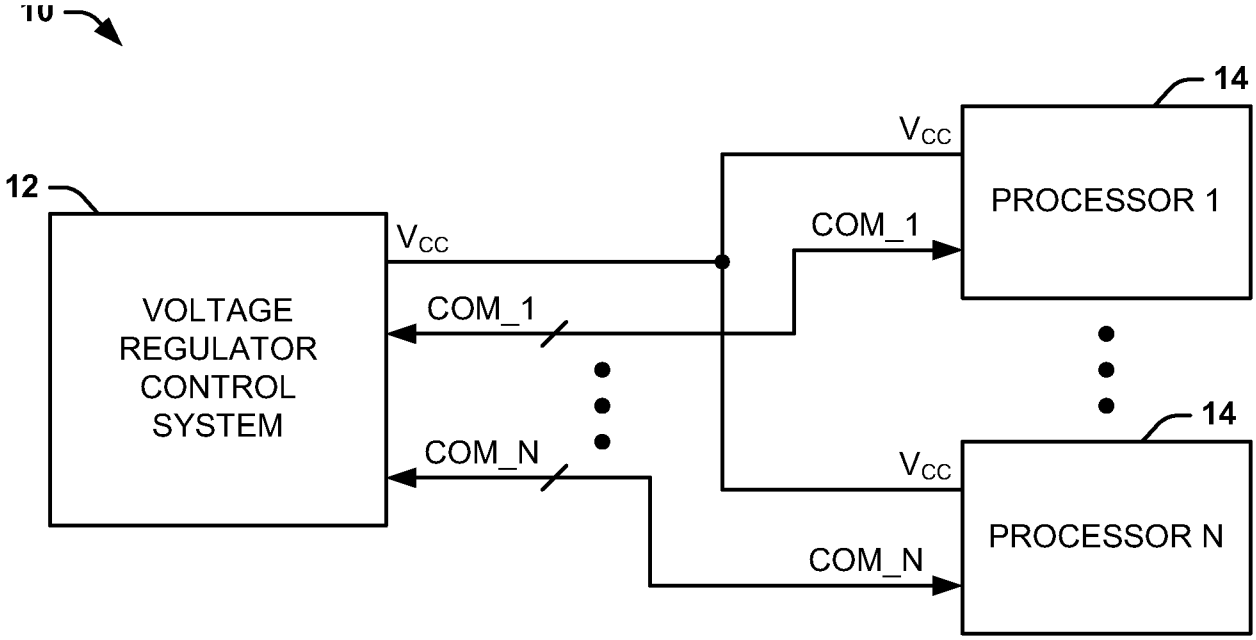

10
12
VOLTAGE REGULATOR CONTROL SYSTEM
V_{CC}
COM_1
COM_N
14
PROCESSOR 1
PROCESSOR N

FIG. 1

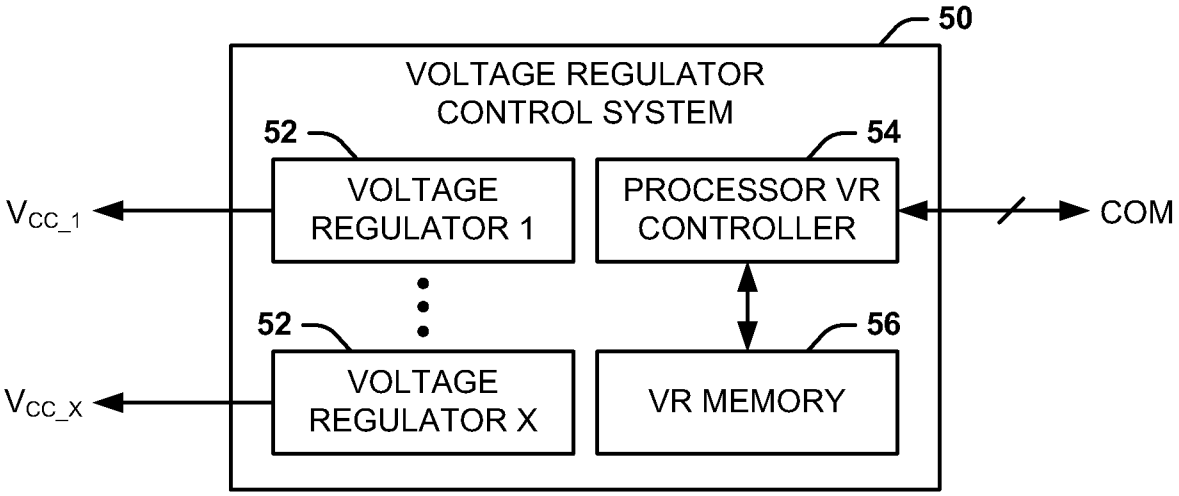

50
VOLTAGE REGULATOR CONTROL SYSTEM
52
VOLTAGE REGULATOR 1
52
VOLTAGE REGULATOR X
54
PROCESSOR VR CONTROLLER
56
VR MEMORY
V_{CC_1}
V_{CC_X}
COM

FIG. 2

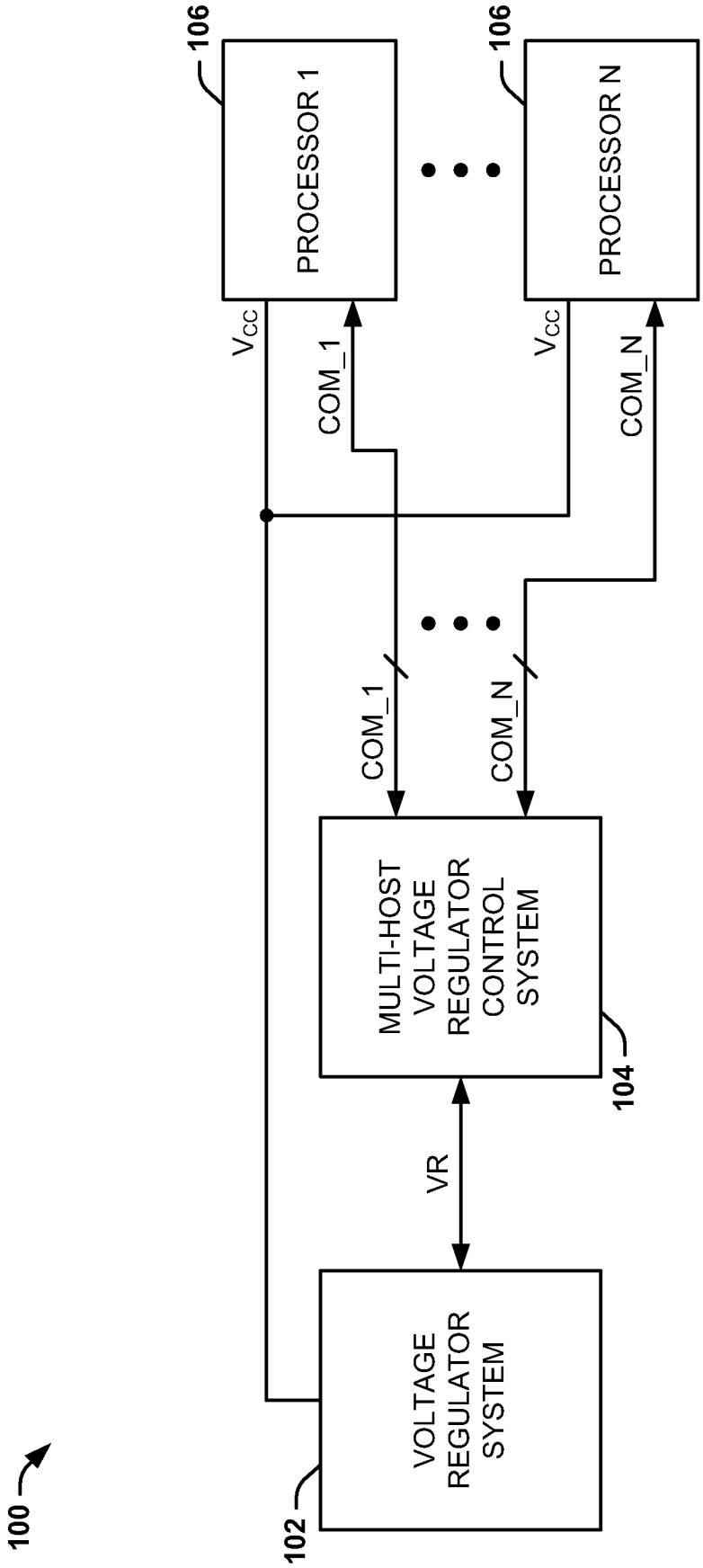

100
102
VOLTAGE REGULATOR SYSTEM
VR
104
MULTI-HOST VOLTAGE REGULATOR CONTROL SYSTEM
COM_1
COM_N
COM_1
COM_N
VCC
VCC
106
PROCESSOR 1
106
PROCESSOR N

FIG. 3

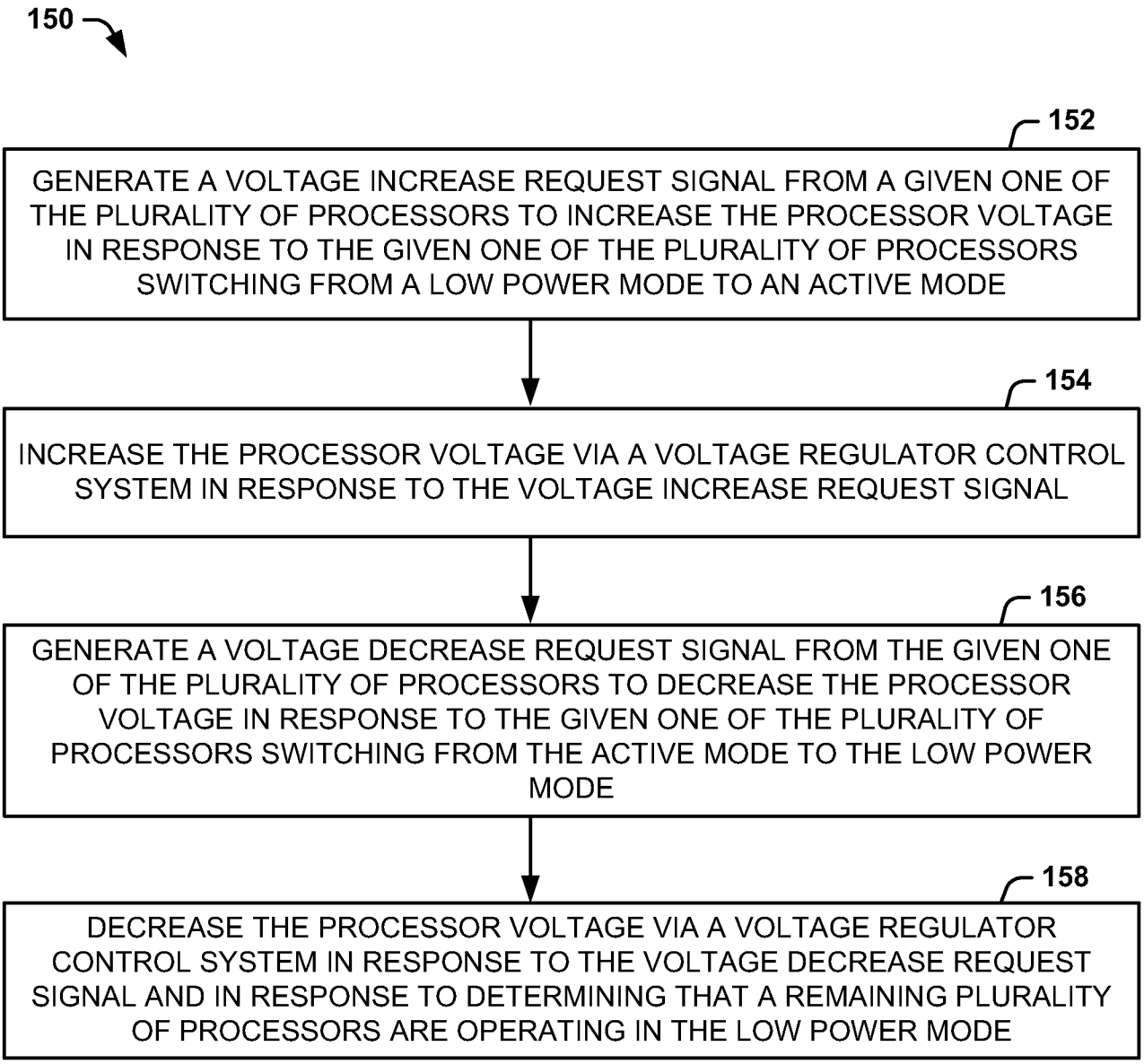

150
152
GENERATE A VOLTAGE INCREASE REQUEST SIGNAL FROM A GIVEN ONE OF THE PLURALITY OF PROCESSORS TO INCREASE THE PROCESSOR VOLTAGE IN RESPONSE TO THE GIVEN ONE OF THE PLURALITY OF PROCESSORS SWITCHING FROM A LOW POWER MODE TO AN ACTIVE MODE
154
INCREASE THE PROCESSOR VOLTAGE VIA A VOLTAGE REGULATOR CONTROL SYSTEM IN RESPONSE TO THE VOLTAGE INCREASE REQUEST SIGNAL
156
GENERATE A VOLTAGE DECREASE REQUEST SIGNAL FROM THE GIVEN ONE OF THE PLURALITY OF PROCESSORS TO DECREASE THE PROCESSOR VOLTAGE IN RESPONSE TO THE GIVEN ONE OF THE PLURALITY OF PROCESSORS SWITCHING FROM THE ACTIVE MODE TO THE LOW POWER MODE
158
DECREASE THE PROCESSOR VOLTAGE VIA A VOLTAGE REGULATOR CONTROL SYSTEM IN RESPONSE TO THE VOLTAGE DECREASE REQUEST SIGNAL AND IN RESPONSE TO DETERMINING THAT A REMAINING PLURALITY OF PROCESSORS ARE OPERATING IN THE LOW POWER MODE

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2012/034502

A. CLASSIFICATION OF SUBJECT MATTER

G06F 1/26(2006.01)i, G06F 1/32(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G06F 1/26; G06F 1/00; G06F 1/12; G06F 1/32; G06F 9/50

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: multicore, adjust, voltage, active, idle

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y A	US 7650518 B2 (JOSE ALLAREY et al.) 19 January 2010 see abstract, column 2, lines 45-55, claim 1, and figure 1	1-2,4,9,10,13 3,5-8,11-12,14-15
Y A	US 2009-0138737 A1 (DAEIK KIM et al.) 28 May 2009 see abstract, paragraph [0039], claim1, and figure 9	1-2,4,9,10,13 3,5-8,11-12,14-15
A	US 2009-0328055 A1 (PRADIP BOSE et al.) 31 December 2009 see abstreact, paragraphs [0061]-[0063], claims 1.	1-15
A	US 2011-0213991 A1 (ANDREW WOLFE et al.) 01 September 2011 see abstract, paragraphs [0011],[0013], claim 1, and figure 1	1-15

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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Information on patent family members

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