



- (51) International Patent Classification:
H01F 17/00 (2006.01)
- (21) International Application Number:
PCT/US2016/063081
- (22) International Filing Date:
21 November 2016 (21.11.2016)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
14/973,115 17 December 2015 (17.12.2015) US
- (63) Related by continuation (CON) or continuation-in-part (CIP) to earlier application:
US 14/973,115 (CON)
Filed on 17 December 2015 (17.12.2015)
- (71) Applicant: INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, California 95054 (US).
- (72) Inventors: LAMBERT, William; 2279 W Megan St, Chandler, Arizona 85224 (US). ROY, Mihir K.; 2734 West Highland Street, Chandler, Arizona 85224 (US). MANUSHAROW, Mathew J; 16667 S. 37th Place, Phoenix, Arizona 85048 (US). DENG, Yikang; 5000 W Chandler BLVD, CH2-205, Chandler, Arizona 85226 (US).
- (74) Agents: PERDOK, Monique M. et al.; SCHWEGMAN LUNDBERG & WOESSNER, P.A., P.O. Box 2938, Minneapolis, Minnesota 55402 (US).
- (81) Designated States (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.
- (84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU,

[Continued on next page]

(54) Title: HELICAL PLATED THROUGH-HOLE PACKAGE INDUCTOR

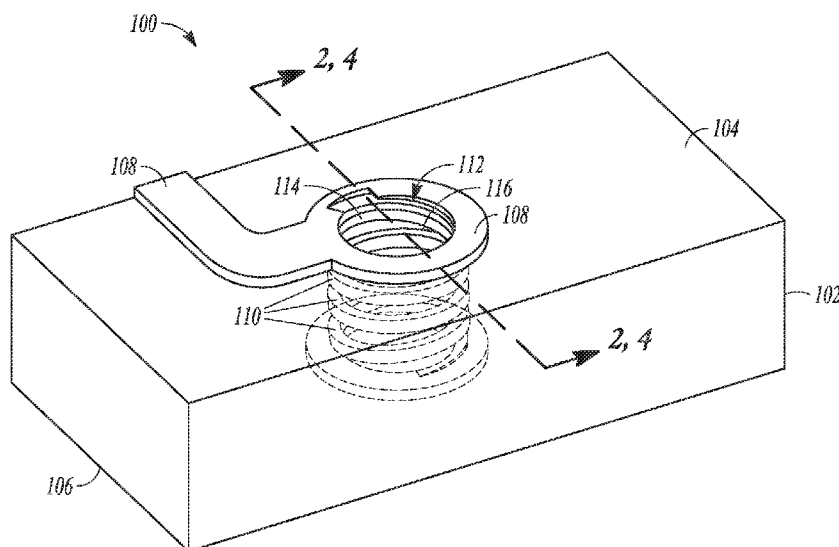


FIG. 1

(57) Abstract: Devices and methods including a through-hole inductor for an electronic package are shown herein. Examples of the through-hole inductor include a substrate including at least one substrate layer. Each substrate layer including a dielectric layer having a first surface and a second surface. An aperture included in the dielectric layer is located from the first surface to the second surface. The aperture includes an aperture wall from the first surface to the second surface. A conductive layer is deposited on the first surface, second surface, and the aperture wall. At least one coil is cut from the conductive layer and located on the aperture wall.



TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

HELICAL PLATED THROUGH-HOLE PACKAGE INDUCTOR

5

PRIORITY APPLICATION

[0001] This application claims the benefit of priority to U.S. Application
Serial No. 14/973,115, filed December 17, 2015, which is incorporated herein by
10 reference in its entirety.

TECHNICAL FIELD

[0002] This document pertains generally, but not by way of limitation, to
electronic packages, such as electronic packages including inductive elements.
15

BACKGROUND

[0003] Electronic packages, such as integrated circuit packages can
include an inductor. The inductor can be used in a circuit to reduce or increase
the voltage of a power supply to an operating voltage of the integrated circuit.
20 Voltage regulation components can be included in the integrated circuit package,
for instance, increase the power efficiency, or reduce the cost of the integrated
circuit as well as reduce the space occupied by the voltage regulator. Some
electronics packages include inductors on the bottom of the package (e.g., the
bottom buildup layers of a substrate) for voltage regulation. The surface area of
25 the package can be limited as there is demand for smaller integrated circuits. In
particular, the surface area on the bottom of the integrated circuit, the side of the
integrated circuit that mounts to a circuit board, for example, can be limited due
to the need for surface mount leads, ball grid arrays, or the like. In some
examples, a flat circular spiral inductor is included in the package for voltage
30 regulation. The flat circular spiral inductor can require a large surface area on the
package. Additionally, the flat circular spiral inductor can be limited to
producing low inductance values and can be difficult to scale in larger integrated
circuit packages. In some examples, inductor windings can be located on a
plurality of copper layers within a substrate of the package. For instance, each

winding can be located on a single layer of the substrate and connected to one or more adjacent windings by a via (i.e., an electronics trace inductor). This type of inductor can occupy one or more copper layers of the substrate and sometimes many layers in order to form a plurality of windings.

5

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] In the drawings, which are not necessarily drawn to scale, like numerals may describe similar components in different views. Like numerals having different letter suffixes may represent different instances of similar components. The drawings illustrate generally, by way of example, but not by way of limitation, various embodiments discussed in the present document.

- Figure 1 is a perspective view of a through-hole inductor according to an example.
- 15 Figure 2 is a cross section view of the through-hole inductor according to an example.
- Figure 3 is a perspective cross section view of an exemplary electronic package including a through-hole inductor within a substrate including a plurality of electrical contacts.
- 20 Figure 4 is an example of the through-hole inductor including a magnetic core located within an aperture of the through-hole inductor.
- Figure 5 is a diagram of a method of making the through-hole inductor according to an example.
- Figure 6 shows an exemplary layout of a plurality of through-hole inductors included in an electronic package.
- 25 Figure 7 is a diagram of an exemplary electronic device including the through-hole inductor.

DETAILED DESCRIPTION

30 [0005] The following description and the drawings sufficiently illustrate specific embodiments to enable those skilled in the art to practice them. Other embodiments may incorporate structural, logical, electrical, process, and other changes. Portions and features of some embodiments may be included in, or

substituted for, those of other embodiments. Embodiments set forth in the claims encompass all available equivalents of those claims.

[0006] Electronic packages, such as Integrated Circuits (ICs) including Integrated Voltage Regulators (IVRs) include one or more inductors (e.g., a high
5 frequency inductor). In some examples, the inductor can include an Air Core Inductor (ACI), such as a surface mount ACI, a planar spiral ACI, or an inductor including coils located on one or more layers of a substrate and interconnected by vias. In some examples, the ACI includes a dielectric core. For instance a dielectric core having the same or similar relative magnetic permeability as air
10 (i.e., a magnetic permeability of about 1.0). Placing the ACI can be difficult in some electronic packages as a result of limited surface area on the placement side of the electronic package. For instance, Land Grid Array (LGA) or Ball Grid Array (BGA) contacts may require specific locations on the placement side (contact side) of the electronic package. Furthermore, signal routing (e.g., input
15 and output signals, power, other electrical signals) may also be required on the placement side of the electronic package. In some electronic packages, there may be insufficient surface area on the placement side of the electronic package for the ACI. Moreover, ACIs can have low inductance values and are difficult to scale for packages including a die having a 14 nm feature size or less. For
20 instance, an area available to construct the ACI within the substrate of the electronics package including a die having a 14 nm feature size can be reduced as compared to a corresponding area in an electronic package including a die of greater feature size (e.g., 22 nm or larger feature size).

[0007] The device and method discussed herein can include an inductor,
25 such as a through-hole inductor, formed within a Plated Through-Hole (PTH) of a substrate or a substrate layer. A conductive layer (e.g., copper) within the PTH can be shaped into a helical structure by a coil cutting bit configured to produce the helical structure. In one or more examples, the through-hole inductor can be an ACI. Optionally, the through inductor can be filled with a material including
30 magnetic particles suspended therein to form a Magnetic Core Inductor (MCI), such as a through-hole magnetic core inductor. The magnetic core can increase the inductance value of the through-hole inductor. In some examples, the MCI

can include a magnetic core having a magnetic permeability including, 3, 5, 100, 200, or the like.

[0008] Figure 1 shows a perspective view of a through-hole inductor 100 according to an example. The through-hole inductor 100 can include a dielectric layer 102. A first dielectric layer can include a first surface 104 and a second surface 106. The second surface 106 can be located on the opposing side of the first surface 104. An aperture 112 can be located within the dielectric layer 102, for instance to form a passage in the dielectric layer 102. The aperture 112 can be formed by any number of processes including, but not limited to, drilling, laser cutting, punching, etching, molding the aperture 112 into the dielectric layer 102, or the like. The aperture 112 can include an aperture wall 114 extended from the first surface 104 to the second surface 106 of the dielectric layer 102. In an example, the aperture can include a diameter of 100, 250, 400, 700, 1000 microns, or the like. A conductive layer 108 can be deposited on the dielectric layer 102. For instance the conductive layer 108 can be deposited on all or a portion of the first surface 104, the second surface 106, and the aperture wall 114. For instance, the conductive layer can include a plated through-hole in the dielectric layer 102.

[0009] The dielectric layer 102 can include dielectric properties to prevent electrical conductivity between one or more conductive layers or components. In an example, the dielectric layer 102 can be substantially rigid, such as a printed circuit board. For instance, the material of the dielectric layer 102 can include glass-epoxy (e.g., FR-4, CEM-3, G-10, or other), Bismaleimide-Triazine epoxy, silica-filled epoxy, Cyanate Ester, Polyimide, Polytetrafluoroethylene (PTFE), Mylar (Biaxially-oriented polyethylene terephthalate), polyester film, polyethylene terephthalate (PET), beryllium oxide, aluminum, ceramic, porcelain, mica, glass, glass-cloth, prepreg, other metal oxides, other plastics, or the like. The thickness of the dielectric layer 102 can include, but is not limited to, 0.50 mm, 1.0 mm, 3.0 mm, 10.0 mm, or the like.

[0010] In an example, the dielectric layer 102 can include a flexible material, such a dielectric layer 102 of a flexible printed circuit. Optionally, a stiffener can support the flexible printed circuit for mechanical support. For instance, the stiffener can be located at, adjacent to, or around the location of the

through-hole inductor 100. Mechanical support can reduce the risk of damage to the conductive layer 108. The flexible printed circuit materials can include polyester, polyethylene terephthalate (PET), polyimide (PI), polyethylene naphthalate (PEN), Polyetherimide (PEI), fluoropolymers (e.g., FEP), copolymers, or the like. The thickness of the flexible printed circuit dielectric layer 102 can include 0.012 mm to 1.3 mm.

[0011] The conductive layer 108 can include, but is not limited to, leaded solder (tin/lead), lead free solder (tin/copper), Electroless Nickel Immersion Gold (ENIG)(nickel, copper, gold), soft gold, hard gold, immersion silver, immersion gold, immersion tin, conductive ink, or the like. In an example, the conductive layer 108 can be covered with an organic surface protectant to reduce oxidation. In an example, the conductive layer can include a Copper Clad Laminate (CCL). In an example, the conductive layer on the first surface 104 and the second surface 106 can include a rolled conductive material (e.g., copper) or an electroplated conductive material as previously described. In an example, the conductive layer 108 on the aperture wall 114 can include an electro-deposited or electroplated conductive material. The conductive layer 108 can include a total thickness including, but not limited to, 8.0–250.0 microns. In an example, the conductive layer can be 36 microns thick.

[0012] An example at least one coil 110 can be located on the aperture wall 114. As shown in the example of Figure 1, the through-hole inductor 100 can include a plurality of coils 110, such as a plurality of coils 110 arranged in a helical shape. Each coil 110 can include one or more revolutions around the aperture 112. The helical shape can include a first end on the first surface 104 and a second end on the second surface 106. In an example, the aperture 112 can include two or more through-hole inductors, 100 for instance, in a double-helix shape. In other words, the conductive layer 108 located on the first surface 104 can include two independent electronic circuits (e.g., a first circuit and a second circuit). The conductive layer 108 located on the second surface 106 can include respective portions of the first and second circuits of the conductive layer 108 located on the first surface. The first electronic circuit can include a first coil 110 encircling the aperture wall 114, for instance, in at least one revolution of the aperture 112 from the first circuit of the first surface 104 to the first circuit of the

second surface 106. Likewise, the second electronic circuit can include a second coil 110 encircling the aperture wall 114, for instance, in at least one revolution of the aperture 112 from the second circuit of the first surface 104 to the second circuit of the second surface 106. The through-hole inductor 100 can be
5 configured to include one or more coils 110 including one or more turns (e.g., revolutions) that occupy a relatively small amount of surface area (e.g., area on the first surface 104 or second surface 106) on the dielectric layer 102 as a result of the location of the coils 110 within the aperture 112. The helical shape of the one or more coils 110 can also generate higher inductance values than planar
10 coils (e.g. coils that lie on a flat surface and revolve around a coil center with an increasing radius).

[0013] In an example, the coil 110 can be cut from the conductive layer 108 located on the aperture wall 114. An entire thickness of the conductive layer 108 can be removed (e.g., cut) from the aperture wall 114 to form the one or
15 more coils 110. The coil 110 cut from the conductive layer 108 can be identifiable by marks left on the coil 110 by the cutting tool. These identifiable marks can include, but are not limited to, chatter marks, feed marks, residual stress marks, work hardening, phase transformation, micro cracks, hanging chips, surface roughness, or the like. The conductive layer 108 located on the
20 first surface 104, the second surface 106, or both can include an entrance or exit feature at the beginning or end of the coil 110 where a cutting bit started or ended a cutting path to form the one or more coils 110.

[0014] Figure 2 depicts an exemplary cross section of the through-hole inductor 100 (located at 2-2 shown in Figure 1). As previously discussed, the
25 through-hole inductor 100 includes the dielectric layer 102. The conductive layer 108 is shown on the top surface 104, the bottom surface 106, and on the aperture wall 114. The conductive layer 108 is shown as a solid layer in Figure 2 for the purposes of illustration. The conductive layer 108 can be etched (or otherwise arranged) into a more complex layout design in other examples.

30 [0015] One or more coils 110 can be located on the aperture wall 114. For instance, the one or more coils 110 can encircle the aperture wall from the conductive layer 108 on the first surface 104 to the conductive layer 108 on the second surface 106 in at least one revolution of the aperture 108. The one or

more coils 110 can be cut from the conductive layer 108 located on the aperture wall 114. The example of Figure 2 shows at least two revolutions of the coil 110 located along the aperture wall 114. In an example, the coil 110 can include, but is not limited to, a helical shape. For instance, the coil 110 can include a
5 continuous helical shape extended from either the first surface 104 or the second surface 106 or from the first surface 104 to the second surface 106. The helical shape can include, but is not limited to, a pitch of 100, 160, 220, 260, 300, 400, 600 μm , or the like. The coil 110 can include a width including, but not limited to, 50, 100, 150, 200, 400 μm , or other width. In an example, the coil 110 can
10 include a shape with a non-uniform pitch from the first surface 104 to the second surface 106. For instance, a first coil 110 can be located partially around the aperture wall 114 at a first distance from the first surface 104. A second coil 110 can be connected to the first coil 110. The second coil 110 can include a second distance from the first surface 104. In an example, the through-hole inductor 100
15 can include a plurality of coils 110, each including a distance from the first surface 104 that is staggered from an adjacent coil 110. Stated another way, the one or more coils 110 can be arranged in a step-wise progression extended from at least the first surface 104, the second surface 106, or both.

[0016] The coil 110 can be configured to generate an electromagnetic
20 flux as a result of a current flowing through the one or more coils 110 of the through-hole inductor 100. For instance, the through-hole inductor 100 can include an Air Core Inductor (ACI). In some examples, the through-hole inductor 100 can be incorporated into a buck converter, voltage regulator, Integrated Voltage Regulator (IVR), radio frequency filter, phased-locked
25 looped (PLL) filter, or the like. For instance, the through-hole inductor 100 can include an input voltage and an input current. An output voltage of the through-hole inductor 100 can be maintained within a range of output voltages. For instance, the output voltage of the through-hole inductors can be less than 0.9 volts, 1.8 volts, or other threshold voltage. The output current can fluctuate
30 according to the demand of the circuit. In an example, the output current can increase, decrease, or remain constant according to a feedback loop within the circuit. A current 204 flowing through the one or more coils 110 can generate an electromagnetic flux 202 in a direction perpendicular to the one or more coils

110. In an example, the through-hole inductor 100 can include a Quality Factor (Q-factor) of 5, 8, 10 or greater (at 100 MHz). In an example, the through-hole inductor 100 can include inductance values (AC) of 1, 2, 3, 5, 7 nanohenry, or the like.

5 [0017] Figure 3 depicts an example of an electronic package 300, such as an electronic package 300 including the through-hole inductor 100. The electronic package 300 can include, but is not limited to, a processor, microprocessor, memory module, radio-frequency circuit, radio-frequency filter, PLL filter, other type of filter, or the like. In an example, the electronic package
10 300 can include an IVR. The IVR can include the through-hole inductor 100. In an example, the IVR can include a buck converter or other type of voltage regulator with an inductive component, such as the through-hole inductor 100. Locating the inductive component within the electronic package 300, can among other things, improve the power efficiency, reduce the size, reduce the cost,
15 mitigate voltage ripple of the electronic package 300, or any combination thereof. In an example, the electronic package 300 can be included in an electronic device (as shown in Figure 7 and described herein), such as a computer, mobile phone, radio, game console, or other electronic device. The electronic package 300 can be coupled to the electronic device. For instance, the
20 electronic package 300 can include a substrate 302. The substrate 302 can include one or more electrical contacts 308 in electrical communication with a circuit board of the electronic device.

[0018] In the example shown in figure 3, the substrate 302 can include one or more substrate layers, such as a first substrate layer 310 and one or more
25 secondary substrate layers 312. Each substrate layer can include a dielectric layer 102. As previously described, the dielectric layer 102 can include the first surface 104 and the second surface 106. Each substrate layer 310,312 can include at least one conductive layer 108 on the first surface 104, second surface 106, or both. Optionally, the substrate 302 can include a plurality of substrate
30 layers, such as 2, 4, 6, 8, or more substrate layers. An example of the substrate 302 including three substrate layers (e.g., a first substrate layer 310 and two secondary substrate layers 312) is shown in Figure 3. In an example, the substrate 302 can include a sequential layer build-up construction. For instance,

the first substrate layer 310 can be a substrate core. The substrate core can include materials including, but are not limited to, glass-cloth, prepreg (resin impregnated fiberglass), or the like. One or more substrate layers can be laminated on one or both sides of the substrate core (e.g., a sequential layer build-up). In an example, the first substrate layer 310, the second substrate layer 312, or any substrate layer can include, but is not limited to, the substrate materials previously described herein. The first substrate layer 310 can include at least one through-hole inductor 100. The one or more second substrate layers 310 (e.g., build-up layers) can be located subjacent or superjacent to the first substrate layer 310. At least one of the secondary substrate layers 312 can include one or more electrical contacts 308, such as an exposed conductive pad of the conductive layer 108 or an electrical contact 308 placed on the conductive layer 108. In an example, one of the secondary substrate layers 312 (e.g., including the electrical contacts 308) can be referred to as a bottom build-up layer. The electrical contacts 308 can include any type of electrical contact including, but not limited to, a Ball Grid Array (BGA), Land Grid Array (LGA), Pin Grid Array (PGA), surface mount, through-hole, or the like. The through-hole inductor 100 can be located on a single substrate layer, such as within the substrate core or other substrate layer. For instance, one or more coils 110 can encircle the aperture 112 in at least one revolution within the thickness of a single substrate layer. In an example, one or more coils 110 can encircle the aperture 112 in a plurality of revolutions within the thickness of a single substrate layer. In an example, the through-hole inductor 100 can include a plurality of coils 110. Each coil 110 can include an equal diameter and can be aligned along the axis of the aperture 112 and aperture wall 114 (e.g., in a helical shape). Arranging the coils 110 to encircle a common cylindrical axis can increase the inductance value of the through-hole inductor 100, for instance, by increasing the number of turns of the coil 110 and accordingly the amount of electromagnetic flux generated.

[0019] The electronics package 300 can include a die 304. The die 304 can include a circuit, such as an integrated circuit. In an example, the die 304 can be fabricated from a silicon wafer, gallium arsenide, or other semiconductor. The die 304 can include, but is not limited to, a processor, microprocessor, random

access memory, radio, arithmetic unit, any combination thereof, or the like. The die 304 can be in electrical communication with one or more conductive layers 108 via an electrical connection with one or more conductive layers 108. The electrical connection can include, but is not limited to, Ball Grid Array (BGA),
5 Land Grid Array (LGA), Pin Grid Array (PGA), wire bonding, surface mount, through-hole, or other type of connection. In an example, the die 304 can include a controlled collapse chip connection (e.g., a flip chip construction). The die 304 can be in electrical communication with the electronic device via one or more conductive layers 108. For instance, the die 304 can be electronically
10 coupled to the electronic device by one or more electrical contacts 308. In an example, one or more components of the IVR can be located on the die 304. For instance, capacitors or resistors of the IVR can be located on the die 304. The through-hole inductor 100 can be located in the substrate 302. Locating some of the components of the IVR on the die 304 can reduce the size of the electronic
15 package 300 or the electronic device (described further herein), for example, a motherboard within the electronics device. In an example, the electronic package can include a cover 306. The cover 306 can encapsulate the die 304 and the top surface 104 of the substrate 302 as shown in Figure 3. The cover 306 can include an overmold or encapsulant material that includes, but is not limited to, a
20 thermoset, epoxy, thermoplastic, polymer, or the like.

[0020] In an example, the through-hole inductor 100 can be located on a substrate layer that is superjacent to the bottom build-up layer (e.g., the bottom secondary layer 312 as shown in Figure 3) as previously described. For instance, the through-hole inductor 100 can be located on the first substrate layer 310,
25 such as the substrate core. Where the substrate 302 includes one or more layers, such as a sequential layer build-up, the location of the through-hole inductor 100 avoids interfering with trace routing on the conductive layers 108 located within the build-up. For instance, the through-hole inductor 100 can be located within the substrate core, and accordingly, the build-up (e.g., secondary layers 312) can
30 include a greater area for trace routing. In an example, locating the through-hole inductor 100 on the first substrate layer 310 avoids routing difficulties around components that require a specific position on the substrate 302, such as BGA or LGA contacts. The location of the through-hole inductor 100 can also avoid

input-output (IO) routing and/or placement of decoupling components (e.g., capacitors and/or resistors).

[0021] Figure 4 is a cross section of a through-hole inductor 400 including an inductor core, such as a magnetic core 402. The magnetic core can be located within the aperture 112. In an example, the magnetic core 402 can include magnetic particles suspended or dispersed within a carrier material. The magnetic core 402 can be applied during the manufacture of the substrate 302. The magnetic particles can include, but are not limited to, a material such as iron powder, manganese-zinc ferrite, molybdenum permalloy powder, nickel-zinc ferrite, sendust, silicon steel, or the like. In an example, the magnetic core 402 can include magnetic nanoparticles. The magnetic core 402 can include a magnetic permeability of 3, 5, 100, 200, or the like. The magnetic core 402 can increase the inductance values of the through-hole inductor 100. In an example, the magnetic core 402 can surround a portion of the one or more coils 110. For instance, where the magnetic core 402 is located between the one or more coils 110, the reluctance to the electromagnetic field surrounding the coil 110 is reduced. Accordingly, the electromagnetic flux 202 can be increased. In other words, the magnetic core 402 includes a lower reluctance to the electromagnetic field than the substrate 302 or air gap. In an example, the magnetic core 402 can include a slug of material. For instance, the slug of material can be inserted into the aperture 112.

[0022] Figure 5 shows a diagram of an exemplary technique 500 for making the through-hole inductor 100 previously described herein and shown for instance in Figures 1–4. In describing the technique 500, reference is made to one or more components, features, functions, and steps previously described herein. Where convenient, reference is made to the components, features, steps and the like with reference numerals. Reference numerals provided are exemplary and are nonexclusive. For instance, features, components, functions, steps, and the like described in the technique 500 include, but are not limited to, the corresponding numbered elements provided herein. Other corresponding features described herein (both numbered and unnumbered) as well as their equivalents are also considered.

[0023] At 502, a dielectric layer 102 can be provided with a first surface 104 and a second surface 106 as previously described herein. For instance, the first surface 104 and the second surface 106 can be located on opposing sides of the dielectric layer 102. In an example, the dielectric layer 102 can include a
5 substrate core, such as a glass-cloth core, prepreg core, or the like. The core can include a thickness including, but not limited to, 100, 400, 700, 1000 microns or the like.

[0024] At 504, the dielectric layer 102 can be drilled from the first surface 104 to the second surface 106 to form an aperture 112 in the first surface
10 104 and the second surface 106. The aperture 112 can include an aperture wall 114 from the first surface 104 to the second surface 106. In an example, the aperture 112 can be drilled with a drill bit including, but not limited to, a high-speed drill bit, high-speed steel drill bit, carbide drill bit, tungsten carbide drill bit, polycrystalline diamond drill bit, or the like. In an example, an automated
15 drilling machine can perform the drilling operation. The automated drilling machine can include a processor with instructions thereon for drilling one or more apertures 112 at one or more locations within the dielectric layer 102. In some examples, the aperture 112 can be drilled by a laser, formed by a punch, or molded into the dielectric layer 102, or other aperture forming process.

20 [0025] At 506, a conductive layer 108 can be deposited on the first surface 104, second surface 106, and the aperture wall 114. For instance, the conductive layer 108 can be deposited by an electroplating process. The conductive layer 108 can include, but is not limited to, leaded solder (tin/lead), lead free solder (tin/copper), Electroless Nickel Immersion Gold (ENIG)(nickel,
25 copper, gold), soft gold, hard gold, immersion silver, immersion gold, immersion tin, conductive ink, or the like. In an example, the conductive layer 108 can be covered with an organic surface protectant to reduce oxidation.

[0026] At 508, a portion of the conductive layer 108 can be cut through the entire thickness of the conductive layer 108 to form one or more coils 110 on
30 the aperture wall 114. Stated another way, the conductive layer 108 can be removed from the aperture wall 114 to form at least one coil 110. The coil 110 can encircle the aperture wall 114 in at least one revolution from the first surface 104 to the second surface 106. In the example, of Figures 1–4 the coils 110 can

include a helical shape. A coil cutting bit can be used to cut (i.e., remove) the conductive layer 108 from the aperture wall 114. Cutting the portion of the conductive layer 108 on the aperture wall 114 with the coil cutting bit can include rotating and translating the coil cutting bit in a sequence along a path
5 from the first surface 104 to the second surface 106 thereby removing the conductive layer 108 on the aperture wall 114. Cutting the portion of the conductive layer 108 can further include rotating and translating the coil cutting bit in a reverse sequence along the path to withdrawal the coil cutting bit from the aperture 112. For instance, the sequence can include a helical path, such as to
10 form coils 110 including the helical shape. Other shapes are also possible, for instance, a first coil can be substantially parallel with the first surface 104 or second surface 106 and including a step at the start and/or the end of the first coil to connect with one or more adjacent coils 110.

[0027] In an example, the coil cutting bit can be configured to produce
15 the shape of the coil 110. The coil cutting bit can include, but is not limited to, a twist bit or other configuration of drill bit. In an example, the coil cutting bit can include a bit with one or more teeth having a larger diameter than the shank of the coil cutting bit. For instance, the teeth can have a diameter equal to or exceeding the diameter of the aperture 112. The shank of the coil cutting bit can
20 be equal to or less than the diameter of the copper layer 108 located on the aperture wall 114. In an example, the coil cutting bit can include a geometry that matches the shape of the coil 110. As previously discussed with regards to the drill bit used to form the aperture 112, the coil cutting bit can include, but is not limited to, a high-speed drill bit, high-speed steel drill bit, carbide drill bit,
25 tungsten carbide drill bit, polycrystalline diamond drill bit, or the like. In an example, the automated drilling machine can perform the drilling operation. The automated drilling machine can include a processor with instructions thereon for cutting a portion of the conductive layer 108 on the one or more aperture walls 114 to form one or more coils 110 on the aperture wall 114. In an example, the
30 automated drilling machine can be programmed to rotate and translate the one or more cutting edges of the coil cutting bit in the sequence along the path from the first surface 104 to the second surface 106 thereby removing the conductive layer 108 on the aperture wall 114. The automated drilling machine can be

programmed to rotate and translate the coil cutting bit in the reverse sequence along the path to withdrawal the coil cutting bit from the aperture 112. In an example, the coil 110 cut from the conductive layer 108 can be identifiable by marks left on the coil 110 by the coil cutting tool. These identifiable marks can include, but are not limited to, chatter marks, feed marks, residual stress marks, work hardening, phase transformation, micro cracks, hanging chips, surface roughness, or the like.

[0028] In an example, the technique 500 can further include locating a magnetic core 402 within the aperture 112. The magnetic core 402 can be deposited within the aperture 112. For instance, the magnetic core 402 can include magnetic particles suspended within a carrier, including but not limited to, a flux, polymer, epoxy material, or the like. For instance, the magnetic particles can include, but are not limited to, a material such as iron powder, manganese-zinc ferrite, molybdenum permalloy powder, nickel-zinc ferrite, sendust, silicon steel, or the like. In an example, the magnetic core 402 can include magnetic nanoparticles. The magnetic core 402 can be applied to the substrate layer and into the aperture 112 by injecting the magnetic core 402 from a nozzle (e.g., an inkjet printing head) or spreading the material of the magnetic core 402 (e.g., with a squeegee) over a stencil with an opening over the aperture 112. In an example, the magnetic core 402 can include a solid slug of material, such as ferrite, manganese-zinc ferrite, molybdenum permalloy, nickel-zinc ferrite, silicon steel, or the like. The slug can be inserted into the aperture 112 by a pick and place machine or by hand in some examples.

[0029] In an example, a second substrate layer (e.g., second substrate layer 312) can be coupled to (e.g., applied to) the first substrate layer 310. For instance, a secondary dielectric layer can be laminated over the conductive layer 108 located on the first surface 104 or the second surface of the first dielectric layer 102. An additional conductive layer 108 can then be electro-deposited over the secondary dielectric layer, forming a secondary substrate layer 312. The conductive layer 108 can be etched to form a pattern of traces therein, for instance, into an electrical circuit layout design. In an example, the one or more secondary substrate layers 312 can be laminated symmetrically on either side of

the first substrate layer 310 (e.g., the core). In other words, a build-up can be formed on the core using the sequential layer build-up process.

[0030] In an example, the through-hole inductor 100 can be located on the first substrate layer 310. For instance, the dielectric layer 102 of the first substrate layer 310 is drilled and the second substrate layer 312 does not include a through-hole inductor 100. In an example, where the first substrate layer 310 includes the core, the core can be drilled and the through-hole inductor 100 can be formed therein. The second substrate layer 312 can be laminated on the first substrate layer 310, such as bonded to the first substrate layer 310 by one or more of pressure, heat, adhesive, or other lamination or additive process. The one or more conductive layers 108 on either side of the second substrate layer 312 can include signal traces (e.g., printed circuits). In an example, the second or subsequent layers can be a build-up or a bumpless build-up construction. The technique 500 can further comprise attaching at least one electrical contact 308 to the substrate 302. For instance, the electrical contact can be located on the placement side of the electronic package 300. The electrical contact 308 can be in electrical communication with at least one through-hole inductor 100.

[0031] The through-hole inductor 100 resulting from the technique 500 can be operative to generate electromagnetic flux through the aperture 112 in response to the application of a voltage differential between the conductive layer 108 located on the first surface 104 and the conductive layer 108 located on the second surface. In other words, the through-hole inductor 100 can generate an electromagnetic flux through the aperture 112 in response to a voltage differential across the one or more coils 110. The technique 500 can further include incorporating the through-hole inductor 100 in an electrical circuit, such as an electrical circuit configured as a IVR, a switching power regulator, a processor, microprocessor, memory module, radio-frequency circuit, radio-frequency filter, PLL filter, other type of filter, or the like.

[0032] Figure 6 depicts an exemplary layout 600 of a plurality of through-hole inductors 100 on a substrate 302. In the example shown in Figure 6, the substrate 302 can include six or more through-hole inductors 100. The through-hole inductors 100 can be located within the keep-in zones of the substrate 302 to avoid thin walls along the edges of the substrate 302 and

possible damage during depanelization. In the example, of Figure 6, the through-hole inductors 100 can include an aperture 112 having a diameter of 250 microns. Three or more plated through-holes 602 can be included in the substrate 302. The plated through-holes 602 can be located between the through-hole inductors 100, for instance, to maximize the thickness of substrate 302 between each of the plated through-holes 602 and the through-hole inductors 100. In an example, the plated through-holes 602 can be vias connecting one or more conductive layers 108. The layout 600 allows for more area to place input voltage (V_{in}) decoupling capacitors on the electronic package 300. For instance, the through-hole inductors 100 can be located in the first substrate layer 310 and accordingly, decoupling components can be placed on the second substrate layer 312 or other substrate layers. As a result of the location of the through-hole inductor 100 within the first substrate layer 310, the number of additional substrate layers (e.g., layers of the sequential layer build-up) can be reduced. In an example, the second substrate layer 312 can include power distribution components or traces instead of one or more inductors.

[0033] An example of an electronic device (e.g., electronic system) using the through-hole inductor 100 and/or the electronic package 300 as described in the present disclosure is included to show an example of a higher level device application for the present invention. Figure 7 is a block diagram of an electronic device 700 incorporating at least one through-hole inductor 100 and/or method in accordance with at least one embodiment of the invention. Electronic device 700 is merely one example of an electronic system in which embodiments of the present invention can be used. Examples of electronic devices 700 include, but are not limited to personal computers, tablet computers, mobile telephones, game devices, MP3 or other digital music players, etc. In this example, electronic device 700 comprises a data processing system that includes a system bus 702 to couple the various components of the system. System bus 702 provides communications links among the various components of the electronic device 700 and can be implemented as a single bus, as a combination of busses, or in any other suitable manner.

[0034] An electronic assembly 710 is coupled to system bus 702. The electronic assembly 710 can include any circuit or combination of circuits. In

one embodiment, the electronic assembly 710 includes a processor 712 which can be of any type. As used herein, “processor” means any type of computational circuit, such as but not limited to a microprocessor, a microcontroller, a complex instruction set computing (CISC) microprocessor, a reduced instruction set computing (RISC) microprocessor, a very long instruction word (VLIW) microprocessor, a graphics processor, a digital signal processor (DSP), multiple core processor, or any other type of processor or processing circuit.

[0035] Other types of circuits that can be included in electronic assembly 710 are a custom circuit, an application-specific integrated circuit (ASIC), or the like, such as, for example, one or more circuits (such as a communications circuit 714) for use in wireless devices like mobile telephones, personal data assistants, portable computers, two-way radios, and similar electronic systems. The IC can perform any other type of function.

[0036] The electronic device 700 can also include an external memory 720, which in turn can include one or more memory elements suitable to the particular application, such as a main memory 722 in the form of random access memory (RAM), one or more hard drives 724, and/or one or more drives that handle removable media 726 such as compact disks (CD), flash memory cards, digital video disk (DVD), and the like.

[0037] The electronic device 700 can also include a display device 716, one or more speakers 718, and a keyboard and/or controller 730, which can include a mouse, trackball, touch screen, voice-recognition device, or any other device that permits a system user to input information into and receive information from the electronic device 700.

[0038] Each of these non-limiting examples can stand on its own, or can be combined in various permutations or combinations with one or more of the other examples. To better illustrate the method and apparatuses disclosed herein, a non-limiting list of embodiments is provided here:

[0039] Example 1 can include a through-hole inductor for an electronic package including, a substrate including at least one substrate layer, each substrate layer including a dielectric layer having a first surface and a second surface opposing the first surface. The through-hole inductor of example 1 can

further include an aperture in at least one dielectric layer located from the first surface to the second surface, the aperture including an aperture wall from the first surface to the second surface. The through-hole inductor of example 1 can further include a conductive layer deposited on the first surface, second surface,
5 and the aperture wall. The through-hole inductor of example 1 can further include at least one coil cut from the conductive layer, the at least one coil located on the aperture wall.

[0040] Example 2 includes the through-hole inductor of claim 1, wherein the at least one coil includes a helical shape.

10 [0041] Example 3 includes the through-hole inductor of any one of examples 1–2, further including a magnetic core within the aperture.

[0042] Example 4 includes the through-hole inductor of any one of examples 1–3, wherein the magnetic core includes magnetic particles suspended in a carrier.

15 [0043] Example 5 includes the through-hole inductor of any one of examples 1–4, wherein the substrate includes a second substrate layer including at least one electrical contact, the electrical contact configured for electrical communication.

[0044] Example 6 includes the through-hole inductor of any one of
20 examples 1–5, wherein the substrate includes a substrate core and at least one secondary substrate layer includes a sequential layer build-up.

[0045] Example 7 includes a method of making a through-hole inductor Including providing a dielectric layer with a first surface and a second surface, drilling the dielectric layer from the first surface to the second surface to form an
25 aperture in the first and second surfaces, the aperture including an aperture wall from the first surface to the second surface, depositing a conductive layer on the first surface, second surface, and the aperture wall, and cutting a portion of the conductive layer through the entire thickness to form one or more coils on the aperture wall, wherein the coil encircles the aperture wall in at least one
30 revolution from the first surface to the second surface.

[0046] Example 8 includes the method of example 7, wherein cutting a portion of the conductive layer on the aperture wall includes removing the conductive layer with a coil cutting bit.

[0047] Example 9 includes the method of any one of examples 7–8, wherein cutting the portion of the conductive layer on the aperture wall with the coil cutting bit includes, rotating and translating the coil cutting bit in a sequence along a path from the first surface to the second surface thereby removing the conductive layer on the aperture wall, and rotating and translating the coil cutting bit in a reverse sequence along the path to withdrawal the coil cutting bit from the aperture.

[0048] Example 10 includes the method of any one of examples 7–9, wherein the sequence includes a helical path.

10 [0049] Example 11 includes the method of any one of examples 7–10, further comprising locating a magnetic core within the aperture.

[0050] Example 12 includes the method of any one of examples 7–11, wherein locating the magnetic core within the aperture includes depositing, within the aperture, magnetic particles suspended in a carrier.

15 [0051] Example 13 includes the method of any one of examples 7–12, wherein providing the dielectric layer includes providing a substrate core.

[0052] Example 14 includes an electronic package including a through-hole inductor including a substrate including at least one substrate layer, each substrate layer including a dielectric layer having a first surface and a second surface, an aperture in the dielectric layer located from the first surface to the second surface, the aperture including an aperture wall extended from the first surface to the second surface, a conductive layer deposited on the first surface, second surface, and the aperture wall, and at least one coil cut from the conductive layer, the at least one coil includes a helical shape located on the aperture wall from the first surface to the second surface, wherein the at least one coil is configured to generate an electro-magnetic flux.

[0053] Example 15 includes the electronic package of example 14, wherein the electronic package includes an integrated voltage regulator.

[0054] Example 16 includes the electronic package of any one of examples 14–15, further comprising a magnetic core disposed within the aperture.

[0055] Example 17 includes the electronic package of any one of examples 14–17, wherein the magnetic core includes magnetic particles suspended within a carrier.

5 [0056] Example 18 includes the electronic package of any one of examples 1–17, wherein the magnetic core includes magnetic nanoparticles.

[0057] Example 19 includes the electronic package of any one of examples 14–18, wherein the substrate includes a second substrate layer, the second substrate layer can include a secondary conductive layer, the secondary conductive layer includes at least one electrical contact configured for electrical
10 communication.

[0058] Example 20 includes the electronic package of any one of examples 14–19, wherein the substrate includes a substrate core and at least one second substrate layer includes a sequential layer build-up.

15 [0059] Example 21 includes the electronic package of any one of examples 14–20, further comprising a buck converter circuit, the buck converter circuit including at least a capacitor and a resistor located on a silicon die.

[0060] The above detailed description includes references to the accompanying drawings, which form a part of the detailed description. The drawings show, by way of illustration, specific embodiments in which the
20 invention can be practiced. These embodiments are also referred to herein as “examples.” Such examples can include elements in addition to those shown or described. However, the present inventors also contemplate examples in which only those elements shown or described are provided. Moreover, the present inventors also contemplate examples using any combination or permutation of
25 those elements shown or described (or one or more aspects thereof), either with respect to a particular example (or one or more aspects thereof), or with respect to other examples (or one or more aspects thereof) shown or described herein.

[0061] In the event of inconsistent usages between this document and any documents so incorporated by reference, the usage in this document
30 controls.

[0062] In this document, the terms “a” or “an” are used, as is common in patent documents, to include one or more than one, independent of any other instances or usages of “at least one” or “one or more.” In this document, the

term “or” is used to refer to a nonexclusive or, such that “A or B” includes “A but not B,” “B but not A,” and “A and B,” unless otherwise indicated. In this document, the terms “including” and “in which” are used as the plain-English equivalents of the respective terms “comprising” and “wherein.” Also, in the following claims, the terms “including” and “comprising” are open-ended, that is, a system, device, article, composition, formulation, or process that includes elements in addition to those listed after such a term in a claim are still deemed to fall within the scope of that claim. Moreover, in the following claims, the terms “first,” “second,” and “third,” etc. are used merely as labels, and are not intended to impose numerical requirements on their objects.

[0063] Method examples described herein can be machine or computer-implemented at least in part. Some examples can include a computer-readable medium or machine-readable medium encoded with instructions operable to configure an electronic device to perform methods as described in the above examples. An implementation of such methods can include code, such as microcode, assembly language code, a higher-level language code, or the like. Such code can include computer readable instructions for performing various methods. The code may form portions of computer program products. Further, in an example, the code can be tangibly stored on one or more volatile, non-transitory, or non-volatile tangible computer-readable media, such as during execution or at other times. Examples of these tangible computer-readable media can include, but are not limited to, hard disks, removable magnetic disks, removable optical disks (e.g., compact disks and digital video disks), magnetic cassettes, memory cards or sticks, random access memories (RAMs), read only memories (ROMs), and the like.

[0064] The above description is intended to be illustrative, and not restrictive. For example, the above-described examples (or one or more aspects thereof) may be used in combination with each other. Other embodiments can be used, such as by one of ordinary skill in the art upon reviewing the above description. The Abstract is provided to comply with 37 C.F.R. §1.72(b), to allow the reader to quickly ascertain the nature of the technical disclosure. It is submitted with the understanding that it will not be used to interpret or limit the scope or meaning of the claims. Also, in the above Detailed Description, various

features may be grouped together to streamline the disclosure. This should not be interpreted as intending that an unclaimed disclosed feature is essential to any claim. Rather, inventive subject matter may lie in less than all features of a particular disclosed embodiment. Thus, the following claims are hereby

5 incorporated into the Detailed Description as examples or embodiments, with each claim standing on its own as a separate embodiment, and it is contemplated that such embodiments can be combined with each other in various combinations or permutations. The scope of the invention should be determined with reference to the appended claims, along with the full scope of equivalents to

10 which such claims are entitled.

THE CLAIMED INVENTION IS:

1. A through-hole inductor for an electronic package comprising:
a substrate including at least one substrate layer, each substrate layer
5 including a dielectric layer having a first surface and a second surface opposing
the first surface;
an aperture in at least one dielectric layer located from the first surface
to the second surface, the aperture including an aperture wall from the first
surface to the second surface;
10 a conductive layer deposited on the first surface, second surface, and the
aperture wall; and
at least one coil cut from the conductive layer, the at least one coil
located on the aperture wall.
- 15 2. The through-hole inductor of claim 1, further comprising a magnetic core
within the aperture.
3. The through-hole inductor of claim 2, wherein the magnetic core
includes magnetic particles suspended in a carrier.
20
4. The through-hole inductor of claim 1, wherein the substrate includes a
second substrate layer including at least one electrical contact, the electrical
contact configured for electrical communication.
- 25 5. The through-hole inductor of claim 4, wherein the substrate includes a
substrate core and at least one secondary substrate layer includes a sequential
layer build-up.
6. The through-hole inductor of any one of claims 1–5, wherein the at least
30 one coil includes a helical shape.
7. A method of making a through-hole inductor comprising:
providing a dielectric layer with a first surface and a second surface;

drilling the dielectric layer from the first surface to the second surface to form an aperture in the first and second surfaces, the aperture including an aperture wall from the first surface to the second surface;

5 depositing a conductive layer on the first surface, second surface, and the aperture wall; and

cutting a portion of the conductive layer through the entire thickness to form one or more coils on the aperture wall, wherein the coil encircles the aperture wall in at least one revolution from the first surface to the second surface.

10

8. The method of claim 7, wherein cutting a portion of the conductive layer on the aperture wall includes removing the conductive layer with a coil cutting bit.

15 9. The method of claim 8, wherein cutting the portion of the conductive layer on the aperture wall with the coil cutting bit includes:

rotating and translating the coil cutting bit in a sequence along a path from the first surface to the second surface thereby removing the conductive layer on the aperture wall; and

20 rotating and translating the coil cutting bit in a reverse sequence along the path to withdrawal the coil cutting bit from the aperture.

10. The method of claim 7, further comprising locating a magnetic core within the aperture.

25

11. The method of claim 10, wherein locating the magnetic core within the aperture includes depositing, within the aperture, magnetic particles suspended in a carrier.

30 12. The method of claim 7, wherein providing the dielectric layer includes providing a substrate core.

13. The method of any one of claims 9–12, wherein the sequence includes a helical path.
14. An electronic package including a through-hole inductor comprising:
5 a substrate including at least one substrate layer, each substrate layer including a dielectric layer having a first surface and a second surface;
an aperture in the dielectric layer located from the first surface to the second surface, the aperture including an aperture wall extended from the first surface to the second surface;
10 a conductive layer deposited on the first surface, second surface, and the aperture wall; and
at least one coil cut from the conductive layer, the at least one coil includes a helical shape located on the aperture wall from the first surface to the second surface, wherein the at least one coil is configured to generate an electro-
15 magnetic flux.
15. The electronic package of claim 14, further comprising a magnetic core disposed within the aperture.
- 20 16. The electronic package of claim 15, wherein the magnetic core includes magnetic particles suspended within a carrier.
17. The electronic package of claim 16, wherein the magnetic core includes magnetic nanoparticles.
- 25 18. The electronic package of claim 14, wherein the substrate includes a second substrate layer, the second substrate layer can include a secondary conductive layer, the secondary conductive layer includes at least one electrical contact configured for electrical communication.
- 30 19. The electronic package of claim 18, wherein the substrate includes a substrate core and at least one second substrate layer includes a sequential layer build-up.

20. The electronic package of claim 14, further comprising a buck converter circuit, the buck converter circuit including at least a capacitor and a resistor located on a silicon die.

5

21. The electronic package of any one of claims 14–20, wherein the electronic package includes an integrated voltage regulator.

1/4

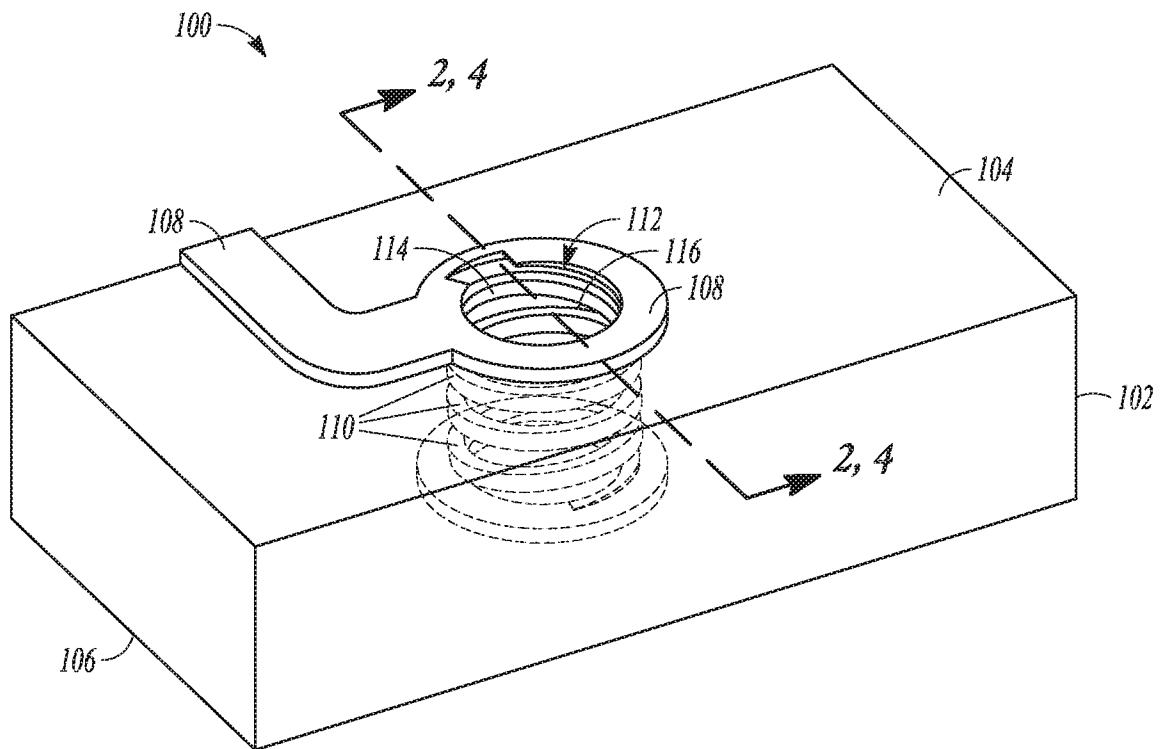


FIG. 1

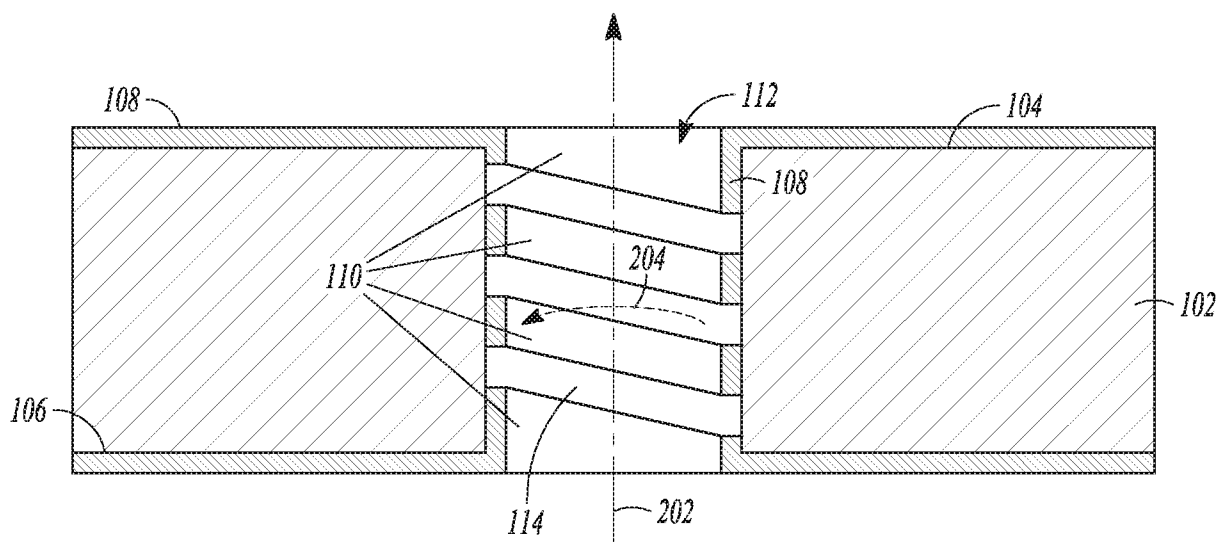


FIG. 2

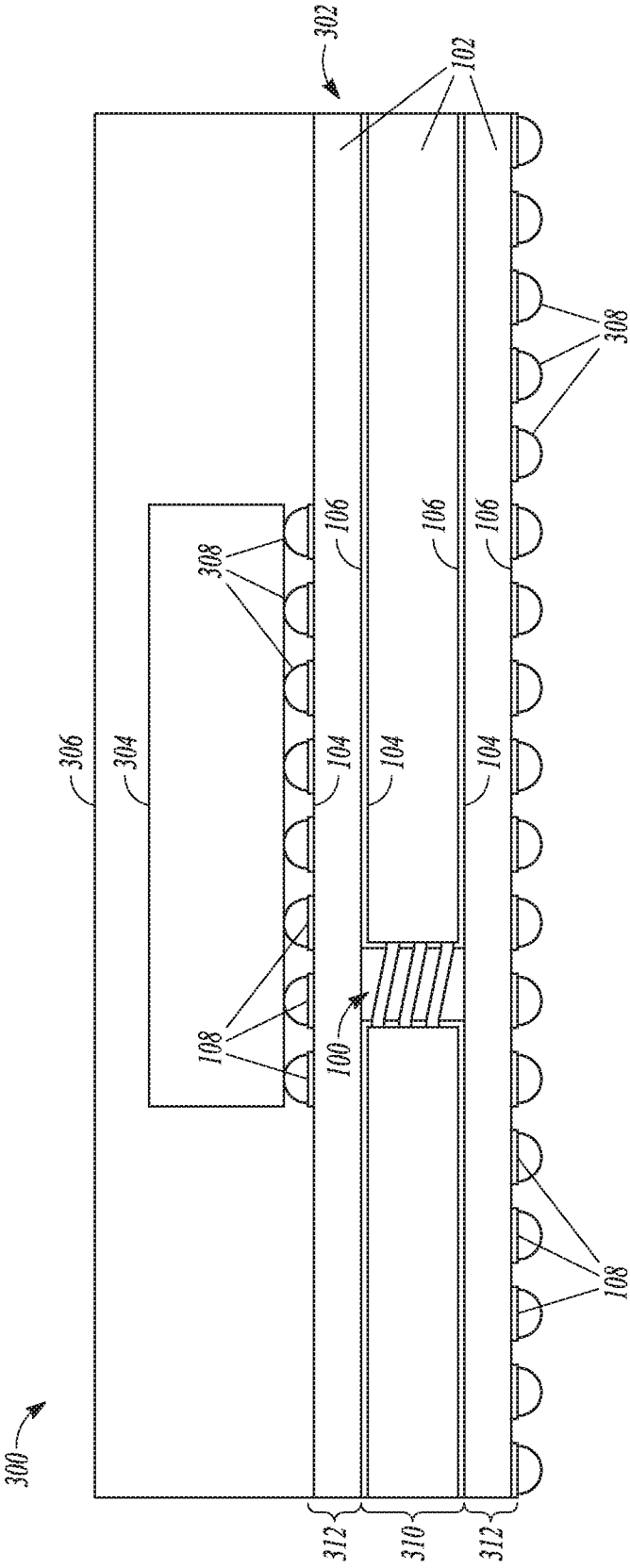
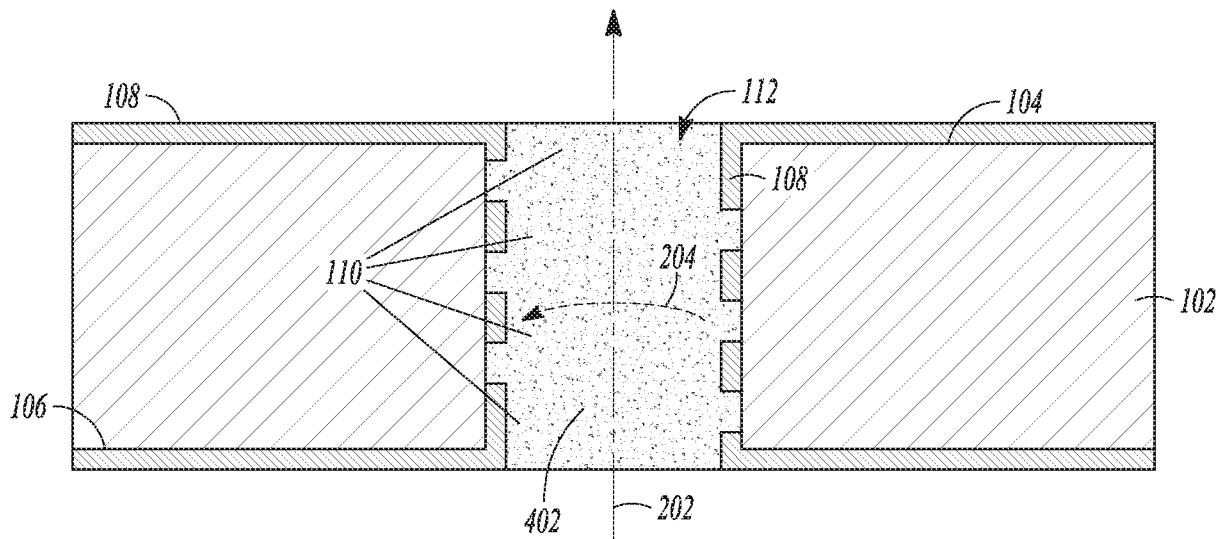
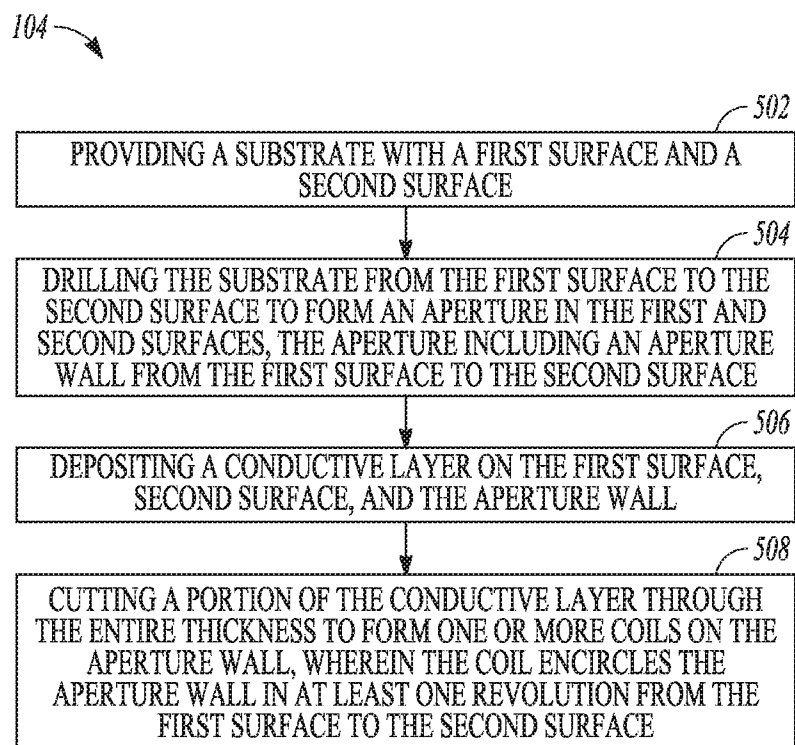


FIG. 3

3/4

**FIG. 4****FIG. 5**

4/4

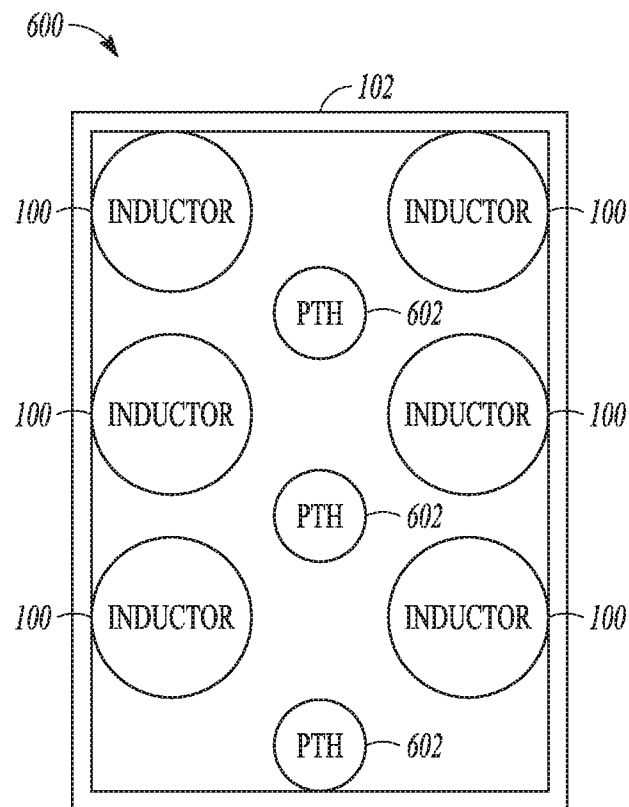


FIG. 6

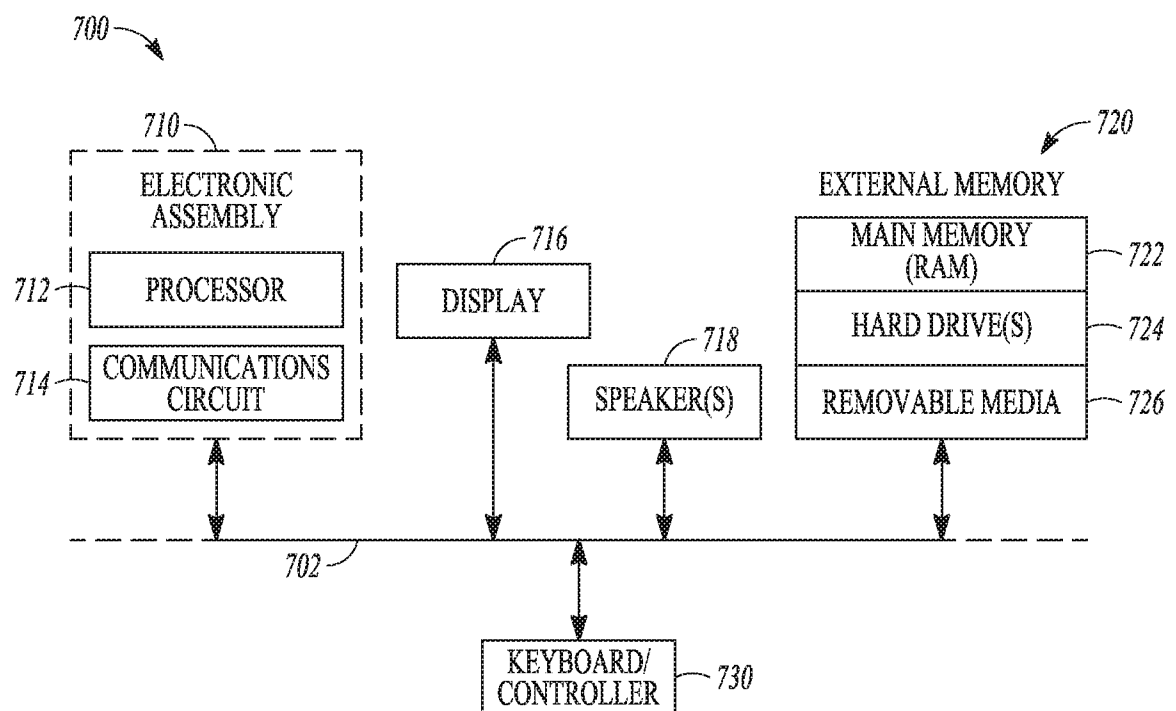


FIG. 7

A. CLASSIFICATION OF SUBJECT MATTER**H01F 17/00(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01F 17/00; H01F 5/00; H01F 41/04; H01F 27/28

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: through-hole, aperature, inductor, coil, dielectric layer

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2007-0090911 A1 (SHENG-YUAN LEE) 26 April 2007	1,4-9,12-13
Y	See paragraphs [0009], [0023]-[0036], claims 1-15 and figures 6A-6B.	2-3,10-11,14-21
Y	US 2009-0224863 A1 (YASUHIKO MANO et al.) 10 September 2009	2-3,10-11,14-21
	See paragraphs [0045]-[0062], claim 1 and figure 5A.	
A	US 2003-0011458 A1 (PETER R. NUYTKENS et al.) 16 January 2003	1-21
	See paragraphs [0005]-[0021] and figure 2.	
A	US 2015-0302975 A1 (SEMICONDUCTOR MANUFACTURING INTERNATIONAL (SHANGHAI) CORPORATION) 22 October 2015	1-21
	See paragraphs [0010]-[0028] and figure 2E.	
A	US 2008-0186123 A1 (CHANG-LIN WEI et al.) 07 August 2008	1-21
	See paragraphs [0006]-[0011] and figure 2A.	



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

09 March 2017 (09.03.2017)

Date of mailing of the international search report

09 March 2017 (09.03.2017)

Name and mailing address of the ISA/KR

International Application Division

Korean Intellectual Property Office

189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea



Facsimile No. +82-42-481-8578

Authorized officer

JANG, Gijeong

Telephone No. +82-42-481-8364



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/063081

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2007-0090911 A1	26/04/2007	TW I260075 B US 7504922 B2	11/08/2006 17/03/2009
US 2009-0224863 A1	10/09/2009	CN 101341807 A CN 101341807 B CN 101697305 A CN 101697305 B EP 2018092 A1 EP 2018092 A4 KR 10-0973447 B1 KR 10-2008-0027371 A TW 200803644 A TW 201106819 A TW I344325 B TW I344805 B US 2007-0257761 A1 US 2009-0225525 A1 US 2010-0117779 A1 US 2011-0102122 A1 US 7760062 B2 US 7812702 B2 US 7843302 B2 US 7855626 B2 US 7868728 B2 US 8207811 B2 WO 2007-129526 A1	07/01/2009 19/09/2012 21/04/2010 17/10/2012 21/01/2009 14/11/2012 02/08/2010 26/03/2008 01/01/2008 16/02/2011 21/06/2011 01/07/2011 08/11/2007 10/09/2009 13/05/2010 05/05/2011 20/07/2010 12/10/2010 30/11/2010 21/12/2010 11/01/2011 26/06/2012 15/11/2007
US 2003-0011458 A1	16/01/2003	US 2005-0005424 A1 US 6696910 B2 US 7231707 B2	13/01/2005 24/02/2004 19/06/2007
US 2015-0302975 A1	22/10/2015	CN 105084291 A	25/11/2015
US 2008-0186123 A1	07/08/2008	CN 101241795 A CN 101241795 B JP 04995062 B2 JP 2008-193059 A KR 10-0991872 B1 KR 10-2008-0074024 A TW 200834613 A TW I347617 B US 2011-0169597 A1 US 8274352 B2	13/08/2008 04/04/2012 08/08/2012 21/08/2008 04/11/2010 12/08/2008 16/08/2008 21/08/2011 14/07/2011 25/09/2012