US 20040259307A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2004/0259307 A1**

Hong (43) **Pub. Date: Dec. 23, 2004**

(54) **SEMICONDUCTOR MEMORY DEVICE HAVING PLUG CONTACTED TO A CAPACITOR ELECTRODE AND METHOD FOR FABRICATING A CAPACITOR OF THE SEMICONDUCTOR MEMORY DEVCIE**

(75) Inventor: **Kwon Hong**, Ichon-shi (KR)

Correspondence Address:
JACOBSON HOLMAN PLLC
400 SEVENTH STREET N.W.
SUITE 600
WASHINGTON, DC 20004 (US)

(73) Assignee: **HYNIX SEMICONDUCTOR INC.**

(21) Appl. No.: **10/217,401**

(22) Filed: **Oct. 9, 2003**

Related U.S. Application Data

(62) Division of application No. 09/882,284, filed on Jun. 18, 2001, now Pat. No. 6,461,913.

(30) **Foreign Application Priority Data**

Jun. 19, 2000 (KR) 2000-33617

Publication Classification

(51) **Int. Cl.**[7] **H01L 21/00**; H01L 21/8242

(52) **U.S. Cl.** **438/253**; 438/256

(57) **ABSTRACT**

The present invention provides a semiconductor memory device and a method capable of preventing the contact between a dielectric layer of a capacitor and a diffusion barrier. The plug to be contacted to an electrode of a capacitor, comprises a diffusion barrier layer and a conducting layer. The conducing layer is formed with a material capable of flowing current nevertheless the conducting layer is oxidized. Accordingly, it is possible to prevent the dielectric layer being contacted with the diffusion barrier, there by the leakage current may be reduced, and the capacitance of the capacitor may be increased.

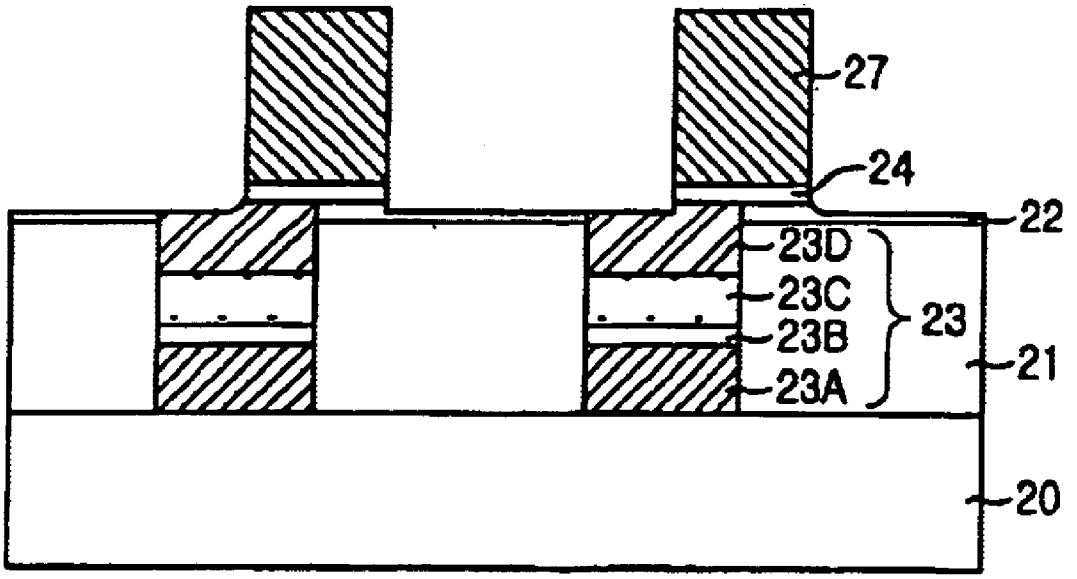


FIG. 1A
(PRIOR ART)

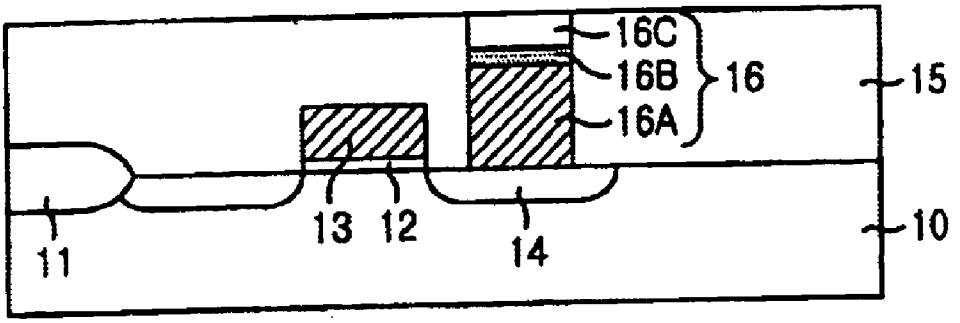


FIG. 1B
(PRIOR ART)

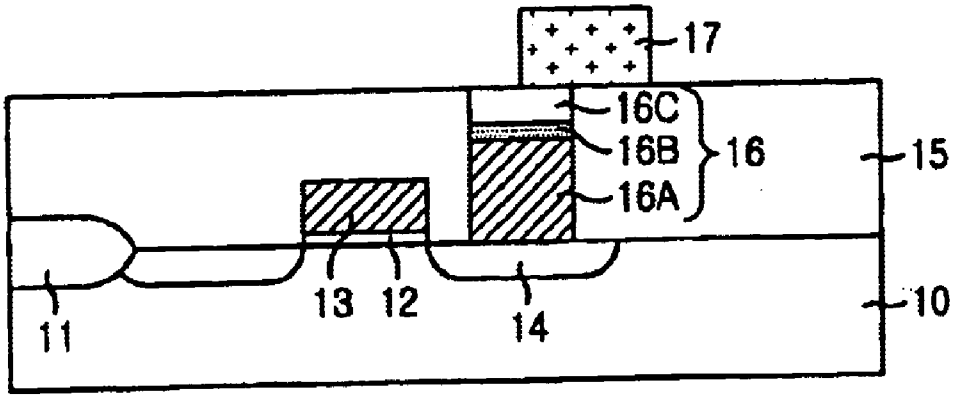


FIG. 1C
(PRIOR ART)

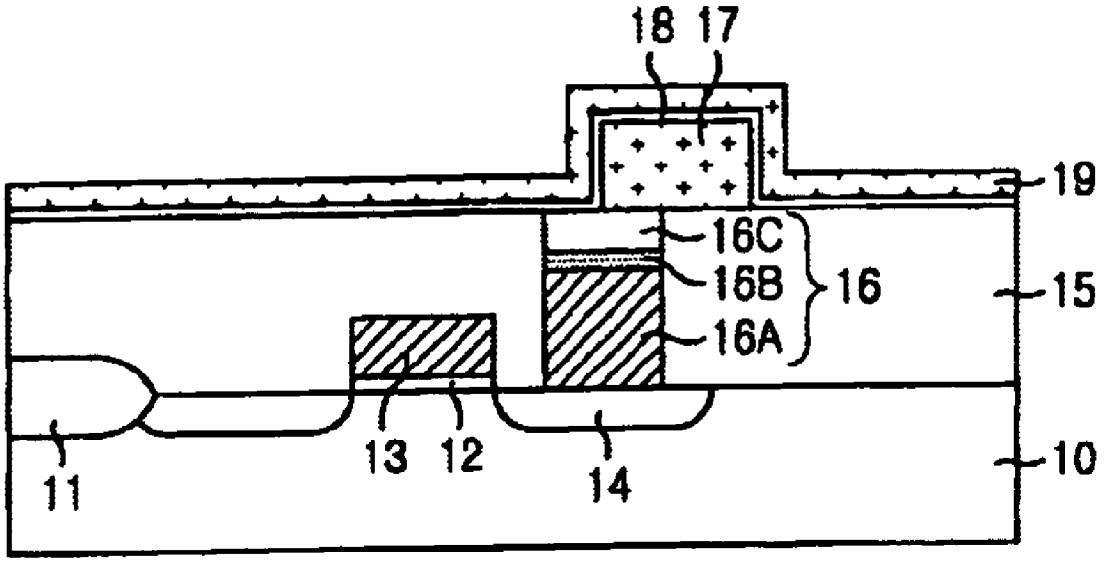


FIG. 2A

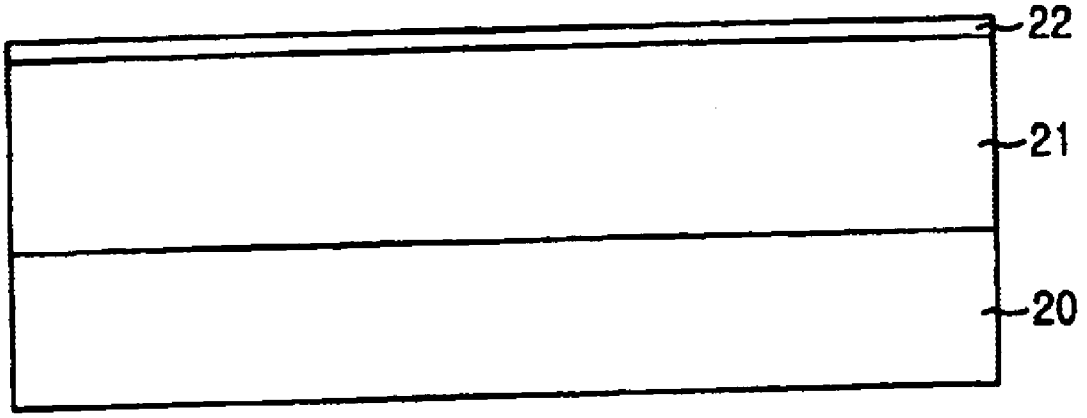


FIG. 2B

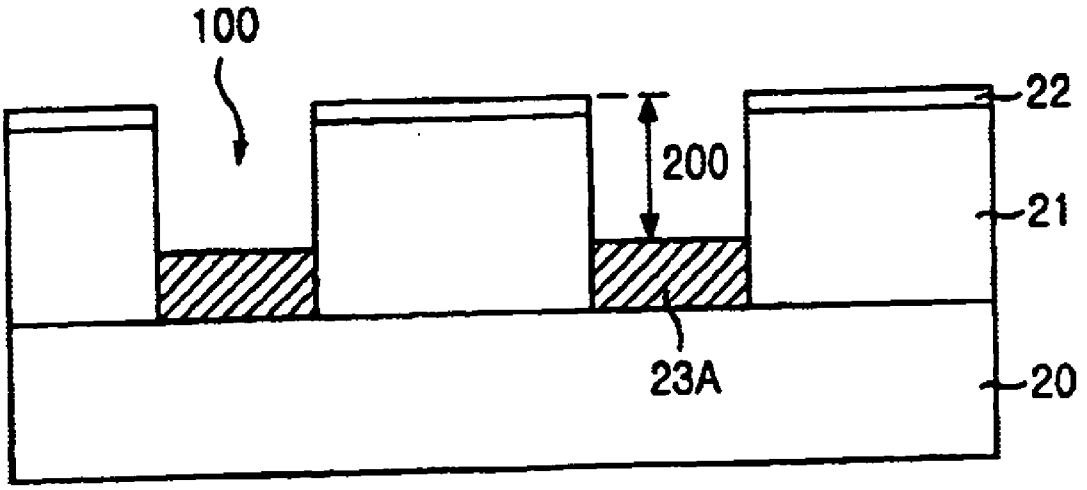


FIG. 2C

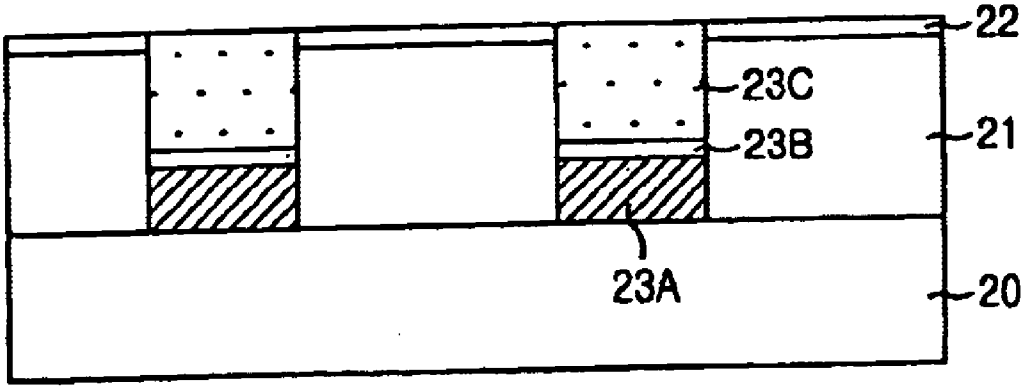


FIG. 2D

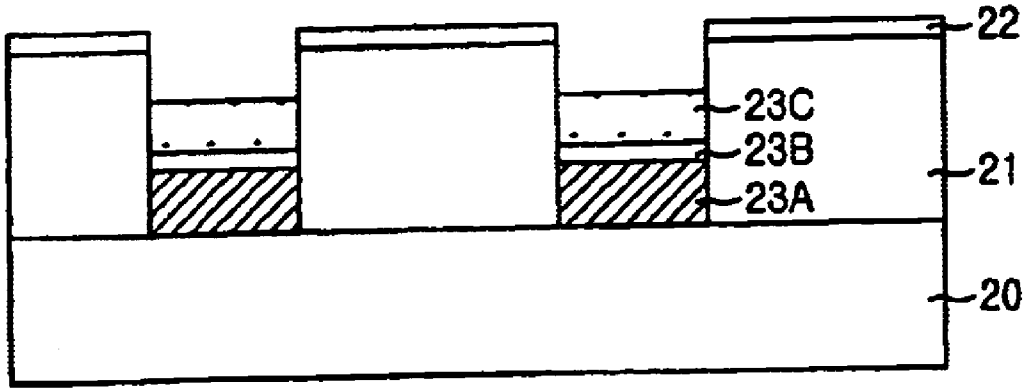


FIG. 2E

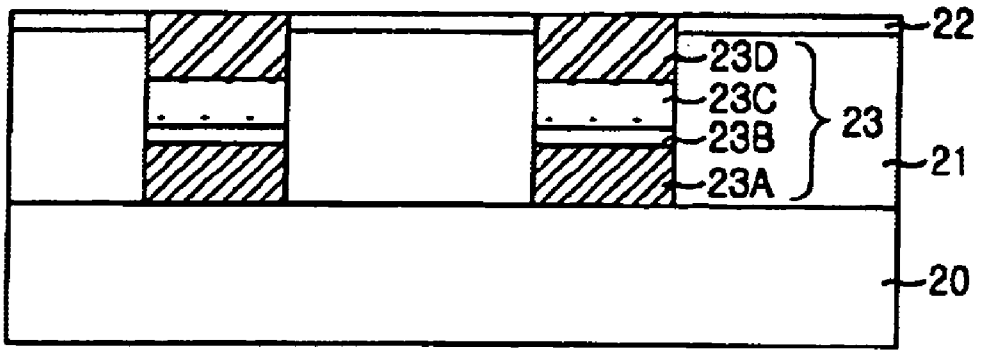


FIG. 2F

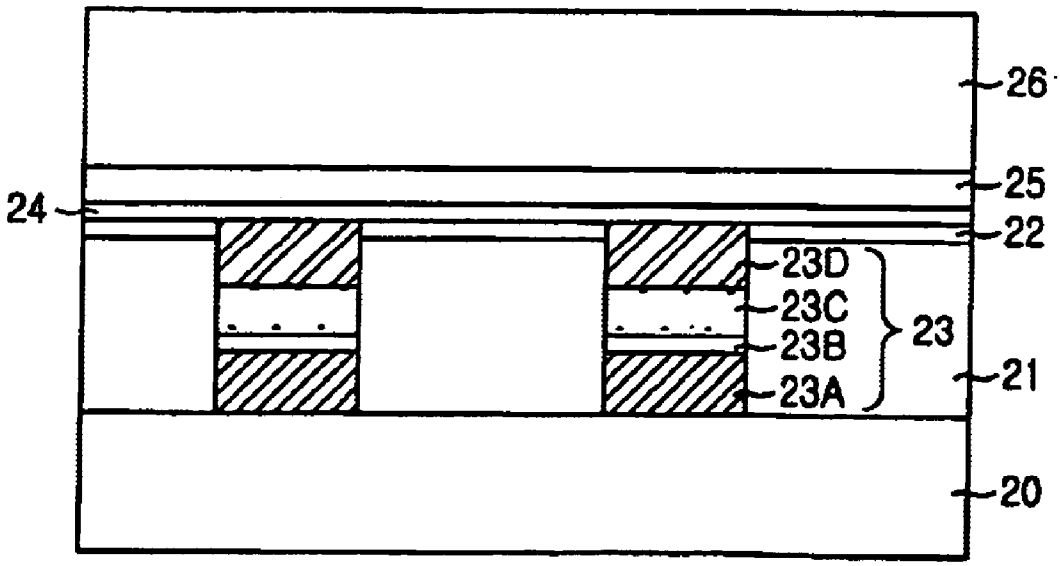


FIG. 2G

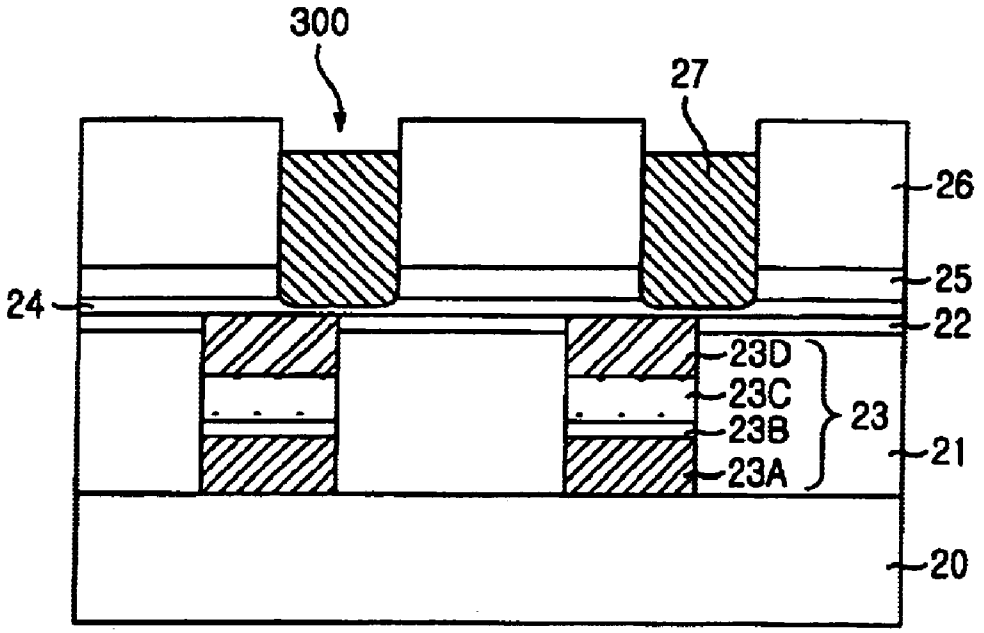

300
27
26
25
24
22
23D
23C
23B
23A
23
21
20

FIG. 2H

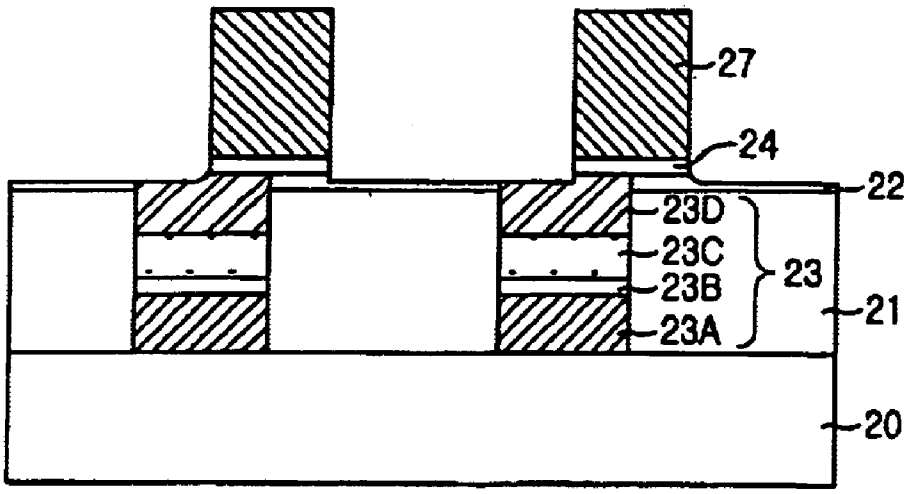
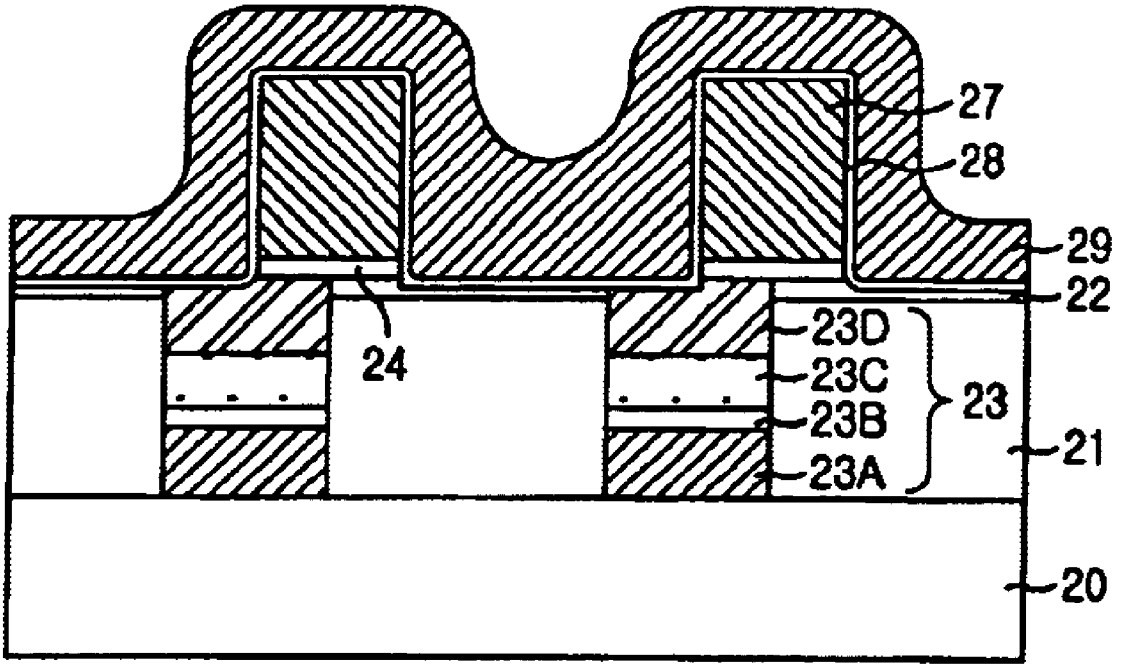

27
24
22
23D
23C
23B
23A
23
21
20

FIG. 2I



SEMICONDUCTOR MEMORY DEVICE HAVING PLUG CONTACTED TO A CAPACITOR ELECTRODE AND METHOD FOR FABRICATING A CAPACITOR OF THE SEMICONDUCTOR MEMORY DEVCIE

FIELD OF THE INVENTION

[0001] The present invention relates to a method for fabricating a semiconductor memory device; and more particularly, to a method for fabricating a capacitor of semiconductor memory device.

DESCRIPTION OF THE PRIOR ART

[0002] A DRAM (Dynamic Random Access Memory) cell is a semiconductor memory device typically comprising one transistor and one capacitor, in which one bit of data is stored in a cell by using an electric charge. A capacitor comprises of a lower electrode, a dielectric layer, and an upper electrode. One electrode of the capacitor is connected to the source/drain junction of the transistor. Another electrode of the capacitor is connected to a reference voltage line.

[0003] Advances in computer applications have increased the demand for higher capacity memory chips. Decreasing the size of the memory cells allows more memory cells to be packed into an integrated circuit.

[0004] The capacitance of a capacitor is proportional to the surface area of the electrodes and a dielectric constant of a dielectric layer. As the area of the memory cell has decreased, the capacitance of the capacitors tends to decrease also, lowering the performance of the memory cells.

[0005] In order to increase the density of memory cells, stacked capacitors have been proposed. Stacked capacitors are formed by partially stacking the storage electrode over the transistor and over the bit/word line, thereby effectively reducing the area used for each memory cell.

[0006] A plug is used to connect the lower electrode of the capacitor with the source/drain junction of the transistor.

[0007] A method for fabricating a capacitor of a semiconductor memory device according to the conventional method is described referring to **FIG. 1A** to **FIG. 1C**.

[0008] As shown in **FIG. 1A**, an insulating layer **15** is formed over a semiconductor substrate **10**, an isolation layer **11**, such as field oxide layer, and a transistor comprising a gate insulating layer **12**, a gate electrode **13** and the source/drain junctions **14**. Thereafter, a plug **16** is formed in the interlayer insulating layer. The plug **16** is composed of a ploysilicon layer **16**A, an ohmic contact layer **16**B and a diffusion barrier layer **16**C formed in a contact hole, exposing one of the source/drain junctions **14**.

[0009] As shown in **FIG. 1B**, a lower electrode **17** is formed on the diffusion barrier layer **16**C by depositing and patterning a first conductive layer. The diffusion barrier layer **16**C may be exposed during the formation of the lower electrode **17** because of a mask misalignment. The mask misalignment is frequently occurred in a manufacturing process of a highly integrated device.

[0010] As shown in **FIG. 1C**, a dielectric layer **18** is formed on the lower electrode **17** and an upper electrode **19** is formed on the dielectric layer **18**. The dielectric layer **18** is formed with a material exhibiting a very high dielectric constant, such as Barium strontium titanate ($BaSrTiO_3$, hereafter abbreviated BST), to increase the capacitance in a highly integrated device.

[0011] According to the preceding conventional method, the exposed part of the diffusion barrier layer **16**C of the plug **16** is contacted to the dielectric layer **18**.

[0012] There are several problems generated by the contact between the diffusion layer **16**C and the dielectric layer **18**. One problem is that the diffusion barrier layer **16**C is oxidized during the process for forming the dielectric layer **18**, because the dielectric layer **18**, such as the BST layer, is formed under oxygen gas atmosphere and at high temperature. The oxidized part of the diffusion barrier layer **16**C, exhibiting low dielectric constant, plays a role of a dielectric layer of a capacitor, thereby the capacitance of the capacitor is reduced. The other problem is that the work function difference, between the diffusion barrier **16**C and the dielectric layer **18**, is low, thereby the leakage current is increased because of the low Schottky barrier height.

SUMMARY OF THE INVENTION

[0013] It is, therefore, an object of the present invention to provide a semiconductor memory device and a fabrication method capable of preventing the contact between a dielectric layer of a capacitor and a diffusion barrier of a plug.

[0014] It is, therefore, another object of the present invention to provide a semiconductor memory device and a fabrication method capable of preventing the lowering the capacitance of a capacitor and the increasing the leakage current between the lower electrode of a capacitor and a diffusion barrier of a plug.

[0015] In accordance with an aspect of the present invention, there is provided a semiconductor memory device, comprising: a semiconductor substrate, wherein a gate electrode is formed on the semiconductor substrate, and wherein source/drain junctions are formed in the semiconductor substrate; an interlayer insulating layer formed over the semiconductor substrate; a plug formed in the interlayer insulating layer, wherein the plug comprises a diffusion barrier layer and a conducting layer, and wherein the conducing layer is formed with a material capable of flowing current nevertheless the conducting layer is oxidized; a lower electrode of capacitor contacted to the conducing layer; a dielectric layer formed on the lower electrode; and an upper electrode formed on the dielectric layer.

[0016] In accordance with another aspect of the present invention, there is provided a method for fabricating semiconductor memory device, comprising the steps of: providing a semiconductor substrate, wherein a gate electrode is formed on the semiconductor substrate, and wherein source/drain junctions are formed in the semiconductor substrate; forming an interlayer insulating layer over the semiconductor substrate; etching the interlayer insulating layer to form a contact hole; forming a diffusion barrier layer and a conducting layer in the contact hole to form a plug, wherein the conducing layer is formed with a material capable of flowing current nevertheless the conducting layer is oxidized; forming a lower electrode contacted to the conducting layer; forming a dielectric layer on the lower electrode; and forming an upper electrode on the dielectric layer.

[0017] In accordance with still further another aspect of the present invention, there is a method for fabricating semiconductor memory device, comprising the steps of: providing a semiconductor substrate, wherein a gate electrode is formed on the semiconductor substrate, and wherein source/drain junctions are formed in the semiconductor substrate; forming an interlayer insulating layer over the semiconductor substrate; etching the interlayer insulating layer to form a contact hole; forming a plug, wherein a diffusion barrier and a conducting layer in the contact hole to form the plug, and wherein the conducing layer is formed with a material capable of flowing current nevertheless, the conducting layer is oxidized; forming a seed layer on the conducting layer; forming a glue layer on the seed layer; forming a sacrificial layer on glue layer; etching the sacrificial layer and the glue layer to form a opening defining a region of a lower electrode; forming a lower electrode on the seed layer in the opening; removing the sacrificial layer and the seed layer; forming a dielectric layer on the lower electrode; and forming a upper electrode on the dielectric layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] The above and other objects and features of the present invention will become apparent from the following description of the preferred embodiments given in conjunction with the accompanying drawings, in which:

[0019] **FIG. 1A** to **FIG. 1C** are cross sectional views showing a method for fabricating a semiconductor memory device according to the conventional method.

[0020] **FIG. 2A** to **FIG. 2I** are cross sectional views showing a method for fabricating a capacitor of a semiconductor device according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0021] Hereinafter, a semiconductor memory device fabrication method according to embodiments of the present invention will be described in detail referring to the accompanying drawings.

[0022] As shown in **FIG. 2A**, an interlayer insulating layer, composed of a first insulating layer **21** and a second insulting layer **22**, is formed over a semiconductor substrate **20**, on which a determined lower structure (not shown), comprising an isolation layer, such as a field oxide layer, and a transistor including a gate insulating layer, a gate electrode and the source/drain junctions. The second insulating layer **22** is formed with a material of which etching selectivity is higher than the first insulating layer **21**. In a preferred embodiment of the present invention, the first insulating layer **21** is formed by depositing a silicon oxide layer to a thickness of 3000-8000 Å, and the second insulating layer **22** is formed by depositing a silicon nitride layer to a thickness of 300 to 1000 Å.

[0023] As shown in **FIG. 2B**, the second insulating layer **22** and the first insulating layer **21** are etched to form a contact hole **100** exposing one of the source/drain junction (not shown) formed in the semiconductor substrate **20**. And then, a polysilicon layer **23**A, for forming a plug is deposited to a thickness of 500-3000 Å on the second insulating layer **22** and the on semiconductor substrate **20** in the contact hole. Thereafter, an etching process is performed to expose the surface of the second insulting layer **22** and to remove a part of the polysilicon layer **23**A in the contact hole. Thereby, the height difference **200** between the surface of the second insulating layer **22** and the surface of the polysilicon layer **23**A becomes 500 to 1500 Å.

[0024] As sown in **FIG. 2C**, an ohmic contact layer **23**B and a diffusion barrier layer **23**C are formed, one by one, on the polysilicon layer **23**A. Subsequently, a chemical mechanical polishing (hereafter, abbreviated CMP) process is performed until the surface of the second insulating layer **22** is exposed. In a preferred embodiment of the present invention, the ohmic contact layer **23**B is formed with $TiSi_x$, and the diffusion barrier layer **23**C is formed with TiN, TiSiN, TiAlN, TaSiN, TaAlN, IrO_2 or RuO_2. For forming the $TiSi_x$, a Ti layer is deposited, an annealing process is performed for reaction between Ti atom in the titanium layer and Si atom in the polysilicon layer **23**A, and a wet etching process is performed to remove the Ti layer remaining on the second insulating layer **22** and the $TiSi_x$ layer.

[0025] As shown in **FIG. 2D**, a part of the diffusion barrier layer **23**C is etched using an etchant, such as a mixed gas comprising Cl_2 and BCl_3, to which the diffusion barrier layer **23**C has higher etching selectivity than the second insulting layer **22**.

[0026] As shown in **FIG. 2E**, a conducting layer **23**D is deposited on the second insulating layer **22** and the diffusion barrier layer **23**C, and a blanket etching process or a CMP process is performed until the second insulating layer **22** is exposed. Thereby, the plug **23** composed of polysilicon layer **23**A, the ohmic contact layer **23**B, the diffusion barrier **23**C and the conducting layer **23**D a, is completely formed. The conducting layer **23**D is formed with a material which can flow current even if it is oxidized. In the preferred embodiment of the present invention, Ru, Pt or Ir is deposited by using chemical vapor deposition technique, for forming the conducting layer **23**D. On the other hand, the blanket etching process or the CMP process may be skipped, in order to use the conducting layer **34**D as a seed layer for forming a lower electrode of a capacitor.

[0027] Also, the process for forming the polysilicon layer **23**A may be omitted, in such case, the plug **23** is composed of the ohmic contact layer **23**B layer, the diffusion barrier layer **23**C and the conducting layer **24**D. Moreover, the process for forming the ohmic contact layer **23**B can be omitted, in such a case, the plug **23** is composed of the polusilicon layer **23**A, diffusion barrier layer **23**C and the conducting layer **24**D. Accordingly, it is possible that the plug **23** is composed of the diffusion barrier layer **23**C and the conducting layer **23**D.

[0028] As shown in **FIG. 2F**, a seed layer **24** is formed on the conducting layer **23**D and the second insulating layer **22**, thereafter a glue layer **25** and a sacrificial layer **26** are stacked, one by one, on the seed layer **24**. In the preferred embodiment of the present invention, the seed layer **24** is formed with Pt or Ru 50-100 Å thick, the glue layer **25** is formed with. TiN, TiAlN, TaN, TaSiN, Al_2O_3 or TiO_2 50-500 Å thick, and the sacrificial layer **26** is formed with silicon oxide 5000-15000 Å thick. In case that the conducting layer **23**D is formed

[0029] On the other hand, the processes for forming the seed layer **24** and the glue layer **25** can be omitted depending the various methods for forming a lower electrode.

[0030] As shown in **FIG. 2G**, the sacrificial layer **26** and the glue layer **25** is selectively etched to form opening **300** exposing the seed layer **24**, and a lower electrode **27** is formed on the seed layer **24** in the opening **300**. In the preferred embodiment of the present invention, a Pt layer as the lower electrode **27**, is deposited to a thickness of 4000-12000 Å by the electroplating. A current density of 0.1-20 mA/cm^2 is imposed on electrodes for electroplating, with DC or DC pulse.

[0031] As shown **FIG. 2H**, the sacrificial layer **26**, the glue layer **25** and the seed layer **24** are removed to separate neighboring the lower electrodes **27**. The sacrificial layer **26** and the glue layer **25** are removed by a wet etching, and the seed layer **24** is removed by a dry etching. Also, the glue layer **25** can be removed by a dry etching.

[0032] According to the preceding process of the present invention, the diffusion barrier layer **23**C of the plug **23** is not exposed, even if the mask misalignment is occurred in the process for forming the opening **300**. That is, the conducting layer **23**D, covering the diffusion layer **23**C, is exposed in case of occurring the mask misalignment.

[0033] As shown in **FIG. 2I**, a dielectric layer **28** is deposited on the lower electrode **27** and the second insulating layer **22**. Thereafter, an upper electrode **29** is formed on the dielectric layer **28**. In the preferred embodiment of the present invention, a BST layer is deposited to a thickness of 150-500 Å at a temperature of 350-600° C. for forming the dielectric layer **28**, and an annealing for crystallizing the dielectric layer **28** is performed in an N_2 gas atmosphere at a temperature of 500-700° C. for 30-180 seconds, thereby dielectric characteristic of the dielectric layer **28** may be improved. The upper electrode **29** is formed with a material, which can flow current even if it is oxidized, such as Pt, Ru, Ir.

[0034] There are several advantages to form the conducing layer on the diffusion barrier. A first advantage is that it is possible to prevent the dielectric layer being contacted with the diffusion barrier. A second advantage is that it is possible to reduce the leakage current. A third advantage is that it is possible to prevent the diffusion barrier from being exposed even if the mask misalign is occurred, thereby the annealing for crystallizing the dielectric layer can be performed at a high temperature. A fourth advantage is that it is possible to obtain high capacitance of the capacitor in the highly integrated semiconductor device.

[0035] Although the preferred embodiments of the invention have been disclosed for illustrative purposes, those skilled in the art will appreciate that various modifications, additions and substitutions are possible, without departing from the scope and spirit of the invention as disclosed in the accompanying claims.

What is claimed is:

1. A semiconductor memory device, comprising:

a semiconductor substrate, wherein a gate electrode is formed on the semiconductor substrate, and wherein source/drain junctions are formed in the semiconductor substrate;

an interlayer insulating layer formed over the semiconductor substrate;

a plug formed in the interlayer insulating layer, wherein the plug comprises a diffusion barrier layer and a conducting layer, and wherein the conducing layer is formed with a material capable of flowing current nevertheless the conducting layer is oxidized;

a lower electrode of capacitor contacted to the conducing layer;

a dielectric layer formed on the lower electrode; and

an upper electrode formed on the dielectric layer.

2. The semiconductor device as recited in claim 1, the conducting layer is selected from a group consisting of Ru layer, Ir layer, Pt layer and Ir layer.

3. The semiconductor device as recited in claim 1, the diffusion barrier layer is selected from a group consisting of TiN layer, TiSiN layer, TiAlN layer, TaSiN layer, TaAlN layer, IrO_2 layer and RuO_2 layer.

4. The semiconductor device as recited in claim 1, further comprising a polysilicon layer between the diffusion barrier layer and the semiconductor substrate.

5. The semiconductor device as recited in claim 1, further comprising an ohmic contact layer between the diffusion barrier layer and the semiconductor substrate.

6. The semiconductor device as recited in claim 5, further comprising a polysilicon layer between the ohmic contact layer and the semiconductor substrate.

7. A method for fabricating semiconductor memory device, comprising the steps of:

providing a semiconductor substrate, wherein a gate electrode is formed on the semiconductor substrate, and wherein source/drain junctions are formed in the semiconductor substrate;

forming an interlayer insulating layer over the semiconductor substrate;

etching the interlayer insulating layer to form a contact hole;

forming a diffusion barrier layer and a conducting layer in the contact hole to form a plug, wherein the conducing layer is formed with a material capable of flowing current nevertheless the conducting layer is oxidized;

forming a lower electrode contacted to the conducting layer;

forming a dielectric layer on the lower electrode; and

forming an upper electrode on the dielectric layer.

8. The method as recited in claim 7, wherein the conducting layer is formed with Ir, Pt or Ru.

9. The method as recited in claim 8, the lower electrode is formed by an electroplating by using the conducting layer as a see layer.

10. The method as recited in claim 7, wherein the diffusion barrier layer is formed with TiN, TiSiN, TiAlN, TaSiN, TaAlN, IrO_2 or RuO_2.

11. The method as recited in claim 7, wherein the dielectric layer is formed with $BaSrTiO_3$ layer, and wherein the upper electrode is formed with Pt layer, Ru layer or Ir layer.

12. A method for fabricating semiconductor memory device, comprising the steps of:

providing a semiconductor substrate, wherein a gate electrode is formed on the semiconductor substrate, and wherein source/drain junctions are formed in the semiconductor substrate;

forming an interlayer insulating layer over the semiconductor substrate;

etching the interlayer insulating layer to form a contact hole;

forming a plug, wherein a diffusion barrier and a conducting layer in the contact hole to form the plug, and wherein the conducing layer is formed with a material capable of flowing current nevertheless the conducting layer is oxidized;

forming a seed layer on the conducting layer;

forming a glue layer on the seed layer;

forming a sacrificial layer on glue layer;

etching the sacrificial layer and the glue layer to form a opening defining a region of a lower electrode;

forming a lower electrode on the seed layer in the opening;

removing the sacrificial layer and the seed layer;

forming a dielectric layer on the lower electrode; and

forming a upper electrode on the dielectric layer.

13. The method as recited in claim 12, the step of forming the plug including:

forming the diffusion barrier layer in the contact hole;

etching the diffusion barrier to remove a part of the diffusion barrier layer in the contact hole; and

forming the conducting layer on the diffusion barrier layer.

14. The method as recited in claim 12, wherein the lower electrode is formed by an electroplating.

15. The method as recited in claim 13, wherein the conducting layer is formed with Ir, Pt or Ir, and wherein the diffusion barrier layer is formed with TiN, TiSiN, TiAlN, TaSiN, TaAlN, IrO_2 or RuO_2.

16. The method as recited in claim 15, wherein a silicon oxide layer and a nitride layer are staked to form the interlayer insulating layer.

17. The method as recited in claim 16, wherein the diffusion barrier layer is etched with a mixed gas comprising Cl_2 and BCl_3.

18. The method as recited in claim 16, the dielectric layer is formed with a $BaSrTiO_3$ layer, and wherein the upper electrode is formed with Pt layer, Ru layer or Ir layer.

* * * * *