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(54) Title: INDUCTORS WITH THROUGH-SUBSTRATE VIA CORES

(57) Abstract: A semiconductor device comprising a substrate is provided. The device further comprises a through-substrate via (TSV) extending into the substrate, and a substantially helical conductor disposed around the TSV. The substantially helical conductor can be configured to generate a magnetic field in the TSV in response to a current passing through the helical conductor. More than one TSV can be included, and/or more than one substantially helical conductor can be provided.

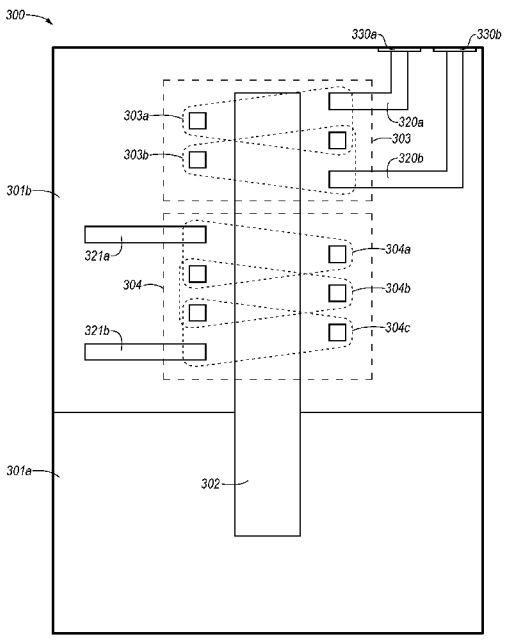


Fig. 3

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INDUCTORS WITH THROUGH-SUBSTRATE VIA CORES

CROSS-REFERENCE TO RELATED APPLICATION(S)

[0001] This application contains subject matter related to a concurrently-filed U.S. Patent Application by Kyle K. Kirby, entitled "SEMICONDUCTOR DEVICES WITH BACK-SIDE COILS FOR WIRELESS SIGNAL AND POWER COUPLING." The related application, of which the disclosure is incorporated by reference herein, is assigned to Micron Technology, Inc., and is identified by attorney docket number 10829-9206.US00.

[0002] This application contains subject matter related to a concurrently-filed U.S. Patent Application by Kyle K. Kirby, entitled "SEMICONDUCTOR DEVICES WITH THROUGH-SUBSTRATE COILS FOR WIRELESS SIGNAL AND POWER COUPLING." The related application, of which the disclosure is incorporated by reference herein, is assigned to Micron Technology, Inc., and is identified by attorney docket number 10829-9207.US00.

[0003] This application contains subject matter related to a concurrently-filed U.S. Patent Application by Kyle K. Kirby, entitled "MULTI-DIE INDUCTORS WITH COUPLED THROUGH-SUBSTRATE VIA CORES." The related application, of which the disclosure is incorporated by reference herein, is assigned to Micron Technology, Inc., and is identified by attorney docket number 10829-9220.US00.

[0004] This application contains subject matter related to a concurrently-filed U.S. Patent Application by Kyle K. Kirby, entitled "3D INTERCONNECT MULTI-DIE INDUCTORS WITH THROUGH-SUBSTRATE VIA CORES." The related application, of which the disclosure is incorporated by reference herein, is assigned to Micron Technology, Inc., and is identified by attorney docket number 10829-9221.US00.

TECHNICAL FIELD

[0005] The present disclosure generally relates to semiconductor devices, and more particularly relates to semiconductor devices including inductors with through-substrate via cores, and methods of making and using the same.

BACKGROUND

[0006] As the need for miniaturization of electronic circuits continues to increase, the need to minimize various circuit elements, such as inductors, increases apace. Inductors are an

important component in many discrete element circuits, such as impedance-matching circuits, linear filters, and various power circuits. Since traditional inductors are bulky components, successful miniaturization of inductors presents a challenging engineering problem.

[0007] One approach to miniaturizing an inductor is to use standard integrated circuit building blocks, such as resistors, capacitors, and active circuitry, such as operational amplifiers, to design an active inductor that simulates the electrical properties of a discrete inductor. Active inductors can be designed to have a high inductance and a high Q factor, but inductors fabricated using these designs consume a great deal of power and generate noise. Another approach is to fabricate a spiral-type inductor using conventional integrated circuit processes. Unfortunately, spiral inductors in a single level (e.g., plane) occupy a large surface area, such that the fabrication of a spiral inductor with high inductance can be cost- and size-prohibitive. Accordingly, there is a need for other approaches to the miniaturization of inductive elements in semiconductor devices.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Figure 1 is a simplified cross-sectional view of a semiconductor device having an inductor with a TSV core configured in accordance with an embodiment of the present technology.

[0009] Figure 2 is a simplified perspective view of a substantially helical conductor disposed around a through-substrate via configured in accordance with an embodiment of the present technology.

[0010] Figure 3 is a simplified cross-sectional view of coupled inductors sharing a through-substrate via core configured in accordance with an embodiment of the present technology.

[0011] Figure 4 is a simplified cross-sectional view of coupled inductors sharing a through-substrate via core configured in accordance with an embodiment of the present technology.

[0012] Figure 5 is a simplified cross-sectional view of a semiconductor device having an inductor with a closed core comprising multiple through-substrate vias configured in accordance with an embodiment of the present technology.

[0013] Figure 6 is a simplified cross-sectional view of coupled inductors with through-substrate via cores configured in accordance with an embodiment of the present technology.

[0014] Figure 7 is a simplified cross-sectional view of coupled inductors with through-substrate via cores configured in accordance with an embodiment of the present technology.

[0015] Figure 8 is a simplified cross-sectional view of coupled inductors with through-substrate via cores configured in accordance with an embodiment of the present technology.

[0016] Figure 9 is a simplified cross-sectional view of an inductor with a through-substrate via core configured in accordance with an embodiment of the present technology.

[0017] Figure 10 is a simplified cross-sectional view of an inductor with a through-substrate via core configured in accordance with an embodiment of the present technology.

[0018] Figure 11 is a simplified perspective view of a substantially helical conductor disposed around a through-substrate via configured in accordance with an embodiment of the present technology.

[0019] Figures 12A through 12D are simplified cross-sectional views of an inductor with a through-substrate via core at various stages of a manufacturing process in accordance with an embodiment of the present technology.

[0020] Figures 12E and 12F are simplified perspective views of an inductor with a through-substrate via core at various stages of a manufacturing process in accordance with an embodiment of the present technology.

[0021] Figure 13 is a flow chart illustrating a method of manufacturing an inductor with a through-substrate via core in accordance with an embodiment of the present technology.

DETAILED DESCRIPTION

[0022] In the following description, numerous specific details are discussed to provide a thorough and enabling description for embodiments of the present technology. One skilled in the relevant art, however, will recognize that the disclosure can be practiced without one or more of the specific details. In other instances, well-known structures or operations often associated with semiconductor devices are not shown, or are not described in detail, to avoid obscuring other aspects of the technology. In general, it should be understood that various other devices, systems, and methods in addition to those specific embodiments disclosed herein may be within the scope of the present technology.

[0023] As discussed above, semiconductor devices are continually designed with ever greater needs for inductors with high inductance that occupy a small area. Accordingly, several

embodiments of semiconductor devices in accordance with the present technology can provide inductors with through-substrate via cores, which can provide high inductance while consuming only a small area.

[0024] Several embodiments of the present technology are directed to semiconductor devices, systems including semiconductor devices, and methods of making and operating semiconductor devices. In one embodiment, a semiconductor device comprises a substrate (*e.g.*, of silicon, glass, gallium arsenide, organic material, *etc.*), a through-substrate via (TSV) extending into the silicon substrate, and a substantially helical conductor disposed around the TSV. The substantially helical conductor can be a non-planar spiral configured to generate a magnetic field in the TSV in response to a current passing through the substantially helical conductor. More than one TSV can be included (*e.g.*, to provide a closed core), and/or more than one substantially helical conductor can be provided (*e.g.*, to provide coupled inductors).

[0025] Figure 1 is a simplified cross-sectional view of a semiconductor device 10 having an inductor 100 with a TSV core configured in accordance with an embodiment of the present technology. The device 10 has a substrate material 101a and an insulating material 101b, and the inductor 100 has one portion in the substrate material 101a and another portion in the insulating material 101b. For example, the inductor 100 can include a TSV 102 having a first portion in the substrate material 101a and a second portion in the insulating material 101b. The TSV 102 accordingly extends out of the substrate material 101a and into the insulating material 102b. The inductor 100 can further include a substantially helical conductor 103 ("conductor 103") around at least a section of the second portion of the TSV 102 in the insulating material 101b. In the embodiment shown in Figure 1, the conductor 103 is illustrated schematically with five complete turns (103a, 103b, 103c, 103d and 103e) around the TSV 102. The conductor 103 is configured to induce a magnetic field in the TSV 102 in response to a current passing through the conductor 103. The conductor 103 can be operably connected to other circuit elements (not shown) by leads 120a and 120b.

[0026] According to one embodiment of the present technology, the substrate material 101a can be any one of a number of substrate materials suitable for semiconductor processing methods, including silicon, glass, gallium arsenide, gallium nitride, organic laminates, molding compounds (*e.g.*, for reconstituted wafers for fan-out wafer-level processing) and the like. As will be readily understood by those skilled in the art, a through-substrate via, such as the TSV 102, can be made by etching a high-aspect-ratio hole into the substrate material 101a and filling

it with one or more materials in one or more deposition and/or plating steps. Accordingly, the TSV 102 extends at least substantially into the substrate material 101a, which is unlike other circuit elements that are additively constructed on top of the substrate material 101a. For example, the substrate material 101a can be a silicon wafer of about 800 μm thickness, and the TSV 102 can extend from 30 to 100 μm into the substrate material 101a. In other embodiments, a TSV may extend even further into a substrate material (*e.g.*, 150 μm, 200 μm, etc.), or may extend into a substrate material by as little as 10 μm.

[0027] The TSV 102 can also include an outer layer 102a and a magnetic material 102b within the outer layer 102a. The outer layer 102a can be a dielectric or insulating material (*e.g.*, silicon oxide, silicon nitride, polyimide, *etc.*) that electrically isolates the magnetic material 102b from the conductor 103. In accordance with one embodiment of the present technology, the magnetic material 102b of the TSV 102 can be a material with a higher magnetic permeability than the substrate material 101a and/or the insulating material 101b to increase the magnetic field in the TSV 102 when current flows through the conductor 103. The magnetic material 102b can be, for example, ferromagnetic, ferrimagnetic, or a combination thereof. For example, the TSV 102 can include nickel, iron, cobalt, niobium, or an alloy thereof. The TSV 102 can include more than one material, either in a bulk material of a single composition, or in discrete regions of different materials (*e.g.*, coaxial laminate layers). The TSV 102 can include a bulk material with desirable magnetic properties (*e.g.*, elevated magnetic permeability provided by nickel, iron, cobalt, niobium, or an alloy thereof), or can include multiple discrete layers, only some of which are magnetic, in accordance with an embodiment of the present technology.

[0028] For example, following a high-aspect ratio etch and a deposition of an insulator (*e.g.*, insulator 102a), the TSV 102 can be provided in a single metallization step by filling in the insulated opening with a magnetic material. In another embodiment, the TSV 102 can be formed in multiple steps to provide coaxial layers (*e.g.*, two or more magnetic layers separated by one or more non-magnetic layers). For example, multiple conformal plating operations can be performed before a bottom-up fill operation to provide a TSV with a coaxial layer of non-magnetic material separating a core of magnetic material and an outer coaxial layer of magnetic material. In this regard, a first conformal plating step can partially fill and narrow the etched opening with a magnetic material (*e.g.*, nickel, iron, cobalt, niobium, or an alloy thereof), a second conformal plating step can further partially fill and further narrow the opening with a non-magnetic material (*e.g.*, polyimide or the like), and a subsequent bottom-up plating step (*e.g.*, following the deposition of a seed material at the bottom of the narrowed opening) can

completely fill the narrowed opening with another magnetic material (*e.g.*, nickel, iron, cobalt, niobium, or an alloy thereof). Such a structure with laminated coaxial layers of magnetic and non-magnetic material can help to reduce eddy current losses in a TSV through which a magnetic flux is passing.

[0029] The turns 103a-103e of the conductor 103 are electrically insulated from one another and from the TSV 102. In one embodiment, the insulating material 101b electrically isolates the conductor 103 from the TSV 102. In another embodiment, the conductor 103 can have a conductive inner region 110a covered (*e.g.*, coated) by a dielectric or insulating outer layer 110b. For example, the outer layer 110b of the conductor 103 can be an oxide layer, and the inner region 110a can be copper, gold, tungsten, or alloys thereof. One aspect of the conductor 103 is that the individual turns 103a-103e define a non-planar spiral with respect to the longitudinal dimension "L" of the TSV 102. Each subsequent turn 103a-103e is at a different elevation along the longitudinal dimension L of the TSV 102 in the non-planar spiral of the conductor 103.

[0030] A conductive winding (*e.g.*, the conductor 103) of an inductor disposed around a TSV magnetic core (*e.g.*, the TSV 102) need not be smoothly helical, in accordance with one embodiment of the present technology. Although the conductor 103 is illustrated schematically and functionally in Figure 1 as having turns that, in cross section, appear to gradually increase in distance from a surface of the substrate, it will be readily understood by those skilled in the art that fabricating a smooth helix with an axis perpendicular to a surface of a substrate presents a significant engineering challenge. Accordingly, a "substantially helical" conductor, as used herein, describes a conductor having turns that are separated along the longitudinal dimension L of the TSV (*e.g.*, the z-dimension perpendicular to the substrate surface), but which are not necessarily smoothly varying in the z-dimension (*e.g.*, the substantially helical shape does not possess arcuate, curved surfaces and a constant pitch angle). Rather, an individual turn of the conductor can have a pitch of zero degrees and the adjacent turns can be electrically coupled to each other by steeply-angled or even vertical connectors (*e.g.*, traces or vias) with a larger pitch, such that a "substantially helical" conductor can have a stepped structure. Moreover, the planar shape traced out by the path of individual turns of a substantially helical conductor need not be elliptical or circular. For the convenience of integration with efficient semiconductor processing methodologies (*e.g.*, masking with cost-effective reticles), individual turns of a substantially helical conductor can trace out a polygonal path in a planar view (*e.g.*, a square, a hexagon, an octagon, or some other regular or irregular polygonal shape around the TSV 102). Accordingly,

a "substantially helical" conductor, as used herein, describes a non-planar spiral conductor having turns that trace out any shape in a planar view (*e.g.*, parallel to the plane of the substrate surface) surrounding a central axis, including circles, ellipses, regular polygons, irregular polygons, or some combination thereof.

[0031] Figure 2 is a simplified perspective view of a substantially helical conductor 204 ("conductor 204") disposed around a through-substrate via 202 configured in accordance with an embodiment of the present technology. For more easily illustrating the substantially helical shape of the conductor 204 illustrated in Figure 2, the substrate material, insulating materials, and other details of the device in which the conductor 204 and the TSV 202 are disposed have been eliminated from the illustration. As can be seen with reference to Figure 2, the conductor 204 is disposed coaxially around the TSV 202. The conductor 204 makes three turns (204a, 204b, and 204c) about the TSV 202. As described above, rather than having a single pitch angle, the conductor 204 has a stepped structure, whereby turns with a pitch angle of 0 (*e.g.*, turns laying in a plane of the device 200) are connected by vertical connecting portions that are staggered circumferentially around the turns. In this regard, planar turns 204a and 204b are connected by a vertical connecting portion 206, and planar turns 204b and 204c are connected by a vertical connecting portion 208. This stepped structure facilitates fabrication of the conductor 204 using simpler semiconductor processing techniques (*e.g.*, planar metallization steps for the turns and via formation for the vertical connecting portions). Moreover, as shown in Figure 2, the turns 204a, 204b, and 204c of the conductor 204 trace a rectangular shape around the TSV 202 when oriented in a planar view.

[0032] In accordance with one embodiment, the TSV 202 can optionally (*e.g.*, as shown with dotted lines) include a core material 202a surrounded by one or more coaxial layers, such as layers 202b and 202c. For example, the core 202a and the outer coaxial layer 202c can include magnetic materials, while the middle coaxial layer 202b can include a non-magnetic material, to provide a laminate structure that can reduce eddy current losses. Although the TSV 202 is illustrated in Figure 2 as optionally including a three-layer structure (*e.g.*, a core 202a surrounded by two coaxially laminated layers 202b and 202c), in other embodiments any number of coaxial laminate layers can be used to fabricate a TSV.

[0033] As shown in the foregoing examples of Figure 1 and Figure 2, the number of turns made by a substantially helical conductor about a TSV can vary in accordance with different embodiments of the technology. Providing more turns can increase the inductance of an inductor

compared to having fewer turns, but at an increase in the cost and complexity of fabrication (*e.g.*, more fabrication steps). The number of turns can be as low as one, or as high as is desired. As is shown in the example embodiment of Figure 2, a substantially helical conductor need not make an integer number of turns about a TSV (*e.g.*, the top and/or bottom turn may not be a complete turn).

[0034] Although the foregoing embodiments shown in Figures 1 and 2 have illustrated a single inductor with a single substantially helical conductor disposed around a single TSV, other embodiments of the present technology can be configured with more than one substantially helical conductor and/or TSV. For example, Figure 3 is a simplified cross-sectional view of two coupled inductors sharing a common through-substrate via core, configured in accordance with an embodiment of the present technology. As can be seen with reference to Figure 3, a device 300 includes a substrate material 301a, an insulating material 301b, and a TSV 302. The TSV 302 extends out of the substrate material 301a and into the insulating material 301b. The device 300 also includes a first substantially helical conductor 303 ("conductor 303") disposed around a first portion of the TSV 302 and a second substantially helical conductor 304 ("conductor 304") disposed around a second portion of the TSV 302. In the illustrated embodiment, the first conductor 303 has two complete turns (303a and 303b) around the TSV 302, and the second conductor 304 has three complete turns (304a, 304b, and 304c) around the TSV 302. The first conductor 303 is operably connected to device pads 330a and 330b by leads 320a and 320b, respectively. The second conductor 304 can be operably connected by leads 321a and 321b to other circuit elements (not shown), including one or more rectifiers to revert a coupled alternating current to DC and one or more capacitors or other filter elements to provide steady current.

[0035] According to one embodiment, the first conductor 303 is configured to induce a magnetic field in the TSV 302 in response to a current passing through the conductor 303 (*e.g.*, provided by a voltage applied across the pads 330a and 330b). By changing the current passing through the first conductor 303 (*e.g.*, by applying an alternating current, or by repeatedly switching between high and low voltage states), a changing magnetic field can be induced in the TSV 302, which in turn induces a changing current in the second conductor 304. In this fashion, signals and/or power can be coupled between a circuit comprising the first conductor 303 and another comprising the second conductor 304 (*e.g.*, operating the device 300 as a power transformer).

[0036] As is shown in Figure 3, the first conductor 303 and the second conductor 304 have different numbers of turns. As will be readily understood by one skilled in the art, this arrangement allows the device 300 to be operated as a step-up or step-down transformer (depending upon which substantially helical conductor is utilized as the primary winding and which the secondary winding). For example, the application of a first changing current (*e.g.*, 2V of alternating current) to the first conductor 303 will induce a second changing current with a higher voltage (*e.g.*, 3V of alternating current) in the second conductor 304, given the 2:3 ratio of turns between the primary and secondary windings in this configuration. When operated as a step-down transformer (*e.g.*, by utilizing the second conductor 304 as the primary winding, and the first conductor 303 as the secondary winding), the application of a first changing current (*e.g.*, 3V of alternating current) to the second conductor 304 will induce a changing current with a lower voltage (*e.g.*, 2V of alternating current) in the first conductor 303, given the 3:2 ratio of turns between the primary and secondary windings in this configuration.

[0037] Although Figure 3 illustrates two substantially helical conductors or windings disposed around a TSV at two different heights (*e.g.*, coaxially but not concentrically), in other embodiments, multiple substantially helical conductors with different diameters can be provided at the same height (*e.g.*, with radially-spaced conductive turns in the same layers). As the inductance of a substantially helical conductor depends, at least in part, on its diameter and radial spacing from the TSV around which it is disposed, such an approach can be used where a reduction in the number of layer processing steps is more desirable than an increase in the inductance of the substantially helical conductor so radially spaced.

[0038] Although in the example of Figure 3 a pair of coupled inductors are shown with different numbers of turns in their windings, in other embodiments of the present technology coupled inductors can be provided with the same number of windings (*e.g.*, to couple two electrically isolated circuits without stepping up or down the voltage from the primary winding). For example, Figure 4 is a simplified cross-sectional view of coupled inductors sharing a through-substrate via core configured in accordance with an embodiment of the present technology. As can be seen with reference to Figure 4, a device 400 includes a substrate material 401a, an insulating material 401b, and a TSV 402. The TSV 402 extends out of the substrate material 401a and into the insulating material 402b. The device 400 also includes a first substantially helical conductor 403 ("conductor 403") disposed around a first portion of the TSV 402, a second substantially helical conductor 404 ("conductor 404") disposed around a second portion of the TSV 402, and a third substantially helical conductor 405 ("conductor 405")

disposed around a third portion of the TSV 402. In the present embodiment, each of the conductors 403, 404 and 405 is shown to include two complete turns (403a and 403b, 404a and 404b, and 405a and 405b, respectively) around the TSV 402. The first conductor 403 is operably connected to device pads 430a and 430b by leads 420a and 420b, respectively. The second conductor 404 can be operably connected to other circuit elements (not shown) by leads 421a and 421b, as can the third conductor 405 by corresponding leads 422a and 422b.

[0039] According to one embodiment, the first conductor 403 is configured to induce a magnetic field in the TSV 402 in response to a current passing through the first conductor 403 (*e.g.*, provided by a voltage differential applied across pads 430a and 430b). By changing the current passing through the first conductor 403 (*e.g.*, by applying an alternating current, or by repeatedly switching between high and low voltage states), a changing magnetic field can be induced in the TSV 402, which in turn induces a changing current in both the second conductor 404 and the third conductor 405. In this fashion, signals and/or power can be coupled between a circuit comprising the first conductor 403 and others comprising the second and third conductors 404 and 405.

[0040] The foregoing example embodiments illustrated in Figures 1 through 4 include inductors having an open core (*e.g.*, a core wherein the magnetic field passes through a higher magnetic permeability material for only part of the path of the magnetic field), but embodiments of the present technology can also be provided with a closed core (*e.g.*, a core in which a substantially continuous path of high magnetic permeability material passes through the middle of a conductive winding). For example, Figure 5 is a simplified cross-sectional view of a semiconductor device 50 having an inductor 500 with a closed core comprising multiple through-substrate vias configured in accordance with an embodiment of the present technology. As can be seen with reference to Figure 5, the device 50 includes a substrate material 501a and an insulating material 501b, and the inductor 500 has one portion in the substrate material 501a and another portion in the insulating material 501b. For example, the inductor 500 can include a first TSV 502a and a second TSV 502b, each having a first portion in the substrate material 501a and a second portion in the insulating material 501b. The TSVs 502a and 502b accordingly extend out of the substrate material 501a and into the insulating material 501b. The inductor can further include a substantially helical conductor 503 ("conductor 503") around at least a section of the second portion of the TSV 502a in the insulating material 501b. In the embodiment shown in Figure 5, the conductor 503 has five turns (503a, 503b, 503c, 503d, and 503e) around the

TSV 502a. The TSVs 502a and 502b are coupled above the conductor 503 by an upper coupling member 550a, and are coupled below the conductor 503 by a lower coupling member 550b.

[0041] The upper coupling member 550a and the lower coupling member 550b can include a magnetic material having a magnetic permeability higher than that of the substrate material 501a and/or the insulating material 501b. The magnetic material of the upper and lower coupling members 550a and 550b can be either the same material as the TSVs 502a and 502b, or a different material. The magnetic material of the upper and lower coupling members 550a and 550b can be a bulk material (*e.g.*, nickel, iron, cobalt, niobium, or an alloy thereof), or a laminated material with differing layers (*e.g.*, of magnetic material and non-magnetic material). Laminated layers of magnetic and non-magnetic material can help to reduce eddy current losses in the upper and lower coupling members 550a and 550b. In accordance with one aspect of the present technology, the first TSV 502a, the second TSV 502b, the upper coupling member 550a and the lower coupling member 550b can together provide a closed path for the magnetic field induced by the conductor 503 (illustrated with magnetic field lines, such as magnetic field line 560), such that the inductance of the inductor 500 is greater than it would be if only the first TSV 502a were provided.

[0042] Although in the example embodiment illustrated in Figure 5 an inductor with a completely closed core is illustrated, in other embodiments one or both of the upper and lower coupling members could be omitted. In such an embodiment, a second TSV with elevated magnetic permeability could be situated near a first TSV around which a winding is disposed to provide an open core embodiment with improved inductance over the single-TSV embodiments illustrated in Figures 1 through 4.

[0043] According to one embodiment, a closed magnetic core as illustrated by way of example in Figure 5 can provide additional space in which one or more additional windings can be disposed (*e.g.*, to provide a transformer or power couple). For example, Figure 6 is a simplified cross-sectional view of coupled inductors with through-substrate via cores configured in accordance with an embodiment of the present technology. As can be seen with reference to Figure 6, a device 600 includes a substrate material 601a, an insulating material 601b, and two TSVs 602a and 602b. The TSVs 602a and 602b extend out of the substrate material 601a and into the insulating material 601b. The device 600 also includes a first substantially helical conductor 603 ("conductor 603") with six turns disposed around the first TSV 602a, and a second substantially helical conductor 604 ("conductor 604"), also with six turns, disposed

around the second TSV 602b. The first conductor 603 is connected to other circuit elements (not shown) by leads 620a and 620b. The second conductor 604 is connected to pads 631a and 631b on a top surface of the device 600 by leads 621a and 621b, respectively. The TSVs 602a and 602b are coupled (a) above the first and second conductors 603 and 604 by an upper coupling member 650a, and (b) below the first and second conductors 603 and 604 by a lower coupling member 650b.

[0044] According to one embodiment, the first conductor 603 is configured to induce a magnetic field in the first and second TSVs 602a and 602b (as well as in the upper and lower coupling members 650a and 650b) in response to a current passing through the first conductor 603 (*e.g.*, provided by a voltage applied across leads 620a and 620b). By changing the current passing through the first conductor 603 (*e.g.*, by applying an alternating current, or by repeatedly switching between high and low voltage states), a changing magnetic field can be induced in the first and second TSVs 602a and 602b (as well as in the upper and lower coupling members 650a and 650b), which in turn induces a changing current in the second conductor 604. In this fashion, signals and/or power can be coupled between a circuit comprising the first conductor 603 (*e.g.*, in a device electrically coupled to leads 620a and 620b) and another circuit comprising the second conductor 604 (*e.g.*, in a device in another die electrically coupled via the pads 631a and 631b).

[0045] Although in the embodiment illustrated in Figure 6 two coupled inductors on proximate TSVs are shown with the same number of turns, in other embodiments of the present technology different numbers of windings can be provided on similarly-configured inductors. For example, Figure 7 is a simplified cross-sectional view of coupled inductors with through-substrate via cores configured in accordance with an embodiment of the present technology. As can be seen with reference to Figure 7, the device 700 includes a substrate material 701a, an insulating material 701b, and two TSVs 702a and 702b. The TSVs 702a and 702b extend out of the substrate material 701a and into the insulating material 701b. The device 700 also includes a first substantially helical conductor 703 ("conductor 703") with six turns disposed around the first TSV 702a, and a second substantially helical conductor 704 ("conductor 704") with four turns disposed around the second TSV 702b. The first conductor 703 can be operably connected to other circuit elements (not shown) by leads 720a and 720b. The second conductor 704 can be operably connected to other circuit elements (not shown) by leads 721a and 721b. The first and second TSVs 702a and 702b are coupled above the first and second conductors 703 and 704 by

an upper coupling member 750a, and are coupled below the first and second conductors 703 and 704 by a lower coupling member 750b.

[0046] According to one embodiment, the first conductor 703 is configured to induce a magnetic field in the first and second TSVs 702a and 702b (as well as in the upper and lower coupling members 750a and 750b) in response to a current passing through the first conductor 703. By changing the current passing through the first conductor 703 (*e.g.*, by applying an alternating current, or by repeatedly switching between high and low voltage states), a changing magnetic field can be induced in the first and second TSVs 702a and 702b (as well as in the upper and lower coupling members 750a and 750b, as shown above with reference to Figure 5), which in turn induces a changing current in the second conductor 704. In this fashion, signals and/or power can be coupled between a circuit comprising the first conductor 703 (*e.g.*, in a device electrically coupled via leads 720a and 720b) and another circuit comprising the second conductor 704 (*e.g.*, in a device electrically coupled via leads 721a and 721b).

[0047] The first conductor 703 and the second conductor 704 shown in Figure 7 have different numbers of turns. As will be readily understood by one skilled in the art, this arrangement allows the device 700 to be operated as a step-up or step-down transformer (depending upon which conductor is utilized as the primary winding and which the secondary winding). For example, the application of a first changing current (*e.g.*, 3V of alternating current) to the second conductor 704 will induce a second changing current with lower voltage (*e.g.*, 2V of alternating current) in the first conductor 703, given the 6:4 ratio of turns between the primary and secondary windings in this configuration.

[0048] Although in the embodiments illustrated in Figures 6 and 7 devices with an equal number of TSVs and windings are illustrated, other embodiments of the present technology can provide more than one winding on either or both of a pair of proximate or coupled TSVs. For example, Figure 8 is a simplified cross-sectional view of coupled inductors with through-substrate via cores configured in accordance with an embodiment of the present technology. As can be seen with reference to Figure 8, the device 800 includes a substrate material 801a, an insulating material 801b, and two TSVs 802a and 802b. The TSVs 802a and 802b extend out of the substrate material 801a and into the insulating material 801b. The device 800 also includes a first substantially helical conductor 803 ("conductor 803") with three turns around a first portion of the first TSV 802a, and a second substantially helical conductor 804 ("conductor 804") with two turns around a second portion of the first TSV 802a. The device further includes a third

substantially helical conductor 805 ("conductor 805") with six turns around the second TSV 802b. The first conductor 803 can be operably connected to other circuit elements (not shown) by leads 820a and 820b, the second conductor 804 can be operably connected to other circuit elements (not shown) by leads 821a and 821b, and the third conductor 805 can be operably connected to other circuit elements (not shown) by leads 822a and 822b. The first and second TSVs 802a and 802b are coupled (a) above the three conductors 803, 804 and 805 by an upper coupling member 850a, and (b) below the three conductors 803, 804 and 805 by a lower coupling member 850b.

[0049] According to one embodiment, the first conductor 803 is configured to induce a magnetic field in the first and second TSVs 802a and 802b (as well as in the upper and lower coupling members 850a and 850b) in response to a current passing through the first conductor. By changing the current passing through the first conductor 803 (*e.g.*, by applying an alternating current, or by repeatedly switching between high and low voltage states), a changing magnetic field can be induced in the first TSV 802a and the second TSV 802b (as well as in the upper and lower coupling members 850a and 850b), which in turn induces a second changing current in the second conductor 804 and a third changing current in the third conductor 805. In this fashion, signals and/or power can be coupled between a circuit comprising the first conductor 803 and other circuits comprising the second conductor 804 and the third conductor 805.

[0050] Although in the embodiments illustrated in Figures 5 through 8 a single additional TSV is provided to enhance the magnetic permeability of the return path for the magnetic field generated by a primary winding around a TSV, in other embodiments of the present technology multiple return path TSVs can be provided to further improve the inductance of the inductors so configured. For example, Figure 9 is a simplified cross-sectional view of a semiconductor device 90 including an inductor 900 with a closed core configured in accordance with an embodiment of the present technology. Referring to Figure 9, the device 900 includes a substrate material 901a and an insulating material 901b, and the inductor 900 has one portion in the substrate material 901a and another portion in the insulating material 901b. For example, the inductor 900 can include three TSVs 902a, 902b and 902c, each having a first portion in the substrate material 901a and a second portion in the insulating material 901b. The three TSVs 902a, 902b and 902c accordingly extend out of the substrate material 901a and into the insulating material 901b. The inductor 900 can further include a substantially helical conductor 903 ("conductor 903") with five turns around the first TSV 902a. The three TSVs 902a, 902b and 902c are coupled (a) above the conductor 903 by an upper coupling member 950a, and (b) below the conductor 903 by a

lower coupling member 950b. In accordance with one aspect of the present technology, the three TSVs 902a, 902b and 902c, together with the upper and lower coupling members 950a and 950b, provide a closed path for the magnetic field generated by the conductor 903 such that the inductance of the inductor 900 is greater than it would be if only the first TSV 902a were provided.

[0051] Although in the example embodiment illustrated in Figure 9 an inductor with a completely closed core (*e.g.*, a core in which a continuous path of high magnetic permeability material passes through the middle of a winding) is illustrated, in other embodiments one or both of upper and lower coupling members could be omitted. In such an embodiment, multiple additional TSVs (*e.g.*, in addition to the TSV around which the winding is disposed) with elevated magnetic permeability could be situated near the TSV around which the winding is disposed to provide an open core embodiment with improved inductance.

[0052] For example, Figure 10 is a simplified cross-sectional view of a semiconductor device 1010 including an inductor 1000 with a through-substrate via core configured in accordance with an embodiment of the present technology. In this embodiment, the device 1010 includes a substrate material 1001a and an insulating material, and the inductor 1000 has one portion in the substrate material 1001a and another portion in the insulating material 1001b. For example, the inductor 1000 can include three TSVs 1002a, 1002b and 1002c that each have a first portion in the substrate material 1001a and a second portion in the insulating material 1001b. The three TSVs 1002a, 1002b and 1002c accordingly extend out of the substrate material 1001a and into the insulating material 1001b. The inductor 1000 can further include a substantially helical conductor 1003 ("conductor 1003") with five turns around the first TSV 1002a. In accordance with one aspect of the present technology, the additional TSVs 1002b and 1002c contribute to a high magnetic permeability path for the magnetic field induced by the conductor 1003 (and illustrated with magnetic field lines, such as magnetic field line 1060) such that the inductance of the inductor 1000 is greater than it would be if only the first TSV 1002a were provided.

[0053] Although in the foregoing examples set forth in Figures 1 to 10 each substantially helical conductor has been illustrated as having a single turn about a TSV at a given distance from the surface of the substrate, in other embodiments a substantially helical conductor can have more than one turn about a TSV at the same distance from the substrate surface (*e.g.*, multiple turns arrange coaxially at each level). For example, Figure 11 is a simplified

perspective view of a substantially helical conductor 1104 ("conductor 1104") disposed around a through-substrate via 1102 configured in accordance with an embodiment of the present technology. As can be seen with reference to Figure 11, the conductor 1104 includes a first substantially helical conductor 1104a ("conductor 1104a") disposed around the TSV 1102, which is connected to a second coaxially-aligned substantially helical conductor 1104b ("conductor 1104b"), such that a single conductive path winds downward around TSV 1102 at a first average radial distance, and winds back upward around TSV 1102 at a second average radial distance. Accordingly, the conductor 1104 includes two turns about the TSV 1102 (*e.g.*, the topmost turn of conductor 1104a and the topmost turn of conductor 1104b) at the same position along the longitudinal dimension "L" of the TSV 1102. In another embodiment, a substantially helical conductor could make two turns about a TSV at a first level (*e.g.*, spiraling outward), two turns about a TSV at a second level (*e.g.*, spiraling inward), and so on in a similar fashion for as many turns as were desired.

[0054] Figures 12A-12F are simplified views of a device 1200 having an inductor with a through-substrate via core in various states of a manufacturing process in accordance with an embodiment of the present technology. In Figure 12A, a substrate 1201 is provided in anticipation of further processing steps. The substrate 1201 may be any one of a number of substrate materials, including silicon, glass, gallium arsenide, gallium nitride, an organic laminate, or the like. In Figure 12B, a first turn 1203 of a substantially helical conductor has been disposed in a layer of the insulating material 1202 over the substrate 1201. The insulating material 1202 can be any one of a number of insulating materials which are suitable for semiconductor processing, including silicon oxide, silicon nitride, polyimide, or the like. The first turn 1203 can be any one of a number of conducting materials which are suitable for semiconductor processing, including copper, gold, tungsten, alloys thereof, or the like.

[0055] In Figure 12C, a second turn 1204 of the substantially helical conductor has been disposed in the now thicker layer of the insulating material 1202, and spaced from the first turn 1203 by a layer of the insulating material 1202. The second turn 1204 is electrically connected to the first turn 1203 by a first via 1205. A second via 1206 has also been provided to route an end of the first turn 1203 to an eventual higher layer of the device 1200. In Figure 12D, a third turn 1207 of the substantially helical conductor has been disposed in the now thicker layer of the insulating material 1202, and spaced from the second turn 1204 by a layer of the insulating material 1202. The third turn 1207 is electrically connected to the second turn 1204 by a third

via 1208. The second via 1206 has been further extended to continue routing an end of the first turn 1203 to an eventual higher layer of the device 1200.

[0056] Turning to Figure 12E, the device 1200 is illustrated in a simplified perspective view after an opening 1209 has been etched through the insulating material 1202 and into the substrate 1201. The opening 1209 is etched substantially coaxially with the turns 1203, 1204 and 1207 of the substantially helical conductor using any one of a number of etching operations capable of providing a substantially vertical opening with a high aspect ratio. For example, deep reactive ion etching, laser drilling, or the like can be used to form the opening 1209. In Figure 12F, a TSV 1210 has been disposed in the opening 1209. The TSV 1210 can include a magnetic material (*e.g.*, a material with a higher magnetic permeability than the substrate 1201 and/or the insulating material 1202) to increase the magnetic field in the TSV 1210 when current is flowing through the substantially helical conductor. The magnetic material can be ferromagnetic, ferrimagnetic, or a combination thereof. The TSV 1210 can include more than one material, either in a bulk material of a single composition, or in discrete regions of different materials (*e.g.*, coaxial laminate layers). For example, the TSV 1210 can include nickel, iron, cobalt, niobium, or an alloy thereof. Laminated layers of magnetic and non-magnetic material can help to reduce eddy current losses in the TSV 1210. The TSV 1210 can be provided in a single metallization step filling in the opening 1209, or in multiple steps of laminating layers (*e.g.*, multiple magnetic layers separated by non-magnetic layers). In one embodiment, to provide a TSV with a multiple layer structure, a mixture of conformal and bottom-up fill plating operations can be utilized (*e.g.*, a conformal plating step to partially fill and narrow the etched opening with a first material, and a subsequent bottom-up plating step to completely fill the narrowed opening with a second material).

[0057] Figure 13 is a flow chart illustrating a method of manufacturing an inductor with a through-substrate via core in accordance with an embodiment of the present technology. The method begins in step 1310, in which a substrate is provided. In step 1320, a substantially helical conductor is disposed in an insulating material over the substrate. In step 1330, an opening is etched through the insulating material and into the substrate along an axis of the substantially helical conductor. In step 1340, a TSV is disposed into the opening.

[0058] From the foregoing, it will be appreciated that specific embodiments of the invention have been described herein for purposes of illustration, but that various modifications

may be made without deviating from the scope of the invention. Accordingly, the invention is not limited except as by the appended claims.

CLAIMS

I/We claim:

1. A semiconductor device, comprising:
a substrate,
a through-substrate via (TSV) extending into the substrate, and
a substantially helical conductor disposed around the TSV.

2. The semiconductor device of claim 1, wherein the substantially helical conductor is configured to generate a magnetic field in the TSV in response to a current passing through the substantially helical conductor.

3. The semiconductor device of claim 2, wherein the substantially helical conductor is configured to induce a change in the magnetic field in the TSV in response to a changing current in the substantially helical conductor.

4. The semiconductor device of claim 1, wherein the TSV comprises a ferromagnetic or a ferrimagnetic material.

5. The semiconductor device of claim 1, wherein the TSV is separated from the substantially helical conductor by an insulating material.

6. The semiconductor device of claim 1, wherein the substantially helical conductor comprises more than one turn around the TSV.

7. The semiconductor device of claim 1, wherein the substantially helical conductor is coaxially aligned with the TSV.

8. A semiconductor device, comprising:
a substrate,
a through-substrate via (TSV) extending into the substrate,

a first substantially helical conductor disposed around the TSV, and

a second substantially helical conductor disposed around the TSV.

9. The semiconductor device of claim 8, wherein the first substantially helical conductor is configured to induce a change in a magnetic field in the TSV in response to a first changing current in the first substantially helical conductor, and wherein the second substantially helical conductor is configured to have a second changing current induced therein in response to the change in the magnetic field.

10. The semiconductor device of claim 9, further comprising:

a third substantially helical conductor disposed around the TSV,

wherein the third substantially helical conductor is configured to have a third changing current induced therein in response to the change in the magnetic field.

10. The semiconductor device of claim 8, wherein the TSV comprises a ferromagnetic or a ferrimagnetic material.

11. The semiconductor device of claim 8, wherein the TSV is separated from the first and second substantially helical conductors by an insulating material.

12. The semiconductor device of claim 8, wherein the first substantially helical conductor comprises a different number of turns around the TSV than the second substantially helical conductor.

13. The semiconductor device of claim 8, wherein the first and second substantially helical conductors comprise a same number of turns around the TSV.

14. The semiconductor device of claim 8, wherein one of the first and second substantially helical conductors comprises more than one turn around the TSV.

15. The semiconductor device of claim 8, wherein the first and second substantially helical conductors are coaxially aligned with the TSV.

16. The semiconductor device of claim 8, wherein the first substantially helical conductor and the second substantially helical conductor are electrically isolated from each other and from the TSV.

17. The semiconductor device of claim 8, wherein the first substantially helical conductor is electrically connected to a power supply and the second substantially helical conductor is electrically connected to a load.

18. A semiconductor device, comprising:
a substrate,
a first through-substrate via (TSV) extending into the substrate,
a second TSV extending into the substrate,
a first substantially helical conductor disposed around the first TSV, and
a second substantially helical conductor disposed around the second TSV.

19. The semiconductor device of claim 18, wherein the first substantially helical conductor is configured to induce a change in a magnetic field in the first TSV and the second TSV in response to a first changing current in the first substantially helical conductor, and wherein the second substantially helical conductor is configured to have a second changing current induced therein in response to the change in the magnetic field in the second TSV.

20. The semiconductor device of claim 19wherein the first TSV is coupled to the second TSV by an upper coupling member above the first and second substantially helical conductors, and by a lower coupling member below the first and second substantially helical conductors, such that the first and second TSVs and the upper and lower coupling members form a closed path for the magnetic field.

21. The semiconductor device of claim 18, wherein each of the first and second TSVs comprise a ferromagnetic or a ferrimagnetic material.

22. The semiconductor device of claim 18, wherein the first TSV is electrically insulated from the first substantially helical conductor, and the second TSV is electrically insulated from the second substantially helical conductor.

23. The semiconductor device of claim 18, wherein the first substantially helical conductor and the second substantially helical conductor are electrically isolated from each other and from the first and second TSVs.

24. The semiconductor device of claim 18, wherein the first substantially helical conductor comprises a different number of turns around the first TSV than the second substantially helical conductor comprises around the second TSV.

25. The semiconductor device of claim 18, wherein the first substantially helical conductor comprises a same number of turns around the first TSV as the second substantially helical conductor comprises around the second TSV.

26. The semiconductor device of claim 18, wherein the first substantially helical conductor comprises more than one turn around the first TSV.

27. The semiconductor device of claim 18, wherein the second substantially helical conductor comprises more than one turn around the second TSV.

28. The semiconductor device of claim 18, wherein the first substantially helical conductor is coaxially aligned with the first TSV, and the second substantially helical conductor is coaxially aligned with the second TSV.

29. The semiconductor device of claim 18, wherein the first substantially helical conductor is electrically connected to a power supply and the second substantially helical conductor is electrically connected to a load.

30. A semiconductor device, comprising:
a substrate,
a through-substrate via (TSV) extending into the substrate, and
a non-planar spiral conductor disposed around the TSV.

31. The semiconductor device of claim 30, wherein the non-planar spiral conductor is configured to generate a magnetic field in the TSV in response to a current passing through the non-planar spiral conductor.

32. The semiconductor device of claim 31, wherein the non-planar spiral conductor is configured to induce a change in the magnetic field in the TSV in response to a changing current in the non-planar spiral conductor.

33. The semiconductor device of claim 30, wherein the TSV comprises a ferromagnetic or a ferrimagnetic material.

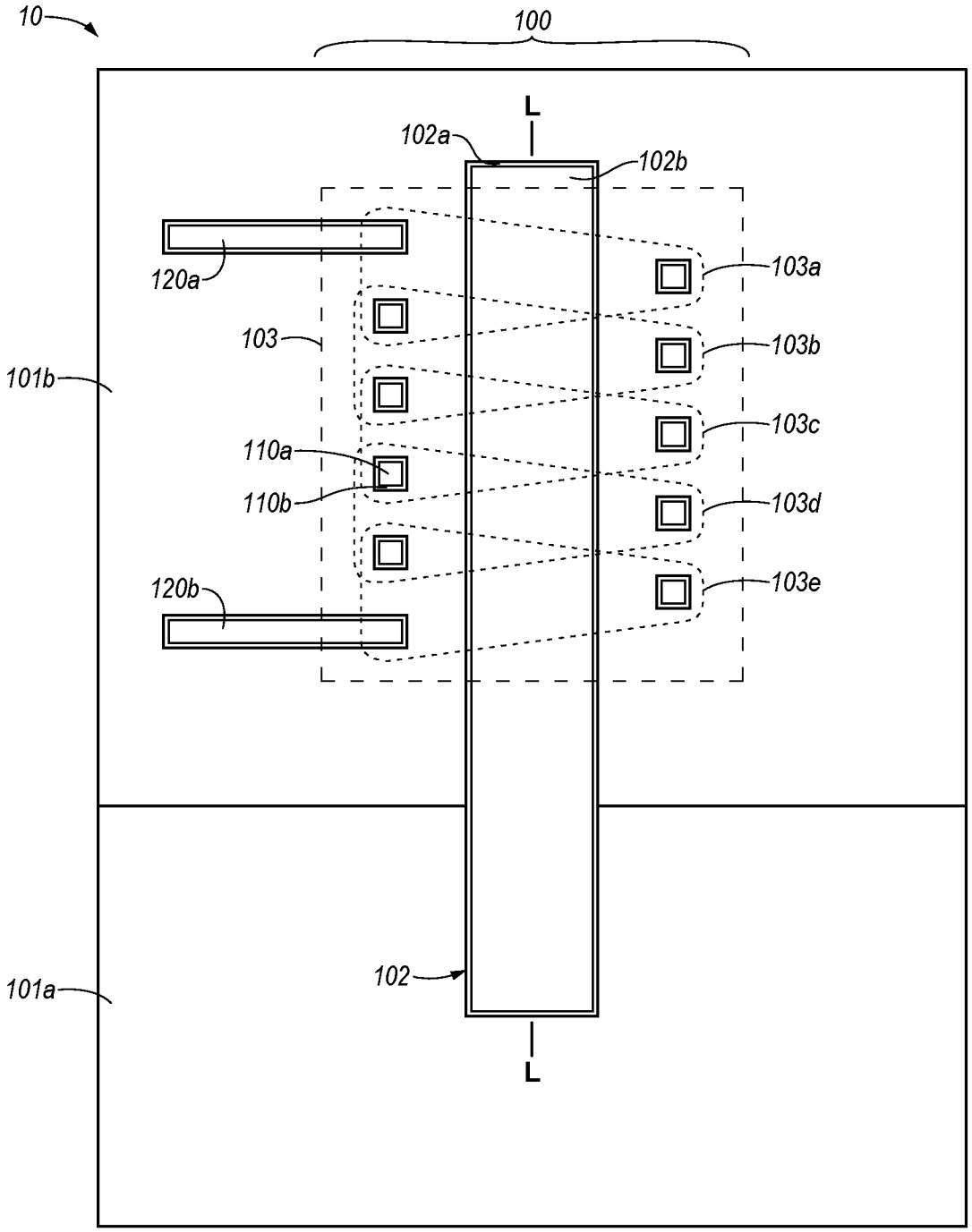

10
100
L
102a
102b
120a
103a
103
103b
101b
103c
110a
110b
103d
103e
120b
102
101a
L

Fig. 1

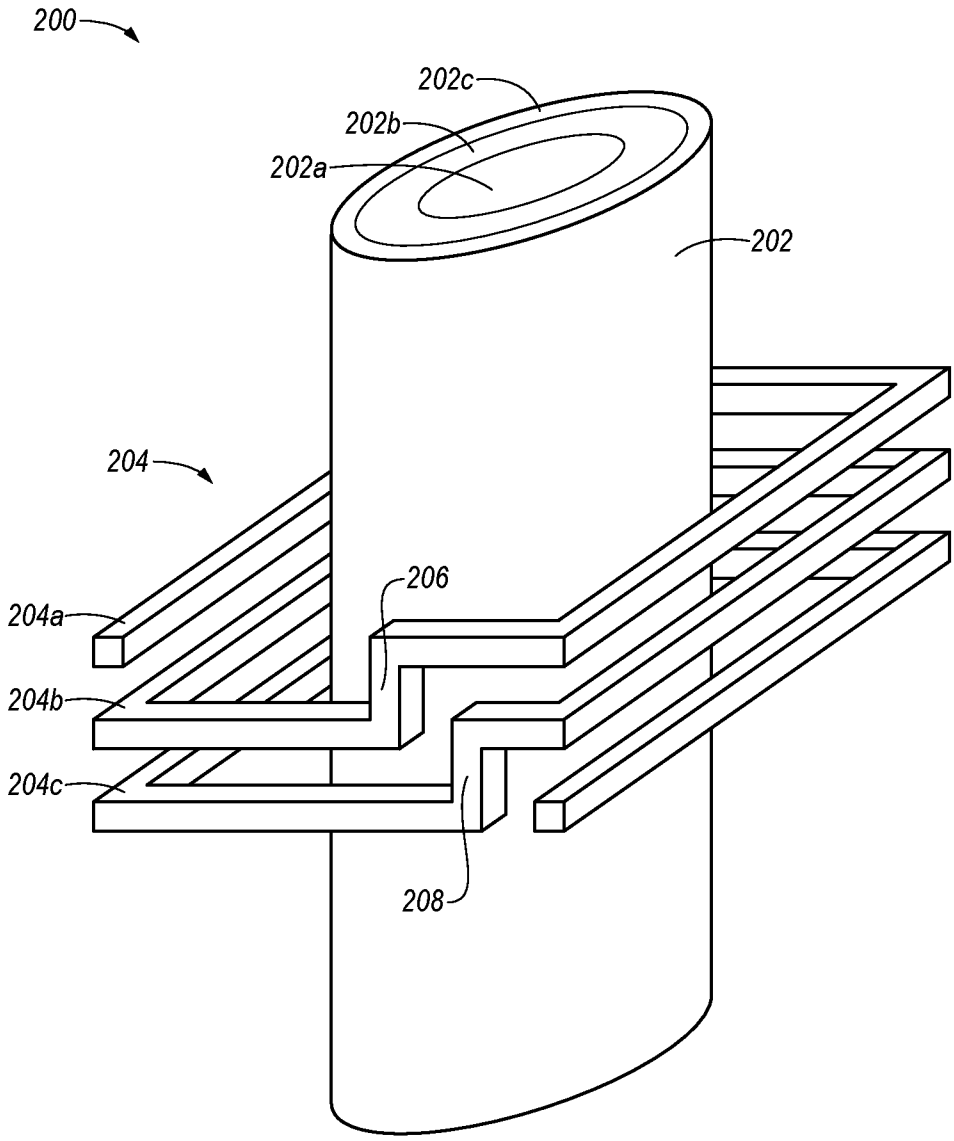


Fig. 2

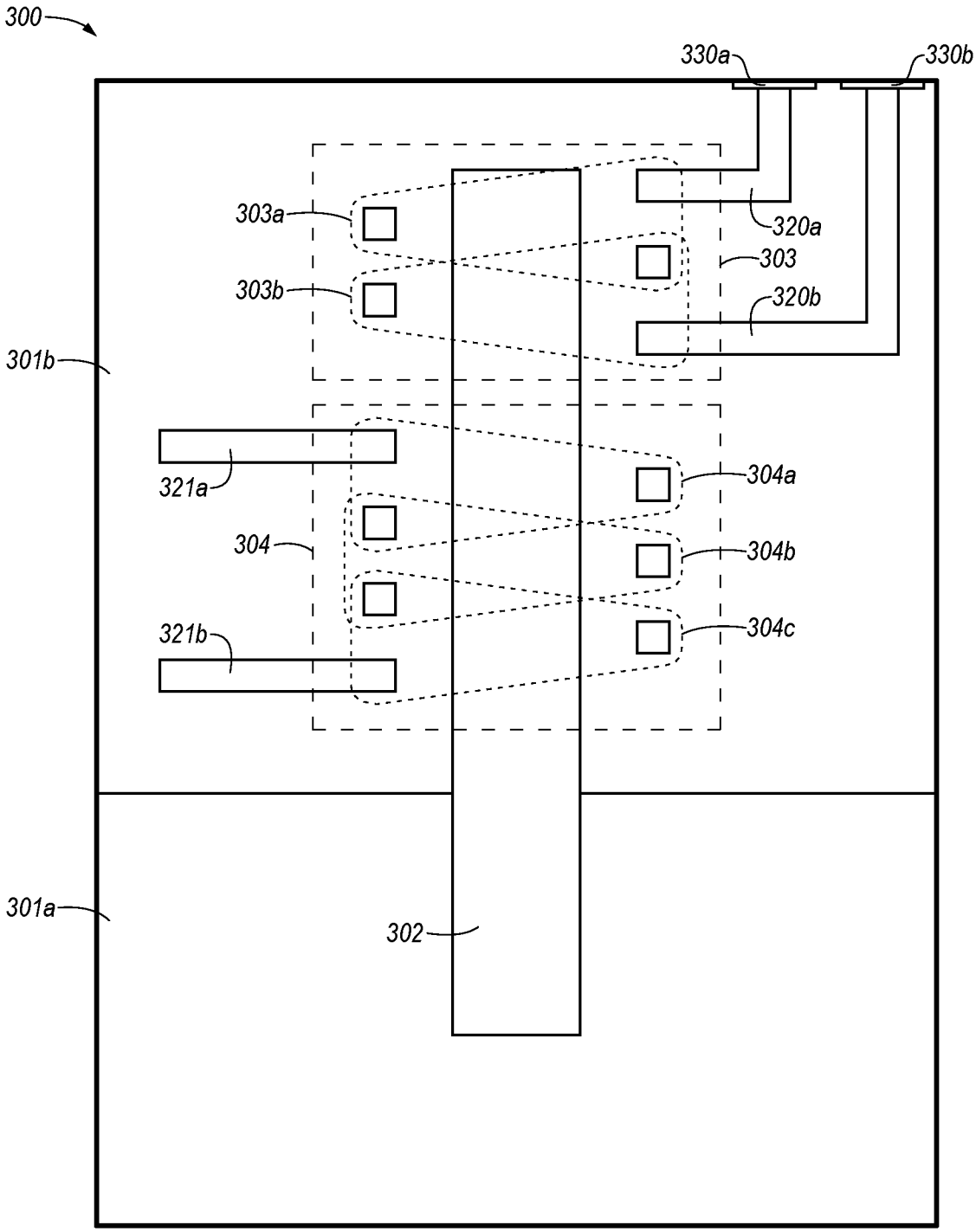

300
330a
330b
303a
303b
303
320a
320b
301b
321a
304a
304
304b
321b
304c
301a
302

Fig. 3

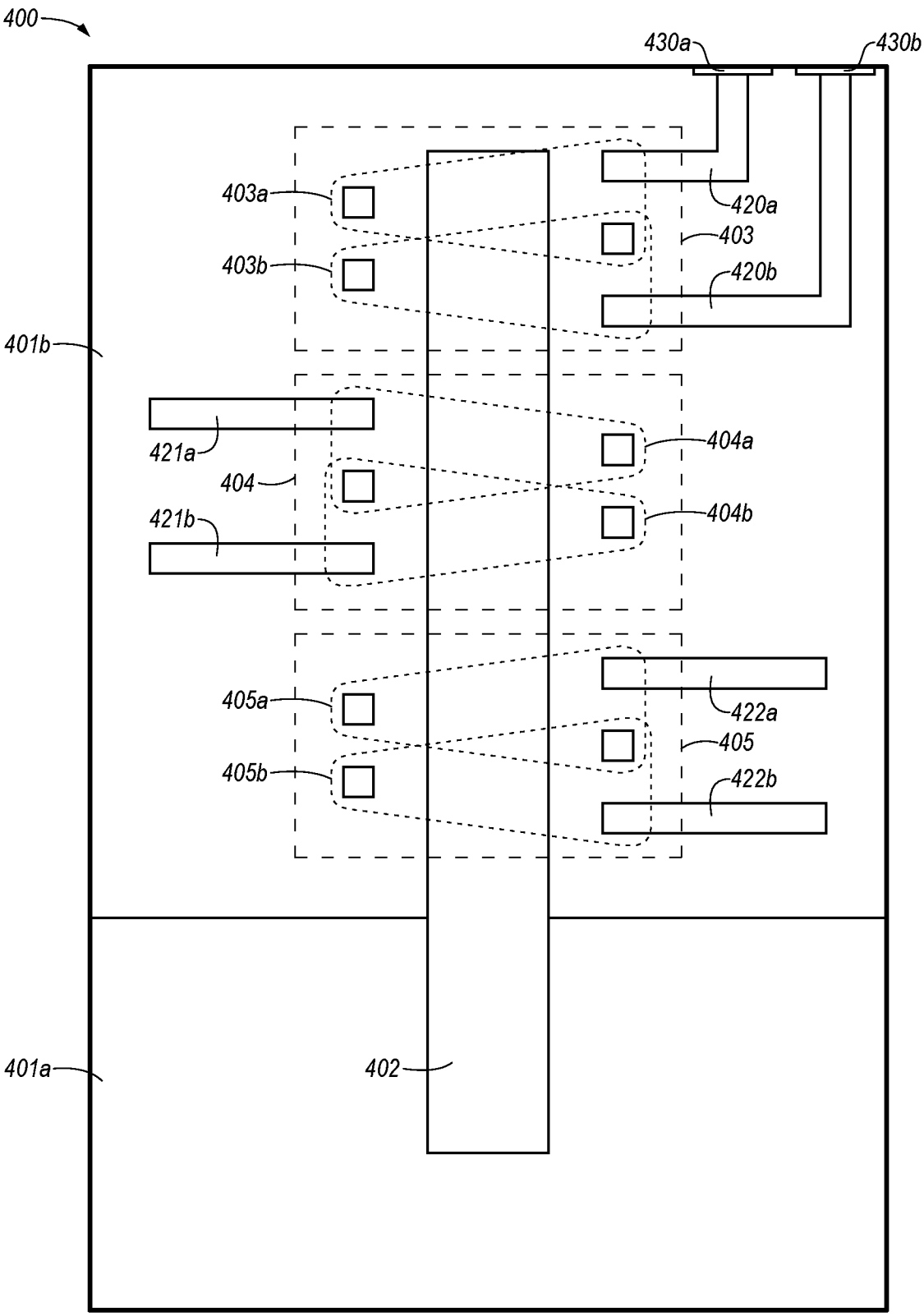

400
430a
430b
403a
403b
403
420a
420b
401b
421a
404
421b
404a
404b
405a
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422a
422b
401a
402

Fig. 4

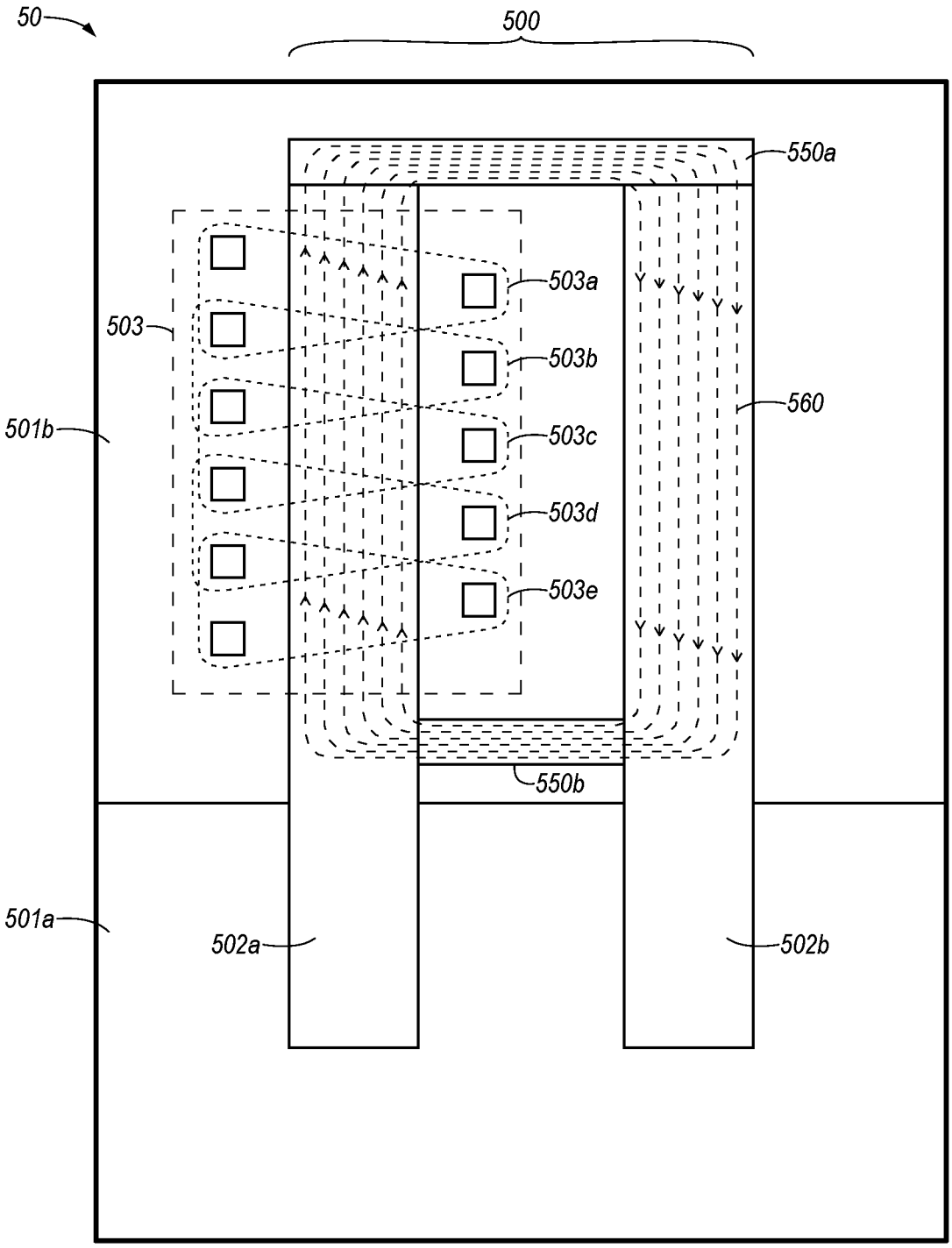

50
500
550a
503a
503
503b
503c
560
501b
503d
503e
550b
501a
502a
502b

Fig. 5

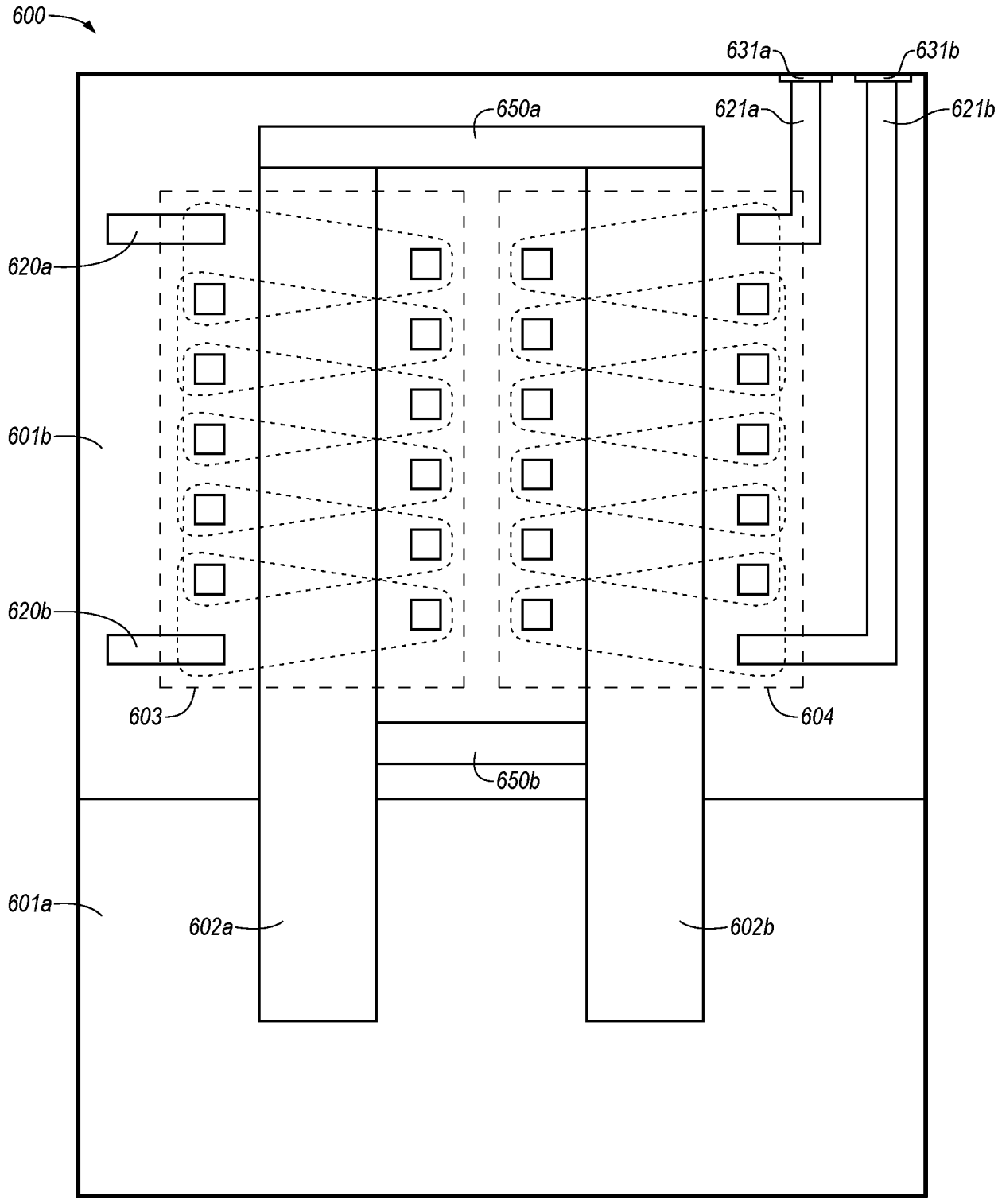

600
631a
631b
650a
621a
621b
620a
601b
620b
603
604
650b
601a
602a
602b

Fig. 6

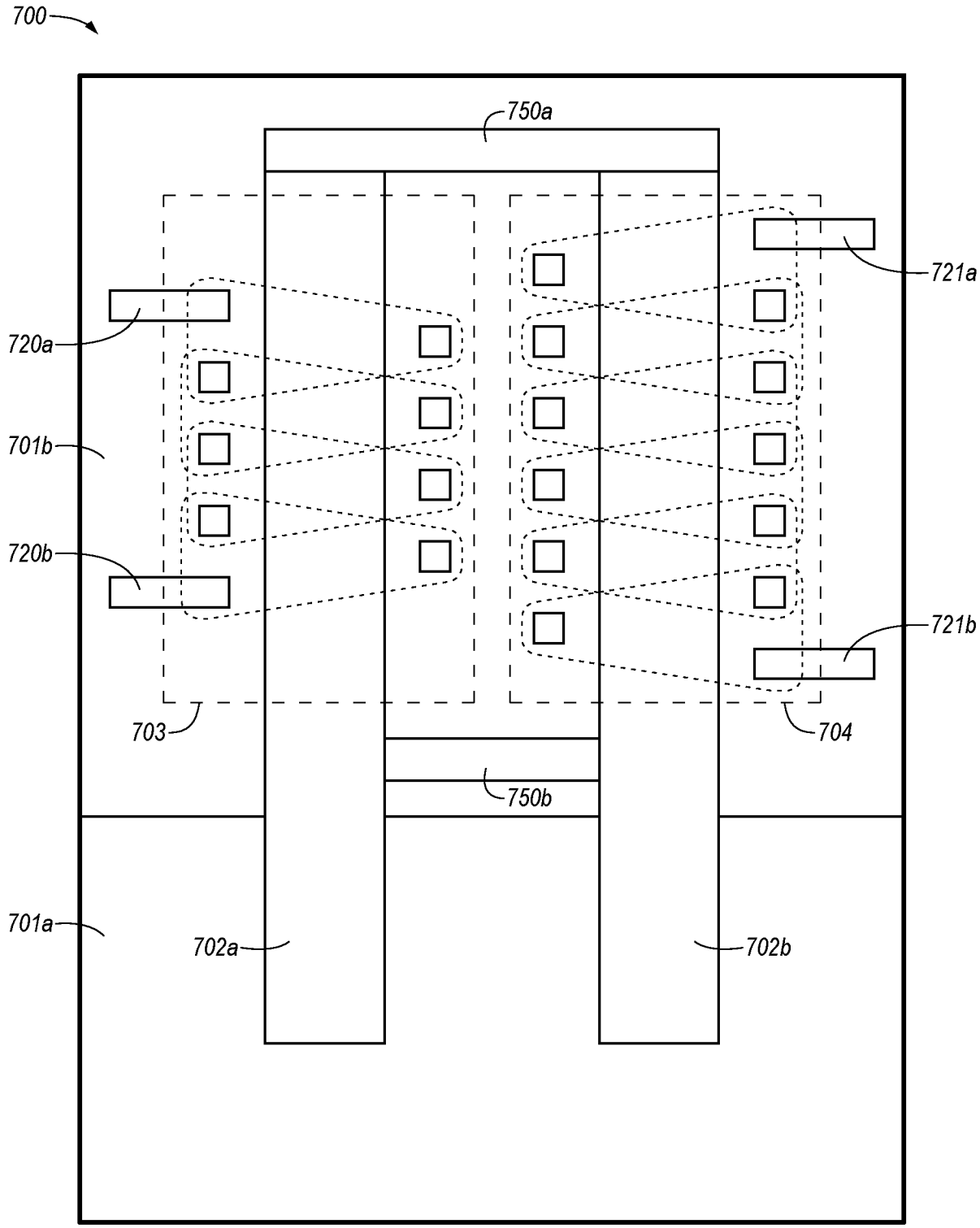


Fig. 7

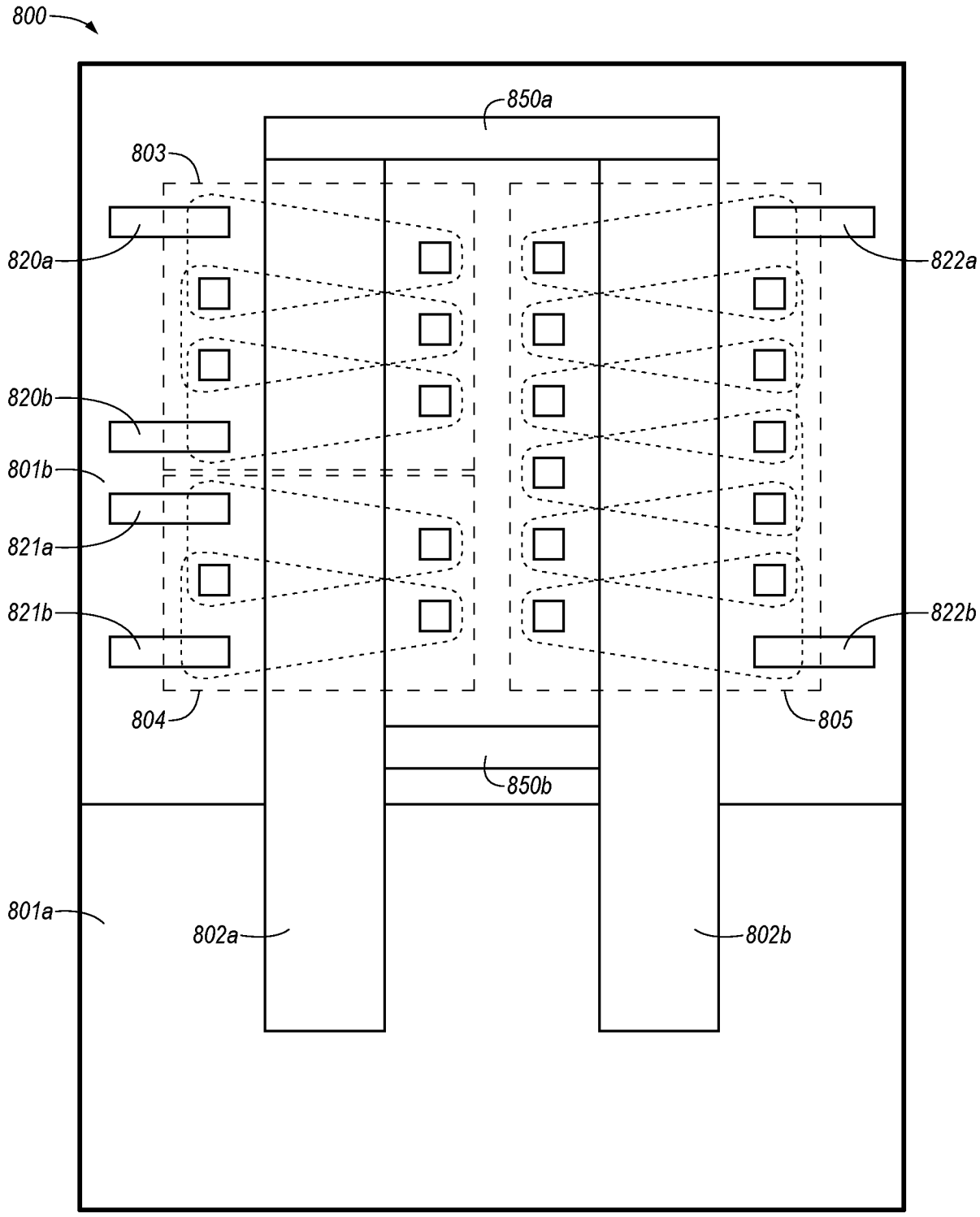

800
850a
803
820a
822a
820b
801b
821a
821b
822b
804
805
850b
801a
802a
802b

Fig. 8

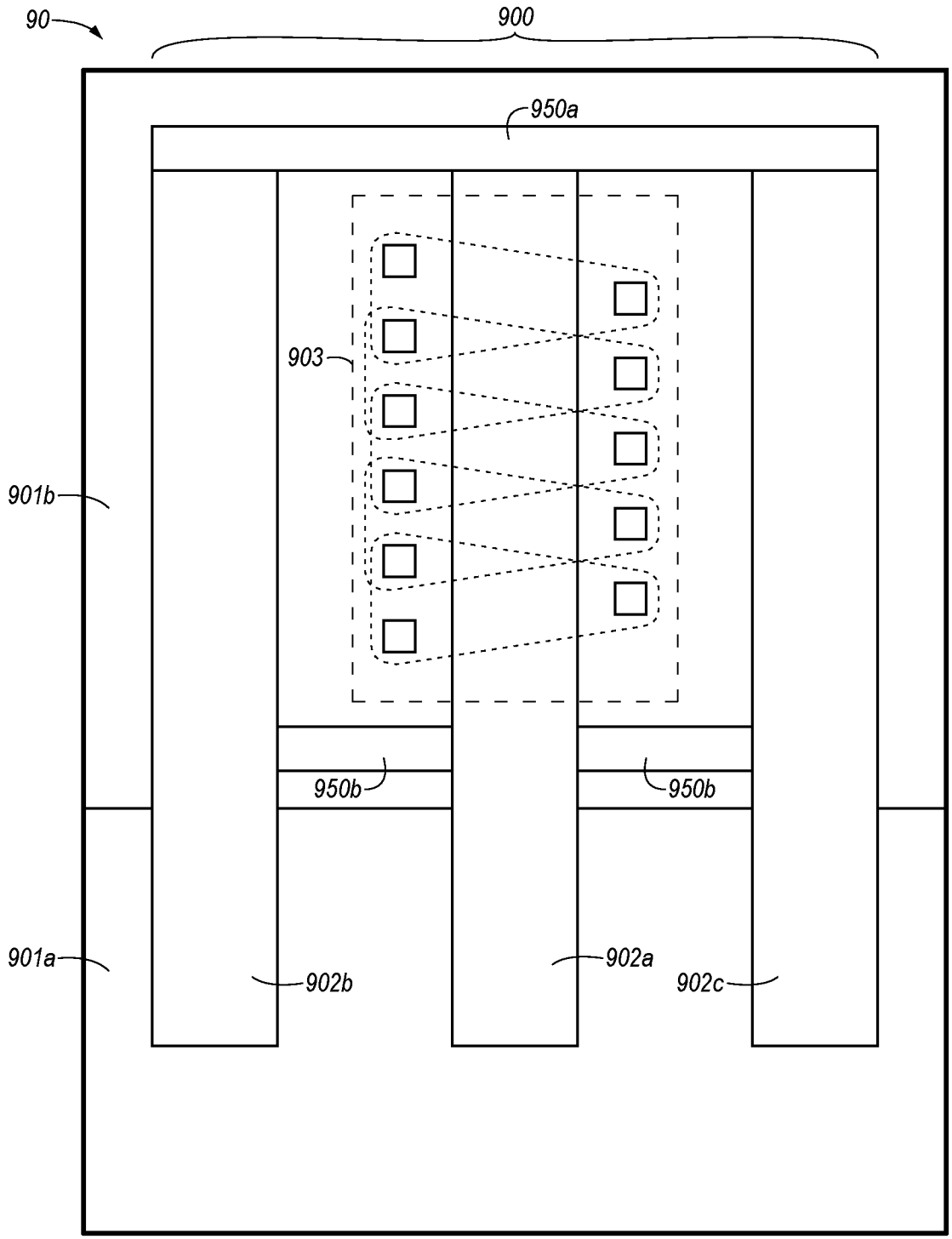


Fig. 9

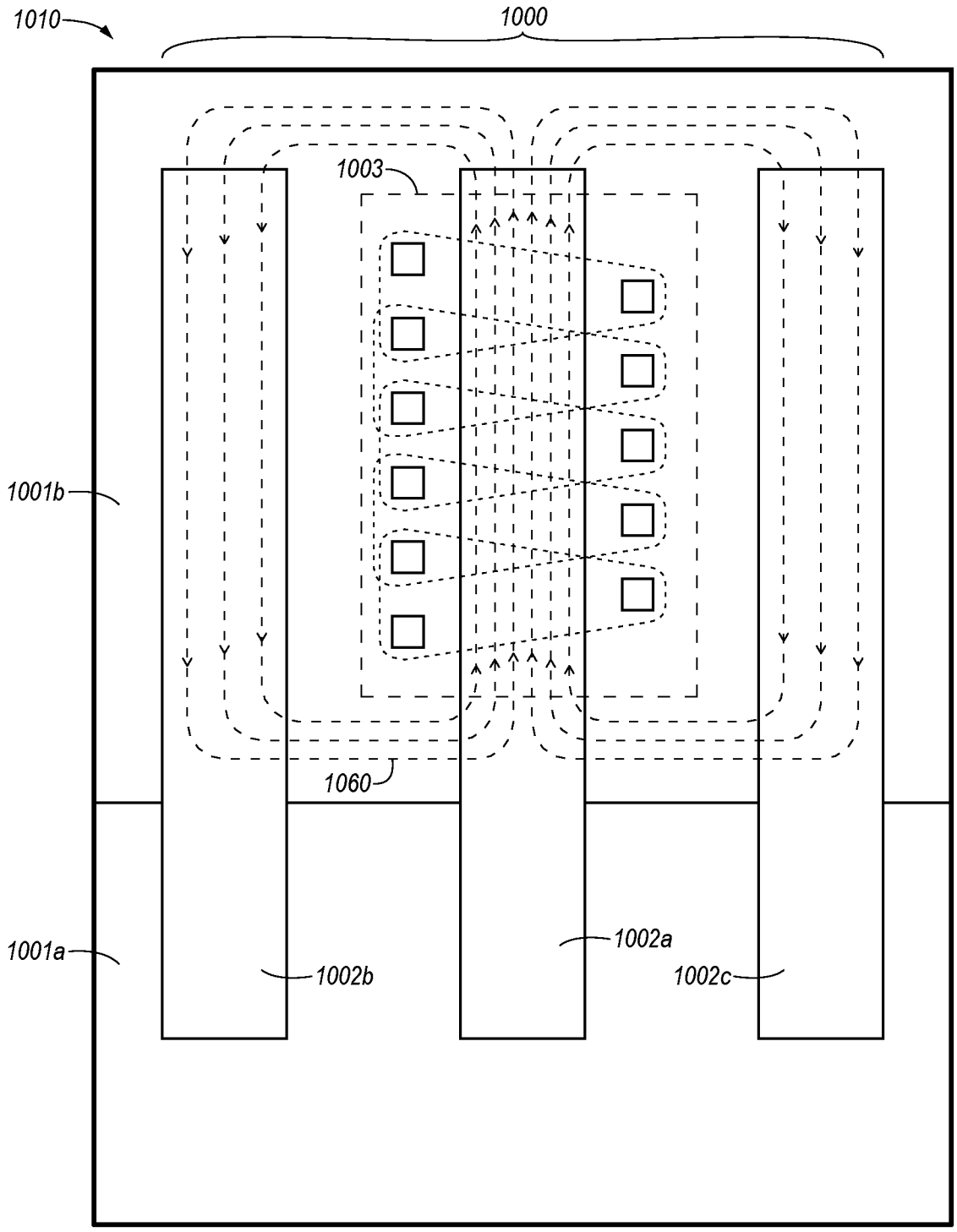


Fig. 10

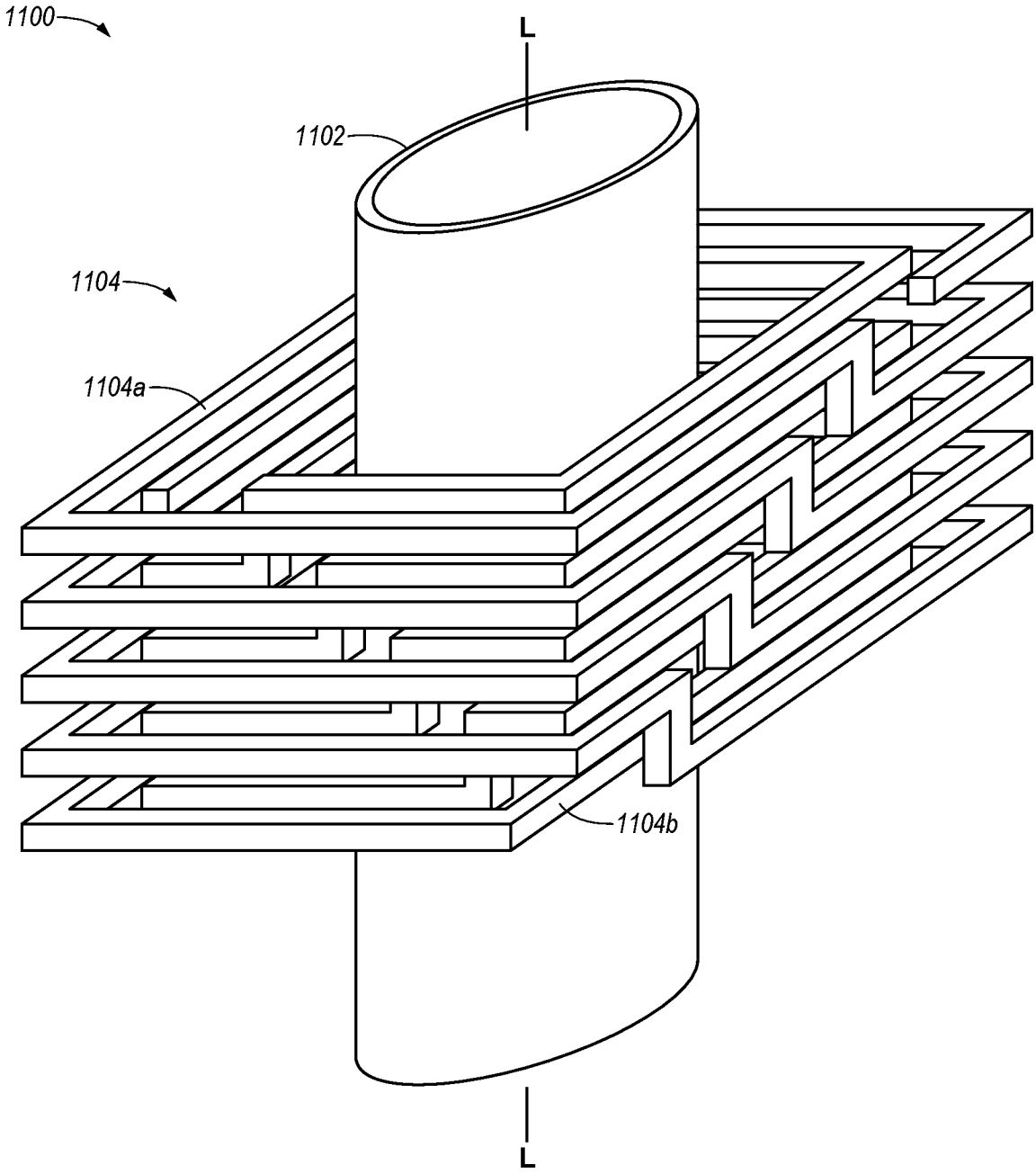


Fig. 11

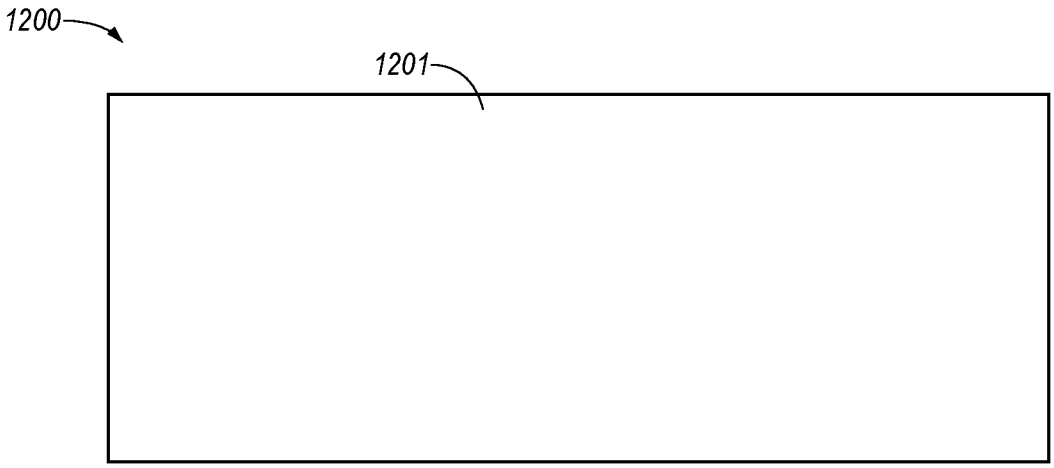


Fig. 12A

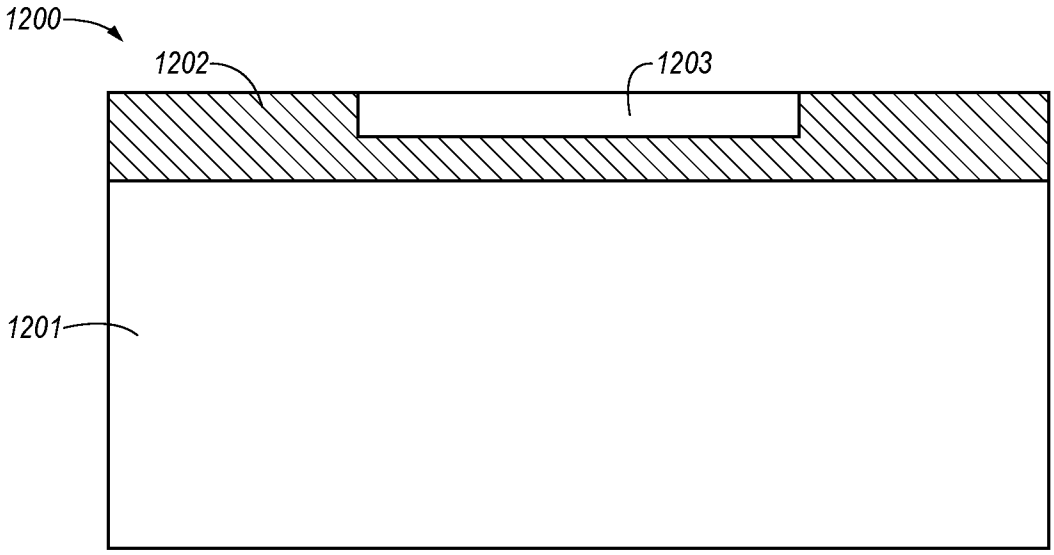


Fig. 12B

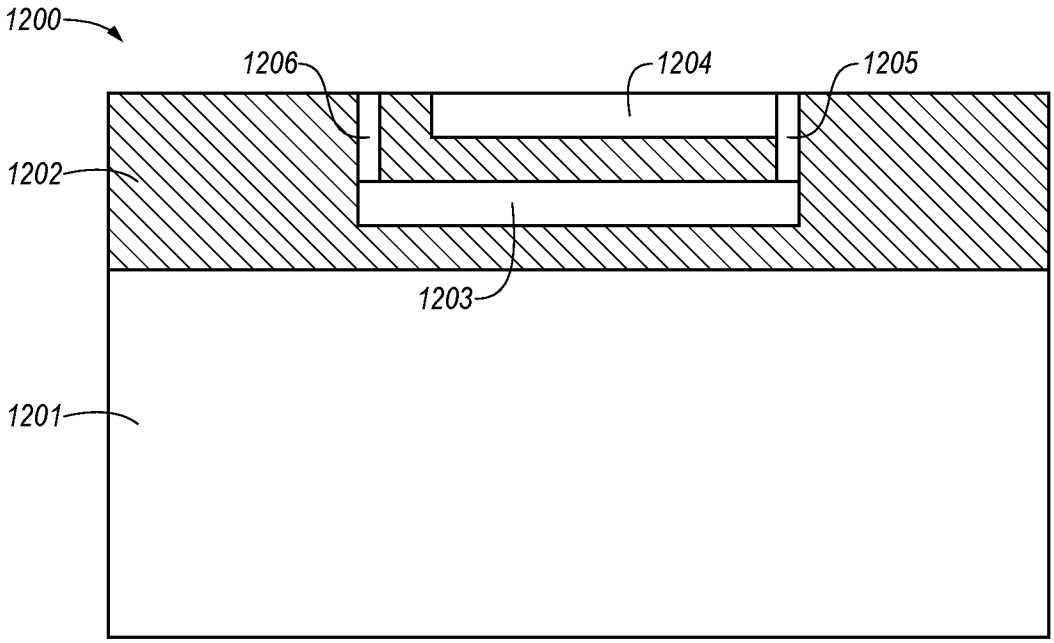


Fig. 12C

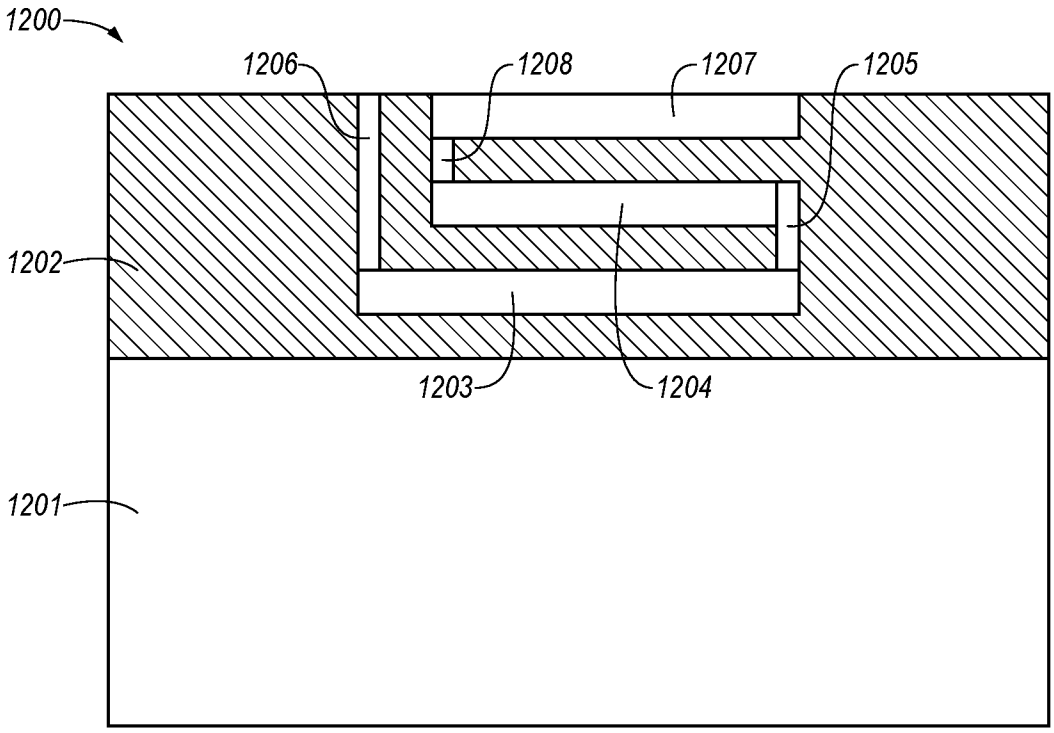


Fig. 12D

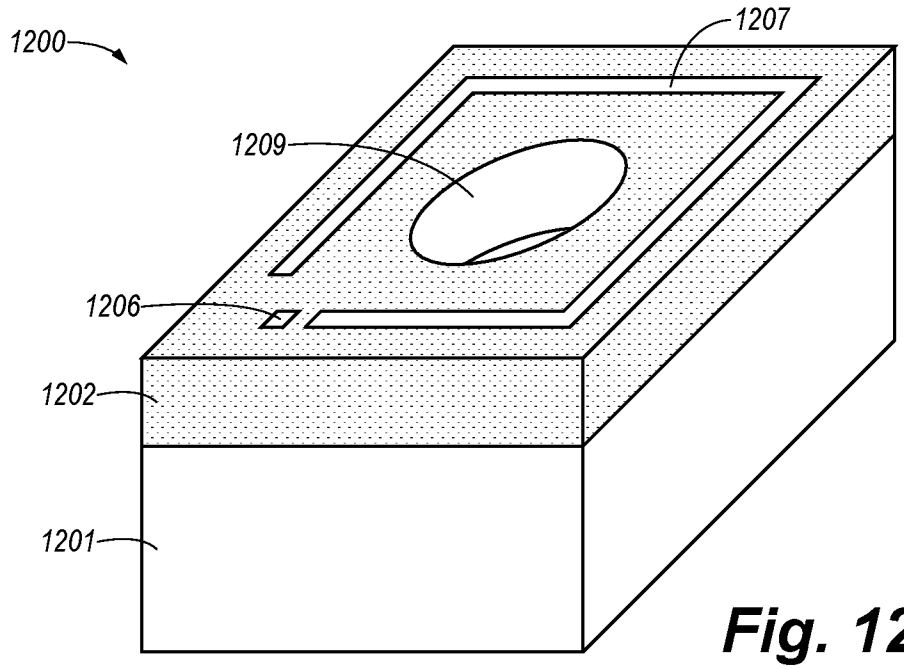


Fig. 12E

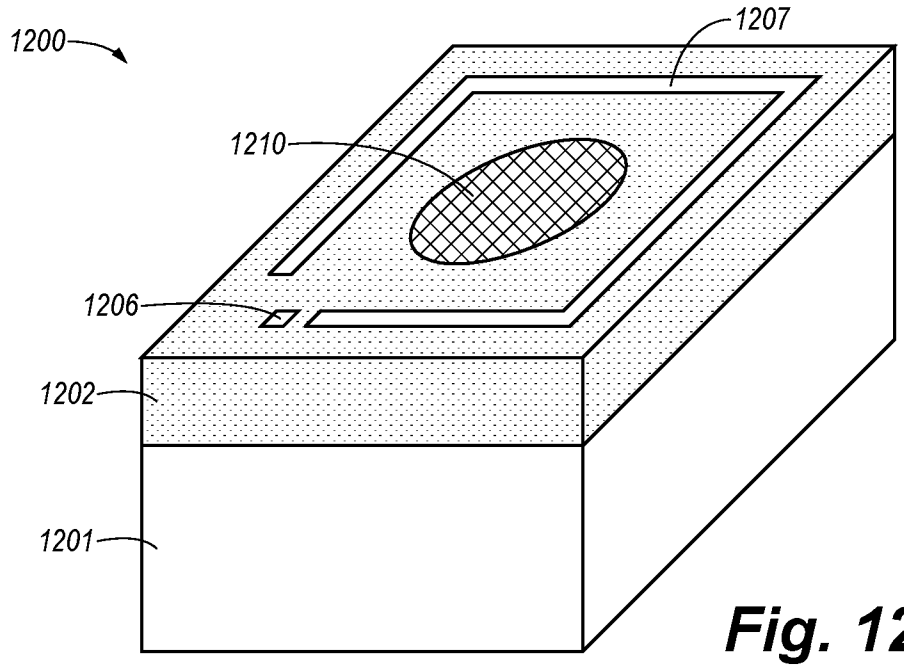


Fig. 12F

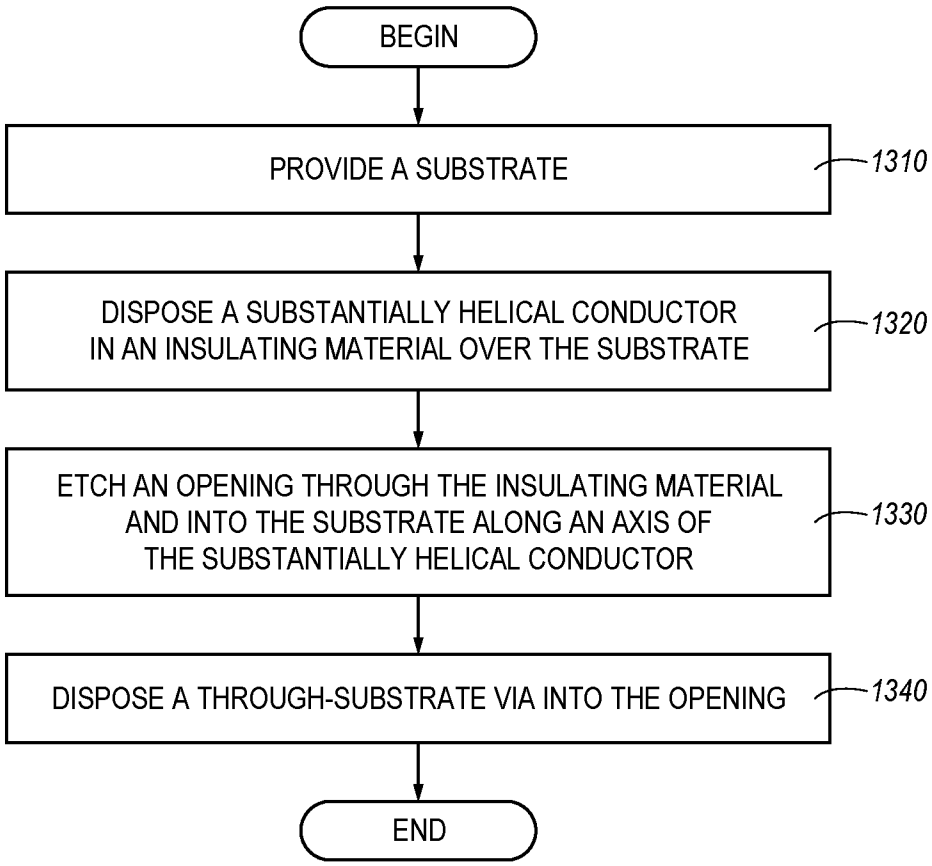

BEGIN
PROVIDE A SUBSTRATE
1310
DISPOSE A SUBSTANTIALLY HELICAL CONDUCTOR IN AN INSULATING MATERIAL OVER THE SUBSTRATE
1320
ETCH AN OPENING THROUGH THE INSULATING MATERIAL AND INTO THE SUBSTRATE ALONG AN AXIS OF THE SUBSTANTIALLY HELICAL CONDUCTOR
1330
DISPOSE A THROUGH-SUBSTRATE VIA INTO THE OPENING
1340
END

Fig. 13

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2018/026256

A. CLASSIFICATION OF SUBJECT MATTER

H01L 49/02(2006.01)i, H01L 21/768(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 49/02; H01L 23/64; H01L 23/528; H01F 17/00; H01L 23/522; H01L 21/768

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: through-substrate via (TSV), helical conductor, coupling member, inductor

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2016-094651 A1 (WASHINGTON STATE UNIVERSITY) 16 June 2016 See paragraphs [0022], [0031]-[0036]; claim 1; and figures 1, 3, 5.	1-7,30-33
Y		8-10,10(1)-29
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	Note: For the claim 10(1), the claim was renumbered by this authority because the claim 10 was found twice.	

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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04 July 2018 (04.07.2018)	**04 July 2018 (04.07.2018)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

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