



(51) International Patent Classification:
G11C 29/42 (2006.01)

(21) International Application Number:
PCT/CA2011/000229

(22) International Filing Date:
2 March 2011 (02.03.2011)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
61/316,138 22 March 2010 (22.03.2010) US

(71) Applicant (for all designated States except US): **MO-SAID TECHNOLOGIES INCORPORATED**
[CA/CA]; 11 Hines Road, Suite 203, Ottawa, Ontario K2K 2X1 (CA).

(72) Inventor; and

(75) Inventor/Applicant (for US only): **KIM, Jin-Ki**
[CA/CA]; 46 Ironside Court, Ottawa, Ontario K2K 3H6 (CA).

(74) Agent: **SMART & BIGGAR**; 1000 De La Gauchetiere Street West, Suite 3300, Montreal, Quebec H3B 4W5 (CA).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: COMPOSITE SEMICONDUCTOR MEMORY DEVICE WITH ERROR CORRECTION

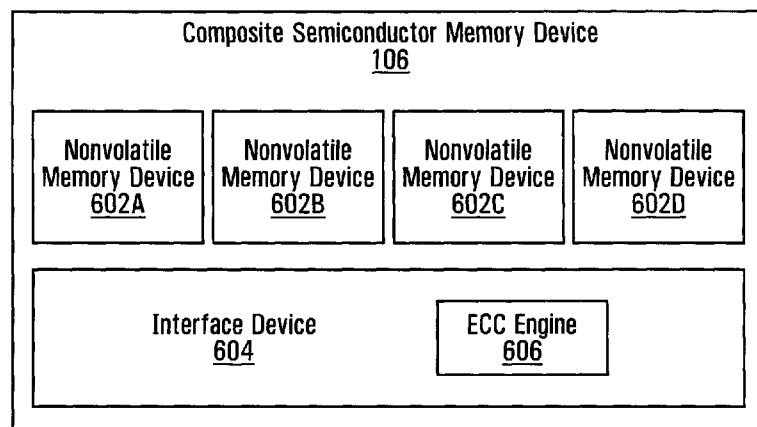


FIG. 6

(57) Abstract: A composite semiconductor memory device, comprising: a plurality of nonvolatile memory devices; and an interface device connected to the plurality of nonvolatile memory devices and for connection to a memory controller, the interface device comprising an error correction coding (ECC) engine. Also, a memory system, comprising: a memory controller; and at least one composite semiconductor memory device configured for being written to and read from by the memory controller and comprising a built-in error correction coding (ECC) engine. Also, a memory system, comprising: a composite semiconductor memory device comprising a plurality of nonvolatile memory devices; and a memory controller connected to the at least one composite semiconductor memory device, for issuing read and write commands to the composite semiconductor memory device to cause data to be written to or read from individual ones of the nonvolatile memory devices; the composite semiconductor memory device providing error-free writing and reading of the data.



COMPOSITE SEMICONDUCTOR MEMORY DEVICE WITH ERROR CORRECTION

BACKGROUND

5

[0001] There has been a significant increase in the data storage requirements of consumer electronic devices such as digital audio/video players, cell phones, portable universal serial bus (USB) drives and solid state drives (SSDs). This density requirement can be satisfied at relatively low cost by nonvolatile semiconductor memory devices incorporating flash memory, commonly known as flash devices. At present, there are two
10 main types of flash memory, namely NOR flash and NAND flash, and of the two, NAND flash has proven to be especially popular.

[0002] However, as flash devices become denser and cheaper, the amount of storage they are expected to provide increases even further. This expectation, in turn, exerts
15 further pressure to render these devices even more dense at an even lower cost costlly.

SUMMARY

[0003] According to one aspect of the present invention, there is provided a
20 composite semiconductor memory device, comprising: a plurality of nonvolatile memory devices; and an interface device connected to the plurality of nonvolatile memory devices and for connection to a memory controller, the interface device comprising an error correction coding (ECC) engine.

[0004] According to another aspect of the present invention, there is provided a
25 memory system, comprising: a memory controller; and at least one composite semiconductor memory device configured for being written to and read from by the memory controller and comprising a built-in error correction coding (ECC) engine.

[0005] According to another aspect of the present invention, there is provided a
30 memory system, comprising: a composite semiconductor memory device comprising a plurality of nonvolatile memory devices; and a memory controller connected to the at least one composite semiconductor memory device, for issuing read and write commands to the

composite semiconductor memory device to cause data to be written to or read from individual ones of the nonvolatile memory devices; the composite semiconductor memory device providing error-free writing and reading of the data, from a perspective of the memory controller.

- 5 **[0006]** Other aspects and features of the present invention will become apparent to those ordinarily skilled in the art upon review of the following description of specific embodiments of the invention in conjunction with the accompanying figures.

BRIEF DESCRIPTION OF THE DRAWINGS

10

[0007] Embodiments of the present invention will now be described, by way of example only, with reference to the attached Figures, wherein:

[0008] Fig. 1 is a block diagram showing a nonvolatile memory system, according to a non-limiting embodiment;

- 15 **[0009]** Fig. 2 is a block diagram showing a nonvolatile memory system using a single composite semiconductor memory device, according to a non-limiting embodiment;

[0010] Figs. 3-5 are block diagrams showing a nonvolatile memory system using plural composite semiconductor memory devices, according to non-limiting embodiments;

- 20 **[0011]** Fig. 6 is a block diagram showing certain components of a composite semiconductor memory device, according to a non-limiting embodiment;

[0012] Figs. 7A, 7B, 8A and 8B depict cross-sectional views of a composite semiconductor memory device, according to ,non-limiting embodiments;

[0013] Fig. 9 is a block diagram showing a NAND flash functional block;

[0014] Fig. 10 is a block diagram showing a NAND flash cell array structure;

- 25 **[0015]** Fig. 11 is a block diagram showing a NAND flash block structure;

[0016] Fig. 12 is a block diagram showing a NAND flash page structure;

[0017] Fig. 13 is a block diagram showing a page-based read operation in NAND flash;

[0018] Fig. 14 is a block diagram showing a page-based program operation in NAND flash;

[0019] Fig. 15 is a block diagram showing a blockpage-based erase operation in NAND flash;

5 **[0020]** Fig. 16 is a block diagram showing an internal functional architecture of a composite semiconductor memory device according to a non-limiting embodiment, wherein a plurality of nonvolatile semiconductor memory devices are interconnected in a multi-drop fashion;

10 **[0021]** Fig. 17 is a block diagram showing more detail regarding the multi-drop interconnection to the plurality of nonvolatile semiconductor memory devices in Fig. 16;

[0022] Fig. 18 is a block diagram showing an internal functional architecture of a composite semiconductor memory device according to a non-limiting embodiment, wherein a plurality of nonvolatile semiconductor memory devices are interconnected using dedicated interface channels;

15 **[0023]** Fig. 19 is a block diagram showing an internal functional architecture of a composite semiconductor memory device according to a non-limiting embodiment, wherein a plurality of nonvolatile semiconductor memory devices are interconnected using group-based interface channels;

20 **[0024]** Figs. 20, 21 and 22 are block diagrams showing different internal configurations of a composite semiconductor memory device according to non-limiting embodiments;

[0025] Fig. 23 is a block diagram illustrating an error correction coding process;

[0026] Fig. 24 is a block diagram illustrating an error correction decoding process;

25 **[0027]** Figs. 25-26 highlight the difference between data written to the interface device and the data written by the interface device to a nonvolatile memory device, according to non-limiting embodiments; and

[0028] Fig. 27 is a functional block diagram of a memory controller, according to a non-limiting embodiment.

DETAILED DESCRIPTION

[0029] Fig. 1 shows a block diagram of a nonvolatile memory system 100 according to a non-limiting embodiment. The nonvolatile memory system 100 comprises a memory controller 102 for communicating with a main system or processor 98 via a communication link 104. The nonvolatile memory system 100 also comprises at least one composite semiconductor memory device 106 connected to the memory controller 102 via a communication link 108. The memory controller 102 can be a flash memory controller.

[0030] In a non-limiting embodiment, shown in Fig. 2, there may be a single composite semiconductor memory device 106 in the nonvolatile memory system 100. In other non-limiting embodiments, shown in Figs. 3, 4 and 5, there may be a plurality of semiconductor memory devices 106 in the nonvolatile memory system 100. Although four (4) semiconductor memory devices 106 are illustrated, it should be understood that there is no particular limit on the number of composite semiconductor devices 106 that can be included in the nonvolatile memory system 100.

[0031] In embodiments where there are plural composite semiconductor devices 106 in the nonvolatile memory system 100, the communication link 108 can take on various forms. In particular, according to the non-limiting embodiment shown in Fig. 3, the communication link 108 can include a common interface channel (e.g., a multi-drop parallel bus) 302. In addition, dedicated chip-enable signals 304 can be provided to the various composite semiconductor memory devices 106. An individual composite semiconductor memory device 106 can be selected by asserting the corresponding dedicated chip-enable signal 304. According to the non-limiting embodiment shown in Fig. 4, the communication link 108 can employ multiple dedicated interface channels 406 between the memory controller 102 and the composite semiconductor memory devices 106. In this case, each of the composite semiconductor memory devices 106 has its own dedicated interface channel 406. According to the non-limiting embodiment shown in Fig. 5, the communication link 108 can employ multiple dedicated interface channels 506 between the memory controller 102 and the composite semiconductor memory devices 106. In this case, each of the common interface channels 506 is shared by a group of two (2) or more composite semiconductor memory devices 106.

[0032] In a non-limiting embodiment, and with reference to Fig. 6, the composite

semiconductor memory device 106 comprises a plurality of nonvolatile memory devices 602A, 602B, 602C, 602D and an interface device 604. Although four (4) nonvolatile memory devices 602A, 602B, 602C, 602D are illustrated, it should be understood that there is no particular limit on the number of nonvolatile memory devices 602A, 602B, 602C, 602D that
5 may be connected to the interface device 604. Communication between the interface device 604 and the nonvolatile memory devices 602A, 602B, 602C, 602D is achieved using interface channels, as will be described later on with reference to Figs. 16-19. The interface device 604 can include an error correction coding (ECC) engine 606. The ECC engine 606 allows the composite memory device 106 to exhibit error-free (as judged from the
10 perspective of the memory controller 102) writing of data to, and error-free (as judged from the perspective of the memory controller 102) reading of data from, the nonvolatile memory devices 602A, 602B, 602C, 602D.

[0033] With reference to Figs. 7A, 7B, 8A and 8B, the interface device 604 and the nonvolatile memory devices 602A, 602B, 602C, 602D can be encapsulated in a single
15 enclosure 704, such as a multi-chip package (MCP). Specifically, nonvolatile memory devices 602A, 602B, 602C, 602D are stacked together onto a substrate 706. In Figs. 7A and 8A, the interface device 604 is shown as being placed on top of nonvolatile memory devices 602D, while in Figs. 7B and 8B, the interface device 604 is shown as being at the bottom of a stack of nonvolatile memory devices. Still other configurations are possible without departing
20 from the scope of the invention. Also shown are bonding pads 708 attached to the substrate 706 to allow electrical connections between the composite semiconductor memory device 106 and other components external thereto. Connections are also provided between the interface device 604 and each of the nonvolatile memory devices 602A, 602B, 602C, 602D. Also, in the embodiments of Figs. 7A and 7B, wire bonds 702 are established between the
25 interface device 604 and each of the nonvolatile memory devices 602A, 602B, 602C, 602D through the substrate 706. In contrast, in the embodiments of Figs. 8A and 8B, direct connections 802 are established between the interface device 604 and each of the nonvolatile memory devices 602A, 602B, 602C, 602D. Still other manners of interconnecting the interface device 604 and each of the nonvolatile memory devices 602A, 602B, 602C,
30 602D are possible. Also, while a stacked die configuration is shown, this is not to be interpreted as limitative.

[0034] Nonvolatile memory devices 602A, 602B, 602C, 602D

[0035] The nonvolatile memory devices 602A, 602B, 602C, 602D can be NAND flash memory devices, NOR flash memory devices or phase-change memory devices, to name just a few non-limiting possibilities. The nonvolatile memory devices 602A, 602B, 602C, 602D can operate asynchronously or synchronously, to name just a few non-limiting possibilities. Also, the nonvolatile memory devices 602A, 602B, 602C, 602D can operate as single data rate (SDR) devices or double data rate (DDR) devices, to name just a few non-limiting possibilities. In a specific non-limiting embodiment, nonvolatile memory devices 602A, 602B, 602C, 602D can abide by an industry specification such as Samsung's 16Gb Multi Level Cell NAND Flash Specification for products K9GAG08U0D, K9LBG08U1D, K9HCG08U5D (as described in a document entitled 2G x 8 Bit / 4G x 8 Bit / 8G x 8 Bit NAND Flash Memory, available from Samsung Electronics), which provides device operation and timing details and is incorporated by reference herein. Of course, other makes or models of available flash memories can be used as the nonvolatile memory devices 602A, 602B, 602C, 602D.

[0036] Fig. 9 conceptually illustrates various functional components of a nonvolatile memory device (such as, in this example, device 602A) implemented as a NAND flash memory device.

[0037] The device 602A utilizes the following ports and signals:

- Input/Output (I/O) ports (I/O0 to I/O7): the I/O ports are used for transferring address, command and input/output data to and from the device 602A. In particular, data to be written to the device 602A arrives on the I/O ports I/O0 to I/O7 and is temporarily placed in a set of global buffers 916 prior to being stored in a memory cell array 902. Data to be read from the device 602A is extracted from the memory cell array 902 and is placed in the set of global buffers 916 prior to being released on the I/O ports I/O0 to I/O7;
- Write Enable port (WE#): the WE# port receives a WE# signal used to control the acquisition of data from the I/O ports;
- Command Latch Enable (CLE) port: the CLE port receives a CLE signal used to control loading of an operation mode command into a command register 910. The command is latched into the command register 910 from the I/O ports on the rising edge of the WE# signal while the CLE signal is asserted;

- Address Latch Enable (ALE) port: the ALE port receives an ALE signal used to control loading of address information into an internal address register 912. The address information is latched into the address register 912 from the I/O ports on the rising edge of the WE# signal while the ALE signal is asserted;

5 • Ready/Busy (R/B#) port: the R/B# port is an open drain pin and the output R/B# signal is used by the device 602A to indicate its operating state. Specifically, the R/B# signal indicates whether the device is ready or busy. R/B# circuitry 914 in the device 602A will de-assert the R/B# signal when the device 602A is in a busy state (such as during the read, program and erase operations). After completion of the operation, the R/B# circuitry 914 will re-assert the R/B# signal, indicating that the device 602A is in a ready state.

10 • Chip Enable (CE#) port: the CE# port receives a CE# signal. When the CE# signal is de-asserted while the device 602A is in a ready state (when the R/B# signal is asserted), the device 602A goes into a low-power standby mode. However, the CE# signal is ignored when the device 602A is in a busy state (when the R/B# signal is de-asserted), such as during a read, program or erase operation. That is to say, if the device 602A is in a busy state, the device 602A will not enter standby mode regardless of whether the CE# signal is de-asserted.

15 • Read Enable (RE#) port: the RE# port receives a RE# signal used to control serial data output. Specifically, data to be output by the device 602 is placed on the I/O ports I/O0 to I/O7 after the falling edge of the RE# signal (i.e., when the RE# signal is asserted). An internal column address counter is also incremented (Address = Address + 1) on the falling edge the RE# signal.

20 • Write Protect (WP#) port: the WP# port receives a WP# signal used to protect the device 602A from accidental programming or erasing. An internal voltage regulator (high voltage generator 918, which provides necessary high voltages and reference voltages during read, program and erase operations) is reset when the WP# signal is asserted. The WP# signal can be used for protecting data stored in the memory cell array 902 during the power-on/off sequence when input signals are invalid.

25 **[0038]** Fig. 10 illustrates the cell array structure of the memory cell array 902, which includes n erasable blocks 1002-0 to 1002-(n-1). Each block is subdivided into m

programmable pages 1102-0 to 1102-(m-1) as shown in Fig. 11. In turn, each page is subdivided into (j+k) 8-bit bytes as shown in Fig. 12. Specifically, the bytes of each page are divided into a j-byte data storage region (data field 1202) and a k-byte data storage region (spare field 1204). Therefore, the total size of the memory cell array 902 is n blocks, which corresponds to (n * m) pages and therefore equals (n * m * (j + k)) bytes.

[0039] The spare field 1204 can be used for error management functions (e.g., to store error control coding parity bits). Also, metadata for each page and/or block (such as the number of erase cycles, address information, bad block information, etc) can be stored in the data field 1202 or in the spare field 1204, depending on the embodiment.

[0040] The required size of the spare field 1204 in NAND flash memory is a function of page size, process technology, number of bits per cell (i.e., one bit per cell, two bits per cell, three bits per cell, and so on) and bit error rate. The page size in early generation NAND flash memory was 512 bytes for the data field 1202 and 16 bytes for the spare field 1204. The page size has grown as the process technology has evolved, which has allowed greater memory densities to be achieved. However, this growth has also brought higher bit error rates and hence a need to use stronger error correction coding. An example of a contemporary page size is 8K bytes for the data field 1202 and 436 bytes for the spare field 1204. Also, the size of the data field 1202 and the spare field 1204 can differ among manufacturers of flash memory. However, those skilled in the art should appreciate that embodiments of the present invention impose no specific limitation on the absolute or relative size of the data field 1202 or on the spare field 1204.

[0041] With reference again to Fig. 9, the memory core of the device 602A includes, in addition to the memory cell array 902, a row decoder 920, a sense amplifier / page buffer 904 and a column decoder 922. The row decoder 920 is used to select a page for either the read operation or the program operation, or to select a block for the erase operation.

[0042] More specifically, during the read operation, the data on the selected page in the memory cell array 902 is sensed and latched into the sense amplifier / page buffer 904. Then, the data stored in the sense amplifier / page buffer 904 is sequentially read out through the column decoder 922 and the global buffers 916. During the program operation, the input data from the global buffers 916 is sequentially loaded into the sense amplifier / page buffer 904 via the column decoder 922. The input data latched in the sense amplifier / page buffer 904 is then programmed into the selected page of the memory cell array 902.

[0043] The device 602A also includes a status register 928, which tracks the status of the device 602A during the read, program or erase operations. The status can be encoded to reflect whether an operation has passed or failed, and whether the device 602A is busy or ready.

5 **[0044]** The device 602A further includes a control circuit 930, which is a central unit having a state machine that controls the device 602A during various operating modes. For example, the aforementioned command register 910 decodes input commands from the global buffer 916, and the decoded command is input to the control circuit 930.

[0045] In addition, the device 602A includes control buffers 932 that determine the
10 current operating mode (such as command input, address input, data input, data output and status output) based on the current combination of signals on the input ports, namely the CE#, CLE, ALE, WE#, RE# and WP# ports.

[0046] Moreover, the device 602A includes the aforementioned address register 912, which stores a multiplexed column address and row address. This address is demultiplexed
15 by the address register and transferred into a row pre-decoder 934 and a column pre-decoder 936.

[0047] In operation, read, program and erase operations are driven by commands. The read and program operations are executed on a page basis, while erase operations are executed on a block basis. For the present example, assume that $j=4096$ ($=4K$), $k=218$,
20 $m=128$ and $n=4096$. Thus, the capacities of a page, block, plane and device are given as follows:

[0048] 1 Page = $(4K + 218)$ bytes;

[0049] 1 Block = 128 Pages = $(4K + 218)$ bytes $\times$ 128 = $(512K + 27.25K)$ bytes;

[0050] 1 Plane = 2048 Blocks = $(512K + 27.25K)$ Bytes $\times$ 2048 = $(8\text{ G} + 436M)$ bits;

25 **[0051]** 1 Device = 2 Planes = $(8G + 436M)$ Bits $\times$ 2 = $(16G + 872M)$ bits.

[0052] Consider now the read operation, which is executed on a page basis (having a size of $(4K + 218)$ bytes = 4,314 bytes per page). This operation starts after latching a read command arriving via common I/O pins (I/O0 to I/O7) into the command register 910, followed by latching an address arriving via common I/O pins (I/O0 to I/O7) into the address
30 register 912. With reference to Fig. 13, the 4,314 bytes of data in the identified page are

sensed and transferred to the sense amplifier / page buffer 904 in less than t_R (data transfer time). Once the 4,314 bytes of data are sensed and transferred from the selected page in the memory cell array 902 to the sense amplifier / page buffer 904, the data in the sense amplifier / page buffer 904 can be sequentially read from the device 602A.

5 **[0053]** Next, consider the program operation, which is also executed on a page basis. This operation starts after latching a program command arriving via common I/O pins (I/O0 to I/O7) into the command register 910, followed by latching an address arriving via common I/O pins (I/O0 to I/O7) into the address register 912, followed by latching 4,314 bytes of data arriving via common I/O pins (I/O0 to I/O7) into the sense amplifier / page buffer 904. With
10 reference to Fig. 14, these 4,314 bytes of data are programmed to the selected page of the memory cell array 902 in less than t_{PROG} (page program time).

[0054] Consider now the erase operation, which is executed on a block basis. This operation starts after latching an erase command arriving via common I/O pins (I/O0 to I/O7) into the command register 910, followed by latching an address arriving via common I/O pins
15 (I/O0 to I/O7) into the address register 912. With reference to Fig. 15, the (512K + 27.25K) bytes of data are erased in less than t_{BERS} (block erase time).

[0055] Communication with the devices 602A, 602B, 602C, 602D

[0056] With reference now to Figs. 16 and 17, the composite semiconductor memory device 106 can employ a common internal interface channel 1602 to support communication
20 between the interface device 604 and the nonvolatile memory devices 602A, 602B, 602C, 602D. The common interface channel 1602 may be implemented as a multi-drop parallel bus for all the signals CLE, ALE, WE#, RE#, WP#, R/B# and the common I/O pins I/O0 to I/O7. In addition, dedicated chip enable signals CE#_1604A, CE#_1604B, CE#_1604C, CE#_1604D are provided to the nonvolatile memory devices 602A, 602B, 602C, 602D,
25 respectively, allowing selection of an individual nonvolatile memory device on which to carry out a read, program or erase operation. For example, nonvolatile semiconductor device 602A can be selected and accessed by asserting CE#_1604A. The rest of devices (i.e., devices 602B, 602C, 602D) are unselected by de-asserting CE#_1604B, CE#_1604C and CE#_1604D, which results in any input (commands, addresses or data) from the memory
30 controller 102 being ignored. Also, the output signals of the unselected devices are in a high-impedance (i.e., Hi-Z) state.

[0057] With reference to Fig. 18, the composite semiconductor memory device 106

can employ multiple dedicated interface channels 1802A, 1802B, 1802C, 1802D, which are respectively connected to the nonvolatile memory devices 602A, 602B, 602C, 602D.

[0058] With reference to Fig. 19, the composite semiconductor memory device 106 can employ multiple dedicated interface channels 1902, 1904 to support communication between the interface device 604 and the nonvolatile memory devices 602A, 602B, 602C, 602D. In this case, a first group of two nonvolatile memory devices (e.g., devices 602A and 602B) shares common interface channel 1902, while a second group of two nonvolatile memory devices (e.g., the devices 602C, 602D) shares common interface channel 1904. However, it should be understood that the number of groups (and therefore the number of common interface channels), as well as the number of nonvolatile memory devices per common interface channel, is not particularly limited.

[0059] Fig. 20 shows certain functional elements of the interface device 604 according to a non-limiting embodiment. According to this non-limiting embodiment, the interface device 604 can include an external interface block 2004, which interfaces to/from the memory controller 102 over the previously described communication link 108. Among other functions, the external interface block 2004 buffers/generates control signals from/for the memory controller 102, as well as inputs/outputs data from/to the memory controller 102. The external interface block 2004 may have a behavior or functionality characterized as asynchronous NAND flash, asynchronous Double Data Rate (DDR), or synchronous DDR, to name a few non-limiting possibilities. The interface device 604 can also include an internal interface block 2002, which interfaces to/from the nonvolatile memory devices 602A, 602B, 602C, 602D over one or more interface channels (namely, 1602 or 1802A, 1802B, 1802C, 1802D, or 1902, 1904) as has been previously described. Among other functions, the internal interface block 2002 buffers/generates control signals from/for the nonvolatile memory devices 602A, 602B, 602C, 602D, and inputs/outputs data from/to memory controller 102. The internal interface block 2002 may have a behavior or functionality characterized as asynchronous NAND flash, asynchronous Double Data Rate (DDR), or synchronous DDR, to name a few non-limiting possibilities.

[0060] In addition, the interface device 604 includes the aforementioned ECC engine 606. The ECC engine 606 provides error correction coding of data received from the memory controller 102 before it is written to any of the nonvolatile memory devices 602A, 602B, 602C, 602D, as well as error correction decoding of data read from any of the

nonvolatile memory devices 602A, 602B, 602C, 602D before it is sent to the memory controller 102.

[0061] In addition, the interface device 604 can include buffer memory 2006 (such as static random access memory – SRAM), which temporarily stores input data from the memory controller 102 before ECC encoding, and outputs data to the memory controller 102 after ECC decoding.

[0062] The interface device 604 also comprises a control block and timing control signal generator 2008, which generates various control signals including timing control signals required for controlling the external interface block 2004, the internal interface block 2002, the buffer memory 2006 and the ECC engine 606.

[0063] A variant of the embodiment of Fig. 20 is shown in Fig. 21. Here, the ECC engine is implemented as a first ECC engine 2102 and a second ECC engine 2104 configured for operating in parallel in order to share the error control coding and decoding workload. It should be appreciated that the number of ECC engines 2102, 2104 that can be implemented in order to combinedly execute the overall workload of the ECC engine 606 is not particularly limited.

[0064] Although it would be possible in this non-limiting embodiment to assign each of the ECC engines 2102, 2104 to a respective pre-determined subset of the nonvolatile memory devices 602A, 602B, 602C, 602D, this is not required. In particular, the flexibility of dynamically assigning each of the ECC engines 2102, 2104 to a different one of the nonvolatile memory devices 602A, 602B, 602C, 602D as the need arises is rendered possible by virtue of the internal interface block 2002 providing access to all the nonvolatile memory devices 602A, 602B, 602C, 602D via the common interface channel 1602.

[0065] In the embodiment of Fig. 21, it is also noted that the buffer memory is implemented as a first memory store 2106 associated with the first ECC engine 2102 and a second memory store 2108 associated with the second ECC engine 2104. However, it is also feasible to use a single, larger memory store that is shared between the ECC engines 2102, 2104.

[0066] A second variant of the embodiment of Fig. 20 is shown in Fig. 22. Here, the ECC engine is again implemented as the first ECC engine 2102 and the second ECC engine 2104 configured for operating in parallel in order to share the error control coding and

decoding workload. Also, as in the embodiment of Fig. 21, it is noted that the buffer memory is implemented as a first memory store 2106 associated with the first ECC engine 2102 and a second memory store 2108 associated with the second ECC engine 2104. Again, the number of ECC engines 2102 that can be implemented in order to combinedly execute the overall workload of the ECC engine 606 is not particularly limited, and it may also be recalled that it is feasible to use a single, larger memory store that is shared between the ECC engines 2102, 2104.

[0067] In this embodiment, each of the ECC engines 2102, 2104 is assigned to a respective pre-determined subset of the nonvolatile memory devices 602A, 602B, 602C, 602D. This assignment is determined by the configuration of the internal interface block, which is implemented as a first internal interface block 2202 (communicating with nonvolatile memory devices 602A, 602B over common interface channel 1902) and a second internal interface block 2204 (communicating with nonvolatile memory devices 602C, 602D over common interface channel 1904).

[0068] ECC engine 606

[0069] During a program operation, the ECC engine 606 generates ECC control data such as parity data (hereinafter, parity bits) corresponding to input data from the memory controller 102, combines this input data with the ECC parity data, and then programs both to a selected one of the nonvolatile memory devices 602A, 602B, 602C, 602D.

[0070] More specifically, with reference to Fig. 23 and merely by way of non-limiting example, there is shown an ECC encoding process using a BCH ECC code and a 4KB page size's worth of input data. The ECC engine 606 is equipped with a parity generator 2304. The parity generator 2304 generates parity data 2306 using 4KB of input data 2302 destined for a target page in, say, nonvolatile memory device 602A. The parity data 2306 may be generated by segments of the input data 2302 (e.g. 1KB of 4KB) or using the complete input data 2302 (see Robert Pierce, "Mr. NAND's Wild Ride: Warning — Surprises Ahead," Denali Software Inc., 2009, hereby incorporated by reference herein). The input data 2302 is programmed to the data field 1202 of the target page, while the parity data 2306 is programmed to the spare field 1204 of the target page.

[0071] During a read operation, the ECC engine 606 reads output data with ECC parity data from a selected one of the nonvolatile memory devices 602A, 602B, 602C, 602D, and then performs an ECC operation to generate ECC parity data corresponding to the

output data. The ECC engine 606 then compares the extracted and generated ECC parity data and, if necessary, corrects the output data before providing it to the memory controller 102.

[0072] More specifically, with reference to Fig. 24 and merely by way of non-limiting example, there is shown an ECC decoding process using a BCH ECC code and a 4KB page size's worth of output data. The ECC engine 606 is equipped with a syndrome generator 2406, a Berlekamp block 2408, a Chien block 2410 and a data corrector 2412. The syndrome generator 2406 computes and generates syndromes using 4Kb of output data 2402 and parity data 2404 read out from, say, nonvolatile memory device 602A in order to determine whether there is (are) any error(s). The syndromes are input to Berlekamp block 2408 that determines an error locator polynomial and the number of errors. The Chien block 2410 finds the polynomial roots (that are the error positions) in the error locator polynomial output by the Berlekamp block 2408. Finally, the output data 2402 is corrected by the data corrector block 2412 if indeed there was (were) found to be any error(s) based on the output of the Chien block 2410. The output of the data corrector block 2412 is therefore corrected data 2414 which is then provided to the memory controller 102.

[0073] For simplicity, the above embodiment has assumed that the input data and output data subjected to error correction coding and decoding occupied the entire data field 1202. Where it is desired to include metadata, this metadata can be stored in the spare field 1204. In an alternative embodiment, the metadata can occupy part of the data field 1202, and the input data / output data subjected to error correction coding / decoding can occupy the portion of the data field 1202 that does not include the metadata.

[0074] It should be appreciated that the ECC operations described above are simplified and in no way limiting. Those skilled in the art will understand that there are numerous possible ways to implement error correction coding and decoding in the context of reading and writing data to a nonvolatile memory device, and which can be used within the context of the present invention. Error correction coding (ECC) algorithm correction strength (the number of bit errors that can be corrected) depends on the ECC algorithm used to correct the errors (these algorithms may be implemented in either hardware or software). Simple Hamming codes can correct single bit errors. Reed-Solomon codes can correct more errors and are widely used. BCH (Bose, Ray-Chaudhuri, Hocquenghem) codes can also correct multiple bit errors and are popular because of their improved efficiency over Reed-

Solomon codes. Still other non-limiting examples exist, such as Low Density Parity Code (LDPC), turbo codes, Golay codes and various other concatenated, convolutional and block codes, .

5 **[0075]** From the point of view of the memory controller 102, and with reference to the non-limiting embodiment in Fig. 25, the final page format (i.e., the size of the data exchanged between the memory controller 102 and the composite memory device 106) can include only the data in the data field 1202, without regard for the data in the spare field 1204. That is to say, the memory controller 102 does not write data to or read data from the spare field 1204. Rather, it is the interface device 604 that fills the spare field 1204 with the parity bits
10 generated by the ECC engine 606. In such an embodiment, the spare field 1204 is hidden to users (and indeed to the memory controller 102) and the memory controller 102 does not need to concern itself with error control coding or decoding. This allows the memory controller 102 to function with disabled ECC functionality or without any ECC functionality at all.

15 **[0076]** In the embodiment of Fig. 25 described above, it will be appreciated that either metadata is not provided to the composite semiconductor device 106 by the memory controller 102, or such metadata was already embedded in the data field 1202. An embodiment also exists where the metadata is provided separately, outside the data field 1202. Specifically, in a non-limiting embodiment shown in Fig. 26, the final page format (i.e.,
20 the size of the data exchanged between the memory controller 102 and the composite memory device 106) can include not only the data in the data field 1202, but also a small added spare field 2602 (e.g., 16 or 20 bytes without being limited thereto), which is smaller than the size of the spare field 1204. The added spare field 2602 can be used to store metadata for the page (such as the number of erase cycles, address information, bad block
25 information, etc). In this embodiment, the interface device 604 fills the spare field 1204 with (i) the parity bits generated by the ECC engine 606 and (ii) the metadata from the spare field 2602. In such an embodiment, only the added spare field 2602 is visible to users, while the spare field 1204 remains hidden to users, as well as to the memory controller 102. Here again, the memory controller 102 does not need to concern itself with error control coding or
30 decoding, thus allowing the memory controller 102 to function with disabled ECC functionality or without any ECC functionality at all.

[0077] Memory controller 102

[0078] With reference now to Fig. 27, there is shown a functional block diagram of the memory controller 102 according to a non-limiting embodiment. The memory controller 102 comprises a crystal 2702, which provides a base clock signal that is fed to a clock generator and control block 2704. The clock generator and control block 2704 provides
5 various clock signals to a central processing unit (CPU) 2706, a device management block 2710 and a physical layer transceiver 2740 (in this example, a serial ATA PHY). The CPU 2706 (which can be a microprocessor controller) communicates with other subsystems by a common bus 2742. In addition, a memory store 2708 containing random access memory (RAM) and read-only memory (ROM) can be provided; RAM is used as buffer memory and
10 ROM stores computer-readable code (instructions) executable by the CPU 2706.

[0079] The device management block 2710 includes a physical interface 2714, and a file and memory management block 2712. The at least one composite semiconductor memory device 106 is (are) accessed through the physical interface 2714. The file and memory management block 2712 provides logical-to-physical address translation and
15 applies a wear-leveling algorithm.

[0080] In one non-limiting embodiment, the device management block 2710 includes an ECC (Error Correction Code) engine 2716 that can be controllably disabled upon receipt of a disable signal 2718 from the CPU 2706. In another non-limiting embodiment, the ECC engine 2716 is disabled in hardware. In yet another non-limiting embodiment, the device
20 memory controller 102 does not include an ECC engine or error correction circuitry. If provided, the ECC engine 2716 can check and correct data accessed from the at least one composite semiconductor memory device 106.

[0081] It should be appreciated that the connection of increasingly greater numbers of composite semiconductor memory devices 106 to the memory controller 102 does not
25 change the ECC processing load of the memory controller 102. This is because the ECC requirements are distributed among the composite semiconductor memory devices 106. In fact, the memory controller 102 is not required to perform any error correction coding or decoding at all, since error-free performance of the nonvolatile memory devices 602A, 602B, 602C, 602D (as judged from the perspective of the memory controller 102) is assured by the
30 ECC engine 606 in the interface device 604.

[0082] Moreover, the interface device 604 can be designed to carry out ECC in parallel for multiple reads and/or writes in parallel, leading to potentially improved memory

access times.

[0083] In addition, as each composite semiconductor memory device 106 has its own ECC engine 606, the memory controller 102 is not constrained to a single read or write at a time. Rather, the memory controller 102 can issue two (or possibly more) commands that cause data related to these commands (e.g., read data or write data for each command) to flow simultaneously through the memory controller 102.

[0084] Moreover, it should be appreciated that since the ECC engine 606 is located in the interface device 604, evolving ECC requirements will be tracked by progress in the design of the interface device 604, but meanwhile the same memory controller 102 can continue to be used. Advantageously, re-use of the same inventory of memory controller can potentially last over multiple different generations of flash memory devices and can also span numerous manufacturers and process technologies. Furthermore, changes in the size of the spare field 1204 (which can be driven by evolving ECC requirements) will not have an effect on the design of the memory controller 102.

[0085] In addition, hiding the spare field 1204 from a user's point of view, simplifies developer effort when designing and using the memory controller 102. Moreover, if a spare field 2602 is employed by the user, it can be kept small and of a consistent size, so as to store the requisite metadata for page management (e.g., the number of erase cycle, address information, bad block information, etc).

[0086] In the embodiments described above, the device elements and circuits are connected to each other as shown in the figures, for the sake of simplicity. In practical applications of the present invention, elements, circuits, etc. may be connected directly to each other. As well, elements, circuits etc. may be connected indirectly to each other through other elements, circuits, etc., necessary for proper operation. Thus, in an actual configuration, the circuit elements and circuits are directly or indirectly coupled with or connected to each other.

[0087] The above-described embodiments of the present invention are intended to be examples only. Alterations, modifications and variations may be effected to the particular embodiments by those of skill in the art without departing from the scope of the invention, which is defined solely by the claims appended hereto.

WHAT IS CLAIMED IS:

1. A composite semiconductor memory device, comprising:
a plurality of nonvolatile memory devices; and
5 an interface device connected to the plurality of nonvolatile memory devices and for connection to a memory controller, the interface device comprising an error correction coding (ECC) engine.
2. The composite semiconductor memory device defined in claim 1, wherein the ECC engine provides error correction coding of data received from the memory controller
10 before it is written to any of the nonvolatile memory devices; and wherein the ECC engine further provides error correction decoding of data read from any of the nonvolatile memory devices before it is sent to the memory controller.
3. The composite semiconductor memory device defined in claim 2, wherein the interface device comprises:
15 buffer memory connected to the ECC engine;
a first interface connected between the ECC engine and the nonvolatile memory devices;
a second interface connected to the buffer memory and for connection to the memory controller; and
a control signal producer for controlling the ECC engine, the buffer memory, the first
20 interface and the second interface.
4. The composite semiconductor memory device defined in claim 3, further comprising a parallel bus for connecting the first interface to each of the nonvolatile memory devices.
5. The composite semiconductor memory device defined in claim 3, wherein the first interface comprises first internal interface circuitry and second internal interface circuitry,
25 wherein the composite semiconductor memory device further comprises a first parallel bus for connecting the first internal interface circuitry to each device in a first subset of the nonvolatile memory devices, and wherein the composite semiconductor memory device further comprises a second parallel bus for connecting the second internal interface circuitry to each device in a second subset of the nonvolatile memory devices.

6. The composite semiconductor memory device defined in claim 3, wherein the composite semiconductor memory device further comprises a dedicated connection between the first interface and each of the nonvolatile memory devices.
- 5 7. The composite semiconductor memory device defined in claim 2, wherein the ECC engine comprises a first ECC engine and a second ECC engine, the first ECC engine and the second ECC engine operating in parallel to provide said error correction coding and said error correction decoding.
8. The composite semiconductor memory device defined in claim 7, wherein the interface device comprises:
 - 10 buffer memory connected to the ECC engine;
 - a first interface connected between the ECC engine and the nonvolatile memory devices; and
 - a second interface connected to the buffer memory and for connection to the memory controller; and
 - 15 a control signal producer for controlling the first ECC engine, the second ECC engine, the buffer memory, the first interface and the second interface.
9. The composite semiconductor memory device defined in claim 8, further comprising a parallel bus for connecting the first interface to each of the nonvolatile memory devices.
10. The composite semiconductor memory device defined in claim 8, wherein the first
20 interface comprises first internal interface circuitry and second internal interface circuitry, wherein the composite semiconductor memory device further comprises a first parallel bus for connecting the first internal interface circuitry to each device in a first subset of the nonvolatile memory devices, and wherein the composite semiconductor memory device further comprises a second parallel bus for connecting the second internal
25 interface circuitry to each device in a second subset of the nonvolatile memory devices.
11. The composite semiconductor memory device defined in claim 8, wherein the composite semiconductor memory device further comprises a dedicated connection between the first interface and each of the nonvolatile memory devices.
12. The composite semiconductor memory device defined in claim 2, wherein the ECC
30 engine comprises a first ECC engine and a second ECC engine, wherein the first ECC

engine provides error correction coding of write data received from the memory controller before it is written to any device in a first subset of the nonvolatile memory devices and further provides error correction decoding of read data received from any device in the first subset of the nonvolatile memory devices before it is sent to the memory controller, and wherein the second ECC engine provides error correction coding of write data received from the memory controller before it is written to any device in a second subset of the nonvolatile memory devices and further provides error correction decoding of read data received from any device in the second subset of the nonvolatile memory devices before it is sent to the memory controller.

13. The composite semiconductor memory device defined in claim 12, wherein the interface device comprises:

buffer memory connected to the ECC engine;

a first interface connected between the ECC engine and the nonvolatile memory devices; and

a second interface connected to the buffer memory and for connection to the memory controller; and

a control signal producer for controlling the first ECC engine, the second ECC engine, the buffer memory, the first interface and the second interface.

14. The composite semiconductor memory device defined in claim 13, further comprising a parallel bus for connecting the first interface to each of the nonvolatile memory devices.

15. The composite semiconductor memory device defined in claim 13, wherein the first interface comprises first internal interface circuitry and second internal interface circuitry, wherein the composite semiconductor memory device further comprises a first parallel bus for connecting the first internal interface circuitry to each device in the first subset of the nonvolatile memory devices, and wherein the composite semiconductor memory device further comprises a second parallel bus for connecting the second internal interface circuitry to each device in the second subset of the nonvolatile memory devices.

16. The composite semiconductor memory device defined in claim 13, wherein the composite semiconductor memory device further comprises a dedicated connection between the first interface and each of the nonvolatile memory devices.

17. The composite semiconductor memory device defined in claim 13, wherein the buffer memory comprises a first memory store connected between the first ECC engine and the second interface and a second memory store connected between the second ECC engine and the second interface.
- 5 18. The composite semiconductor memory device defined in claim 2, wherein the error correction coding of certain data received from the memory controller and destined for a particular one of the nonvolatile memory devices produces control data and wherein the interface device causes the certain data and the control data to be written to the particular memory device.
- 10 19. The composite semiconductor memory device defined in claim 18, wherein the control data comprises parity bits.
20. The composite semiconductor memory device defined in claim 18, wherein each of the nonvolatile memory devices comprises a plurality of pages, each page having a data field and a spare field, wherein the interface device causes the certain data to be written to the data field of a particular page of the particular memory device and causes the control data to be written to the spare field of the particular page of the particular memory device.
- 15 21. The composite semiconductor memory device defined in claim 20, wherein the certain data received from the memory controller is accompanied by metadata.
22. The composite semiconductor memory device defined in claim 21, wherein the metadata comprises at least one of a number of erase cycles, address information and bad block information.
- 20 23. The composite semiconductor memory device defined in claim 21, wherein the interface device causes the metadata to be written to the data field of the particular page of the particular memory device.
- 25 24. The composite semiconductor memory device defined in claim 21, wherein the interface device causes the metadata to be written to the spare field of the particular page of the particular memory device.
25. The composite semiconductor memory device defined in claim 18, wherein the certain data received from the memory controller does not include control data resulting from having previously performed error correction coding on any portion of the certain data.
- 30

26. The composite semiconductor memory device defined in claim 2, wherein the error correction decoding of certain data read from a particular one of the nonvolatile memory devices comprises:

producing control data from the certain data;

5 reading previously generated control data associated with the certain data; and

in case of a mismatch between the produced control data and the previously generated control data, modifying the certain data before transmitting it to the memory controller.

27. The composite semiconductor memory device defined in claim 26, wherein the particular memory device comprises a plurality of pages, each page having a data field and a spare field, wherein the certain data resides in the data field of a particular one of the pages, and wherein reading previously generated control data associated with the certain data comprises reading the previously generated control data from the spare field of the particular page.

15 28. The composite semiconductor memory device defined in claim 27, further comprising reading metadata from the particular one of the nonvolatile memory devices and transmitting the metadata to the memory controller.

29. The composite semiconductor memory device defined in claim 28, wherein the metadata comprises at least one of a number of erase cycles, address information and bad block information.

20 30. The composite semiconductor memory device defined in claim 28, wherein the metadata resides in the data field of the particular page.

31. The composite semiconductor memory device defined in claim 28, wherein the metadata resides in the spare field of the particular page.

25 32. The composite semiconductor memory device defined in claim 2, wherein the nonvolatile memory devices are stacked together.

33. The composite semiconductor memory device defined in claim 2, wherein the interface device and the nonvolatile memory devices are stacked together onto a substrate.

30 34. The composite semiconductor memory device defined in claim 33, further comprising electrical connections between the interface device and each of the nonvolatile memory devices.

35. The composite semiconductor memory device defined in claim 34, wherein the connections are made through the substrate.
36. The composite semiconductor memory device defined in claim 2, wherein at least one of the nonvolatile memory devices comprises a multi-chip package including a plurality of stacked nonvolatile memory devices.
37. The composite semiconductor memory device defined in claim 1, wherein the nonvolatile memory devices are flash memory devices.
38. The composite semiconductor memory device defined in claim 1, wherein the nonvolatile memory devices are phase-change memory devices.
39. The composite semiconductor memory device defined in claim 1, wherein the ECC engine causes the composite semiconductor memory device to perform error-free writing and reading, as judged from a perspective of the memory controller.
40. A memory system, comprising:
a memory controller; and
at least one composite semiconductor memory device configured for being written to and read from by the memory controller and comprising a built-in error correction coding (ECC) engine.
41. The memory system defined in claim 40, wherein the memory controller comprises error control coding circuitry configured for being disabled through application of a control signal.
42. The memory system defined in claim 40, wherein the memory controller lacks error control coding circuitry.
43. The memory system defined in claim 40, wherein at least one of the at least one composite semiconductor memory device comprises:
a plurality of nonvolatile memory devices; and
an interface device for interfacing between the memory controller and the nonvolatile memory devices, the interface device comprising the built-in ECC engine.
44. The memory system defined in claim 43, wherein the built-in ECC engine provides error correction coding of data received from the memory controller before it is written to any of

the nonvolatile memory devices; and wherein the built-in ECC engine further provides error correction decoding of data read from any of the nonvolatile memory devices before it is sent to the memory controller.

45. The memory system defined in claim 43, wherein the plurality of nonvolatile memory devices and the interface device are stacked together on a substrate.

46. The memory system defined in claim 45, wherein the plurality of nonvolatile memory devices are flash memory devices.

47. The memory system defined in claim 46, wherein the memory controller is a flash controller.

48. The memory system defined in claim 40, wherein the at least one composite semiconductor memory device comprises a plurality of composite semiconductor memory devices, each of which is configured for being written to and read from by the memory controller and comprising a respective built-in ECC engine.

49. A memory system, comprising:

a composite semiconductor memory device comprising a plurality of nonvolatile memory devices; and

a memory controller connected to the composite semiconductor memory device, for issuing read and write commands to the composite semiconductor memory device to cause data to be written to or read from individual ones of the nonvolatile memory devices;

the composite semiconductor memory device providing error-free writing and reading of said data, from a perspective of the memory controller.

50. The memory system defined in claim 49, wherein the memory controller is configured for issuing at least two commands for causing data related to the respective commands to flow through the memory controller simultaneously.

51. The memory system defined in claim 50, wherein the composite semiconductor memory device comprises:

a plurality of nonvolatile memory devices; and

an interface device for interfacing between the memory controller and the nonvolatile

memory devices, the interface device comprising an ECC engine.

52. The memory system defined in claim 51, wherein the ECC engine provides error correction coding of data received from the memory controller before it is written to any of the nonvolatile memory devices; and wherein the ECC engine further provides error correction decoding of data read from any of the nonvolatile memory devices before it is sent to the memory controller.

53. The memory system defined in claim 51, wherein the at least two commands include (i) a first command to read data from or write data to a given first one of the nonvolatile memory devices and (ii) a second command to read data from or write data to a given second one of the nonvolatile memory devices different from the given first one of the nonvolatile memory devices.

54. The memory system defined in claim 51, wherein the plurality of nonvolatile memory devices and the interface device are stacked together on a substrate.

55. The memory system defined in claim 51, wherein the plurality of nonvolatile memory devices are flash memory devices.

56. The memory system defined in claim 55, wherein the memory controller is a flash controller.

57. The memory system defined in claim 49, wherein the memory controller comprises error control coding circuitry configured for being disabled through application of a control signal.

58. The memory system defined in claim 49, wherein the memory controller lacks error control coding circuitry.

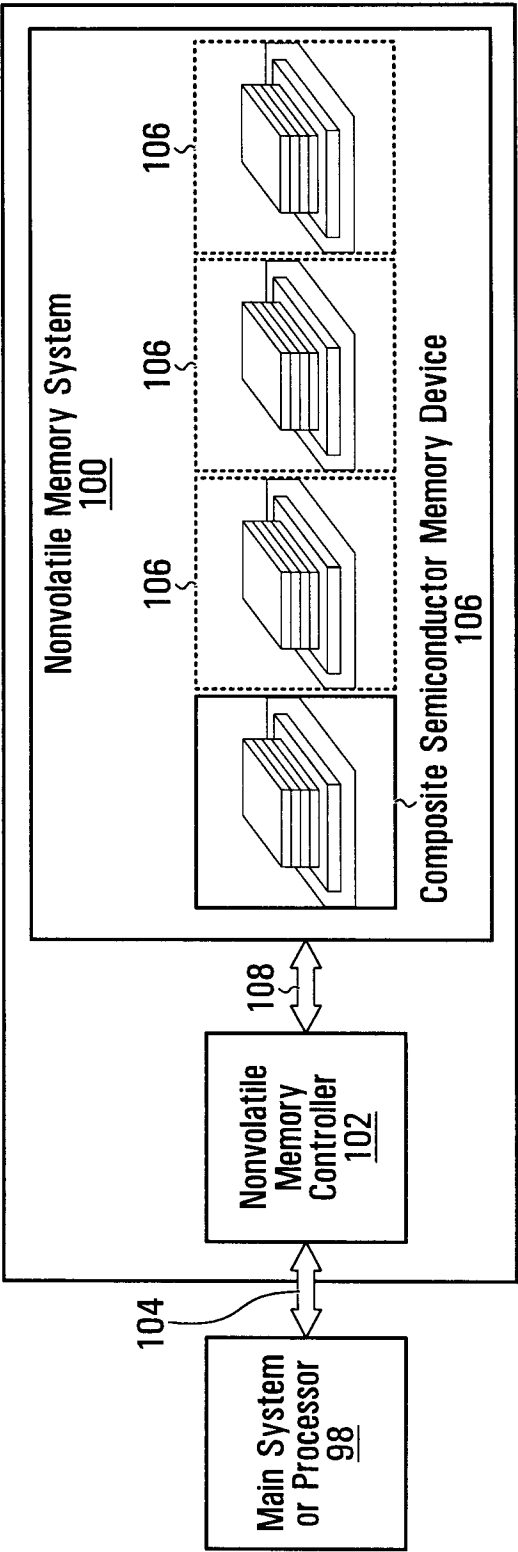


FIG. 1

2/22

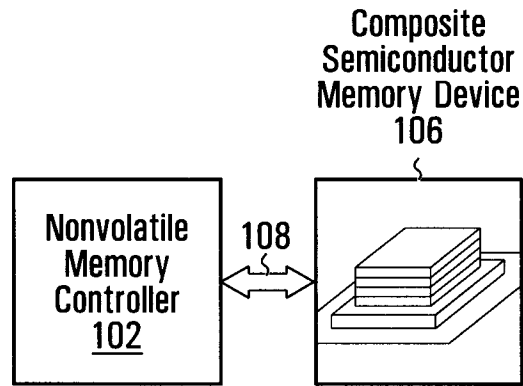


FIG. 2

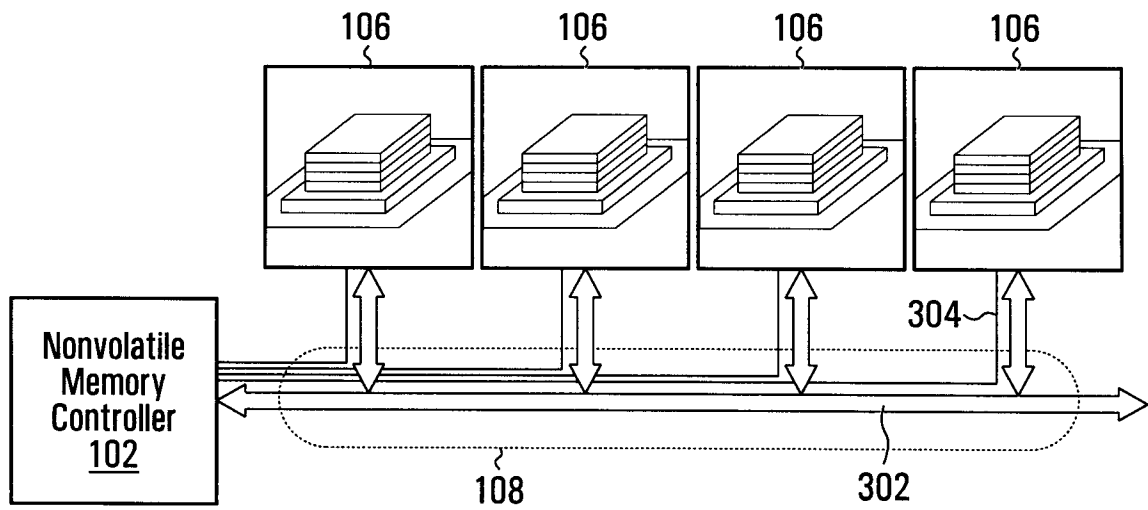
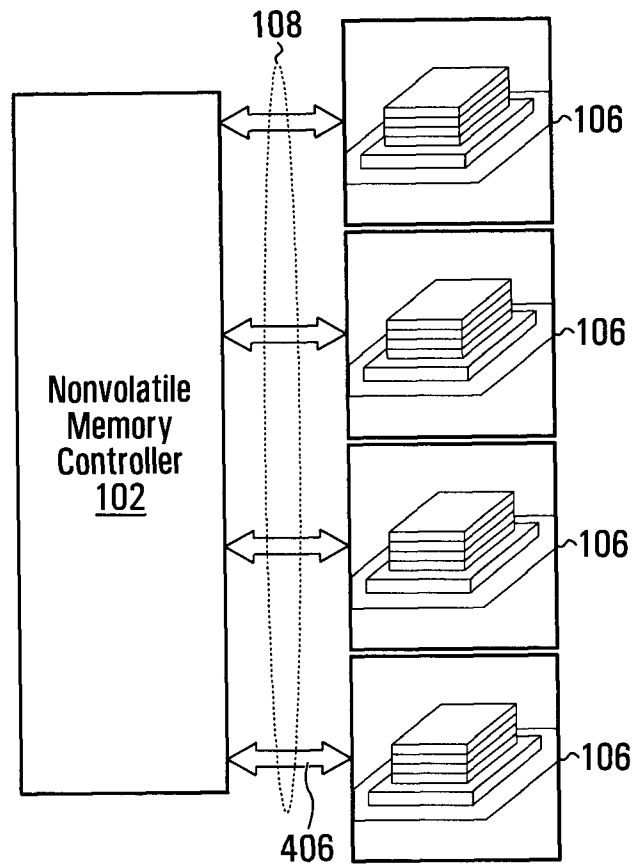


FIG. 3

3/22

**FIG. 4**

+

4/22

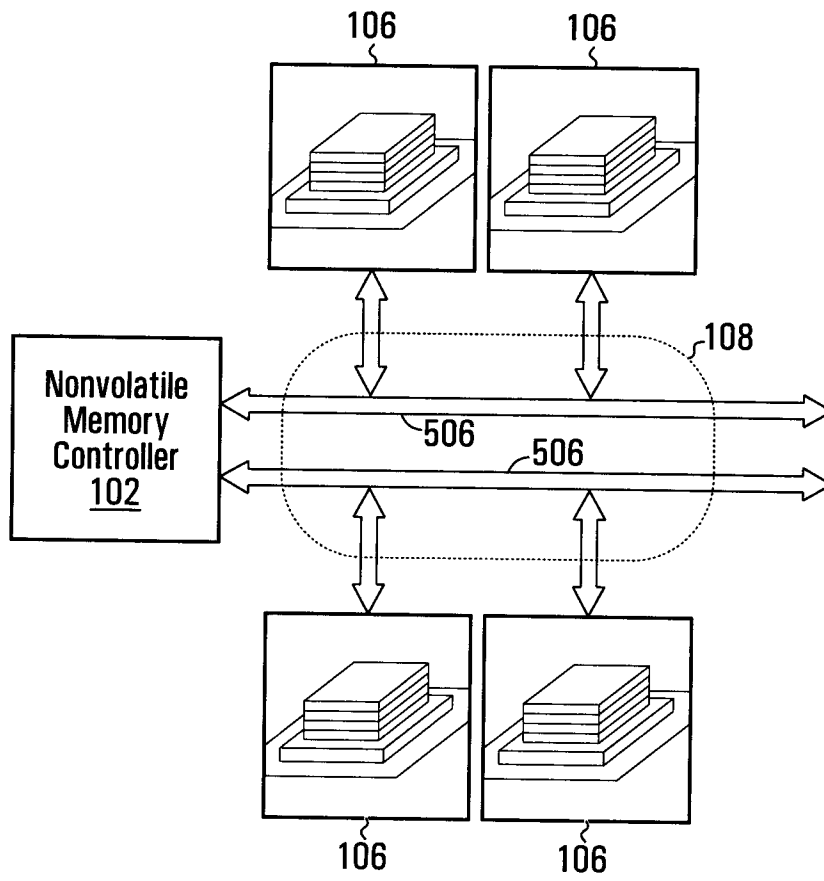
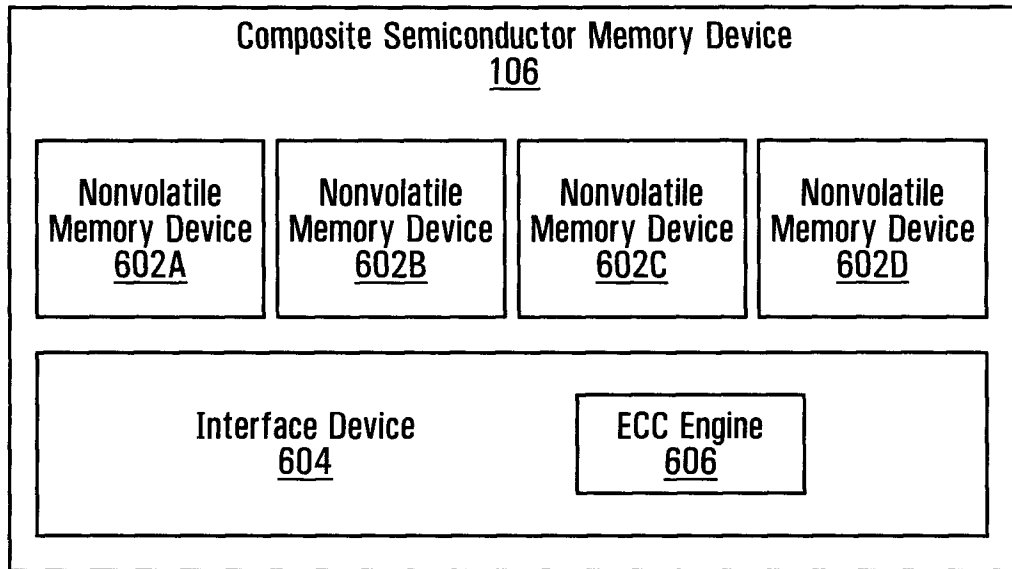


FIG. 5

+

5/22

**FIG. 6**

+

6/22

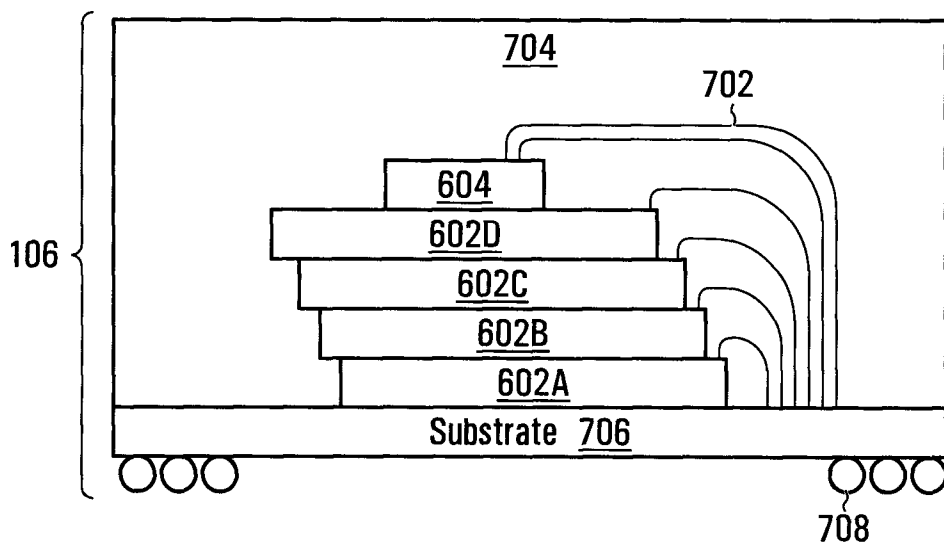


FIG. 7A

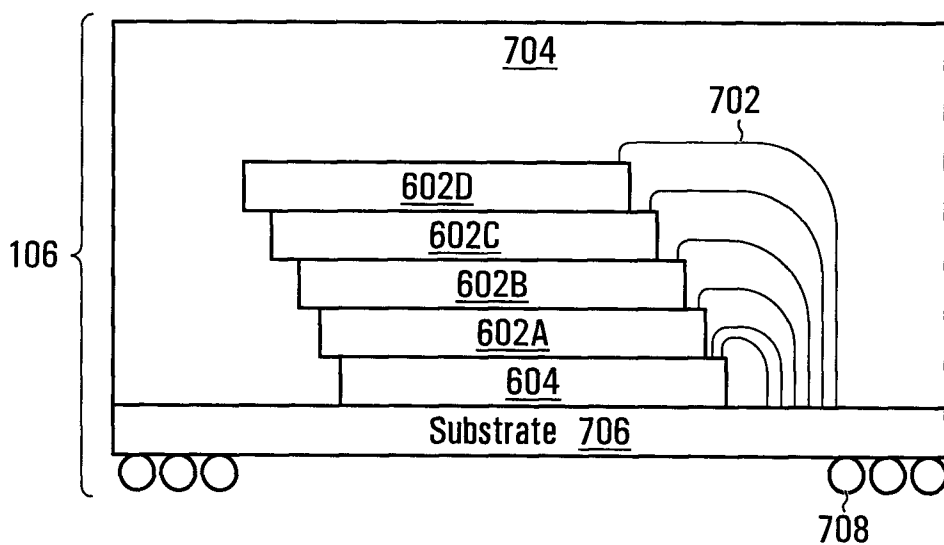


FIG. 7B

+

+

7/22

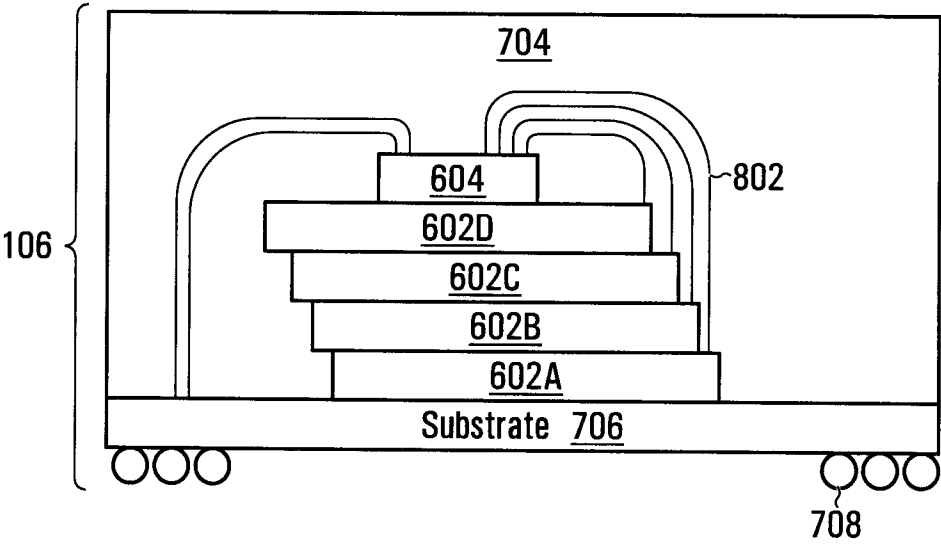


FIG. 8A

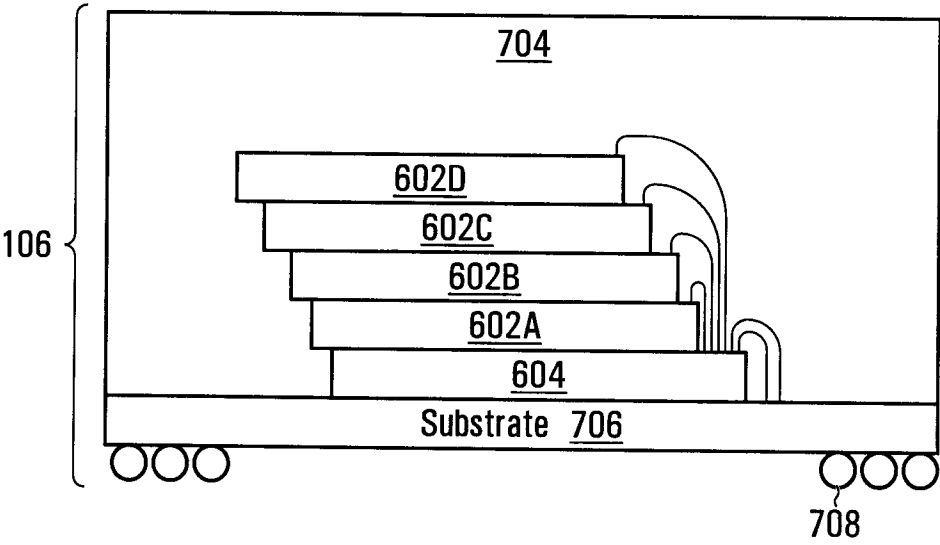


FIG. 8B

+

8/22

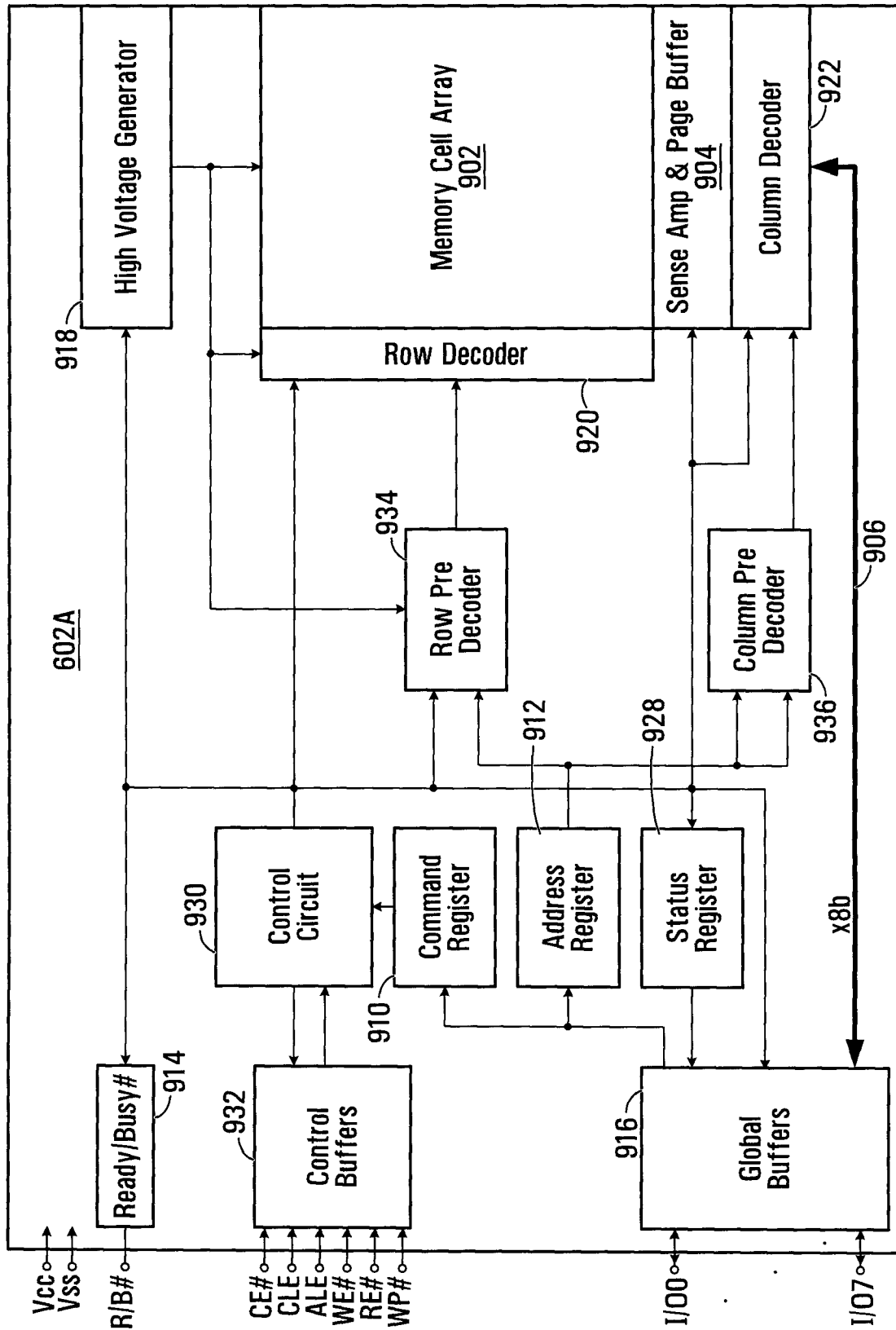


FIG. 9

+

9/22

FIG. 10

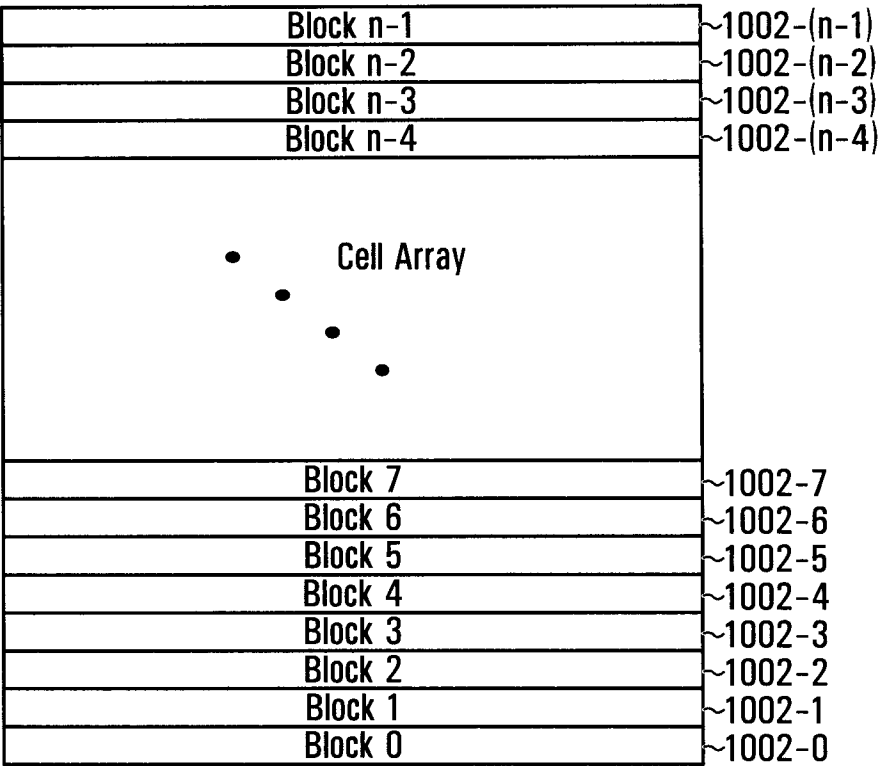


FIG. 11

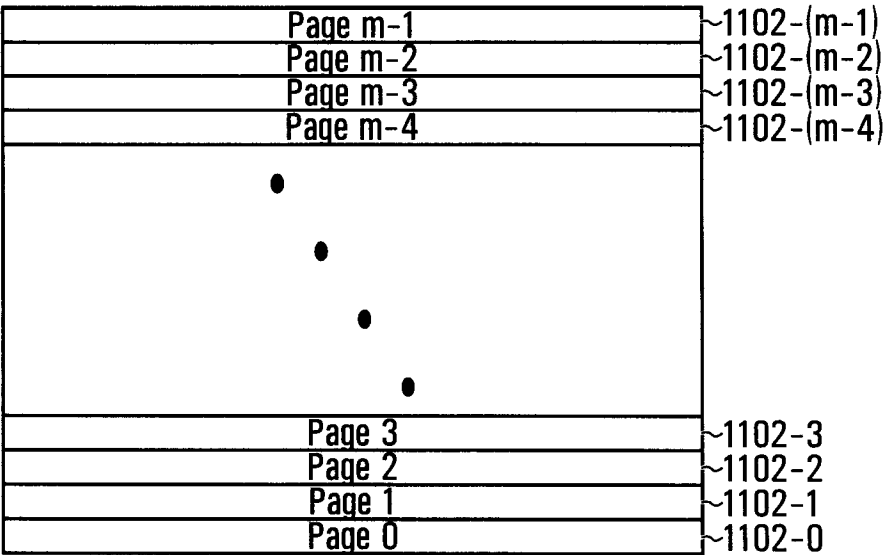
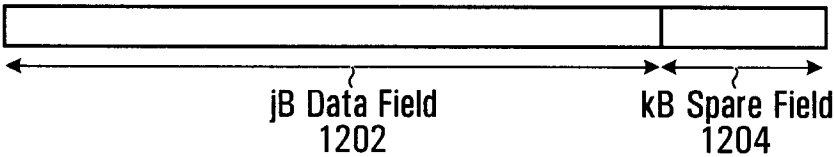


FIG. 12



+

+

10/22

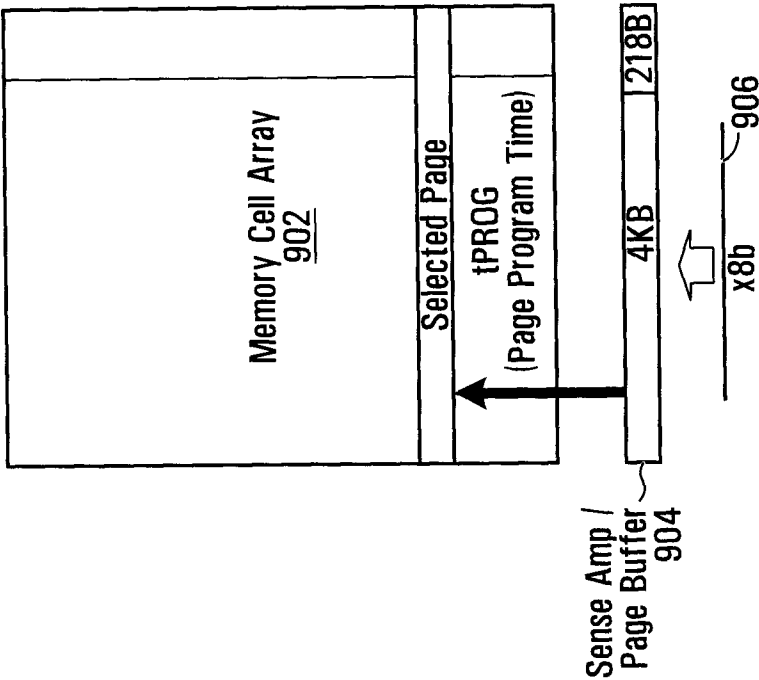


FIG. 14

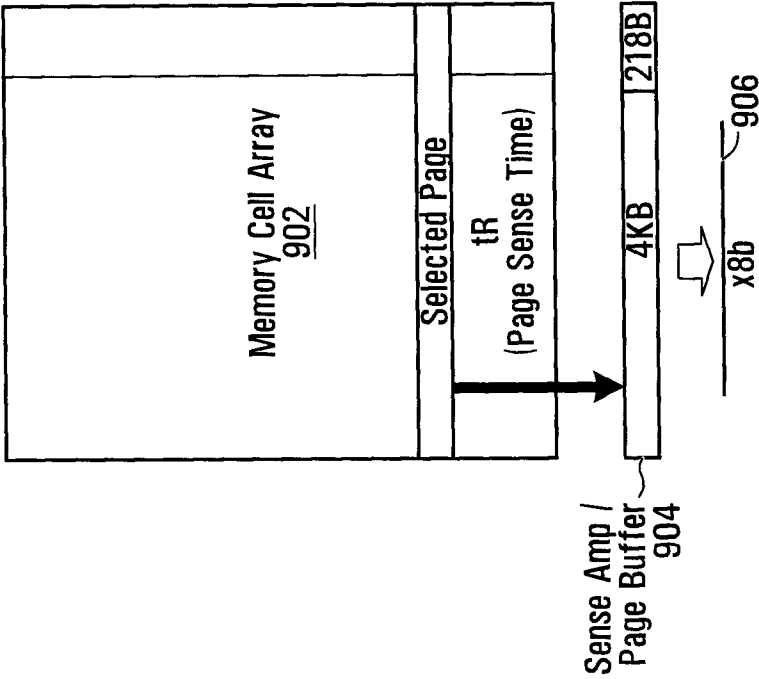


FIG. 13

+

+

11/22

Memory Cell Array <u>902</u>		
Selected Block		
tBERS (Block Erase Time)		

FIG. 15

+

+

12/22

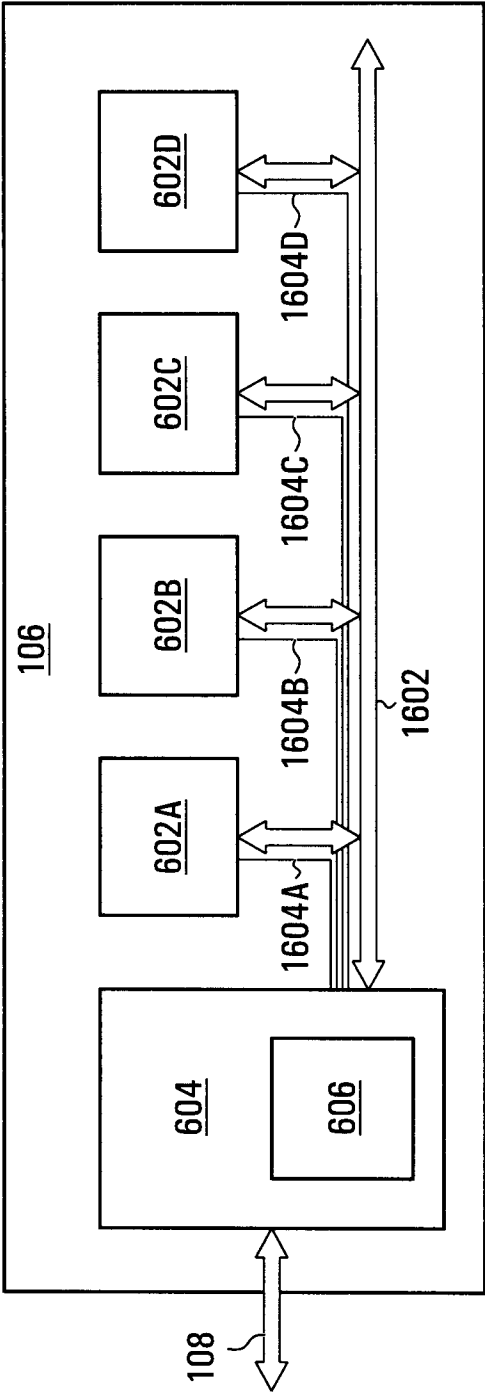


FIG. 16

+

13/22

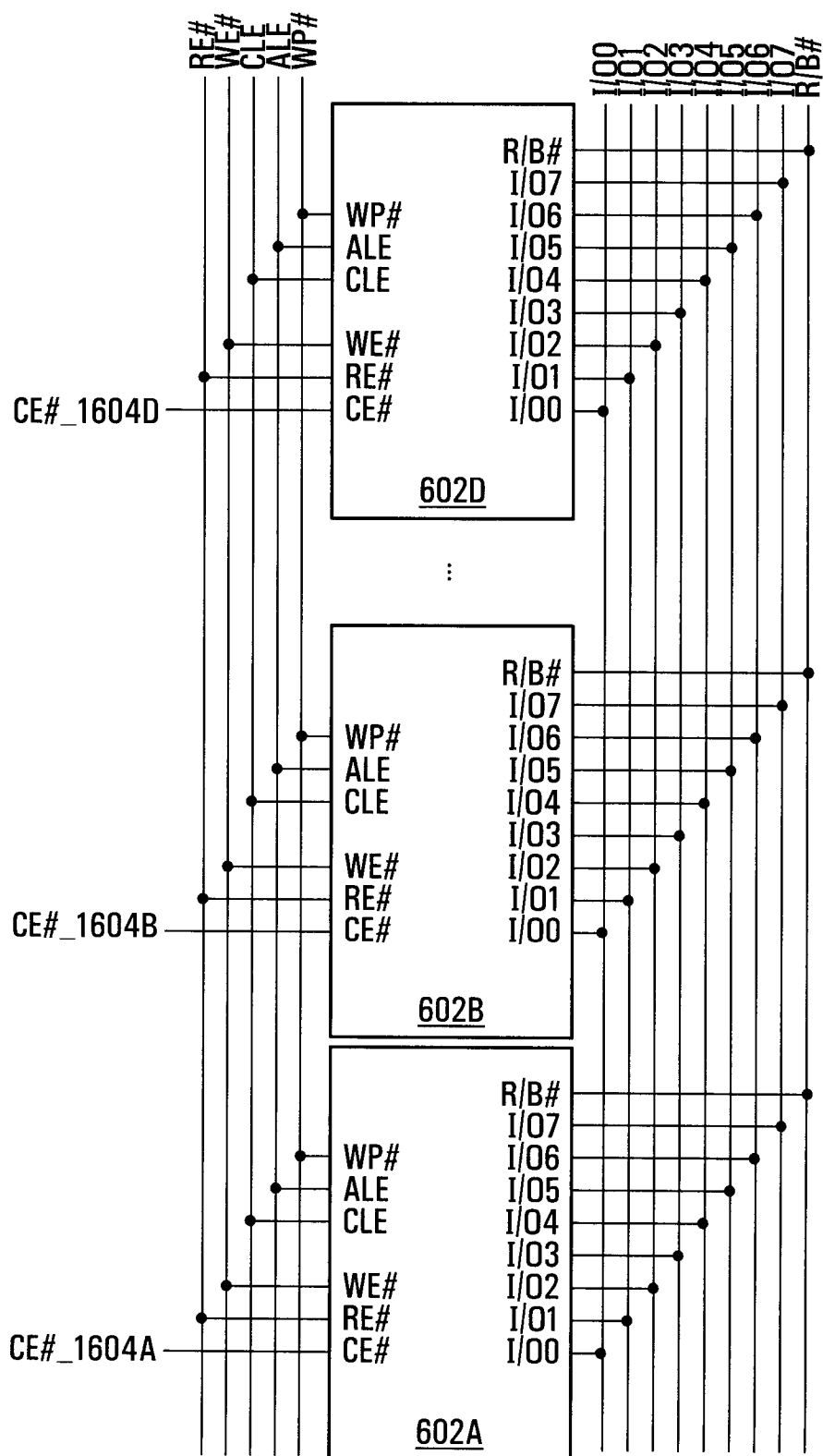


FIG. 17

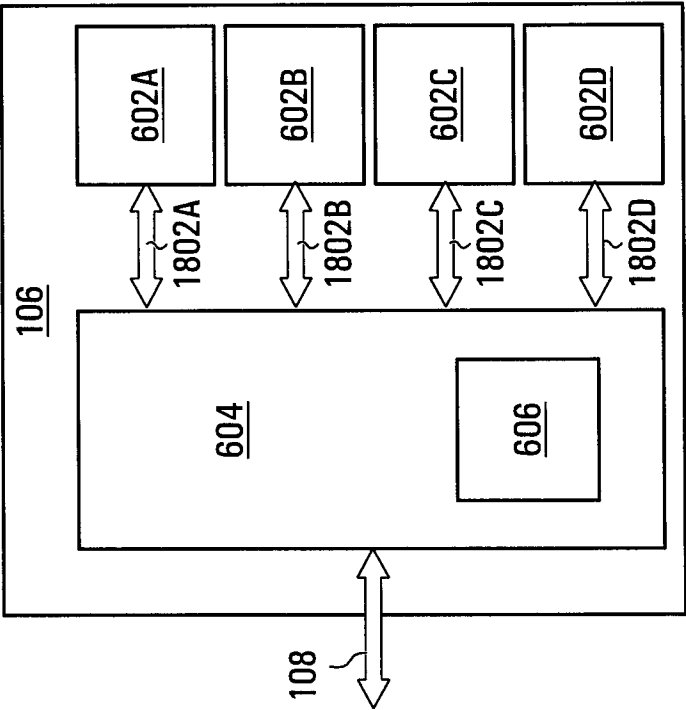


FIG. 18

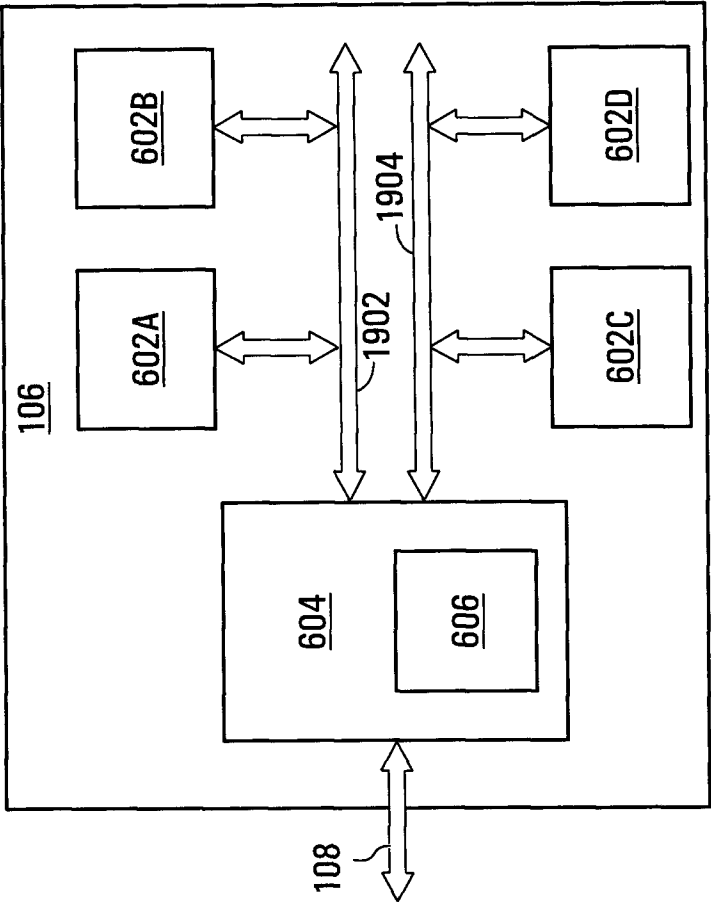


FIG. 19

+

16/22

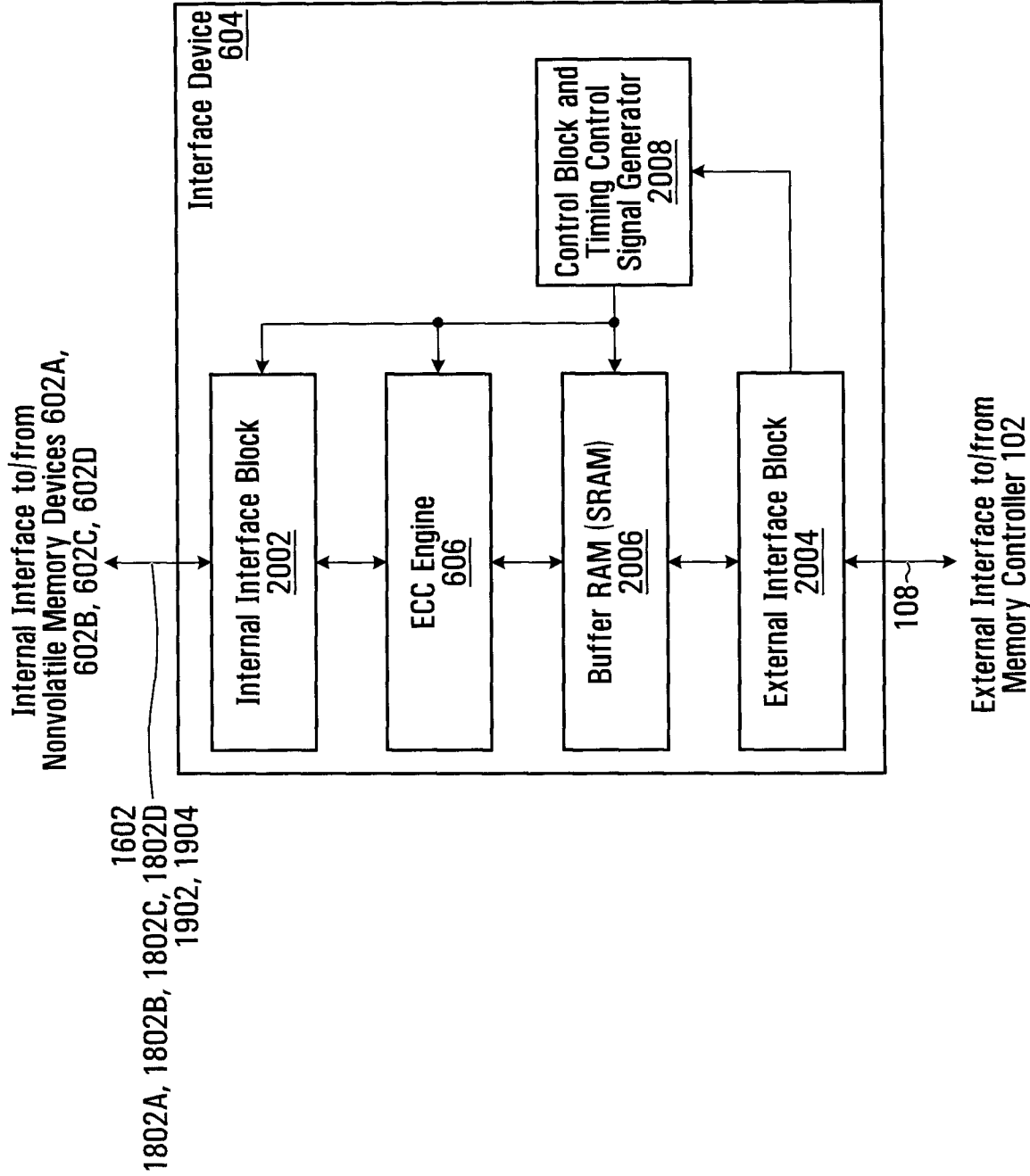


FIG. 20

+

+

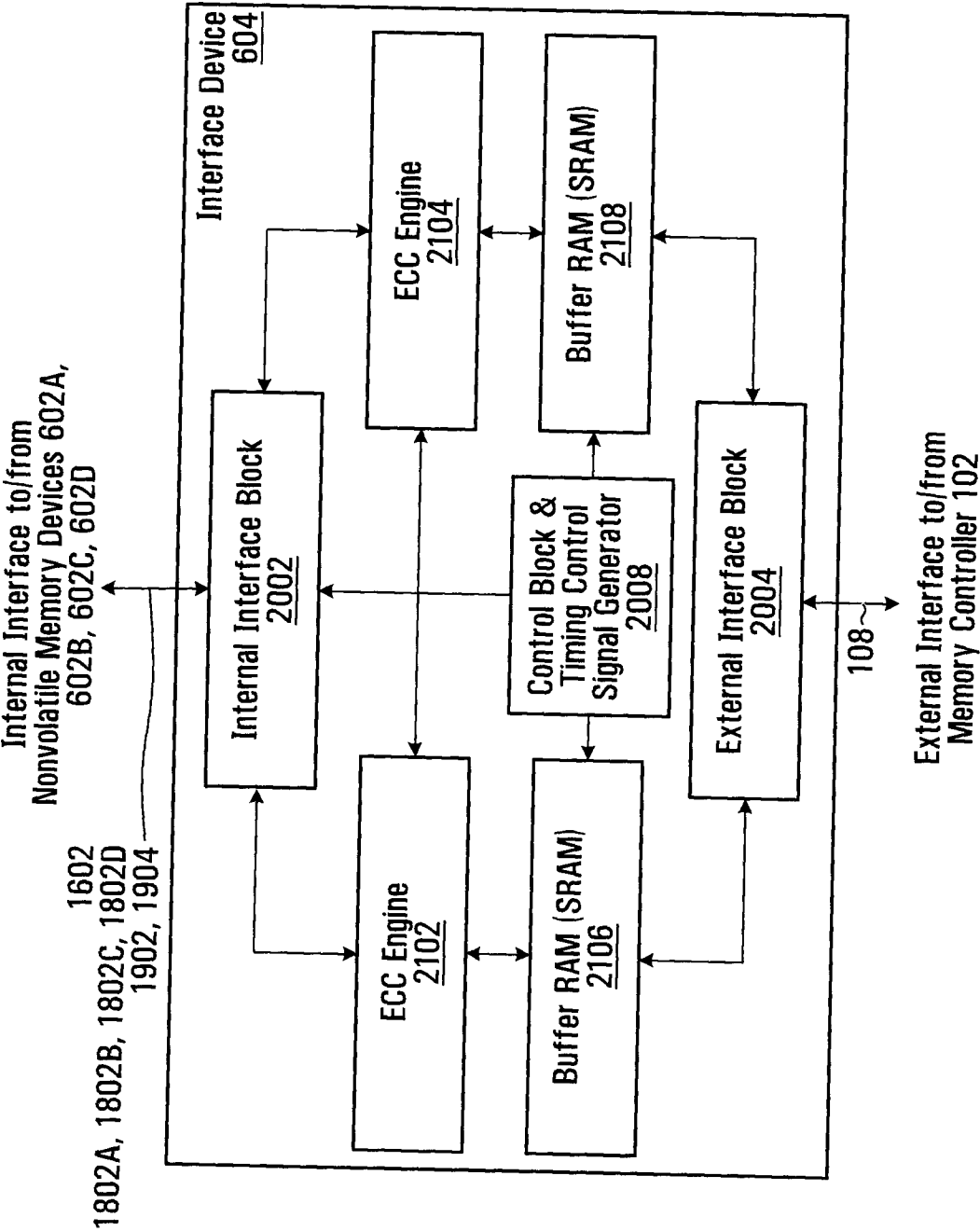


FIG. 21

+

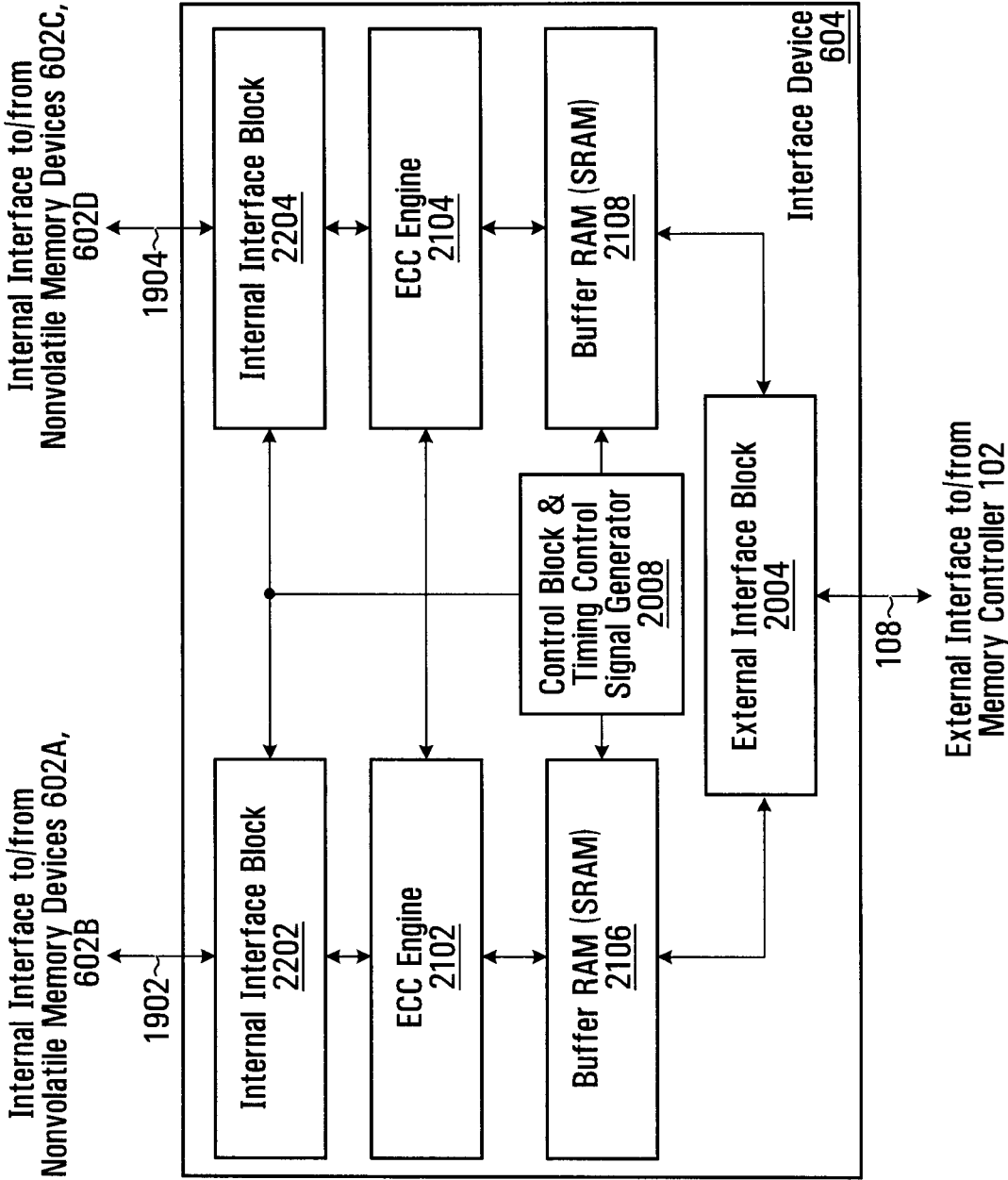


FIG. 22

+

19/22

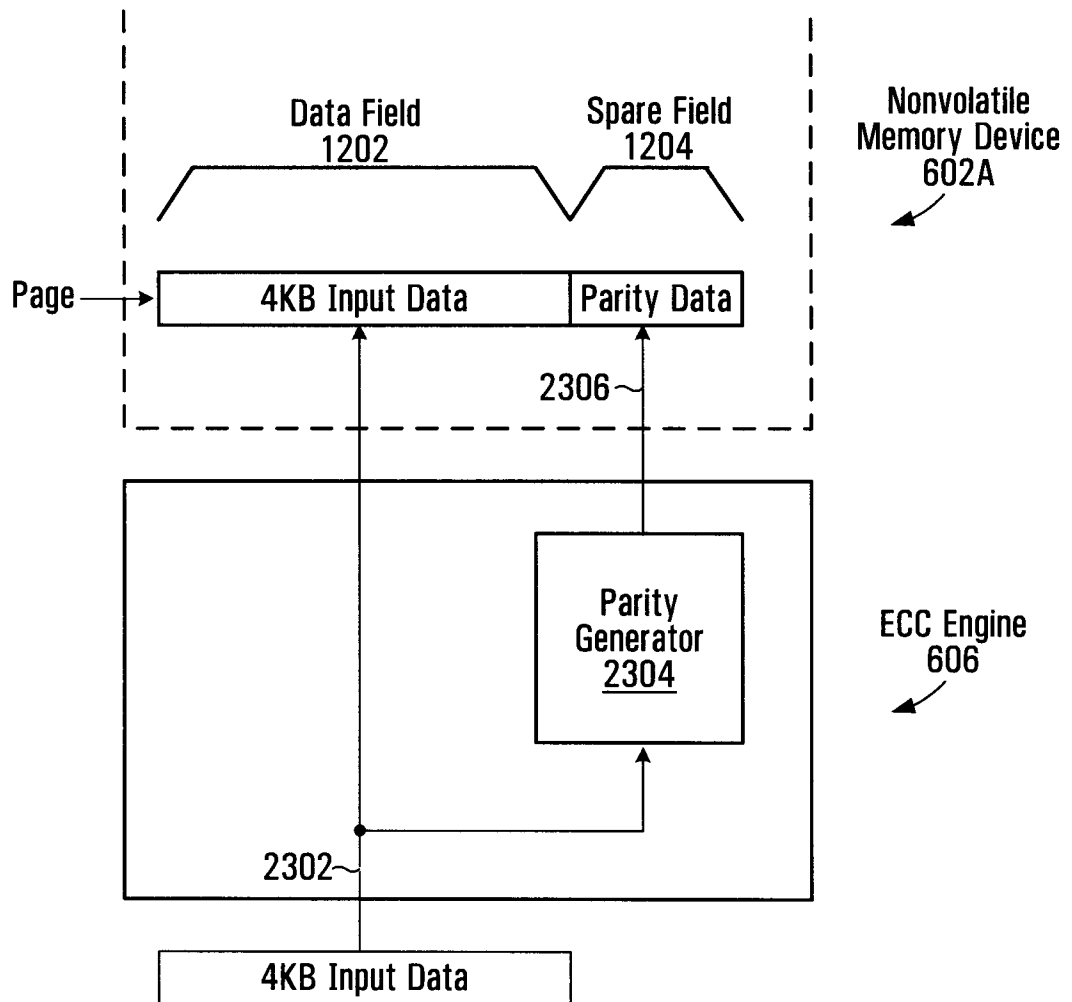


FIG. 23

+

20/22

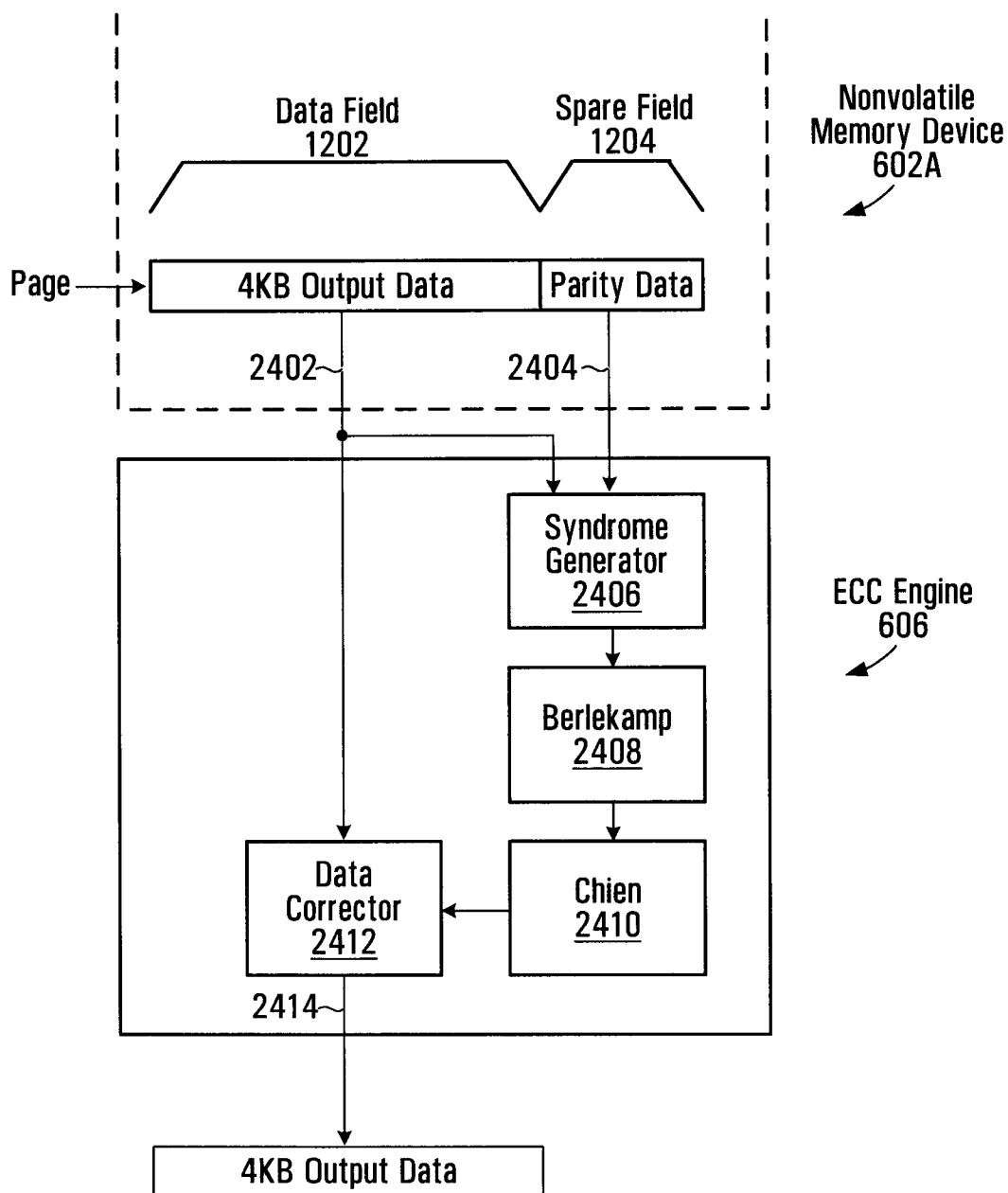


FIG. 24

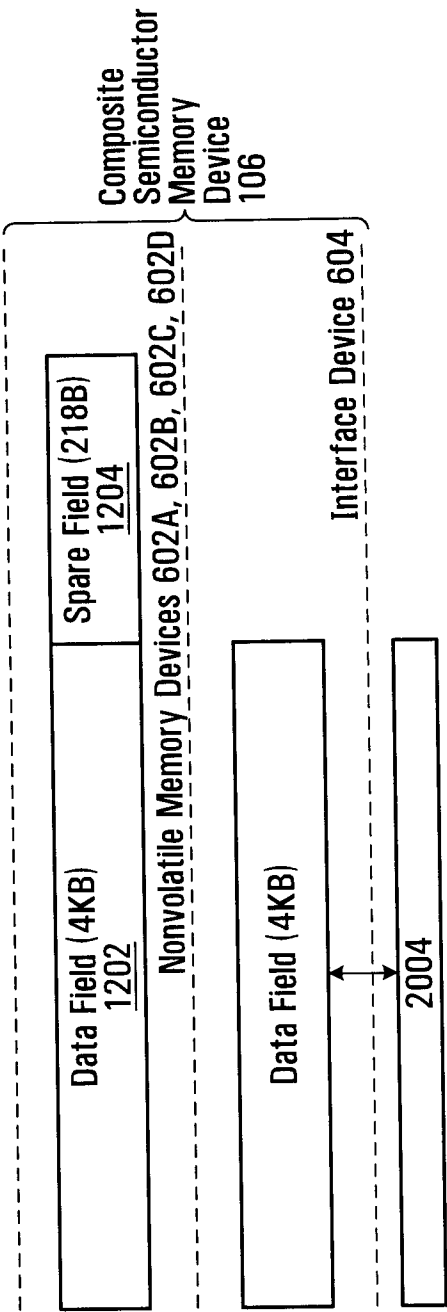


FIG. 25

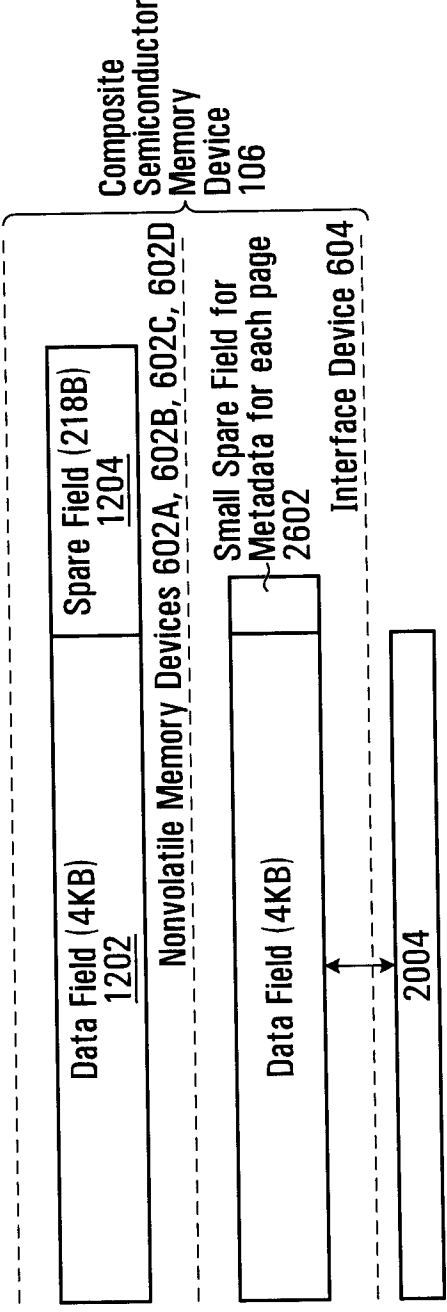


FIG. 26

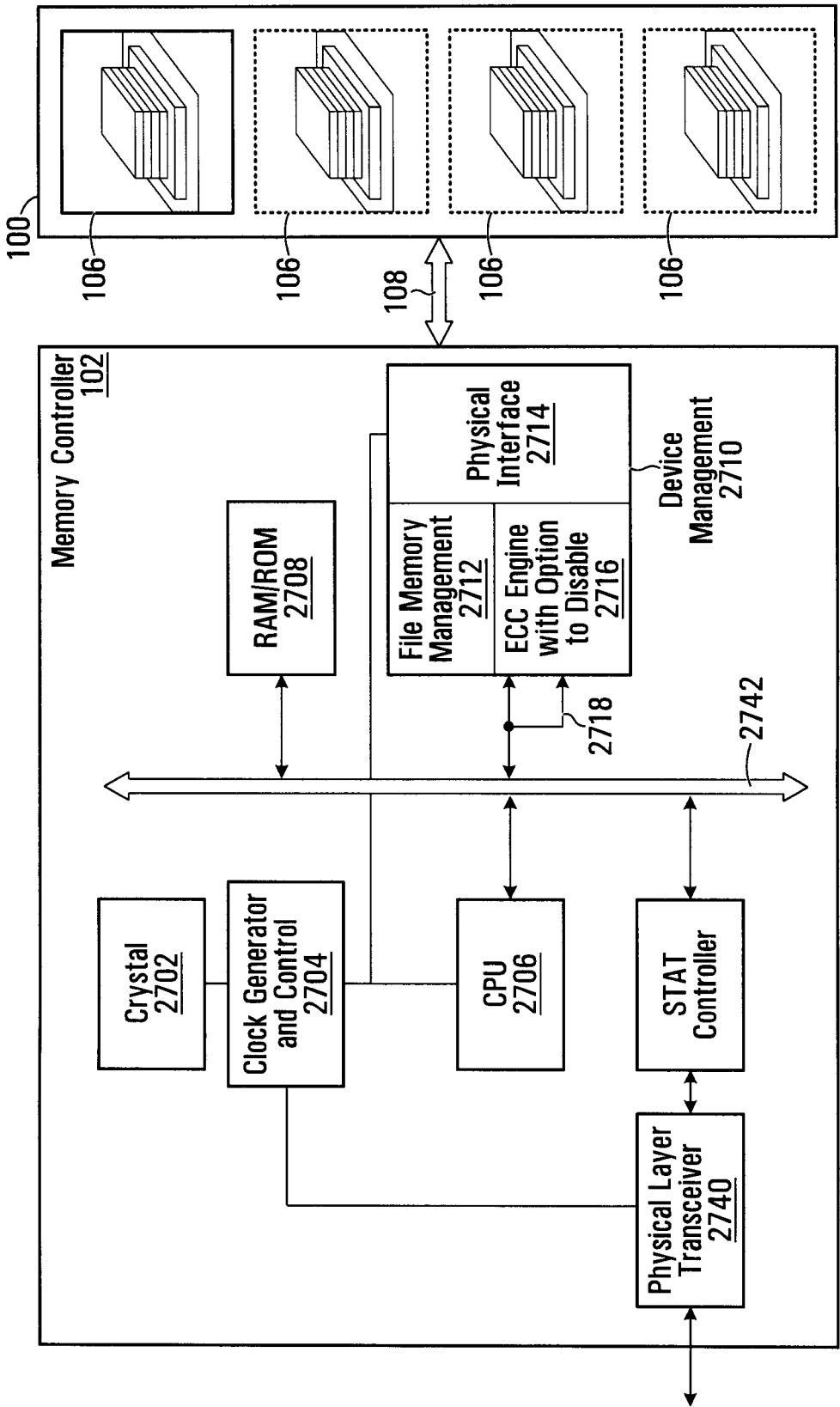


FIG. 27

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CA2011/000229

A. CLASSIFICATION OF SUBJECT MATTER IPC: G11C 29/42 (2006.01) According to International Patent Classification (IPC) or to both national classification and IPC														
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) IPC (2006.01): G11C 29/42 in combination with keywords Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Electronic database(s) consulted during the international search (name of database(s) and, where practicable, search terms used) Databases: Canadian Patent Database, TotalPatent Keywords: memory controller, error correction														
C. DOCUMENTS CONSIDERED TO BE RELEVANT														
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.												
X	US 20040181733 A1 (HILTON R. L. et al.) 16 September 2004 (16-09-2004) * [0004] - [0043], Table A, Table B, Fig 2, Fig. 4, Fig. 5 *	1-58												
☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.														
<table border="0"> <tr> <td>* Special categories of cited documents :</td> <td>"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</td> </tr> <tr> <td>"A" document defining the general state of the art which is not considered to be of particular relevance</td> <td>"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone</td> </tr> <tr> <td>"E" earlier application or patent but published on or after the international filing date</td> <td>"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art</td> </tr> <tr> <td>"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)</td> <td>"&" document member of the same patent family</td> </tr> <tr> <td>"O" document referring to an oral disclosure, use, exhibition or other means</td> <td></td> </tr> <tr> <td>"P" document published prior to the international filing date but later than the priority date claimed</td> <td></td> </tr> </table>			* Special categories of cited documents :	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention	"A" document defining the general state of the art which is not considered to be of particular relevance	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone	"E" earlier application or patent but published on or after the international filing date	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art	"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&" document member of the same patent family	"O" document referring to an oral disclosure, use, exhibition or other means		"P" document published prior to the international filing date but later than the priority date claimed	
* Special categories of cited documents :	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention													
"A" document defining the general state of the art which is not considered to be of particular relevance	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone													
"E" earlier application or patent but published on or after the international filing date	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art													
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&" document member of the same patent family													
"O" document referring to an oral disclosure, use, exhibition or other means														
"P" document published prior to the international filing date but later than the priority date claimed														
Date of the actual completion of the international search 6 April 2011 (06-04-2011)		Date of mailing of the international search report 20 April 2011 (20-04-2011)												
Name and mailing address of the ISA/CA Canadian Intellectual Property Office Place du Portage I, C114 - 1st Floor, Box PCT 50 Victoria Street Gatineau, Quebec K1A 0C9 Facsimile No.: 001-819-953-2476		Authorized officer Andy Wong (819) 953-1562												

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CA2011/000229

Patent Document Cited in Search Report	Publication Date	Patent Family Member(s)	Publication Date
US2004181733A1	16 September 2004 (16-09-2004)	DE102004002219A1 JP2004272900A US7904786B2	07 October 2004 (07-10-2004) 30 September 2004 (30-09-2004) 08 March 2011 (08-03-2011)