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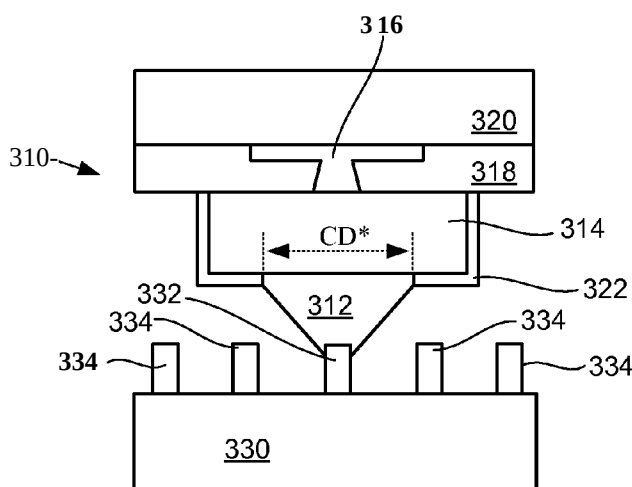
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Fig. 4



(57) Abstract: Electronic assemblies and methods including the formation of interconnect structures are described. In one embodiment an apparatus includes semiconductor die and a first metal bump on the die, the first metal bump including a surface having a first part and a second part. The apparatus also includes a solder resistant coating covering the first part of the surface and leaving the second part of the surface uncovered. Other embodiments are described and claimed.

HIGH DENSITY PACKAGE INTERCONNECTS

BACKGROUND

With the ever increasing feature growth and performance in each integrated circuit device
5 generation, there is a need to correspondingly shrink the feature sizes of integrated circuit die
interconnects and package substrate to provide higher performance in cost-optimized die sizes.
This scaling phenomenon leads to the use of complex design layouts and manufacturing
techniques in order to form reliable interconnect structures having suitable electrical and
mechanical properties. It has proven difficult to continue to shrink the feature size of the
10 interconnect structures while forming a reliable solder connection between the die and substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments are described by way of example, with reference to the accompanying
drawings, which are not drawn to scale.

15 Figure 1 illustrates a cross-sectional view of an interconnect structure in an input/output
(I/O) signal region of a die structure positioned adjacent to a pad region on a package substrate,
in accordance with certain embodiments.

Figure 2 illustrates a cross-sectional view of an interconnect structure in an I/O power or
core power region of a die structure positioned adjacent to a pad region on a package substrate,
20 in accordance with certain embodiments.

Figures 3A-3E illustrate cross-sectional views of operations in the formation of a solder
resistant coating over a portion of a metal bump on a die, in accordance with certain
embodiments.

Figure 4 illustrates a cross-sectional view of an interconnect structure connecting an I/O
25 signal region of a die to a substrate through a solder connection, in accordance with certain
embodiments.

Figure 5 illustrates a package substrate with a die attach region having no photoresist
positioned therein, in accordance with certain embodiments.

Figures 6A and 6B illustrate a comparison of pad regions on a substrate. Figure 6A
30 includes all circular pads. Figure 6B includes a combination of circular pads and rectangular
pads, in accordance with certain embodiments.

Figure 7 illustrates a view of solder connections having a plurality of different sizes and
geometries, in accordance with certain embodiments.

Figures 8A and 8B illustrate memory escape configurations. Figure 8A illustrates a
35 configuration on a substrate including a stripline escape pattern, in accordance with certain

embodiments. Figure 8B illustrates a configuration on a substrate including a microstrip escape pattern, in accordance with certain embodiments.

Figure 9 illustrates a die to die microstrip escape configuration on a substrate, in accordance with certain embodiments.

5 Figures 10A and 10B illustrate flowcharts of operations. Figure 10A is a flowchart of operations for forming a solder connection in an I/O signal region, in accordance with certain embodiments. Figure 10B is a flowchart of operations for forming a solder connection in a core power or I/O power region, in accordance with certain embodiments.

10 Figure 11 illustrates an electronic system arrangement in which embodiments may find application.

DETAILED DESCRIPTION

Reference below will be made to the drawings wherein like structures may be provided with like reference designations. In order to show the structures of various embodiments most
15 clearly, the drawings included herein include diagrammatic representations of electronic device and integrated circuit structures. Thus, the actual appearance of the fabricated structures may appear different while still incorporating the claimed structures of the illustrated embodiments. Moreover, the drawings may show only the structures necessary to understand the illustrated embodiments. Additional structures known in the art have not been included to maintain the
20 clarity of the drawings.

Certain embodiments relate the formation of interconnect architectures that enable high input/output escape density and reduced interlayer dielectric stress in a die structure. Embodiments include a number of features. One feature of certain embodiments relates to the control of the relationship between the size of the die structure copper bump-solder wetted
25 interface to the size of the package substrate pad, for connections including input/output (I/O) signal regions, and for core power and I/O power regions. Another feature of certain embodiments relates to the size of the Cu pad in the I/O signal region and in the core power and I/O power regions. Another feature of certain embodiments relates to the formation of a solder resistant coating on a portion of the copper bump on the die structure. Still another feature of
30 certain embodiments relates to covering the package substrate pads and traces under the die with a thin surface finish layer. Still another feature of certain embodiments relates to controlling the positioning of solder resist on the package substrate so that no solder resist is present under the die and a distance outward from the die shadow. Certain embodiments may include the formation of a full array of high density die to package interconnects.

In accordance with certain embodiments, architectural features in different regions, such as the I/O signal region, the core power region, and the I/O power region, may have different sizes. In certain embodiments, the shapes and sizes within one region, such as within the I/O signal region, may vary in different locations. This may occur for a variety of reasons, including, but not limited to, the routing geometry, the density needs, the control of stresses, and the power needs in the different regions.

Figure 1 illustrates a cross-sectional view of an assembly including an interconnect structure in an I/O signal region of a die structure 10 positioned adjacent to a pad region on a package substrate 30, in accordance with certain embodiments. The die structure 10 includes a solder bump 12 positioned on a metal bump such as a copper (Cu) bump 14 electrically coupled to the metal interconnect region 16 extending through dielectric layer 18 positioned on layer 20, which may comprise one or more layers including, but not necessarily limited to, a semiconductor die or semiconductor layers, dielectric layers, and metal layers. The Cu bump 14 includes a solder-resistant coating 22 that inhibits the wetting of solder, to control the size of the solder bump 12 formed after reflow. The package substrate 30 as illustrated in Figure 1 includes a substrate pad 32 adapted to receive the solder bump 12 from the die structure 10 and form a solder connection therethrough. In certain embodiments the pad 32 is sized to accept a C4 solder bump. The package substrate 30 as illustrated in Figure 1 also includes traces 34 adjacent to the pad 32. The traces 34 may in certain embodiments have the same width as the pad 32 (and thus may be used as a pad) or may have a different width than the pad 32. For example, in certain embodiments, the pad 32 may have a width of about 13 μm and the traces 34 may have a width of about 8 μm .

The package substrate 30 may also include a very thin surface finish layer 38 on the pad 32 and traces 34. In certain embodiments, the surface finish layer 38 is less than 200 nm thick and may be formed from materials including, but not limited to, OSP (Organic Solderability Preservative), Au (gold), Ag (silver), and Sn (tin). In certain embodiments, a thin surface finish layer such as layer 38 may be formed on all exposed metal (e.g., Cu) surfaces on the substrate. The surface finish layer 38 is thin enough that it can be soldered through during the process of attaching the die structure 10 to the package substrate 30. In certain embodiments, the surface finish layer is formed to a thickness of about 100 nm.

In one aspect of certain embodiments, the width of the interface of the solder bump 12 and Cu bump 14 is controlled to ensure that a high density and reliable interconnect structure can be made. If the solder bump 12 extends along the entire width of the Cu bump 14 and up the sidewalls 15, 17 of the Cu bump 14, it may be more difficult to make a reliable solder interconnection. In addition, as the spacing between adjacent solder connections decreases, the

risk of solder bridging between solder connections and/or solder bridging to an adjacent trace on the substrate (causing electrical shorting) increases. One way to control the width of the interface is to coat a portion of the Cu bump 14 with a solder resistant material that inhibits the wetting of solder to keep the solder from spreading along the various surfaces of the Cu bump

5 14. Si nitride deposited to a thickness of about 200 nm is an example of such a solder resistant coating material. Other suitable materials may also be used.

In certain embodiments, it has been found that to form a dense and reliable die to package interconnect in the I/O signal region, the width of the interface of the solder bump 12 and the Cu bump 14 for at least some of the interconnects should be greater than the width of the substrate pad 32 to which the solder bump 12 is coupled. In certain embodiments, such a relationship between solder bump 12 to Cu bump 14 interface and the width of the substrate pad 32 is particularly suitable when a relatively small substrate pad width and a small spacing between substrate pads is used, to ensure that a satisfactory solder bond can be made while at the same time controlling the width of the solder bond to minimize the occurrence of bridging between adjacent solder connections and between a solder connection and an adjacent substrate trace.

The width of the interface of the solder bump 12 and the Cu bump 14 defines a minimum dimension CD^* (as indicated by the dotted line arrow in Figure 1) that provides a die to package interconnect to be bonded directly to a substrate pad 32 to form a reliable connection. To form the reliable interconnection, as noted above, it is beneficial to inhibit the solder from wetting and spreading along the entire width of the Cu bump 14 and the Cu bump vertical walls 15, 17. It should be noted that there are a number of reasons why it may be advantageous to have a relatively large Cu bump 14 width while having a smaller solder interface CD^* formed on the Cu bump 14. First, a smaller solder interface may provide the ability to have a tighter pitch on the substrate. Second, the presence of a larger sized Cu bump 14 may provide improved mechanical properties over a die having smaller Cu bumps 14 because the Cu may act to absorb some of the stresses that would otherwise be transmitted into the dielectric layer 18. In addition, having a larger Cu bump 14 generally enables better maximum current carrying capability to the die structure 10. The solder wetted area on the Cu bump 14 may have any desired shape, including, but not limited to, rectangular, circular, or oval shaped when viewed from above. If the solder wetted area is circular in shape, the CD^* is the diameter of the solder wetted area interface.

In certain embodiments, the CD^* may be determined based on the size of the pad on the substrate to be coupled to, and the tolerances including the chip placement tolerance, the substrate trace and pad width tolerance, and substrate trace and pad thickness tolerance, and the formed solder profile. Such tolerances may vary depending on the processing operations used. Embodiments may utilize any suitable solder attachment process for forming the die to substrate

solder connection, including, but not limited to, thermal compression bonding. In an I/O signal region, in certain embodiments where thermal compression bonding is used, the CD* has been found to be equal to the substrate pad width plus two times a value, the value determined from the substrate pad to substrate trace spacing minus a tolerance factor equal to about $9\text{ }\mu\text{m} \pm 1\text{ }\mu\text{m}$.

- 5 Table 1 below includes architectural information including pitches and dimensions for I/O signal regions and core and I/O power regions, including CD* values for regions having a different I/O signal pitch along an edge of a substrate. For example, as set forth in Table 1, in an embodiment including approximately 37 I/O signal lines per millimeter and a pad width of $13\text{ }\mu\text{m}$, a CD* having a width of $21\text{ }\mu\text{m}$ was determined. This means that for the substrate pad width of $13\text{ }\mu\text{m}$,
 10 the width of the solder to Cu bump interface should be a minimum of $21\text{ }\mu\text{m}$ to ensure the formation of a reliable solder connection between the Cu bump and the substrate pad in an I/O signal region. Architectural information for other embodiments, including an embodiment including approximately 47 I/O signal lines per mm and a pad width of $13\text{ }\mu\text{m}$, and another embodiment including core power or I/O power connections having a $66\text{ }\mu\text{m}$ substrate pad
 15 width, are also provided in Table 1. It should be noted that where a bump or pad is circular in shape, its width is equal to its diameter.

Table 1. Architecture dimensions for I/O signal regions and power regions.

20	Region	<u>~47 I/O signal per mm</u>	<u>~37 I/O signal per mm</u>	<u>Core Power & I/O Power</u>
	Bump pitch	$45\text{ }\mu\text{m}$ (2 row deep)	$55\text{ }\mu\text{m}$ (2 row deep)	$90\text{-}130\text{ }\mu\text{m}$
	Bump pitch	$85\text{ }\mu\text{m}$ (4 row deep)	$107\text{ }\mu\text{m}$ (4 row deep)	
	Bump width	$25\text{-}30\text{ }\mu\text{m}$ (2 row deep)	$35\text{-}40\text{ }\mu\text{m}$ (2 row deep)	$70\text{-}100\text{ }\mu\text{m}$
	Bump width	$60\text{-}70\text{ }\mu\text{m}$ (4 row deep)	$80\text{-}90\text{ }\mu\text{m}$ (4 row deep)	
25	CD*	$20\text{ }\mu\text{m}$ (2 row deep)	$21\text{ }\mu\text{m}$ (2 row deep)	$40\text{-}89\text{ }\mu\text{m}$
	CD*	$20 \times (45\text{-}65)\text{ }\mu\text{m}$ (4 row deep)	$21 \times (45\text{-}84)\text{ }\mu\text{m}$ (4 row deep)	
	Cu bump ht.	$18.5\text{ }\mu\text{m}$	$18.5\text{ }\mu\text{m}$	$18.5\text{ }\mu\text{m}$
	Solder ht.	$25\text{ }\mu\text{m}$	$25\text{ }\mu\text{m}$	$25\text{ }\mu\text{m}$
	Pad width	$13 \times (45\text{-}74)\text{ }\mu\text{m}$	$13 \times (45\text{-}84)\text{ }\mu\text{m}$	$66\text{-}89\text{ }\mu\text{m}$
30	Pad thickness	$15\text{ }\mu\text{m}$	$15\text{ }\mu\text{m}$	$15\text{ }\mu\text{m}$
	Line pitch	$20\text{ }\mu\text{m}$	$27\text{ }\mu\text{m}$	N/A
	Line thickness	$15\text{ }\mu\text{m}$	$15\text{ }\mu\text{m}$	N/A

Figure 2 illustrates a cross-sectional view of an assembly including of an interconnect structure in a core power or I/O power region of a die structure 110 positioned adjacent to a pad 132 on a package substrate 130, in accordance with certain embodiments. The structure is similar to that of Figure 1, with the solder bump 112 positioned on a Cu bump 114 electrically coupled to the metal interconnect region 116 extending through dielectric layer 118 positioned on the layer 120, which may comprise one or more layers including, but not necessarily limited to, a semiconductor die or semiconductor layers, dielectric layers, and metal layers. In the embodiment illustrated in Figure 2, the Cu bump 114, the solder bump 112, and the substrate pad 132 may be sized differently than those described above in connection with the I/O signal region described in connection with Figure 1. The Cu bump 114 includes a solder-resistant coating 122 (like the coating 22 described above) that inhibits the wetting of solder, to control the size of the solder bump 112 formed after reflow.

In certain embodiments, it has been found that in the I/O power and the core power regions, such as illustrated in Figure 2, the CD*, the width of the interface of the solder bump 112 and the Cu bump 114, should be not greater than the width of the substrate pad 32 to which the solder bump 12 will be coupled, to minimize interlayer dielectric (ILD) stress and to optimize electromigration resistance (IMAX). In these power regions, both the Cu bump on the die structure and the substrate pads are typically relatively large, so a reliable solder joint is relatively easy to obtain. As seen in Figure 2, the CD* the width of the solder bump 112 interface with the Cu bump 114, is less than the width of the substrate pad 132.

As noted above, one method to control the width of the interface between the Cu bump and the solder is to form a coating on the Cu bump. Figures 3A-3E illustrate operations in the formation of such a coating. Figure 3A illustrates a cross-sectional view of a die structure including a Cu bump 214 electrically coupled through metal interconnect region 216 extending through dielectric layer 218 positioned on layer 220, which may comprise one or more layers including, but not necessarily limited to, dielectric, metal, and semiconductor layers. The Cu bump 214 includes a solder-resistant coating 222 positioned thereon. The solder resistant coating 222 may be formed from any suitable material, for example, SiN.

Figure 3B illustrates a cross-sectional view of a patterned photoresist layer 236 formed on the Cu bump 214 and on the dielectric layer 218 adjacent to the Cu bump 214. As illustrated in Figure 3C, the photoresist layer 236 is processed to expose a central portion of the Cu bump 214 and the underlying solder resistant coating 222 is also removed in the central portion of the bump 214 using any suitable method. If the solder resistant coating 222 is SiN, then a nitride etch operation may be used to remove the coating 222 from the central portion of the bump 214. As illustrated in Figure 3D, solder may be delivered to the exposed region on the Cu bump 214 (for

example, using a suitable solder paste print operation) and reflowed to form solder bump 212. The photoresist layer 236 remaining may then be stripped, yielding the structure illustrated in Figure 3E, which includes a Cu bump 214 having a solder bump 212 in a central region thereof, and a solder resistant coated region 222 positioned outside of the solder bump 212 on the surface of the Cu bump 214 and on the sidewalls of the Cu bump 214. Such a structure enables careful control of the size of the solder bump 212 formed on the Cu bump 214.

Embodiments also include the formation of solder connections having different morphologies, including, but not limited to, circular, elliptical, oval, rectangular, and triangular shaped bumps.

Figure 4 illustrates a cross-sectional view of an interconnect structure in a I/O signal region of a die structure 310 coupled to a substrate 330 through solder connection 312, in accordance with certain embodiments. The die structure 310 includes a solder connection 312 between a Cu bump 314 electrically coupled to the metal interconnect region 316 extending through dielectric layer 318 positioned on layer 320, which may comprise one or more layers including, but not necessarily limited to, a semiconductor die or semiconductor layers, dielectric layers, and metal layers. The Cu bump 314 includes a solder-resistant coating 322 to control the size of the solder connection 312 formed after reflow. The package substrate 330 as illustrated in Figure 4 includes a pad 332 to which the solder connection 312 is made. As noted above, in certain embodiments, in an I/O signal region, it is preferred to have a CD* width dimension of the solder connection 312 to Cu bump 314 interface be greater than that of the substrate pad width for at least some of the pads, in particular, those pads having a relatively small width. Figure 4 illustrates such a configuration, in which the width of the interface (CD*) of the solder connection 312 and Cu bump 314 (controlled by the solder-resistant coating 322) is greater than the width of the substrate pad 332. In such embodiments, the solder connection may have a substantially triangular shape in cross-section, as illustrated in Figure 4.

Figure 5 illustrates a view of a package substrate 430 with a die attach region or die shadow 431 bounded by dashed lines. The die shadow 431 (also known as die footprint) is the region on the package substrate 430 that is covered by the die when viewed from above. Certain embodiments include package substrate 430 being formed without solder resist 436 under the die shadow 431. Instead, any solder resist 436 is positioned outside of a region 442 about 0.5 to 2 mm outside of the die shadow 431 on the substrate 430.

Certain embodiments permit the use of variable size and shape bumps and pads on the die structure and on the package substrate. Certain regions may be one size and shape, and other regions having the same or different signal needs, power needs, or routing needs may be a different size and shape. Figure 6A illustrates a four row deep pattern of pads PI on a substrate

surface for use in a C4 connection scheme. The pads PI are of uniform shape and size. Fig 6B illustrates an embodiment including a variable pad size and shape for a four row deep pattern of pads PI, P2. The first two rows of pads are rectangular pads P2 and the second two rows are circular pads PI. The rectangular pads P2 are substantially smaller in dimension than the

5 circular pads PI and can be positioned in a tighter pitch. The length X1 in Figure 6A is equal to the length X2 in Figure 6B. However, the length Y1 in Figure 6A is substantially greater than the length Y2 in Figure 6B. As a result, the same number of pads (e.g., I/O signal) can be placed in less area on the surface of the substrate in the embodiment illustrated in Figure 6B.

Figure 7 illustrates an x-ray image of a portion of a test assembly formed in accordance with certain embodiments, showing the solder connections between a die and substrate. The

10 connections include a variety of different shaped solder connections on a variety of different shaped pads. As indicated by regions delineated by brackets in Figure 7, region SI at an upper portion of Figure 7 shows an input/output signal pattern of solder connections made on small rectangular pads on the substrate. The wire traces leading from the pads can also be seen. The

15 bracketed regions P below the region SI include I/O power or core power solder connections made on larger circular substrate pads. The region S2 located in the lower right quadrant of Figure 7 shows another input/output signal pattern of solder connections made on rectangular pads on the substrate. The SI region (I/O signal) solder connections are substantially smaller than the P region solder connections and as a result, the pitch in the S1 region is smaller than the

20 pitch in the P region. As can be seen in Figure 7, the shape of the solder connection may vary from the shape of the pads, and may, for example, take a variety of shapes such as elliptical when viewed from above. Embodiments are not limited to the solder connection shapes and sizes illustrated in Figure 7, and may include a variety of combinations of solder connection shapes and sizes.

25 The use of smaller solder connections and pads also enables a wide variety of trace patterns to be utilized. The added space on surface due to the smaller size of the solder connection and the smaller pad size leaves room to route traces on the surface of the substrate that may not be possible when larger connections and pads, such as the I/O power connections and pads in portion P2, are used.

30 Figures 8A and 8B illustrate embodiments including memory region escape patterns on a substrate including regions of stripline escape in Figure 8A and microstrip escape in Figure 8B.

Figure 8A illustrates a back to back two channel DDR configuration including a stripline escape pattern on a substrate 530, where the pads in the first and second channel regions are coupled to vias that transmit the signals to a lower level of the substrate. The first channel is

35 positioned near the top of the Figure 8A and includes two rows of relatively small rectangular

pads P2 and two rows of larger circular pads PI, when viewed from above. Solder contacts from a die positioned above the substrate are made to the pads PI and P2. The rectangular pads P2 are electrically coupled to microvias V that extend to lower layers of the substrate 530. The circular pads PI may be formed as microvia pads, where the via is directly under the pad and extends to lower layers of the substrate 530. One row of the microvias V electrically coupled to the first row of the rectangular pads P2 is positioned near a substrate 530 edge, outside of the die shadow DS (dotted line corresponding to the position where an outer edge of a die is positioned over the substrate). The second channel includes four rows of the larger circular pads PI. To the sides of the channels are I/O power lines PL, which also contain some of the pads PI and P2. In certain embodiments the rectangular pads P2 may be about 13 μm wide by 45 μm long, and the circular pads PI may be about 66 μm in diameter. Other sizes and shapes of pads (including, but not limited to, elliptical or oval shaped pads) may also be used.

Figure 8B illustrates a back to back two channel DDR configuration including a microstrip escape pattern on a substrate 630, where some of the pads are electrically coupled to traces that extend along the surface to an edge of the substrate 630. The first channel includes both rectangular shaped pads P2 and circular shaped pads 91 on the substrate. As in the embodiment illustrated in Figure 8A, the rectangular pads may be about 13 μm wide by 45 μm long, and the circular pads may be about 66 μm in diameter. The first three rows in the first channel of the memory I/O signal pads P2 all have wiring traces that extend beyond the die shadow and extend towards an edge of the substrate. As illustrated in Figure 8B, the first three rows of the first channel include two rows of rectangular pads and one row of circular pads. The last row in the first channel and the second channel include larger, circular shaped pads PI that are formed as microvia pads (pad directly over via). To the sides of the channels are I/O power lines PL, which also contain some of the pads PI and P2. It will be understood that the exact routing and number of microstrip connections versus microvia connections may be varied in different embodiments.

Both the stripline configuration illustrated in Figure 8A and the microstrip configuration illustrated in Figure 8B offer advantages over conventional escape patterns. For example, the use of the smaller, rectangular shaped pads permits closer spacing and a tighter pitch between solder contacts. The smaller pads also permit a variety of different routing configurations to be possible due to the added space and different pad geometry on the substrate surface.

Figure 9 illustrates a die to die microstrip escape configuration, in accordance with certain embodiments. Microstrip escape routing extends along the surface of the substrate 730 from the first die shadow region 731a to the second die shadow region 731b. As seen in the blown up portion of Figure 9, the microstrip escape pattern includes trace lines TR that extend from

rectangular pads P2 in the first die shadow region 731a to rectangular pads P2 in the second die shadow region 731b of the substrate 730. Power lines PL having circular pads PI are also illustrated in each of the die shadow regions 731a, 731b.

Figure 10A illustrates a flowchart of operations relating to forming a solder connection between a die structure and a substrate in an I/O signal region, in accordance with certain embodiments. Box 851 is providing a metal bump electrically coupled to an I/O signal region on a die structure. The metal bump may be a Cu bump such as described above. Box 853 is forming a solder resistant coating on the bump such that a portion of the bump is covered by the coating and a portion of the bump is uncovered by the coating. The solder resistant coating may in certain embodiments be formed in accordance with the operations described above in connection with Figs. 3A-3E. Box 855 is positioning solder on the bump in the portion uncovered by the solder, so that an interface of the solder and the bump defines a width CD*, such as described above in connection with Figure 1. Box 857 is forming a solder connection to an I/O signal substrate pad so that the CD* is greater than the width of the substrate pad, to ensure a reliable solder joint is formed between the die structure and the substrate. The I/O signal substrate pad may have a relatively small width, for example, a rectangular pad having a width of about 13 μm .

Figure 10B illustrates a flowchart of operations relating to forming a solder connection between a die structure and a substrate, in a core power or I/O power region, in accordance with certain embodiments. Box 871 is providing a metal bump electrically coupled to a core power or I/O power region on a die structure. The metal bump may be a Cu bump such as described above. Box 873 is forming a solder resistant coating on the bump such that a portion of the bump is covered by the coating and a portion of the bump is uncovered by the coating. The solder resistant coating may in certain embodiments be formed in accordance with the operations described above in connection with Figs. 3A-3E. Box 875 is positioning solder on the bump in the portion uncovered by the solder, so that an interface of the solder and the bump defines a width CD*, such as described above in connection with Figure 2. Box 877 is forming a solder connection to a core power substrate pad or I/O power substrate pad so that the CD* is not greater than the width of the substrate pad, to ensure a reliable solder joint is formed between the die structure and the substrate. The core power or I/O power substrate pad may have a relatively large width, for example, a circular pad having a diameter of about 66 μm .

It should be appreciated that the operations in the flowcharts of Figures 10A and 10B may in certain embodiments be carried out simultaneously on a single assembly.

Embodiment permit the use of a variety of architectural configurations. For example, certain embodiments may utilize some I/O signal connections made on small rectangular pads,

with other I/O connections made on larger circular shaped pads. Both I/O signal and power connections may be made on a variety of sized and shaped pads. Embodiments also permit variations in the size of the connections on the die structure, including, for example, different shaped and sized metal bumps and different CD* values for the solder connections.

5 Assemblies including structures formed as described in embodiments above may find application in a variety of electronic components. Figure 11 schematically illustrates one example of an electronic system environment in which aspects of described embodiments may be embodied. Other embodiments need not include all of the features specified in Figure 11, and may include alternative features not specified in Figure 11.

10 The system 901 of Figure 11 may include at least one central processing unit (CPU) 903. The CPU 903, also referred to as a microprocessor, may be a die attached to a package substrate 905, which is then coupled to a printed circuit board 907 (for example, a motherboard). The CPU 903 coupled to the package substrate is an example of an assembly that may be formed in accordance with embodiments such as described above. A variety of other system components,
15 including, but not limited to memory and other components discussed below, may also include structures formed in accordance with embodiments such as described above.

The system 901 may further include memory 909 and one or more controllers 911a, 911b ... 91In, which are also disposed on the motherboard 907. The motherboard 907 may be a single layer or multi-layered board which has a plurality of conductive lines that provide
20 communication between the circuits in the package 905 and other components mounted to the board 907. Alternatively, one or more of the CPU 903, memory 909 and controllers 911a, 911b ... 91In may be disposed on other cards such as daughter cards or expansion cards. The CPU 903, memory 909 and controllers 911a, 911b ... 91In may each be seated in sockets or may be connected directly to a printed circuit board or all integrated in the same package. A display 919
25 may also be included.

Any suitable operating system and various applications execute on the CPU 903 and reside in the memory 909. The content residing in memory 909 may be cached in accordance with known caching techniques. Programs and data in memory 909 may be swapped into storage 913 as part of memory management operations. The system 901 may comprise any suitable
30 computing device, including, but not limited to, a mainframe, server, personal computer, smart phone, workstation, laptop, handheld computer, netbook, tablet, book reader, handheld gaming device, handheld entertainment device (for example, MP3 (moving picture experts group layer - 3 audio) player), PDA (personal digital assistant) telephony device (wireless or wired), network appliance, virtualization device, storage controller, network controller, router, etc.

The controllers 911a, 911b ... 911n may include one or more of a system controller, peripheral controller, memory controller, hub controller, I/O (input/output) bus controller, video controller, network controller, storage controller, communications controller, etc. For example, a storage controller can control the reading of data from and the writing of data to the storage 913 in accordance with a storage protocol layer. The storage protocol of the layer may be any of a number of known storage protocols. Data being written to or read from the storage 913 may be cached in accordance with known caching techniques. A network controller can include one or more protocol layers to send and receive network packets to and from remote devices over a network 921. The network 921 may comprise a Local Area Network (LAN), the Internet, a Wide Area Network (WAN), Storage Area Network (SAN), etc. Embodiments may be configured to transmit and receive data over a wireless network or connection. In certain embodiments, the network controller and various protocol layers may employ the Ethernet protocol over unshielded twisted pair cable, token ring protocol, Fibre Channel protocol, etc., or any other suitable network communication protocol.

Terms such as "first", "second", and the like may be used herein and do not necessarily denote any particular order, quantity, or importance, but are used to distinguish one element from another. Terms such as "top", "bottom", "upper", "lower", "overlying", and the like may be used for descriptive purposes only and are not to be construed as limiting. Embodiments may be manufactured, used, and contained in a variety of positions and orientations.

In the foregoing Detailed Description, various features are grouped together for the purpose of streamlining the disclosure. This method of disclosure is not to be interpreted as reflecting an intention that the claimed embodiments of the invention require more features than are expressly recited in each claim. Rather, as the following claims reflect, inventive subject matter may lie in less than all features of a single disclosed embodiment. Thus the following claims are hereby incorporated into the Detailed Description, with each claim standing on its own as a separate preferred embodiment.

While certain exemplary embodiments have been described above and shown in the accompanying drawings, it is to be understood that such embodiments are merely illustrative and not restrictive, and that embodiments are not restricted to the specific constructions and arrangements shown and described since modifications may occur to those having ordinary skill in the art.

What is claimed:

1. An apparatus comprising:
a semiconductor die;
5 a first metal bump on the die, the first metal bump including a surface having a first part and a second part; and
a solder resistant coating covering the first part of the surface and leaving the second part of the surface uncovered.
- 10 2. The apparatus of claim 1, further comprising:
a substrate including a first pad adapted to receive a solder connection, the first pad having a width;
a solder connection between the first metal bump on the die and the first pad;
wherein the solder connection between the first metal bump and the first pad includes an
15 interface between the solder connection and the metal bump, wherein the interface has a width equal to the second part of the surface uncovered by the solder resistant coating; and
wherein the interface between the solder connection and the metal bump has a width that is greater than the width of the first pad.
- 20 3. The apparatus of claim 2, wherein the first metal bump is electrically coupled to an input/output signal region on the semiconductor die.
4. The apparatus of claim 3, further comprising:
a second metal bump on the die, the second metal bump including a surface having a first
25 part and a second part, a solder resistant coating covering the first part of the surface and leaving the second part of the surface uncovered.
a second pad adapted to receive a solder connection on the substrate, the second pad having a width;
a solder connection between the second metal bump on the die and the second pad,
30 wherein the solder connection between the second metal bump and the second pad includes an interface between the solder connection and the second metal bump, wherein the interface between the solder connection and the second metal bump has a width equal to the second part of the second metal bump surface uncovered by the solder resistant coating; and
wherein the interface between the solder connection and the second metal bump has a
35 width that is no greater than the width of the second pad.

5. The apparatus of claim 4, wherein the second metal bump is electrically coupled to a power region on the semiconductor die, the power region selected from the group consisting of a core power region and an input/output power region.

5

6. The apparatus of claim 5, wherein the first pad is rectangular in shape and the second pad is circular in shape.

7. The apparatus of claim 5, wherein the first pad has a width that is smaller than that of the second pad.

10

8. An apparatus comprising:

a semiconductor die structure including I/O signal lines and power lines, the power lines including at least one of core power lines and I/O power lines;

15

the die structure including a plurality of metal bumps, including a first group of metal bumps coupled to the I/O signal lines, and a second group of metal bumps coupled to the power lines; and

wherein at least some of the metal bumps of the first group have a different pitch than at least some of the metal bumps of the second group.

20

9. The apparatus of claim 8, wherein at least some of metal bumps of the first group have at least one difference selected from the group consisting of a different shape and a different width, than at least some of the metal bumps of the second group.

25

10. The apparatus of claim 8, wherein at least some of the metal bumps of the first group are rectangular in shape.

11. The apparatus of claim 9, wherein at least some of the metal bumps of the second group are circular in shape.

30

12. The apparatus of claim 8, wherein the first group of metal bumps includes a first sub-group of metal bumps and a second sub-group of metal bumps, wherein the first sub-group has a smaller pitch than the second sub-group.

13. The apparatus of claim 8, further comprising a solder coupled to each of the first group of metal bumps, wherein the solder defines an interface on the metal bump where the solder and metal bump are in contact, and wherein the interface has a width that is less than that of the metal bump.

5

14. The apparatus of claim 8, further comprising a solder resistant layer positioned on at least some of the first group of metal bumps, wherein the metal bumps having the solder resistant layer thereon include a first portion covered by the solder resistant layer and a second portion uncovered by the solder resistant layer.

10

15. The apparatus of claim 14, further comprising:

a solder connection on each of the metal bumps having the solder resistant layer thereon, the solder connection being positioned on the second portion uncovered by the solder resistant layer, the solder connection defining an interface where the solder connection and the metal bump are in contact; and

15

a substrate, the substrate including a plurality of pads each connected to a metal bump through one of the solder connections, wherein a width of the interface where the solder connection and the metal bump are in contact is greater than a width of the substrate pad to which the metal bump is connected.

20

16. The apparatus of claim 8, further comprising:

a solder resistant layer positioned on the first group of metal bumps and on the second group of metal bumps;

a substrate including a first group of pads and a second group of pads;

25

a solder connection between each of the first group of metal bumps and the first group of pads,

a solder connection between each of the second group of metal bumps and the second group of pads;

30

wherein for each of the first group of solder connections, an interface between the solder connection and the metal bump has a width that is greater than a width of the pad to which it is connected; and

wherein for each of the second group of solder connections, an interface between the solder connection and the metal bump has a width that no greater than a width of the pad to which it is connected.

35

17. An apparatus comprising:

a package substrate including a die side, the die side including a die structure footprint;
a plurality of package substrate pads adapted to electrically couple with a die including
integrated circuits, the die to be disposed in the die structure footprint;

5 the substrate pads including a first group of substrate pads and a second group of substrate
pads, and

wherein at least some substrate pads of the first group have a smaller pitch than at least
some of the substrate pads of the second group.

10 18. The apparatus of claim 17, wherein at least some of substrate pads of the first group
have a difference from at least some of the substrate pads of the second group, the difference
selected from the group consisting of a different shape and a different width.

15 19. The apparatus of claim 17, wherein the package substrate is free of solder resist
within the die structure footprint.

20 20. The apparatus of claim 17, wherein the package substrate is free of solder resist
within the die structure footprint and free of solder resist for a distance outside of the die
structure footprint in the range of 0.5 mm to 2 mm.

21. The apparatus of claim 17, wherein the first group of substrate pads are adapted to
receive memory signals in a two channel back to back configuration, wherein the first group of
substrate pads includes a first channel pad region and a second channel pad region, the first
channel pad region including a first sub-group of substrate pads having a first pitch and a second
25 sub-group of substrate pads having a second pitch that is larger than the first pitch.

22. The apparatus of claim 21, wherein the first sub-group of substrate pads is positioned
closer to an outer edge of the die footprint than the second sub-group of substrate pads.

30 23. The apparatus of claim 21, wherein the substrate pads in the second channel pad
region have a pitch that is equal to that of the second sub-group of substrate pads in the first
channel pad region.

24. The apparatus of claim 21, wherein the substrate pads in the first sub-group of substrate pads are rectangular in shape and the substrate pads in the second-sub-group of substrate pads are circular in shape.

5 25. The apparatus of claim 17, further comprising:
a die structure coupled to the package substrate, the die structure including a plurality of metal bumps;

a solder connection from the metal bumps on the die structure to the package substrate pads on the package substrate, the solder connection defining a width of an interface between
10 each metal bump and the solder connection thereto; and

wherein for at least some of the package substrate pads in the first group of substrate pads, the solder connection is configured so that the width of the interface between the metal bump and the solder connection is greater than a width of the pad to which that metal bump is connected.

15 26. The apparatus of claim 25, wherein for at least some of the package substrate pads in the second group of substrate pads, the solder connection is configured so that the width of the interface between the metal bump and the solder connection is no greater than a width of the pad to which that metal bump is connected.

20 27. A method for forming an interconnect, comprising:

providing a first metal bump electrically coupled to an I/O signal region on a die, the first metal bump including a solder resistant coating that covers a first portion of the first metal bump and leaves a second portion of the first metal bump uncovered;

25 providing a substrate having a first pad, the first pad having a pad width;

a solder connection between the first metal bump and the first pad, wherein the solder connection includes an interface between the solder connection and the second portion of the first metal bump, the interface having a width; and

30 wherein the solder connection is controlled so that the width of the interface between the solder connection and the second portion of the first metal bump is greater than the first pad width.

28. The method of claim 27, further comprising:

providing a second metal bump electrically coupled to a power region on the die, the second metal bump including a solder resistant coating that covers a first portion of the second metal bump and leaves a second portion of the second metal bump uncovered;

5 providing a second pad on the substrate, the second pad having a pad width;

a second solder connection between the second metal bump and the second pad, wherein the second solder connection includes an interface between the second solder connection and the second portion of the second metal bump, the interface having a width; and

10 wherein the second solder connection is controlled so that the width of the interface between the second solder connection and the second portion of the second metal bump is no greater than the second pad width.

29. The method of claim 28, wherein the first pad width is smaller than the second pad width.

15

30. The method of claim 28, wherein the first pad is rectangular in shape and the second pad is circular in shape.

Fig. 1

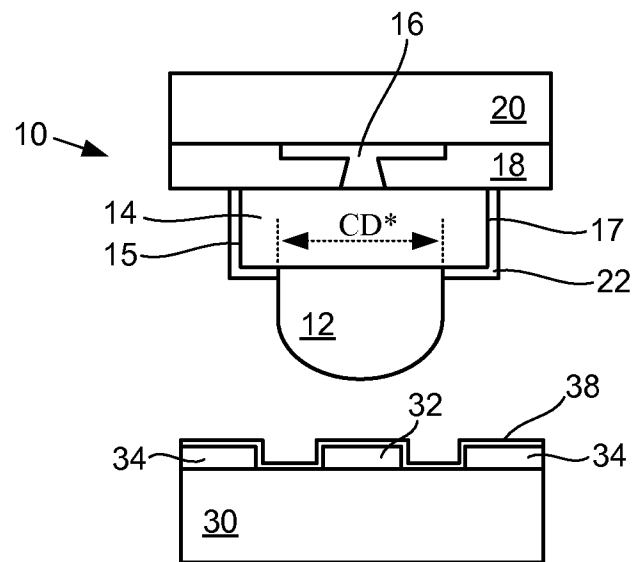


Fig. 2

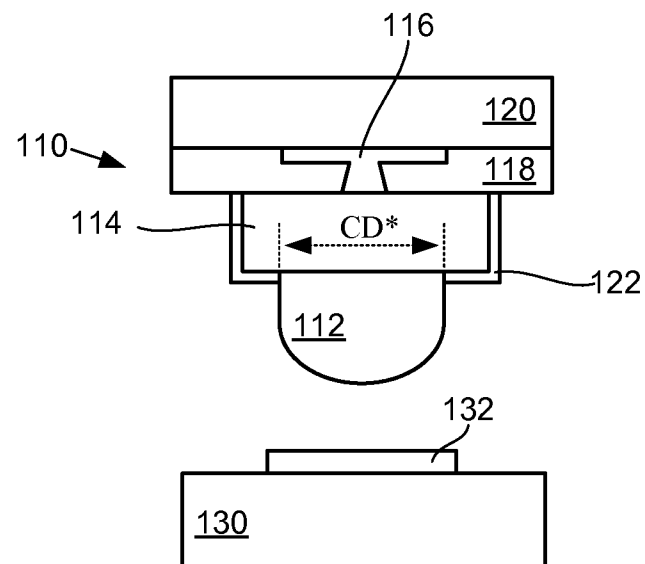


Fig. 3A

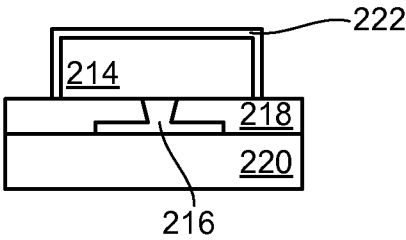


Fig. 3B

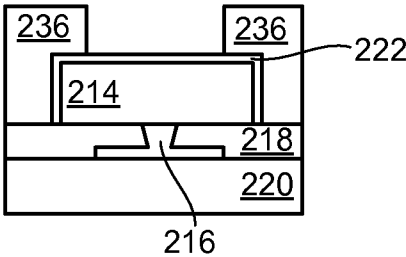


Fig. 3C

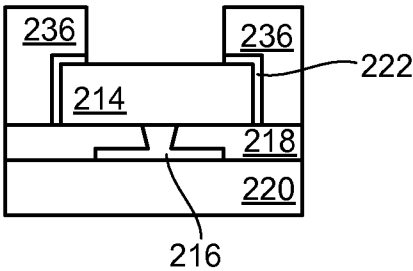


Fig. 3D

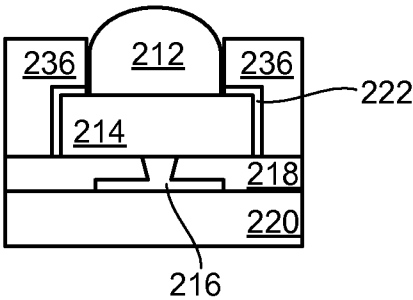


Fig. 3E

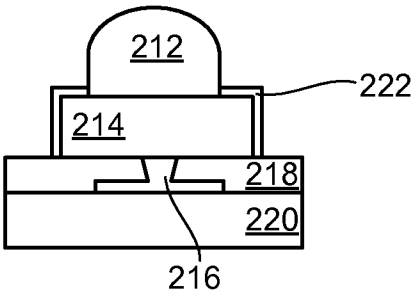


Fig. 4

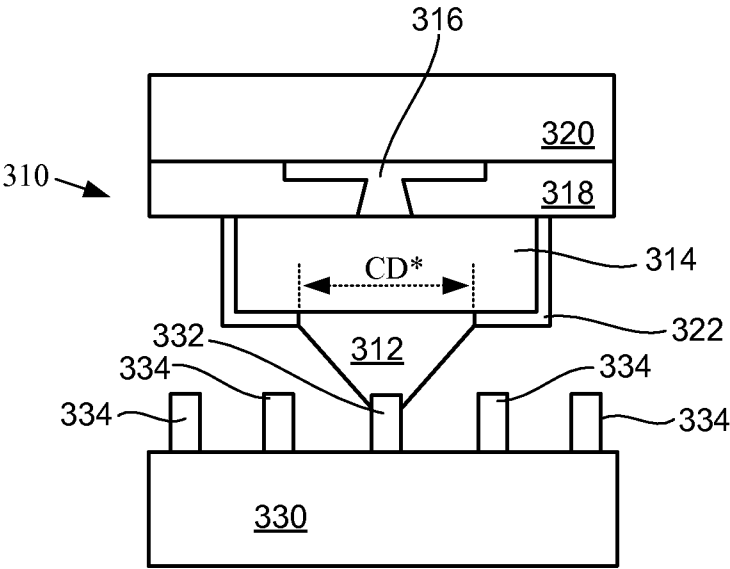
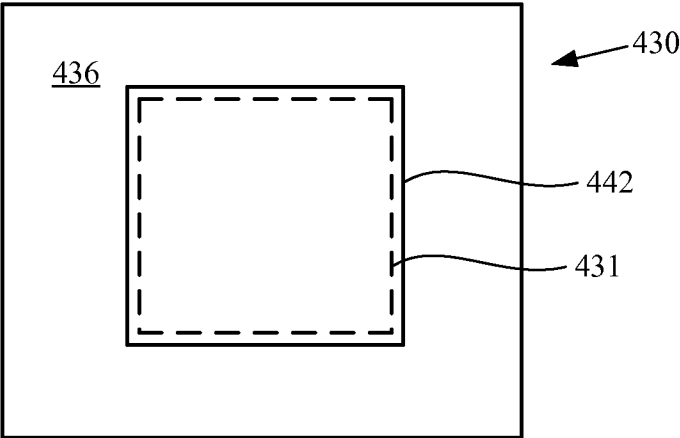


Fig. 5



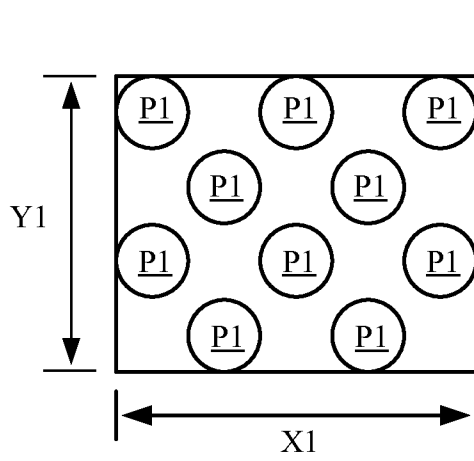


Fig. 6A

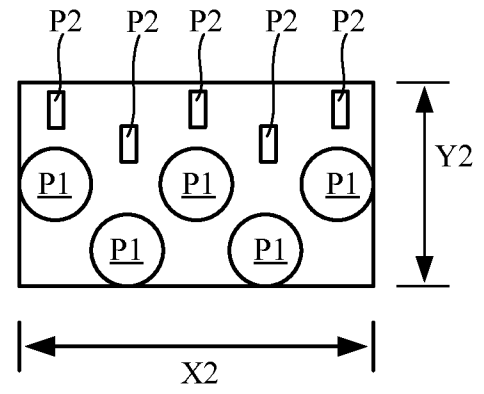


Fig. 6B

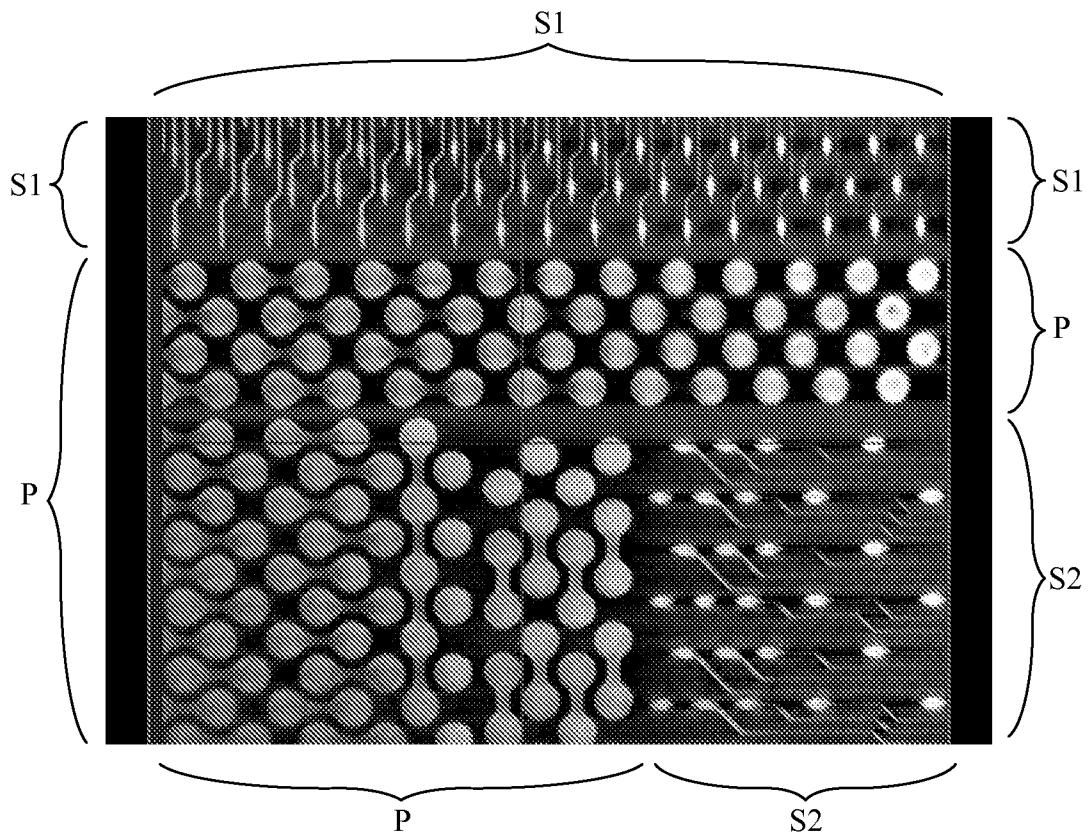


Fig. 7

Fig. 8A

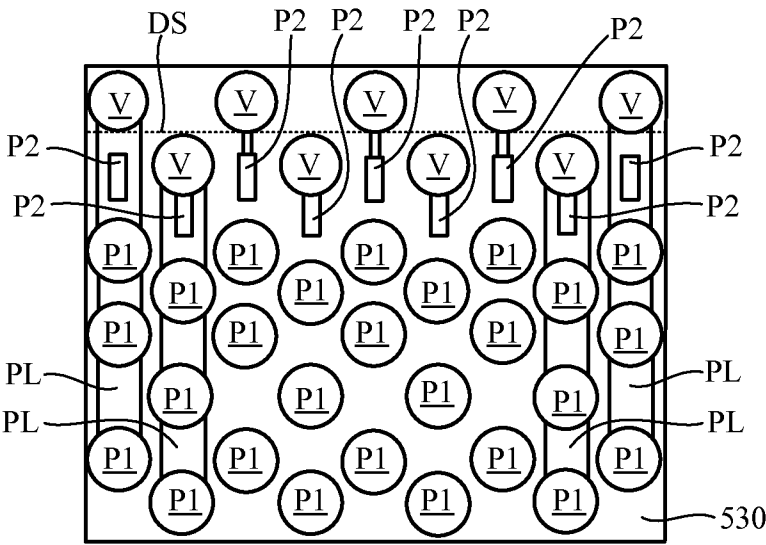
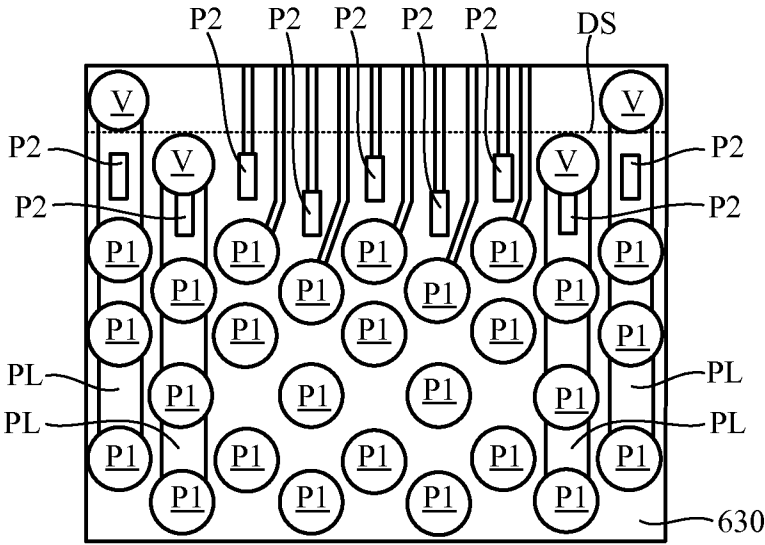


Fig. 8B



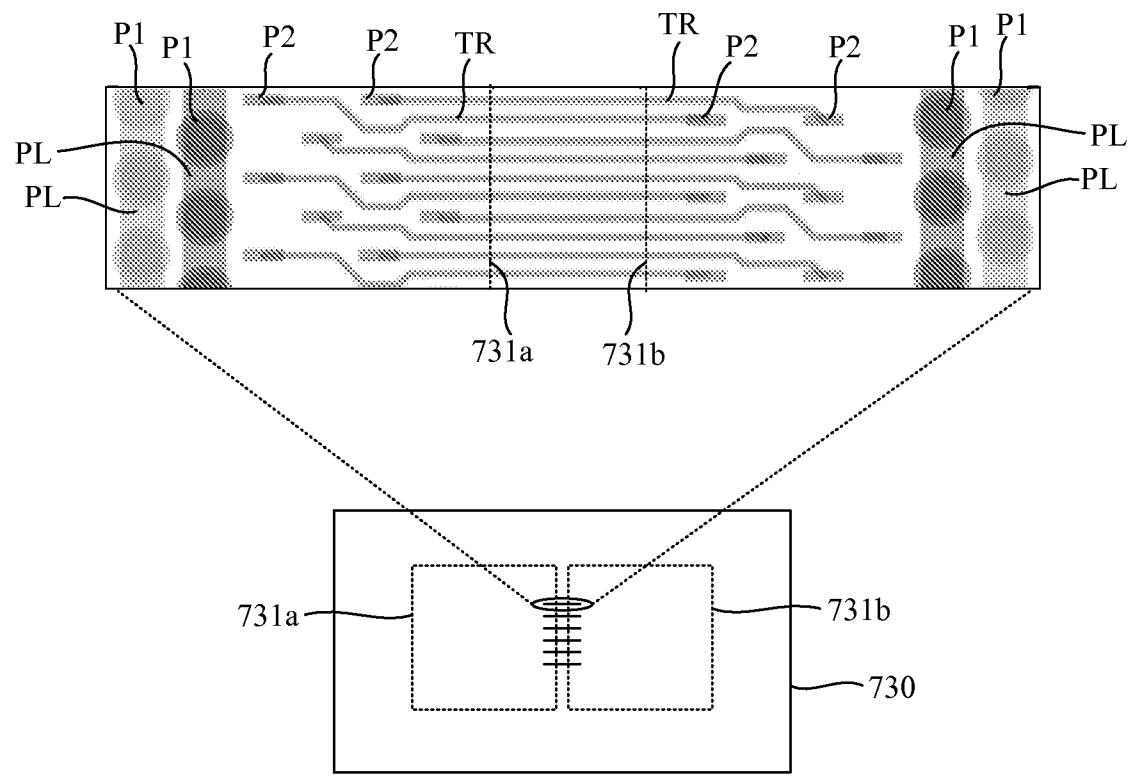


Fig. 9

Fig. 10A

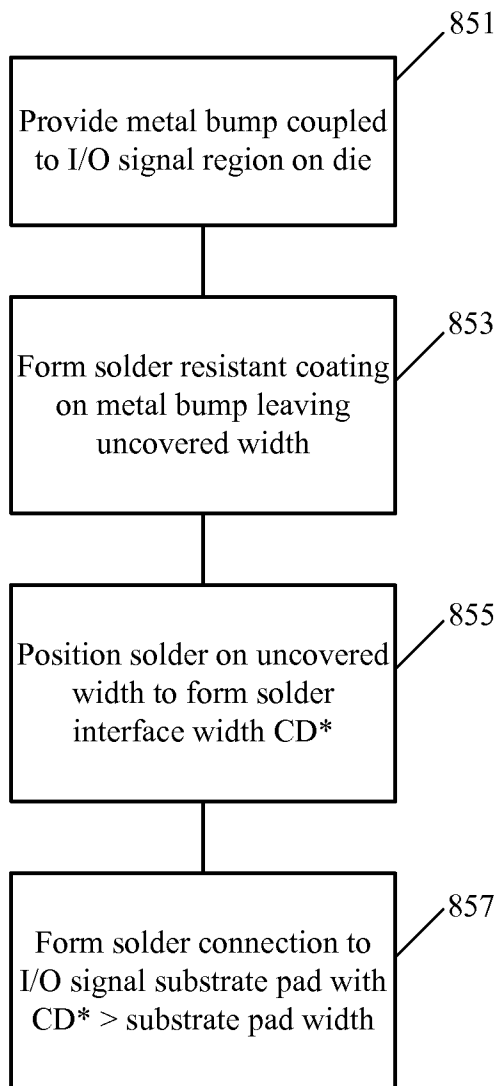


Fig. 10B

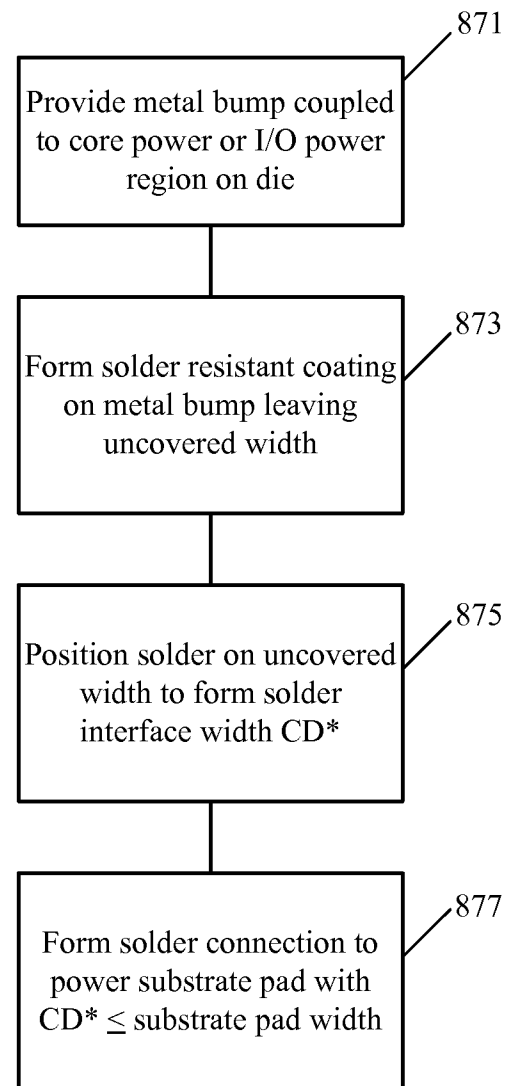
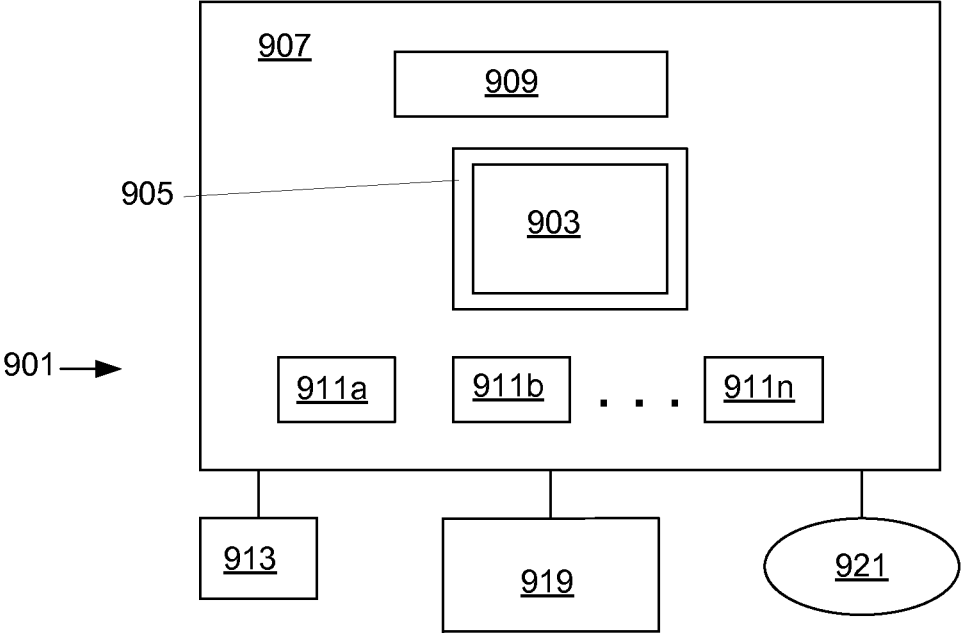


Fig. 11



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US20 11/068278**A. CLASSIFICATION OF SUBJECT MATTER*****H01L 21/60(2006.01)i***

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/60; H01R 12/04; G03F 7/00; H01L 23/12; H01L 23/498; H05K 1/11

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility modelsElectronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: bump,solder,resist,mask,pad,joint,width**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 2006-261641 A (TAIWAN SEMICONDUCTOR MANUFACTURING CO LTD) 28 September 2006 See abstract ; figures 1-3 ; paragraphs [0014]-[0022]	1-7
A	US 2005-0106505 A1 (TZ-CHENG CHIU et al.) 19 May 2005 See figures 5A-5C; paragraphs [0027H0039]	1-7
A	US 2011-0101519 A1 (HSIAO CHING-WEN et al.) 05 May 2011 See abstract ; figures 1A-4 ; paragraphs [0018]-[0029]	1-7
A	US 6420664 B1 (MURAMATSU; SHIGETSUGU et al.) 16 July 2002 See figure 1; column 6 lines 5 - 50	1-7

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

09 NOVEMBER 2012 (09.11.2012)

Date of mailing of the international search report

12 NOVEMBER 2012 (12.11.2012)

Name and mailing address of the ISA/KR

Korean Intellectual Property Office
189 Cheongsu-ro, Seo-gu, Daejeon Metropolitan
City, 302-701, Republic of Korea

Facsimile No. 82-42-472-7140

Authorized officer

Kim, Young Jin

Telephone No. 042 481 5771



INTERNATIONAL SEARCH REPORT

International application No.

PCT/US20 11/068278

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

Claims [1-7] are directed to an apparatus comprising a solder resistant coating partially covering the surface of a metal bump on a die. Claims [8-16] are directed to an apparatus comprising: a first metal bumps coupled to the I/O signal and a second metal bumps coupled to the power, wherein the first metal bumps have a different pitch than the second metal bumps. Claims [17-26] are directed to an apparatus comprising: a package substrate including a die structure footprint and substrate pads; wherein some substrate pads have a different pitch than others. Claims [27-30] are directed to a method comprising: providing a first I/O signal metal bump on a die, wherein the first metal bump is partially covered with a solder resistant coating; providing a substrate having a first pad; providing a solder connection having an interface between the solder connection and the uncovered portion of the first metal bump, wherein the width of the interface is greater than the width of the first pad.

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☒ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
1-7

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☒ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☒ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2011/068278

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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