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Stenstrom et al.

[11] **3,796,991**

[45] **Mar. 12, 1974**

[54] **ERROR-CORRECTING DEVICE FOR THE TRANSMISSION OF DATA**

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[30] **Foreign Application Priority Data**

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[51] **Int. Cl.** **G08c 25/00,** H04l 1/00

[58] **Field of Search** ..... 178/69 R, 69 G, 69.5 R, 178/69.5 G; 325/41; 340/146.1 AB, 146.1 D

[56] **References Cited**

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Assistant Examiner—R. Stephen Dildine, Jr.
Attorney, Agent, or Firm—Craig & Antonelli

[57] **ABSTRACT**

An error-correcting device for the transmission of data on a telegraph line with modulation by coded pulses (MIC) whose sampling sequence is more rapid than the telegraphic speed (number of bits per second), which leads to transmitting in the MIC pattern information bits, doubling bits, called "padded bits," as well as supplementary bits, called "packing or padded indications," which make it possible to recognize whether a given bit is an information bit or a padded bit. The succession of the valances of the packing indications follows a well defined law. The invention furnishes the means to carry out a correction if this law is not complied with.

7 Claims, 5 Drawing Figures

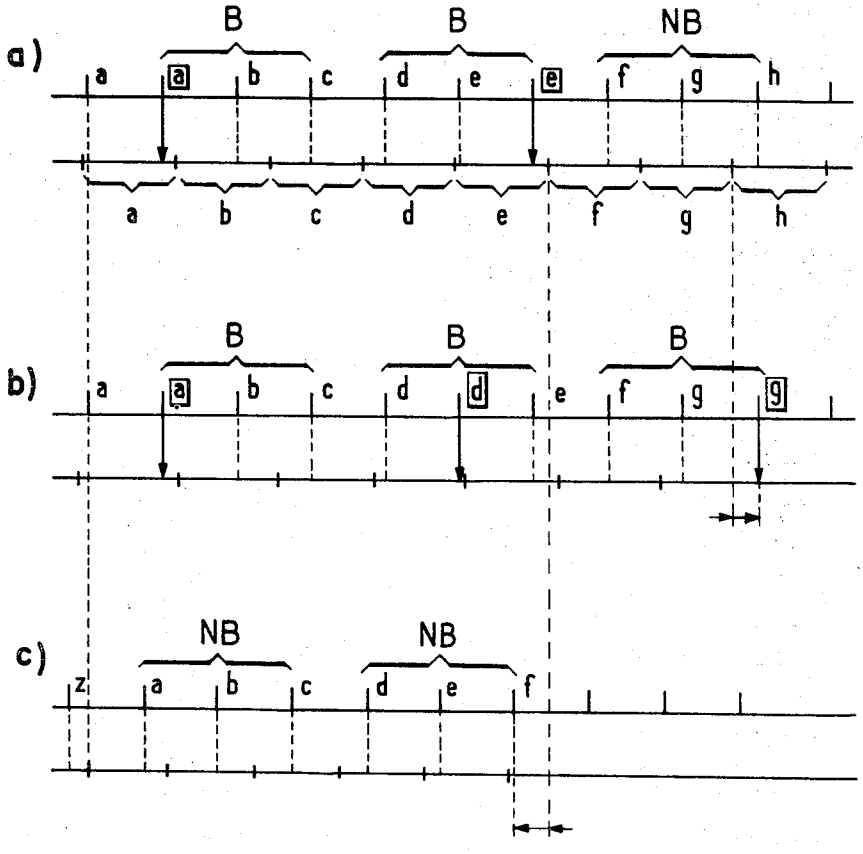


FIG. 1

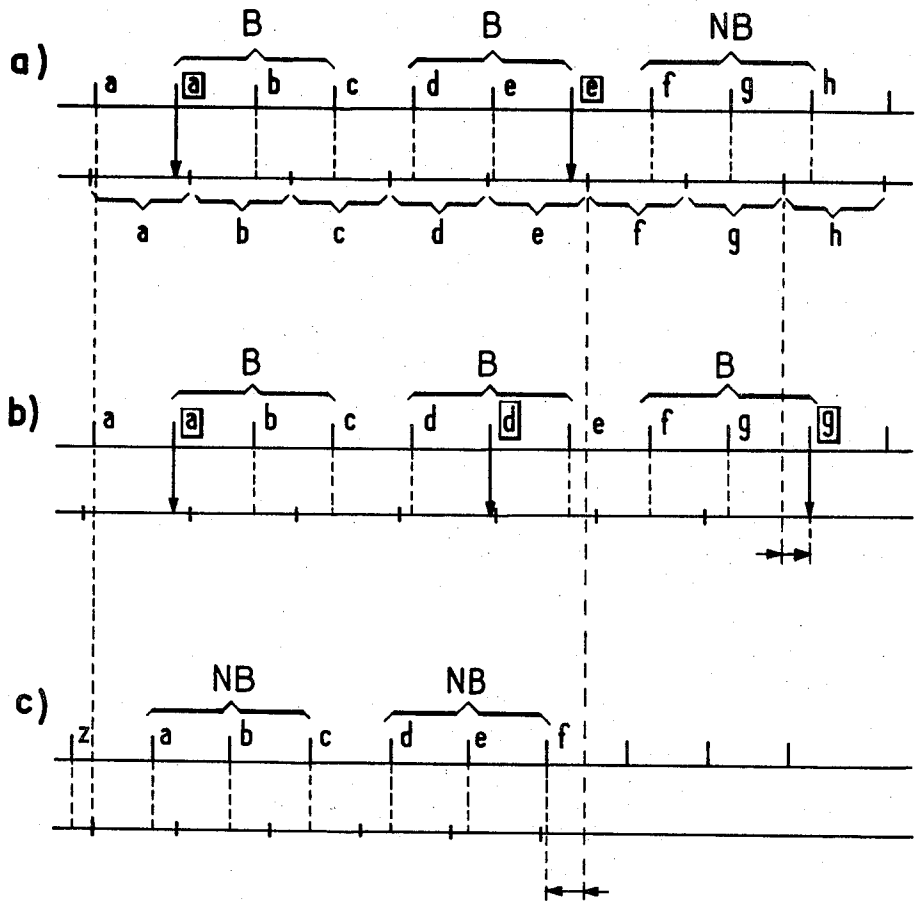
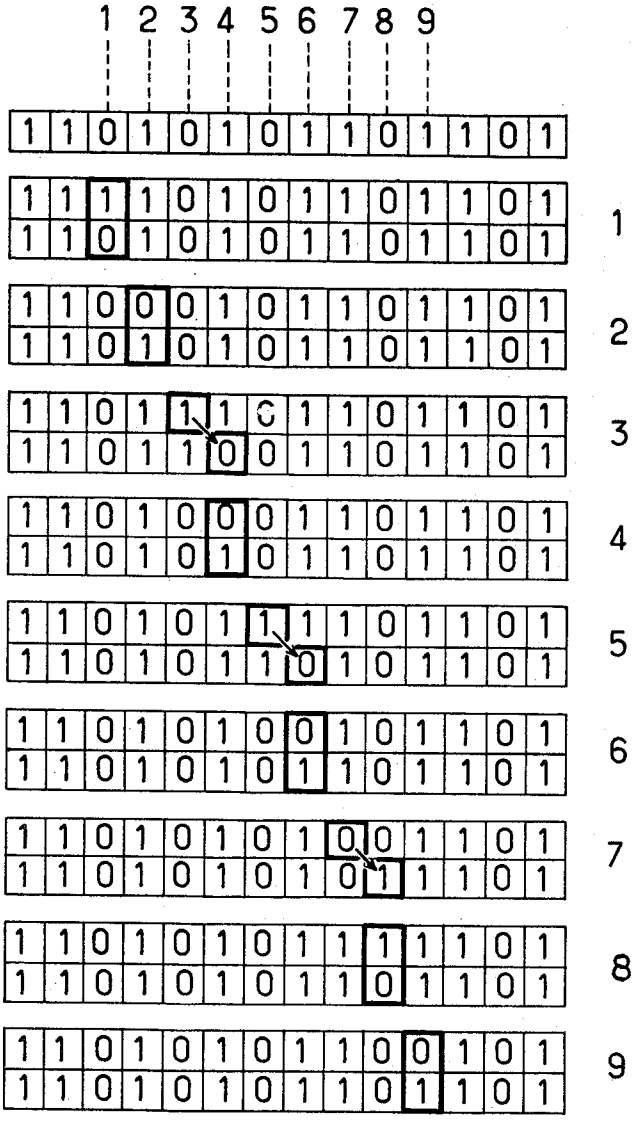


FIG. 2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1 1 0 1 0 1 0 1 1 0 1 1 0 1
2
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3
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1 1 0 1 0 1 0 1 1 0 1 1 0 1
4
1 1 0 1 0 1 1 1 1 0 1 1 0 1
1 1 0 1 0 1 1 0 1 0 1 1 0 1
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1 1 0 1 0 1 0 1 1 0 1 1 0 1
6
1 1 0 1 0 1 0 1 0 0 1 1 0 1
1 1 0 1 0 1 0 1 0 1 1 1 0 1
7
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8
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1 1 0 1 0 1 0 1 1 0 1 1 0 1
9

FIG. 3

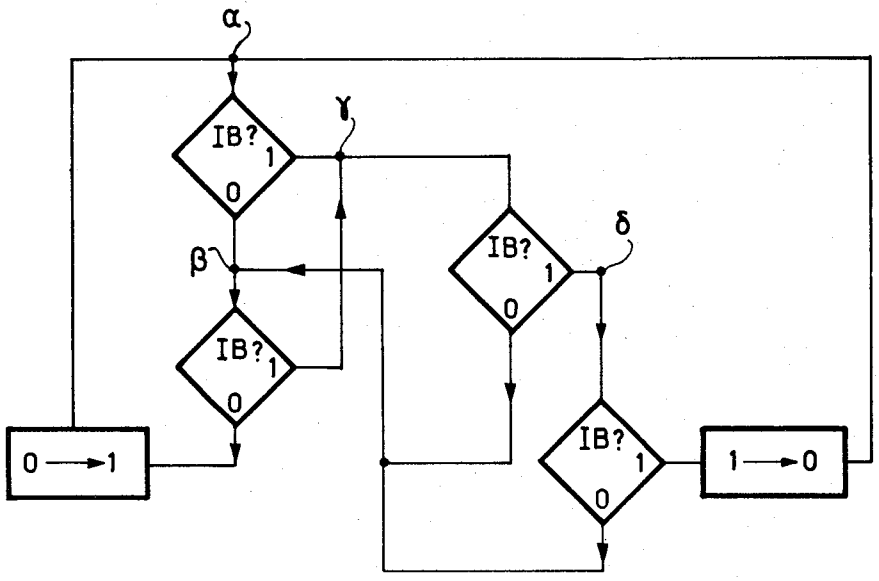


FIG. 4

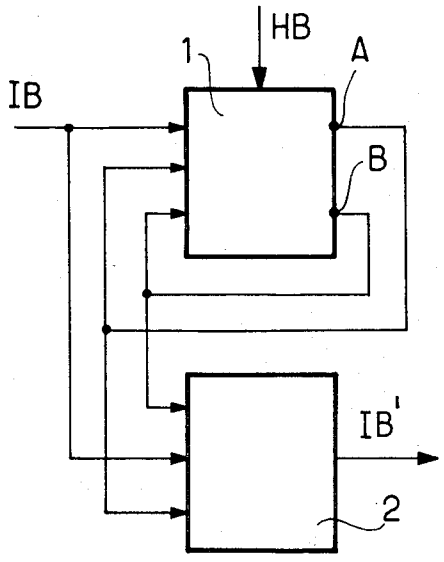
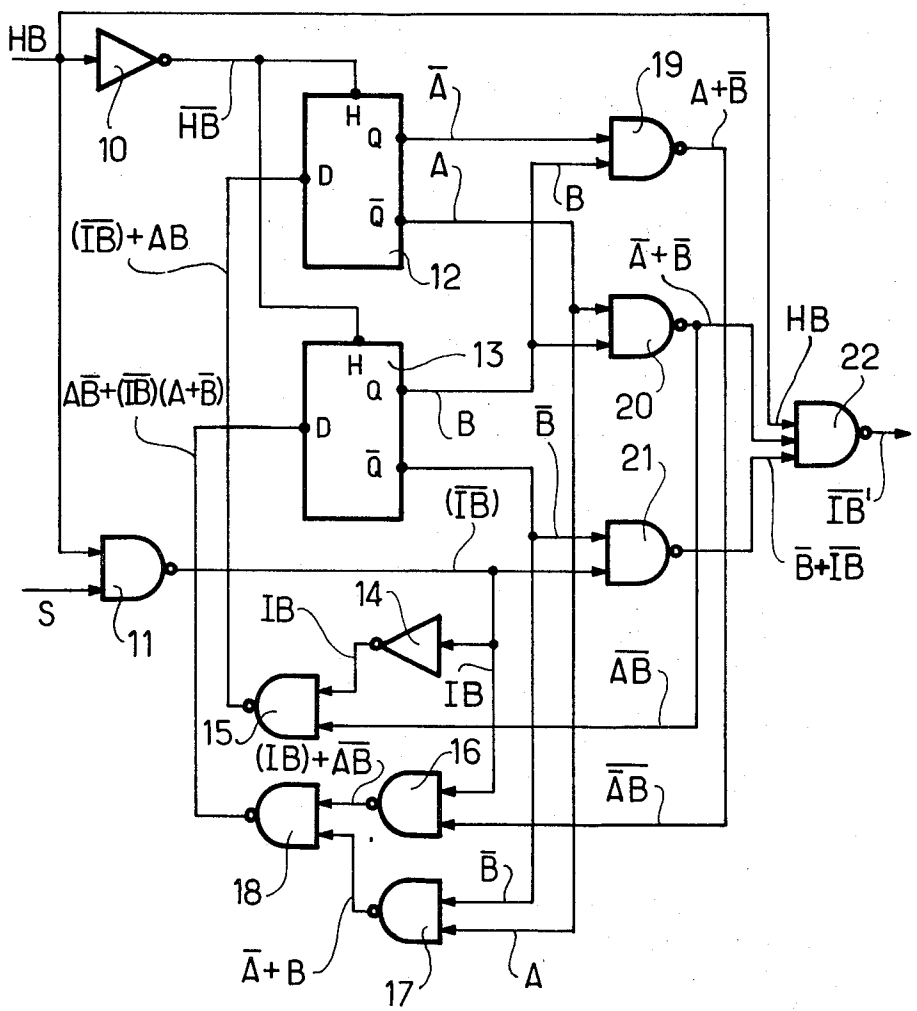


FIG. 5


HB
10
$\overline{HB}$
H
D
Q
$\overline{Q}$
$\overline{A}$
A
12
19
$A+\overline{B}$
B
$(\overline{IB})+AB$
$\overline{A}+\overline{B}$
HB
22
13
20
$A\overline{B}+(\overline{IB})(A+\overline{B})$
B
$\overline{B}$
21
$(\overline{IB})$
$\overline{IB}'$
$\overline{B}+\overline{IB}$
S
11
IB
14
IB
$\overline{AB}$
15
$(IB)+\overline{AB}$
16
$\overline{\overline{AB}}$
18
$\overline{B}$
$\overline{A}+B$
17
A

ERROR-CORRECTING DEVICE FOR THE TRANSMISSION OF DATA

The present invention relates to the transmission of data or characteristics on a telegraph line. It is more particularly concerned with and directed to the transmission of data on a telegraph path or line with a modulation by coded pulses (MIC) whose sampling sequence or repetition is more rapid than the telegraphic speed (number of bits per second), which leads to transmitting in the MIC pattern (1) information bits, (2) doubled bits, the so-called "padded bits," as well as (3) supplementary bits, called "packing indications or signals," which make it possible to recognize whether a given bit is an information bit or a padded bit. The succession of the valences of the packing indications follows a well defined law, and the present invention furnishes the means for producing a correction if this law is not complied with. The application of the present invention is directed toward the transmission of data in an MIC pattern.

The transmission of data on a telegraph line is carried out at a telegraphic speed chosen from among the normal telegraphic speeds, for example at one of the following speeds: 1,200 – 2,400 – 4,800 – 9,600 bits/second.

The sampling sequences or repetitions of the MIC patterns in use for the telegraph transmissions are multiples of 500 Hz. In order not to lose information in a transmission of data on an MIC frame or pattern, it is evidently necessary to adopt a higher frame or pattern sequence and, in fact, in a fixed ratio to the telegraphic speed V. For the telegraphic speeds V referred to above, this leads to the following sampling sequences:

F		V	ratio F/V
1500 Hz	for	1200 b/s	5/4
3000 Hz	for	2400 b/s	5/4
6000 Hz	for	4800 b/s	5/4
12000 Hz	for	9600 b/s	5/4

This speed supplement of the frequency MICF over the telegraphic speed V leads by intermittence to two consecutive samplings of the same bit of information of the data. In this case, the second bit MIC corresponding to the same bit of "data" is called the "packing bit" or "packed bit."

Under these circumstances it is necessary to feed into the line a supplementary information which renders it possible to recognize whether a bit which has been received is an information bit or a packed or padded bit. This is obtained by systematically interposing at a specific sequence bits that are called "packing indications" in accordance with the following rule: if the packing indication (IB) received is 1, the preceding bit is a padded bit (BB); if the packing indication is 0, the preceding bit is an information bit.

The description will be continued within the framework of a transmission of data at a well defined telegraphic speed, for example 4,800 b/s, but it is understood that the conclusions which will be drawn extend and are applicable to any telegraphic speed with a frequency MIC being adapted accordingly.

It is apparent from the table provided above that there is, in principle, a ratio of 5/4 between the frequency MIC (6,000 Hz) and the telegraphic speed (4,800 b/s). In fact, it is necessary to also provide space for the packing indications. Simple arithmetic ratios lead to the possibility of interposing a packing indication one time out of four. Under these conditions, the frequency MIC passes from 6,000 Hz to 8,000 Hz ($6{,}000 \times 4/3$). The MIC frequencies associated with the different telegraphic speeds therefore have the following actual values:

2,000 Hz for 1,200 b/s
4,000 Hz for 2,400 b/s
8,000 Hz for 4,800 b/s
16,000 Hz for 9,600 b/s

It is easy to show that under ideal conditions, with the clock of "data" synchronized with the MIC clock, no distortion, and no error in transmission, the flow of packing indications is periodic (a period = 01011).

When synchronization is not assured, and when distortion phenomena appear, this period becomes a "pseudo-period," nevertheless the fact remains that the following results will be obtained within the limits of distortion which will be specified hereinbelow:

1. The valances 0 (no padding) are always isolated; there are never two or more in a row;
2. The valances 1 (padding) are never present with a sequence higher than two, i.e., there are never three or more in a row.

The result thereof is that any violation of one of these requirements stems from an error in transmission, and conversely, any error in transmission causes a violation of one of these requirements.

It is the role of the correcting device, in such a case, to carry out the necessary valance inversion. It will be shown by a detailed analysis of the various possible eventualities that, in certain cases, the false packing indication or signal is corrected immediately, while in other cases the correction is made with a time lag or delay.

The correcting means or device for the packing indication or signal according to the present invention is based on the following principle: There are never two consecutive false packing indications or signals present. It can be shown that with practical values of the parameters this is verified with a probability of approximately 10^{-10}. On the other hand, one will refrain from proceeding with consecutive corrections whose result would be a propagation of errors. Rather, after a correction has been made, one will wait at least two clock times before making the decision for effecting a possible new correction.

These and other objects, features and advantages of the present invention will be described in greater detail in the following specification, taken in conjunction with the accompanying drawing, wherein:

FIG. 1 comprises three graphs concerning the interposition of "padded bits" between certain information bits;

FIG. 2 indicates the process of correction in different error cases;

FIG. 3 illustrates a flow diagram of the correcting process according to the present invention;

FIG. 4 represents a schematic block diagram of the correcting means or device of the present invention, and

FIG. 5 is a schematic circuit diagram of one embodiment of the correcting means.

FIG. 1 comprises three sampling diagrams of a succession of moments at the speed of 4,800 b/s through an MIC section or pattern at 6,000 Hz. The MIC sampling pulses are shown in groups of three. There is packing if two MIC pulses fall within the same moment

of the "data." In this case, the recall line is marked with an arrow to designate the padded bit. Each diagram contains two lines. On the line at the top, the sampling instants have been indicated; while, on the line at the bottom, the data train is indicated.

Diagram (a) represents a case with little distortion. The formation of the pseudo-period mentioned above, i.e., 01011, 01011, is apparent in this case.

Diagram (b) corresponds to a first case of a distortion limit of the data signal, involving an extension or lengthening by 20 percent of the period within seven periods. The formation of a sequence of three packings or paddings (B) is apparent.

Diagram (c) corresponds to a second case of a distortion limit of the data signal, involving a shortening of the data signal by 20 percent of the period within five periods. The formation of a sequence of two consecutive non-packings (NB) is apparent therefrom.

It is possible to deduce from these two observations that, if one imposes upon the input signal the condition of having a distortion smaller than 20 percent in seven moments for a lengthening and smaller than 20 percent within five moments for a shortening of the time, there will never occur in the succession of packing signals or indications three successive signals equal to 1, nor two successive signals or indications equal to 0.

The principle of the error-correcting device is immediately deduced therefrom. Each time the error-correcting device detects two sucessive packing signals equal to 0, it sets the second one at 1; and, each time the correcting device detects three successive signals equal to 1, it sets the third one at 0. Moreover, once a correction has been made, the correcting device waits for the passage of at least two new signals prior to proceeding with a new correction.

FIG. 2 shows a succession of packing signals on which nine positions have been specified by way of example, and it has been assumed that one error (valence inversion) is produced on each of the nine positions. The law of the correcting device is to replace by a 1 a second 0 occurring after a first zero and to replace by a 0 a third 1 occurring after two 1's.

Under these conditions, the correcting device will either carry out an immediate correction, as seen in cases (1), (2), (4), (6), (8) and (9), or there will be a correction made with a time delay, as seen in cases (3), (5) and (7). In the first case, the correction relates to an erroneous bit. In the second case, the correction is set off by an incompatibility caused by a previous error by one step. The correction in the third case is effected with a delay in time and it will be noted that the corrected sequence is not identical with the data sequence, but allows an error to continue to exist.

If, in cases (3) and (7), once the correction has been made, one were not to take the precaution of waiting through two signal periods before making the decision to effect a possible new correction, one would create a chain of corrections, and this would in fact result in a propagation of errors. Instead of such a prejudicial result for the entire transmission, one allows an incompatibility to continue to exist locally; for example, two 0's in case (3) and three 1's in case (7). In the case of the immediate correction, the advantage is obvious; the error is erased, i.e., there remains no trace of it.

It will be shown hereinbelow that for a particular example in the case of the delayed correction, even though there remains a trace of the error, the correction is no less indispensable. Let it be assumed that the following signal is emitted (and it will be recalled that BB signifies a padded or packed bit and IB signifies a packing indication or packing signal):

Signal MIC emitted — $a\ b\ 1$ IB $c\ d\ e$ IB $f\ g\ h\ \ldots$ (1)

Signal MIC received without error — $a\ b$ BB $1\ c\ d\ e\ 0\ f\ g\ h\ \ldots$ (2)

Signal MIC received with error — $a\ b\ 1\ 0\ c\ d\ e\ 0\ f\ g\ h\ \ldots$ (3)

Signal MIC received corrected — $a\ b\ 1\ 0\ c\ d\ e\ 1\ f\ g\ h\ \ldots$ (4)

data according to (2) — $a\ b\ c\ d\ e\ f\ g\ h\ \ldots$
data according to (3) — $a\ b\ 1\ c\ d\ e\ f\ g\ \ldots$
data according to (4) — $a\ b\ 1\ c\ d\ f\ g\ h\ \ldots$

The error resides in (3) in the passage of the first IB from the valence 1 to the valence 0. The delayed correction resides in the passage of the second IB from the valence 0 to the valence 1.

It is apparent that, in the data according to case (3) where the error is not corrected, beyond *ab* all the bits are displaced; in other words, all the bits are false. In the data according to case (4), there is a disturbance bearing on, or relating to, the bits *c d e*, which after the correct correspondence is reestablished.

FIG. 3 is a flow diagram which indicates the operation of the correcting device. The correcting device is a sequential system whose configuration evolves as a function of the incident packing or padding indications or signals. This system possesses four stages or states which are interconnected by reason of the following conditions, as can be ascertained from the flow diagram of FIG. 3.

One passes from the stage (α) to the stage (β) if IB = 0

One passes from the stage (α) to the stage (γ) if IB = 1

One passes from the stage (β) to the stage (α) if IB = 0

One passes from the stage (β) to the stage (γ) if IB = 1

One passes from the stage (γ) to the stage (β) if IB = 0

One passes from the stage (γ) to the stage (δ) if IB = 1

One passes from the stage (δ) to the stage (β) if IB = 0

One passes from the stage (δ) to the stage (α) if IB = 1

Each time there is a passage to the stage (α), there is a correction of the last incident indication. If the system passes from (β) to (α), the last packing indication passes from 0 to 1; if the system passes from (δ) to (α), the last IB passes from 1 to 0.

On the other hand, the examination of the flow diagram shows clearly that, after making a correction at stage (α), it is necessary to wait at least two times before making another correction.

FIG. 4 is a schematic diagram of the correcting device of the present invention. The correcting device comprises two subgroups, a member 1 following the operations of the stage of the correcting device, receiving the incident packing indication (IB), and receiving the clock of the packing indications HB. There will re-

sult two signals A and B whose combination defines the four stages taken as basis for the flow diagram of FIG. 3. These signals are applied to a member 2 which also receives IB and is the circuit effecting the correction. The result is the corrected packing indication IB'.

The stages A and B are furnished by two memory elements (flip-flops) which serve to mark the four stages. One may, for example, establish the following correspondence which constitutes a code arbitrarily chosen among the 24 that are possible (24 = 4!):

		A	B
stage	α	0	0
stage	β	0	1
stage	γ	1	0
stage	δ	1	1

Deduced from this table is the following truth table:

Instant N IB	Instant N A B stage		Instant N+1 A B stage		Instant N IB'
0	0 0	α	0 1	β	0
1	0 0	α	1 0	γ	1
0	0 1	β	0 0	α	1 +
1	0 1	β	1 0	γ	1
0	1 0	γ	0 1	β	0
1	1 0	γ	1 1	δ	1
0	1 1	δ	0 1	β	0
1	1 1	δ	1 0	α	1 ++

There is a correction 0–1 in the case marked +, and a correction 1–0 in the case marked ++ in accordance with the flow diagram of FIG. 3.

FIG. 5 is a diagram of one embodiment of a correcting device corresponding to the flow diagram of FIG. 3 and to the schematic block diagram of FIG. 4. It comprises at the input an inverter 10 which receives the clock signals of the packing indications HB and an $\overline{\text{AND}}$ circuit 11 which, receiving the incident signal S and the clock signals $\overline{\text{HB}}$, furnishes an output $\overline{\text{IB}}$. Two flip-flops 12 and 13 receive on the clock terminal H thereof the signals HB and on the terminals D signals whose origin will be indicated hereinbelow. The flip-flops 12 and 13 furnish respective outputs $\overline{\text{A}}$ and A, B and $\overline{\text{B}}$.

An inverter 14 and seven $\overline{\text{AND}}$ circuits 15, 16, 17, 18, 19, 20 and 21 serve to apply to the terminal D of the flip-flop 12 a signal $(\overline{\text{IB}}) + \text{AB}$ and to the terminal D of the flip-flop 13 a signal $\overline{\text{AB}} + (\overline{\text{IB}})\ (\text{A} + \overline{\text{B}})$. An $\overline{\text{AND}}$ circuit 22 receiving signals HB, $(\overline{\text{A}} + \overline{\text{B}})$ and $(\overline{\text{B}} + \overline{\text{IB}})$ furnishes signal $\overline{\text{IB}}'$.

The circuits 21 and 22 are part of the subgroup 2 of FIG. 4. The circuit 20 is part, at the same time, of the subgroup 1 and of the subgroup 2. All the other circuits are part of the subgroup 1 of FIG. 4.

While there have been shown and described but specific embodiments of the invention, it will be understood by those skilled in the art that the invention is not limited thereto or thereby.

What is claimed is:

1. A device for correcting the packing indication signals in a transmission of telegraphic data, integrated in an MIC pattern with a sampling frequency higher than the telegraphic speed of the transmission of the data so as to include packing or padded bits, comprising input means for receiving the incident MIC signal and clock signals timing the packing indications, and logic means connected to said input means and including four logic states operating sequentially according to the valence of the successive packing indications received for detecting at least two prohibited sequences of packing indication signals and a device for inverting the valence 0–1 of a packing indication signal in response to an output of the second state of said logic means representing detection of one prohibited sequence and for inverting the valence 1–0 of a packing indication signal in response to an output of the fourth state of said logic means representing detection of the other prohibited sequence.

2. A device for correcting the packing indication according to claim 1 wherein said logic means comprises first and second flip-flops each having respective first and second input terminals, which flip-flops receive respectively on the first input thereof the inverse of said clock signal, and gate means connected to said flip-flops for applying to the second inputs thereof respectively two logical signals derived from the output states of said flip-flops, one of which is $(\overline{\text{IB}}) + \text{AB}$, the other is $\overline{\text{AB}} + (\overline{\text{IB}})\ (\text{A} + \overline{\text{B}})$, wherein IB designates the packing indication signal extracted from the incident MIC signal and signals A, $\overline{\text{A}}$ and B, $\overline{\text{B}}$ are the respective outputs of said first and second flip-flops.

3. A device for correcting the packing indication according to claim 2 wherein said input means includes an AND gate having inputs receiving said clock signals and said incident MIC signal, the output of said AND gate being connected to said gate means.

4. A device for correcting the packing indication according to claim 2 including a first AND gate connected to the A and B outputs of said flip-flops, a second AND gate connected to the $\overline{\text{B}}$ output of the flip-flop and the inverse of said packing indication signal IB, and a third AND gate connected to the outputs of said first and second AND gates and said clock signals.

5. A device for correcting the packing indication according to claim 4 wherein said gate means includes a fourth AND gate connected to the $\overline{\text{A}}$ and B outputs of said flip-flops, a fifth AND gate connected to the output of said fourth AND gate and to the inverse of said packing indication signal IB, a sixth AND gate connected to the A and $\overline{\text{B}}$ outputs of said flip-flops and a seventh AND gate connected to the outputs of said fifth and sixth AND gates and having an output connected to the second input of said second flip-flop.

6. A device for correcting the packing indication according to claim 5 wherein said gate means includes an eighth AND gate connected to the output of said first AND gate and to said packing indication signal IB and an output connected to the second input of said first flip-flop.

7. A device for correcting the packing indication according to claim 6 wherein said input means includes an AND gate having inputs receiving said clock signals and said incident MIC signal, the output of said AND gate being connected to said gate means.

* * * * *