

(12) PATENT
(19) AUSTRALIAN PATENT OFFICE

(11) Application No. AU 199921526 B2
(10) Patent No. 748265

(54) Title
Multi-carrier method and device for implementing said method

(51)⁷ International Patent Classification(s)
H04L 027/30 H04B 003/54

(21) Application No: **199921526**

(22) Application Date: **1998.11.10**

(87) WIPO No: **WO99/31852**

(30) Priority Data

(31) Number	(32) Date	(33) Country
97122042	1997.12.15	EP

(43) Publication Date : **1999.07.05**

(43) Publication Journal Date : **1999.09.02**

(44) Accepted Journal Date : **2002.05.30**

(71) Applicant(s)
ABB Patent GmbH

(72) Inventor(s)
Klaus Dosert; Torsten Waldeck

(74) Agent/Attorney
SPRUSON and FERGUSON, GPO Box 3898, SYDNEY NSW 2001

(56) Related Art
EP 691755
EP 85753
WO 93/01660

21526/99

**PCT**WELTORGANISATION FÜR GEISTIGES EIGENTUM
Internationales BüroINTERNATIONALE ANMELDUNG VERÖFFENTLICHT NACH DEM VERTRAG ÜBER DIE
INTERNATIONALE ZUSAMMENARBEIT AUF DEM GEBIET DES PATENTWESENS (PCT)

(51) Internationale Patentklassifikation ⁶ : H04L 27/30, H04B 3/54		A1	(11) Internationale Veröffentlichungsnummer: WO 99/31852
			(43) Internationales Veröffentlichungsdatum: 24. Juni 1999 (24.06.99)
(21) Internationales Aktenzeichen: PCT/EP98/07181		(81) Bestimmungsstaaten: AU, BR, CN, CZ, HU, IL, NO, NZ, PL, SK.	
(22) Internationales Anmeldedatum: 10. November 1998 (10.11.98)		Veröffentlicht <i>Mit internationalem Recherchenbericht. Vor Ablauf der für Änderungen der Ansprüche zugelassenen Frist; Veröffentlichung wird wiederholt falls Änderungen eintreffen.</i>	
(30) Prioritätsdaten: 97122042.1 15. Dezember 1997 (15.12.97) EP			
(71) Anmelder: ABB PATENT GMBH [DE/DE]; Kallstadter Strasse 1, D-68309 Mannheim (DE).			
(72) Erfinder: DOSERT, Klaus; Bergstrasse 13, D-67706 Krick- bach (DE). WALDECK, Torsten; Hans-Sachs-Strasse 31, D-76122 Karlsruhe (DE).			
(74) Anwälte: MILLER, Toivo usw.; ABB Patent GmbH, Postfach 10 03 51, D-68128 Mannheim (DE).			

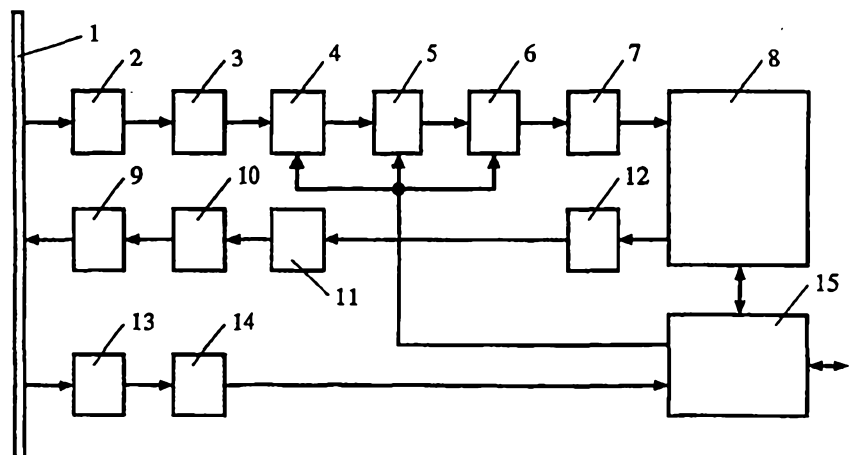


(54) Title: MULTI-CARRIER METHOD AND DEVICE FOR IMPLEMENTING SAID METHOD

(54) Bezeichnung: MEHRTRÄGERVERFAHREN UND EINRICHTUNG ZUR DURCHFÜHRUNG DES VERFAHRENS

(57) Abstract

Disclosed is a multi-carrier method for digital data transfer, especially for electrical power distribution networks. According to the invention, N amounts of symbols are assigned to combinations of $\text{Id}(N)$ data bits on the basis of the data flow to be transmitted in order to achieve quick and interference-free transfer. Each symbol consists of N signal forms with different frequencies. On the receiver side, a series of 2N digital signal-adapted parallel-working filters are used for simultaneous incoherent optimal reception of all N signal forms used to represent a symbol. A digital numerical value corresponding to the signal form energy is formed as correlation value for each of the N signal forms. An evaluation and scaling of N correlation values is carried out by comparison with a freely chosen threshold. The correlation values forming a symbol are added to obtain the corresponding symbolic value. The corresponding functional units can be advantageously integrated into an ASIC to implement the inventive method.



Multicarrier method and device for carrying
out the method

Abstract of the Invention

5

The invention relates to a multicarrier method for transmitting digital data, especially via electrical power distribution systems. To achieve a fast transmission which is resistant to interference, it is proposed to allocate combinations of $I_d(N)$ data bits from a data stream to be transmitted to a number N of symbols, each symbol of which is composed of N signal forms of different frequencies. At the receiving end, a number $2N$ of digital matched filters operating in parallel is used for the simultaneous incoherent optimum reception of all N signal forms in each case used for the representation of a symbol, a digital numerical value corresponding to the respective signal form energy being formed as correlation value for each of the N signal forms. Weighting and scaling of the N correlation values is performed by comparison with a freely selectable threshold. The N correlation values forming a symbol are added together to form the respective symbol value.

25

Functional units required for carrying out the method can be advantageously integrated in an ASIC.

Significant figure: Figure 1



MULTICARRIER METHOD AND DEVICE FOR CARRYING OUT THE
METHOD

5

Field of the Invention

The invention relates to a method and a device for the fast and reliable communication of digital information, especially via electrical power distribution systems, using a number of preferably orthogonal signal forms.

10

Background Art

15

20

In December 1991, European standard EN 50 065, which has the status of a German standard, came into force. This standard regulates the utilization of the frequency band from 3 kHz... 148.5 kHz for signal transmission purposes on electrical power distribution systems. In this standard, the available band is roughly divided into two ranges: the frequency range from 3 kHz... 95 kHz is reserved for the public utilities where transmitting amplitudes of up to a maximum of 134 dB μ V are permissible. The remaining frequency range from 95 kHz... 148.5 kHz is available to the private user without a licensing requirement but a transmitting amplitude of 116 dB μ V must not be exceeded. This rather low transmitting level (less than 1 V) accompanies a narrow available bandwidth. EN 50 065-1 makes high demands on methods and devices for the interference-proof transmission of information via electricity supply lines. Because of the amplitude limitation, transmission methods which can always use the full amplitude have the best chances of success



At present, systems with narrow-band or also with wide-band, band-spreading modulation, which are described, for example, in printed documents DE-A1-44 23 978, DE-A1-43 23 376, DE-C2-40 01 265, DE-C2-40 01 266, EP-B1-0 200 016 and EP-B1-0 199 148, are used for transmitting information via electricity supply systems. The method which is probably the simplest method technically and which can always utilize the complete permissible amplitude is FSK (Frequency Shift Keying). The fact that FSK is simple to implement is certainly a decisive reason for the fact that the majority of systems currently available on the market for transmitting information via electricity systems operates with FSK. The disadvantages of FSK have become apparent incrementally in practical use during numerous field trials and, in accordance with current estimations, it must be said that adequate reliability for services of all types which the public utilities intend to offer via their systems in future will not be achievable by means of FSK. The essential problem of FSK is that the transmission fails completely even when a single carrier frequency is disturbed, either due to selective attenuation which can occur at any time at any point in the time-variant transmission channel, or due to a narrow-band interference source in the form of a television set or of a switched-mode power supply. Band-spreading methods such as, for example, frequency hopping (FH), which allow many types of frequency variation, could provide a remedy here - see, for example, printed document DE-A1-44 23 978. Although the complexity is greater in comparison with an FSK system, it is bearable due to the advances in modern microelectronics. Nevertheless, the practical implementation of currently used FH methods has hitherto not gone beyond a trial stage; in particular, the market has hitherto not provided any operable systems. Although the FH technique is basically capable of overcoming all problems of FSK observed in practice, there are still decisive disadvantages in the method



and in the technical implementation which, in the final analysis, are probably the reason why systems with flexible use of a number of carrier frequencies sent successively in time have hitherto only been used hesitantly.

The significant disadvantage when changing from FSK to FH methods is that it is necessary to increase the chipping rate for the same net data rate (compare printed document DE-A1-44 23 978). With a chipping rate of 1200 s^{-1} , an FSK system thus achieves, for example, a data rate of 1200 bits/s whilst an FH system with 4 carriers per bit can now only offer 300 bits/s, for example. To achieve the same net data rate with FH, a chipping rate of 4800 s^{-1} would thus be required. This leads to an increased complexity in the signal generation and processing in every case, but especially in receiver synchronization which would now have to become more accurate by a factor of four.

SUMMARY OF THE INVENTION

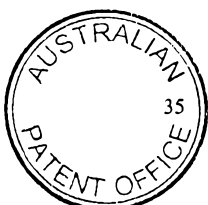
In accordance with one aspect of the invention there is disclosed a multicarrier method for transmitting digital data via electrical power distribution systems for synchronisation of signal synthesis for transmitting and receiving and for the synchronisation of the received-signal processing, the mains AC signal is used as a global reference signal, wherein, the beginning of a data transmission is always coupled to a zero transmission of the mains voltage and wherein, for the purpose of transmitting information by means of fast continuous-phase frequency changes and by means of symbol processing, said method comprising the steps of:

a) from a data stream to be transmitted, combinations of $\log_2(N)$ data bits are allocated to a number N of symbols, each symbol of which is composed of the same number N of signal forms of different frequencies, the number N being a power of two;

b) at the receiving end, a number $2N$ of digital matched filters operating in parallel is used for the simultaneous incoherent optimum reception of all N signal forms in each case used for the representation of a symbol, a digital numerical value corresponding to the respective signal form energy being formed as correlation value for each of the N signal forms;

c) weighting and scaling of the N correlation values is performed by comparison with a freely selectable threshold; and

d) the N correlation values forming a symbol are added together to form the respective symbol value, the symbol with the largest value is determined from this and the data bit combination assigned directly to its output as received data.



An embodiment of the invention is a multicarrier method by means of which the disadvantages listed can be considerably reduced and a fast and interference-resistant transmission can be achieved. In addition, a device for carrying out the method is to be specified.

5

BRIEF DESCRIPTION

The invention is described in greater detail by means of the explanation, given below, of advantages of the solution according to an embodiment of the invention, the fundamental concepts and of illustrative embodiments referring to drawing figures, in which:

10

Fig. 1 shows the overall configuration of a modem,

Fig. 2 shows a microcomputer system for implementing a number of function blocks from Fig. 1, and

Fig. 3 shows a representation for explaining a preferred synchronization method which can be used in the method, according to an embodiment of the invention.

15

DETAILED DESCRIPTION

The advantages of the symbol-processing multicarrier method are, among others, that a constant signal amplitude is always used and thus optimum energy utilization of the channel resources is given whilst adhering to the relevant standards. In the text which follows, a device called a modem (abbreviation for modulator/demodulator) will be used as an example for describing the invention. Such a modem is used for the bidirectional communication of digital information via electrical power distribution systems. The data transmission is in every case resistant to interference on the electricity supply lines and allows reliable fast communications in spite of the adverse transmission characteristics of these lines. Furthermore, simultaneous activity of a number of modems on the same power system is possible without mutual interference (multiple access to the same frequency band).

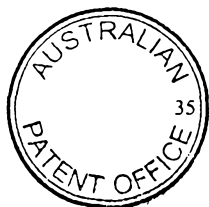
20

25

The manufacture and use of an application-specific integrated circuit with mixed analog and digital functions (mixed-signal ASIC) is advantageous for carrying out the method.

30

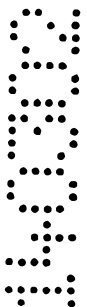
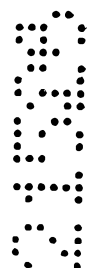
Thus, the signal generation at the transmitter end and the correlative processing at the receiver end up to the bit decision can take place with high accuracy and exact reproducibility on a digital basis. A virtually unlimited multiplicity of signal forms is available without hardware changes, including the capability of freely selecting various



data rates and frequency ranges within wide limits. These digital functions accommodated in the ASIC cannot be implemented in any other way in the current state of the art, not even by using the most elaborate digital programmable signal processors. In addition, the ASIC contains analog functions for amplification and filtering of the received signal and for analog/digital conversion and for digital/analog conversion at the transmitter end, i.e. functional units which are basically not contained in a standard signal processor. The amplification of the received signal is automatically adjusted in such a manner that the analog/digital converter is always operated within a favourable operating range.

The invention is based on the following considerations:

If N carrier frequencies are used in an FH system, these can be used for forming $N!$ (N factorial = $N(N-1)(N-2) \dots 1$) different combinations which will be called symbols in the text which follows. Thus, 6 symbols can be represented by $N = 3$ frequencies; $N = 5$ already provides 120. The 6 symbols with $N = 3$ would be capable of transmitting $[1d(6)] = 2$ bits whilst it would be possible to achieve already $[1d(120)] = 6$ bits with $N = 5$. In "normal" FH, however, these possibilities are not utilized but only two symbols (combinations) are evaluated which corresponds to information content of 1 bit - see, for example, printed document DE-A1-44 23 978. In normal FH technology, this provides redundancy which, for example, makes a transmission resistant to the failure of individual frequency ranges. The resultant disadvantage is obvious: the transmission speed drops in accordance with the number of carrier frequencies used. The basic concept which led to an embodiment of the present invention avoids this speed disadvantage and, at the same time, unrestrictedly guarantees that the resistance to interference which is inherent in the FH principle is maintained. A few examples will be compared in order to explain this essential aspect of the invention in greater detail:



If the three frequencies used are called f_1 , f_2 and f_3 for $N = 3$, the following 6 symbols $S_1 \dots S_6$ are obtained which can be utilized in various ways:

5

Symbol No.	Frequency sequence	FH technique	Symbol processing
S_1	$f_1 f_2 f_3$	0	00
S_2	$f_1 f_3 f_2$	-	01
S_3	$f_2 f_1 f_3$	-	10
S_4	$f_2 f_3 f_1$	-	11
S_5	$f_3 f_1 f_2$	1	-
S_6	$f_3 f_2 f_1$	-	-

Table 1: FH technique and symbol processing for $N = 3$ carrier frequencies

- 10 In the FH technique column, the high number of unused symbols is immediately obvious which, lastly, supplies the resistance. However, the pure number of unused symbols is not in any way the only measure of the achievable resistance to interference but the
- 15 determining factor is the number of chips with different frequency in the symbols used for representing information. It can be seen that the symbols S_1 and S_5 marked by 0 and, respectively, 1 differ in the FH technique column in all three chips
- 20 and can thus be very easily separated in the receiver. Considering the "symbol processing" column, it can be seen that only the symbols S_1 and S_4 marked with 00 and 11 and 01 and 10 corresponding to S_2 and S_3 differ in all three chips whilst the 00 and 01 or 00 and 10
- 25 combinations only differ in two chips. The resistance to interference suffers from this fact. If all 6 symbols were to be used for information transmission,



there would only be one different chip in each case as decision criterion; as a result, the transmission would no longer be more reliable than in the case of FSK because the failure of a single frequency would lead to failure. The above table shows that the use of three carrier frequencies obviously does not lead to an advantageous solution. If, in contrast, a sequence of four frequencies is considered which allows 24 symbols but of which only exactly the four differing in all four chips are used for information transmission - see Table 2,

Frequency sequence	Data symbols
$f_1 f_2 f_3 f_4$	00
$f_2 f_3 f_4 f_1$	01
$f_3 f_4 f_1 f_2$	10
$f_4 f_1 f_2 f_3$	11

Table 2: Optimal symbol processing with $N = 4$

15

the same resistance to interference would be obtained which would be obtained with the standard FH technique but because each one of the symbols shown now represents two data bits, twice the transmission rate is obtained. The principle shown can be used not only for $N = 4$ but whenever exactly N of the $N!$ possible symbols are used for representing information. In this arrangement, it is advantageous if N is a power of 2 because $\text{ld}(N)$ then results in an integral number of bits. If $\text{ld}(N)$ is not integral, only the next smaller integral number can always be used, i.e. the useable net data rate is reduced. After $N = 4$, $N = 8$ would then be advantageous again, in which arrangement 4 bits could be transmitted with each of the symbols used, utilizing 8 of the $8!$ possible symbols. For practical use in power distribution systems, a system based on 4

30



carrier frequencies will reliably offer adequate resistance to interference in order to guarantee the new services planned by the public utilities with high reliability. As can be seen from Table 2, up to three of the four carrier sequences could fail in boundary cases without this resulting in a bit error. In comparison with FSK where even the failure of a single frequency leads to failure, this is a significant advance. Using normal FH, $N = 7$ carrier frequencies would be necessary and the net data rate would drop to $1/7$ of the chipping rate. The method according to the invention provides the same resistance to interference with a ratio of $1/2$ of data rate to chipping rate.

Practice has shown that with a clever selection of carrier frequencies, the probability that two of these will fail at the same time due to attenuation or interference is extremely small. The case that this will occur for three carriers can be virtually eliminated. However, the failure of single carriers is observed relatively frequently.

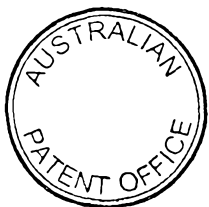
The choice of $N = 4$ carrier frequencies is certainly advantageous for the practical implementation of the method according to an embodiment of the invention. The illustrative embodiment described in the text which follows is therefore based on $N = 4$.

A largely digital concept with a high degree of integration is of decisive significance for an inexpensive and reliably reproducible implementation. Furthermore, it is advantageous if adaptation to various types of task without changing the hardware is possible and if a large proportion of the analog circuit parts required for the complete construction of a modem can also be monolithically integrated. The embodiment of the invention presented in the text which follows demonstrates a universal advantageous solution.



The starting point of the considerations is a transmission of binary information which is mapped onto frequency sequences (symbols) according to Table 2. During the period T_s of a symbol, the transmitting
5 frequency is changed abruptly four times in this example. The larger the N selected, the more resistant to interference can be the transmission of information, with a system complexity, however, which also rises. For the reasons already listed above, $N = 4$ different
10 and suitably selected frequencies are adequate for most applications of the present invention. A suitable choice means that the frequencies used are distributed in the available transmission band in such a manner that strong selective attenuation or a strong narrow-
15 band interference source can never impair two or more frequencies at the same time. To make this choice correctly, adequate background experience is necessary which must be obtained by extensive network investigations (network surveys), field trials and
20 theoretical network modelling based on the measurement results.

The frequency band from 3 kHz to 95 kHz, i.e. a bandwidth of $B = 92$ kHz, is available in the
25 distribution system of a public utility for transmitting information in accordance with the European standard EN 50 065-1. If, for example, it is necessary to transmit binary information with a net data rate (bit rate) $r_D = 1200$ bits/s by means of the
30 symbol-processing multicarrier method, where $N = 4$ carrier frequency hops during a symbol period T_s , the frequency hopping rate $h = 2400s^{-1}$. The inverse value $T = 1/h$ of the frequency hopping rate specifies the duration of the time interval during which one of the N
35 frequencies is transmitted in each case. Communication theory says that, within a frequency bandwidth of $B = 92$ kHz and with a frequency hopping rate $h = 2400s^{-1}$, a maximum number of $\lceil B/h \rceil = \lceil 92000/2400 \rceil = 38$ signal forms having in each case a frequency offset by 2400 Hz are



simultaneously transmitted and can be detected without errors and without mutual interference by receivers which perform correlative signal processing - see also printed document DE-A1-44 23 978.

5

Thus, it would be possible to operate up to $\lceil 38/4 \rceil = 9$ modems with symbol-processing multicarrier methods of the type described simultaneously and without mutual interference on an electrical power distribution system, for example between a transformer station and the connected households. The decisive prerequisite for this is not only a highly accurate signal generation but also the accurate insertion of all transmit signals into a global timing pattern and perfect correlative signal processing in the receiver section of each modem.

Accurate generation of a transmit signal is not only required with dense channel allocation but also of advantage in the case of a single point-to-point connection. It is also important that all signals are derived from a fixed and highly constant basic frequency and that, when the frequency is changed, there is no phase discontinuity but a continuous phase transition takes place. The frequency, in contrast, must change abruptly, i.e. without transient process. The continuous phase transition is required in every case in order to be able to meet the strict limit values for out-of-band interference in accordance with the standard EN 50 065-1 with supportable filter complexity.

As in virtually all high-quality transmission systems, synchronization is basically required with the signal generation and signal processing in a symbol-processing multicarrier system. Synchronization of the received signal with a reference signal existing locally in the receiver is necessary especially in the case of correlative reception. In the case of the symbol-



processing multicarrier method, this reference signal comes from a frequency synthesizer. During the transmission, a synchronized frequency synthesizer is also needed, the information-carrying output signals of which are fed into the power system. In systems operating from electricity supply lines, the problem of synchronization can be solved simply and inexpensively with the aid of the alternating system voltage - see, for example, EP-B1-200 016, EP-B1-0 199 148 and EP-B1-0507 087. In a part of this description which is located below, a correlative synchronization which is independent of the power voltage and which is advantageously obtained directly from the symbol-processing multicarrier method according to the invention will be presented.

The hardware of known transmitting and receiving devices for transmitting information on electrical distribution systems will not allow the use of a symbol-processing multicarrier method. After the method has been described, a device is therefore specified within the context of the present invention, which device includes all essential parts for the synthesis of the transmit signal and for the correlative processing of the received signal for a symbol-processing multicarrier method. The new device contains analog and digital sections and, apart from a few components, can be monolithically integrated, standard CMOS technology being adequate for this. A maximum degree of flexibility is achieved with respect to the choice of frequency (position of the frequencies used within the allowable transmission band).

The transmitting device in a modem with symbol-processing multicarrier method for transmitting digital information via electricity supply lines has the task of accurately generating a multiplicity of signals having relatively closely adjacent frequencies with accurate timing. In this connection, a rapid phase-



continuous frequency change must be possible in dependence on the information to be transmitted without transience occurring during the process. Devices constructed with analog technology cannot handle the above requirements and, in addition, are inflexible with respect to frequency changes.

5 The receiving device of a modem must be capable of perfectly isolating signals having adjacent frequencies of unknown phase relationship. For this purpose, matched filtering by correlative means is necessary in a number of branches of the receiver which operate in parallel. The principle of correlation is adequately well known from standard textbooks. An active correlator which generally consists of a multiplier and an
10 integrating unit becomes a matched filter, e.g. for signal forms of chip period T_C , if synchronization is used to ensure that the integrating unit is set to zero at each chip interval end after the value integrated up during the chip period has been sampled for further processing and, if necessary, stored. In analog technology, the complexity of such a circuit would be intolerably high because a separate phase-insensitive quadrature
15 receiver would be required for each carrier frequency - compare also printed document DE-A1-44 23 978. Thus, producing a receiver based on a symbol-processing multicarrier method with $N = 4$ frequencies requires 8 separate correlators. Such structures have hitherto not been achieved which is why no hardware components for implementing multicarrier methods which are resistant to interference to a higher degree are available
20 on the market although there is no dearth of applications for these.

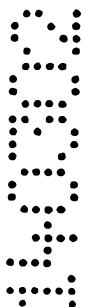
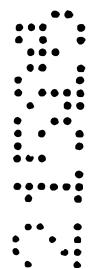
 An embodiment of the invention provides for the first time a hardware basis for the simple and reproducible manufacture of modems for symbol-processing multicarrier methods and industrial series productions will make it possible to achieve a continuous drop in costs as the numbers



produced increase. The embodiment of the invention is thus suitable for assisting in achieving a breakthrough in the widespread use of interference-resistant data transmission on electricity systems, especially in Europe, where the strict restrictions of EN 50 065-1 are in force. Hitherto, no modems which operate reliably, either with conventional modulation methods or with multicarrier technology for data transmission on electrical distribution systems have been available on the European market.

An embodiment of the invention will now be described with reference to Drawing Figures 1 and 2. For reasons of clarity and illustration, the transmission of binary information (i.e. a stream of random successive "H" and "L" bits) having a fixed data rate $r_D = 1/T_B = 1200$ bit/s using 4 orthogonal signal forms of different frequency with the chip period $T_C = T_B/2$ will be considered. This is therefore a symbol-processing multicarrier system where $N = 4$. The change to other technically meaningful values of N can be carried out by the expert by referring to the text.

Incoherent reception is the rule in electrical distribution systems, which is why eight correlators operating in parallel are necessary in the receiver for $N = 4$. If $T_C = T_B/2$, a chipping rate $h = 2400\text{s}^{-1}$ is obtained. In the 9.6 kHz ... 148.8 kHz frequency band, for example, 60 frequencies can be found which, in each case spaced apart by 2400 Hz, form a set of orthogonal frequencies where an integral number of periods in each case fits into each chip period T_C . With a sampling rate of 600 kHz, a maximum of 125 samples are needed for error-free representation. Because of the incoherent reception, 8 reference values are needed for each sample of the received signal, so that a clock frequency of $f_m = 4.8$ MHz is required for outputting the reference signal samples.



In the case of the symbol-processing multicarrier method, an optimum with respect to resistance interference and, at the same time, reliability of manipulation too, can be achieved when the frequencies, over which the user information is distributed, are as far apart as possible. It is then improbable for a number of frequencies to be subject to the same attenuation and/or interference at the same time. For a system with $N = 4$, for example, the following choice of frequencies is appropriate:

f_1	f_2	f_3	f_4
52,800 Hz	62,400 Hz	72,000 Hz	86,400 Hz

Table 3: Example of a frequency determination for $N = 4$

15

Figure 1 shows the overall configuration of a modem, the operation of which will be explained in detail in the text which follows, beginning with the receiving branch. From the power system 1, the received signal passes via a coupler 2 to a band-pass filter 3 which passes the range of the four desired frequencies $f_1 \dots f_4$ but blocks the remaining frequency range as well as possible. Isolating the mains voltage and other low frequencies is already largely handled by the coupler, which acts as high-pass filter. This is followed by a device for automatic gain control consisting of three operational amplifier stages 4, 5 and 6, the gain of which can be set digitally via an integrated microcontroller system 15. The amplified received signal passes to an analog/digital converter 7 which supplies the digitized samples to the symbol-processing system 8, the results of which are accepted and processed further by the integrated microcontroller system 15. Finally, the microcontroller system 15 supplies, on the one hand, the data transmitted and



received here via a serial interface and, on the other hand, calculates the gain to be set for the three operational amplifier stages 4, 5 and 6. A special feature of this is that two of the three amplifiers are
5 "rapidly adjustable", whereas the third one is adjusted at the most by a factor of 2 from symbol to symbol. The rapidly adjustable amplifier has the task of rapidly responding to abrupt, considerable channel changes whereas the slowly adjustable amplifier is only
10 intended to compensate for slight fluctuations. The control algorithm, which is advantageously implemented in the form of software in the microcontroller system 15, always attempts to set the fast amplifiers to the highest possible values of gain so that a large
15 response margin is available with rapid channel changes. A level estimator which supplies the basis for calculating the amplifier adjustments to the microcontroller system 15 is constructed as averaging circuit in digital hardware and is a component of the
20 symbol-processing system 8. The level estimator receives Z digitized values $x(k)$ of the received signal and uses these to determine the estimated value

25
$$X_{sch} = \frac{\pi}{2} \cdot \sum_{k=1}^Z |x(k)|,$$

in each case after a symbol period has elapsed. The ratio between the estimated value X_{sch} and a nominal
30 value X_{soll} supplies the basis for generating the switching commands for the gain adjustment by the microcontroller system 15. The maximum total gain is variable from 1... 4096, each of the three amplifier stages being adjustable to the gain values 1, 2, 4, 8
35 or 16.

Another functional unit within the symbol processing system 8 which will be described in detail with reference to Figure 2 in the next section performs the



processing of the transmit signal, a digital data stream to be transmitted, which reaches the microcontroller system from a data source, being processed in such a manner that the samples of the signal forms to be transmitted are supplied directly to a digital/analog converter 12. The digital/analog-converted transmit signal is filtered in a low-pass recovery filter 11 and, after amplification in a transmission output stage 10, supplied to the power system 1 via the transmit coupler 9. Function blocks 13 and 14 are used for synchronizing the data transmission with the mains alternating voltage. In this process, a highly accurate detection of mains zero transition is carried out in function block 13 and, at the same time, the mains zero transition information is DC-isolated from the power system with the aid of an optocoupler. In block 14, a digital phase-locked loop (PLL) is implemented, with the aid of which high-frequency jitter of any type is removed from the mains zero transmission information so that, finally, a steep-edged and stable synchronization signal is supplied to an interrupt input of the microcontroller system 15. The synchronization with the mains AC is not a general optimum solution, which is why an advantageous feature in an embodiment of the invention will be described below which implements a correlative type of synchronization and thus achieves perfect synchronization even without the mains alternating voltage.

The block diagram shown in Fig. 2 shows an integrated microcomputer system which includes function blocks 7, 8, 12 and 15 from Fig. 1. In the real construction of a complete symbol-processing multicarrier system, it is advantageous to integrate all function units from Figure 1 monolithically in the form of a mixed-signal ASIC with the exception of couplers 2, 9 and of the transmit amplifier 10. At this point, only the section shown in Figure 2 will be considered because it is better suited to explain the essential functions



according to an embodiment of the invention than an extensive and thus relatively confusing overall circuit.

In Figure 2, a filtered and amplified received signal isolated from the power system first reaches an analog/digital converter 21. Since incoherent reception is a rule in electrical distribution systems as explained above, $N = 4$ requires eight correlators operating in parallel in the receiver. Because of the incoherent reception, eight reference values are needed per sample of the received signal. With a sampling rate of 600 kHz, a maximum of 125 samples per frequency are needed so that, with a clock frequency of $f_m = 4.8$ MHz, a memory for 2000 samples is required for outputting the reference signal samples.

In the text which follows, the digitized received signal is designated by $E(iT_a)$, where iT_a is the discrete time, with $i = 0, 1, 2, \dots$. Each of the digitized samples $E(iT_a)$ of the received signal is multiplied by eight reference signal samples $R(iT_a + vT_a/8)$, with $v = 0 \dots 7$, from a signal form or sample memory 214 in a digital multiplier 22. The eight subproducts are then integrated via the signal form period T_c (chip period), i.e. added together digitally in separate accumulators. According to Figure 2, these accumulators are advantageously implemented as follows: an adder 23 can be connected together with eight registers 24...29, 210, 211 following it, and a switch 212, to form a ring structure. At the beginning of the reception of a signal form, the switch 212 is in position II for the period of eight clock cycles of frequency f_m , i.e. the ring structure is opened so that zeros pass to one input of the adder 23 whilst the other input successively receives eight multiplication results $E(iT_a) R(iT_a + vT_a/8)$, with $v = 0 \dots 7$, from the multiplier 22. The following correlation applies:

$$R(iT_a + 0 \cdot T_a/8) / \text{Sine sample } f_1 \text{ chip (in-phase component for } f_1 \text{ chip)}$$



$R(iT_a+1 \cdot T_a/8)$ / Sine sample f_2 chip (in-phase component for f_2 chip)

$R(iT_a+2 \cdot T_a/8)$ / Sine sample f_3 chip (in-phase component for f_3 chip)

$R(iT_a+3 \cdot T_a/8)$ / Sine sample f_4 chip (in-phase component for f_4 chip)

5 $R(iT_a+4 \cdot T_a/8)$ / Cosine sample f_1 chip (quadrature component for f_1 chip)

$R(iT_a+5 \cdot T_a/8)$ / Cosine sample f_2 chip (quadrature component for f_2 chip)

10 $R(iT_a+6 \cdot T_a/8)$ / Cosine sample f_3 chip (quadrature component for f_3 chip)

$R(iT_a+7 \cdot T_a/8)$ / Cosine sample f_4 chip (quadrature component for f_4 chip)

After 8 clock cycles of frequency f_m have passed,
15 registers 24...29, 210, 211 contain the following results:

Register →

24	25	26	27	28	29	210	211
Q_4	Q_3	Q_2	Q_1	I_4	I_3	I_2	I_1

20 where I_j is the in-phase component and Q_j is the quadrature component of the chip having frequency f_j , where $j=1...4$.

Because $i=0$, the following applies at the beginning of
25 a signal form:



$$Q_4(0) = E(0) \cdot R(0+7 \cdot T_s/8) + 0,$$

$$Q_3(0) = E(0) \cdot R(0+6 \cdot T_s/8) + 0,$$

$$Q_2(0) = E(0) \cdot R(0+5 \cdot T_s/8) + 0,$$

$$Q_1(0) = E(0) \cdot R(0+4 \cdot T_s/8) + 0,$$

$$I_4(0) = E(0) \cdot R(0+3 \cdot T_s/8) + 0,$$

$$I_3(0) = E(0) \cdot R(0+2 \cdot T_s/8) + 0,$$

$$I_2(0) = E(0) \cdot R(0+1 \cdot T_s/8) + 0,$$

$$I_1(0) = E(0) \cdot R(0+0 \cdot T_s/8) + 0,$$

The addition of 0 is obtained because the ring structure is opened by the switch 212. After the above-mentioned eight clock cycles of frequency f_m have passed, switch 212 is switched to position I, resulting in the ring structure described, in which the contents of register 211 now reach the adder 23. Now arithmetic operations are carried out which accumulate the contents of registers 24...29, 210, 211 as follows:

$$\text{Register 24 } Q_4(i) = E(iT_s) \cdot R\left(iT_s + \frac{7T_s}{8}\right) + \sum_{\xi=0}^{i-1} E(\xi T_s) \cdot R\left(\xi T_s + 7 \cdot \frac{T_s}{8}\right)$$

$$\text{Register 25: } Q_3(i) = E(iT_s) \cdot R\left(iT_s + \frac{6T_s}{8}\right) + \sum_{\xi=0}^{i-1} E(\xi T_s) \cdot R\left(\xi T_s + 6 \cdot \frac{T_s}{8}\right)$$

$$\text{Register 26: } Q_2(i) = E(iT_s) \cdot R\left(iT_s + \frac{5T_s}{8}\right) + \sum_{\xi=0}^{i-1} E(\xi T_s) \cdot R\left(\xi T_s + 5 \cdot \frac{T_s}{8}\right)$$

$$\text{Register 27: } Q_1(i) = E(iT_s) \cdot R\left(iT_s + \frac{4T_s}{8}\right) + \sum_{\xi=0}^{i-1} E(\xi T_s) \cdot R\left(\xi T_s + 4 \cdot \frac{T_s}{8}\right)$$

$$\text{Register 28: } I_4(i) = E(iT_s) \cdot R\left(iT_s + \frac{3T_s}{8}\right) + \sum_{\xi=0}^{i-1} E(\xi T_s) \cdot R\left(\xi T_s + 3 \cdot \frac{T_s}{8}\right)$$

$$\text{Register 29: } I_3(i) = E(iT_s) \cdot R\left(iT_s + \frac{2T_s}{8}\right) + \sum_{\xi=0}^{i-1} E(\xi T_s) \cdot R\left(\xi T_s + 2 \cdot \frac{T_s}{8}\right)$$

$$\text{Register 210: } I_2(i) = E(iT_s) \cdot R\left(iT_s + \frac{1T_s}{8}\right) + \sum_{\xi=0}^{i-1} E(\xi T_s) \cdot R\left(\xi T_s + 1 \cdot \frac{T_s}{8}\right)$$

$$\text{Register 211: } I_1(i) = E(iT_s) \cdot R\left(iT_s + \frac{0 \cdot T_s}{8}\right) + \sum_{\xi=0}^{i-1} E(\xi T_s) \cdot R\left(\xi T_s + 0 \cdot \frac{T_s}{8}\right)$$



Assuming that a signal form has the chip period $T_c = NAT_a$, the desired eight signal components are obtained in registers 24...29, 210, 211 of Figure 2 after $i-N$ clock cycles of frequency f_a , i.e. after $8AN$ clock cycles of frequency f_m :

24	25	26	27	28	29	210	211
Q_4	Q_3	Q_2	Q_1	I_4	I_3	I_2	I_1

For the symbol decision now following, the geometric addition of signal components I_j , Q_j according to the principle of the quadrature receiver is first required:

$$B_1 = \sqrt{I_1^2 + Q_1^2}; B_2 = \sqrt{I_2^2 + Q_2^2}; B_3 = \sqrt{I_3^2 + Q_3^2}; B_4 = \sqrt{I_4^2 + Q_4^2}.$$

resulting in the amounts $B_1...B_4$.

15

Although the arithmetic operations of squaring and calculating the square route can be achieved without problems by means of digital hardware, the complexity is considerable, especially with a large dynamic range.

20 In the present invention, therefore, the following approximation is advantageously used:

$$B_j \approx \max\{I_j, Q_j\} + \left(\frac{1}{4} + \frac{1}{8}\right) \cdot \min\{I_j, Q_j\}.$$

25 which supplies equivalent results with much less complexity. In this arrangement, the larger correlation value I_j or Q_j of a signal component by amount must be



added in each case to the smaller one multiplied by $(1/4+1/8)$. The simple arithmetic and logic operations necessary for this are implemented in a function block 215, a second switch 216 and a set of absolute-value registers 217. After a chip period has elapsed, switch 212 is changed to position II for exactly eight clock cycles so that the eight correlation values pass into block 215. The four first ones of these ($I_1...I_4$) are directly shifted on into the set of absolute-value registers 217. Switch 212 is now back in position I so that the correlation values of the next signal form can accumulate in registers 24...29, 210, 211. Now the second switch 216 is closed for the further calculation of absolute values B_j in accordance with the above arithmetic rule so that the four values $I_1...I_4$ are successively passed back into function block 215 where each of them is compared with the associated quadrature value $Q_1...Q_4$ still stored in block 215. The larger value in each case is determined and shifted into the set of absolute-value registers 217.

The smaller correlation values in each case are now divided by four or, respectively, by eight by being shifted to the right by two or, respectively, three bit positions in function block 215 and the results are added. For the final addition according to the above arithmetic rule, the maximum values stored in the set of absolute-value registers 217 are fed back via the second switch 216 to function block 215 for the purpose of being added to the minimum values scaled in each case by $(1/4+1/8)$, and the results are shifted into the set of absolute-value registers 217 where the four desired absolute values B_j are now available, by means of which the symbol decision can be carried out next.

35

According to Table 2, a symbol decision can take place in each case after four chip intervals have elapsed. For this purpose, it is necessary to add the absolute values $B_1...B_4$ from the register set 217 in four



successive chip intervals in accordance with the following arrangement and to store the results in the four symbol registers 219...222.

5 Chip interval No.

1	2	3	4		Symbol register	Data symbol
$B_1 +$	$B_2 +$	$B_3 +$	B_4	$\Sigma \Rightarrow$	222	00
$B_2 +$	$B_3 +$	$B_4 +$	B_1	$\Sigma \Rightarrow$	221	01
$B_3 +$	$B_4 +$	$B_1 +$	B_2	$\Sigma \Rightarrow$	220	10
$B_4 +$	$B_1 +$	$B_2 +$	B_3	$\Sigma \Rightarrow$	219	11

Table 4: Calculation of symbol values

The operations needed are carried out with the aid of a multiplexer 225 and an adder 218 interacting with the set of absolute-value registers 217 and the symbol registers 219...222. The symbol registers 219...222 are assumed to be filled with zeros at the end of the first chip interval. The multiplexer 225 now supplies the four absolute values $B_1...B_4$ according to column 1 of table 4 one by one to adder 218, the second input of which, in the meantime, receives zeros. After the second chip interval, the absolute values come from the multiplexer cyclically exchanged according to column 2 of table 4, i.e. B_2, B_3, B_4, B_1 so that, because of the feedback from the symbol registers to the adder 218, the symbol registers now contain the sub-totals according to the first two columns of Table 4 after four addition steps. Continuation of the above considerations supplies the symbol results in registers 219...222 after the two remaining chip intervals have elapsed. It is now only necessary to determine the maximum of the four results in a decision device 226 in order to determine the associated data bit combination which can then be supplied as received data ED to the data sink. From the results of the symbol calculation, however, even more information can be obtained which



can be utilized advantageously for a further development of the invention, namely for the autonomous, mains-AC-independent correlative synchronization which will be described in detail in the next section. Before that, the remaining blocks from Figure 2 must still be explained which contain the essential transmit functions.

The heart of the transmit hardware is the signal form memory 214 which contains the samples of the transmit signal forms which can largely also be used advantageously as reference signal samples in receiving operation. The data to be transmitted, the transmit data SD, first pass to a function block 213 where they are combined to form frequency sequences in accordance with the symbol formation according to Table 2. In the order predetermined according to Table 2, function block 213 successively addresses and reads out the address areas of the signal form memory 214 in which the samples belonging to the desired frequencies are stored. With a sampling clock frequency of 600 kHz, the address areas would in each case have a maximum length of 125. Overall, a maximum of 500 samples would then have to be stored. To keep down the complexity for the low-pass recovery filter 224 following a digital/analog converter 223, it is advantageous to increase the clock frequency to 1.2 MHz or 2.4 MHz during the synthesis of the transmit signal SS. This proportionally increases the required memory. Another important detail in designing the transmit side is that there will be no abrupt phase changes at all both during the frequency change within a symbol and at the symbol boundaries, i.e. that phase continuity is ensured. Otherwise, it would not be possible to adhere to the strict regulations with respect to out-of-band interference power according to EN 50 065-1.

The description of an exemplary embodiment is now followed in the concluding part of the representation of



the invention by a special type of autonomous synchronization which becomes possible as a by-product of the special design of the receiver architecture.

In many cases, it is advantageous if the mains AC can be dispensed with as synchronization reference. In some countries of Eastern Europe, where the stability of the mains frequency is much worse than in the interconnected European power system, it is
5 no longer possible to achieve a sufficiently accurate synchronization for chipping rates of approx. 1000 s^{-1} . Or, if an operative communication is required even in the event of a power failure, autonomous receiver synchronization must be possible from the received signal. In general, it is advantageous always to carry out coarse synchronization with the
10 aid of the mains AC and then to compensate for synchronization errors continuously on the basis of the correlative method presented in the text which follows so that, in the final effect, a synchronization is achieved which is so accurate that it would not be possible on the basis of the mains AC alone even in the interconnected European power system, even if it is possible to remove the jitter to a large extent from the synchronization reference,
15 for example with the aid of a digital phase-locked loop.

In known correlative receivers, autonomous synchronization from the received signal requires, as a rule, more effort than the performance of the correlation itself. In the case of an embodiment of the invention, in contrast, this synchronization can be managed without significant additional effort, using the receiver hardware which is necessary in
20 any case. Because all transmitters and receivers use oscillator crystals for generating the clock as a matter of principle, a sufficiently stable time base is available from the start. It is then ultimately the task of the synchronization device to get the timing pattern existing in the received signal



to match that generated locally in the receiver exactly. This complex process will now be explained with reference to Figure 3, which is based on Table 2, and with reference to Table 5.

5

Figure 3 shows the four symbols carrying information, and the associated data bit combinations. Starting with bit combination '00', it can be seen that the symbol belonging to '10' is produced by cyclic right shifting and that belonging to '01' by left shifting. With respect to synchronization, right shifting means that the timing pattern of the local reference in the receiver leads with respect to the received signal, i.e. correction would require a delay. This analogously applies to the left shifting process.

If '01' had been selected as the starting point, cyclic right shifting would produce '00' and left shifting would produce '11'. Applying the above consideration to each symbol, it becomes clear that it is possible, by considering the largest and second-largest correlation value alone, to determine whether the receiver timing pattern is leading or lagging. The difference of the absolute values also supplies an indication of the magnitude of the synchronization error, i.e., the greater it is, the more accurate is the synchronization and the less corrective action should be taken. According to the above considerations, the synchronization can be corrected in a simple manner (the starting point is assumed to be the reception of the symbol belonging to '00'): If, for example, a lead with a relatively large difference between the largest ('00') and second-largest ('10') correlation value has been detected, the local reference in the receiver is slightly delayed which can be done digitally quite simply by inserting additional clock pulses. After the subsequent correlation process, the largest and second-largest correlation value are examined again. It is now assumed that the symbol belonging to bit combination



'11' has been transmitted; for this reason, the largest correlation value is received for this symbol. After the preceding correction of the lead, it is now expected that the second-largest correlation value for
5 '01' will occur and that the difference to the largest has increased, i.e. synchronization has improved. The correction steps described are continued, if necessary with continuous reduction in size, until a lag of the receiver reference is detected instead of a lead. A
10 stable optimum state is reached when, with a large difference between the largest and second-largest correlation value, after each correlation process, i.e. in each case after one symbol period has elapsed, alternating leading and lagging of the receiver
15 reference is detected. In practice, this ideal condition will probably occur quite infrequently since the difference to be examined is subject to fluctuations, even with ideal synchronization, due to interference signals which are always present, which
20 fluctuations cannot be distinguished from synchronization errors. This means that, as a rule, greater corrections (more shifting steps) than would be expected theoretically will occur for reaching the stable state described.

25

Table 5 below illustrates the relationships described with respect to the timing patterns, transmission of the symbol belonging to bit combination '00' being assumed - see top row (transmitted).



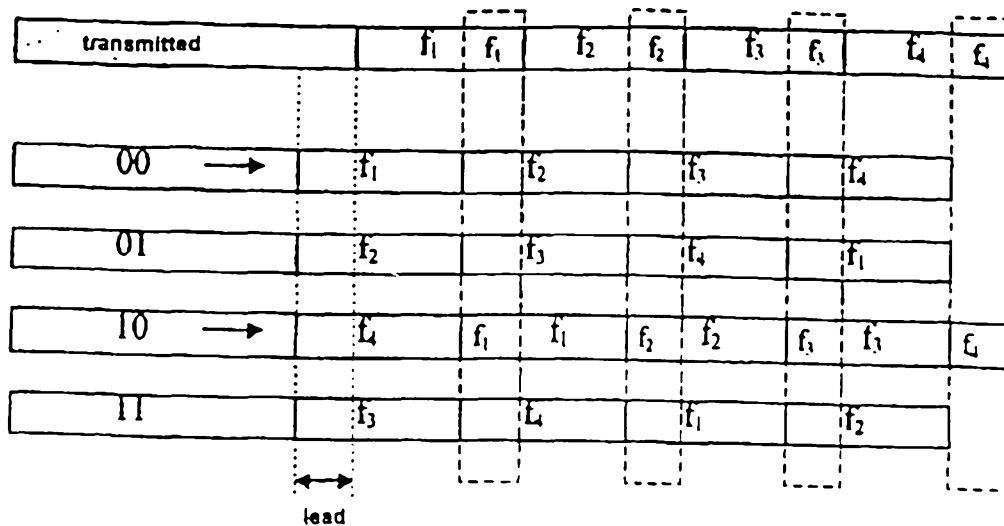


Table 5: Explanation of the principle of correlative synchronization

At the receiver end, a considerable lead of the reference timing pattern can be seen. On the one hand, this leads to too small a correlation value being produced for the transmitted symbol and, on the other hand, contributions being produced in the case of symbols which have not been transmitted. However, in the synchronization method according to an embodiment of the invention this is the case with only a single symbol, namely the one which is allocated to bit combination '10'. In the case of the other two symbols, no correlation contributions are produced. The vertical dashed rectangles in Table 5 comprise the contributions correlated together at the wrong point due to the timing pattern offset for each of the four chips of a symbol. It can be seen that contributions can only occur in the symbol belonging to '10' - there is no match of frequencies in the case of the other ones '01' and '11'.



The claims defining the invention are as follows:

1. A multicarrier method for transmitting digital data via electrical power distribution systems for synchronisation of signal synthesis for transmitting and receiving
5 and for the synchronisation of the received-signal processing, the mains AC signal is used as a global reference signal, wherein, the beginning of a data transmission is always coupled to a zero transmission of the mains voltage and wherein, for the purpose of transmitting information by means of fast continuous-phase frequency changes and by means of symbol processing, said method comprising the steps of:

10 a) from a data stream to be transmitted, combinations of $ld(N)$ data bits are allocated to a number N of symbols, each symbol of which is composed of the same number N of signal forms of different frequencies, the number N being a power of two;

b) at the receiving end, a number $2N$ of digital matched filters operating in parallel is used for the simultaneous incoherent optimum reception of all N signal forms
15 in each case used for the representation of a symbol, a digital numerical value corresponding to the respective signal form energy being formed as correlation value for each of the N signal forms;

c) weighting and scaling of the N correlation values is performed by comparison with a freely selectable threshold; and

20 d) the N correlation values forming a symbol are added together to form the respective symbol value, the symbol with the largest value is determined from this and the data bit combination assigned directly to its output as received data.

2. The method according to claim 1, wherein the threshold used for
25 weighting and scaling is selected as a percentage of the maximum possible autocorrelation value of a signal form and is adaptively set in dependence on received interference.

3. The method according to claim 1, wherein the threshold used for
30 weighting and scaling is selected as a percentage of the maximum possible autocorrelation value of a signal form and is adaptively set in dependence on useful signal energy.

4. The method according to any one of claims 1 to 3, wherein, for the
35 purpose of correlative synchronization, in each case the largest and the second-largest



symbol value are determined from which both the direction of a timing error of the synchronization and the magnitude of this error are determined.

5 5. The method according to claim 4, wherein, from the direction and magnitude of a phase error, a control information item for a synchronization device is generated which adaptively counteracts the error determined.

6. The device for carrying out the method according to any one of the preceding claims, wherein

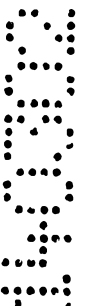
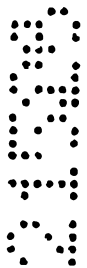
10 a) for transmitting and for the incoherent parallel optimum reception of N signal forms of different frequency, a mixed analog/digital integrated circuit (mixed-signal ASIC) exists by means of which the amplified and filtered received signal coupled out of a power system, after analog/digital conversion, passes through a digital multiplier, the second input of which receives a digital reference signal from a sample memory, wherein 2N reference values corresponding to the in-phase and quadrature samples of the N signal forms used are allocated to each received-signal sample,

20 b) a ring structure of an adder, a set of 2N registers and a switch exists by means of which the products produced in the multiplier are accumulated so that, after a signal form period has elapsed, the in-phase components and the quadrature components of N signal forms used for a symbol are accumulated in the 2N registers,

25 c) the switch is also used for subsequently supplying the 2N results from the registers, with opening the ring structure of adder and set of registers, to a geometric addition circuit which forms a digital numerical value corresponding to the absolute value of the respective signal form energy by means of an approximation,

30 d) a further ring structure of an adder, a set of N registers and a multiplexer exists by means of which symbol values are accumulated so that, after a symbol period has elapsed, the respective symbol values which are subsequently supplied to an analysis and decision device, which finally supplies the received data, are present in the N registers, and

35 e) an integrated clock generation and control unit exists which, apart from the synthesis of the reference signals in the case of reception, addresses the sample memory during transmission in such a manner that its output signals form continuous-phase transmit signal forms which, after analog/digital conversion, low-pass filtering and amplification, are coupled into the power system.



7. The device according to claim 6, wherein

a) for tasks of system control, signal analysis and data transfer, a digital circuit exists which is a monolithically integrated component of the mixed-signal ASIC which contains the essential components of a modem,

5 b) by means of said digital circuit during the transmitting process, the data bit combination to be transmitted can be supplied to the transmitting device and the former first sets the desired data rate and the number N of signal forms of different frequency per symbol by programming the control unit in the mixed-signal ASIC.

10 8. The device according to claim 7, wherein said digital circuit is a microprocessor.

9. The device according to claim 8, wherein said digital circuit is a microcontroller.

15 10. The device according to any one of claims 6 to 9, wherein means exist which have the effect that

a) for synchronization of the signal synthesis for transmitting and receiving and for the synchronization of the received-signal processing, the mains AC is used as a global reference signal, the beginning of a data transmission always being coupled to a zero transmission of the mains voltage and a basic timing pattern of 1/6 mains periods being obtained at the 3-phase power system, from which the time bases for various chipping rates can be obtained in a 50 Hz electrical system by integral division, and wherein

25 b) for suppressing jitter during the zero transition detection, a digital phase-locked loop consisting of a digital correlator used for phase detection and a non-linear digital regulator is used so that a very stable synchronization signal freed of short-term fluctuations of any type is available.

30 11. The device according to claim 10, wherein said chipping rates are one of 300 s^{-1} , 600 s^{-1} , 1200 s^{-1} , 2400 s^{-1} , and 4800 s^{-1} .

12. Device according to any one of claims 6 to 11, wherein

a) the required functional groups, with the exception of the mains coupler, of the zero transmission detector and of the transmission power amplifier are



monolithically integrated in a mixed analog/digital application-specific integrated circuit (ASIC), the memories preferably being constructed as RAM cells, the content of which is loaded via an external read-only memory after a circuit reset, and

- b) the mixed analog/digital application-specific integrated circuit also
5 contains the program memory of the digital circuit.

13. The device according to claim 12, wherein the program memory of the digital circuit is in the form of a ROM.

- 10 14. The device according to claim 13, wherein the program memory of the digital circuit is in the form of EPROM.

15. Device according to any one of claims 12 to 14, wherein said external read-only memory is in the form of a ROM, PROM or EPROM.

15

16. The method according to claim 1, wherein N is 4.

17. A multicarrier method for transmitting digital data via electrical power
distribution systems for synchronization of signal synthesis for transmitting and receiving
20 and for the synchronization of received signal processing, the mains AC signal always
coupled to a zero transmission of the mains voltage and wherein for the purpose of
transmitting information by means of fast continuous-phase frequency changes and by
means of signal processing, said method substantially as described hereinbefore in
relation to any one of the described embodiments with reference to Figs. 1 to 3 of the
25 accompanying drawings.



18. A device for transmitting digital data via electrical power distribution systems for synchronization of signal synthesis for transmitting and receiving and for the synchronization of received signal processing, the mains AC signal always coupled to a
5 zero transmission of the mains voltage and wherein for the purpose of transmitting information by means of fast continuous-phase frequency changes and by means of signal processing, said method substantially as described hereinbefore in relation to any one of the described embodiments with reference to Figs. 1 to 3 of the accompanying drawings.

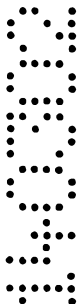
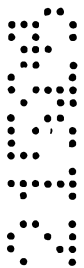
10

DATED this Twelfth Day of March, 2002

ABB Patent GmbH

Patent Attorneys for the Applicant

SPRUSON & FERGUSON



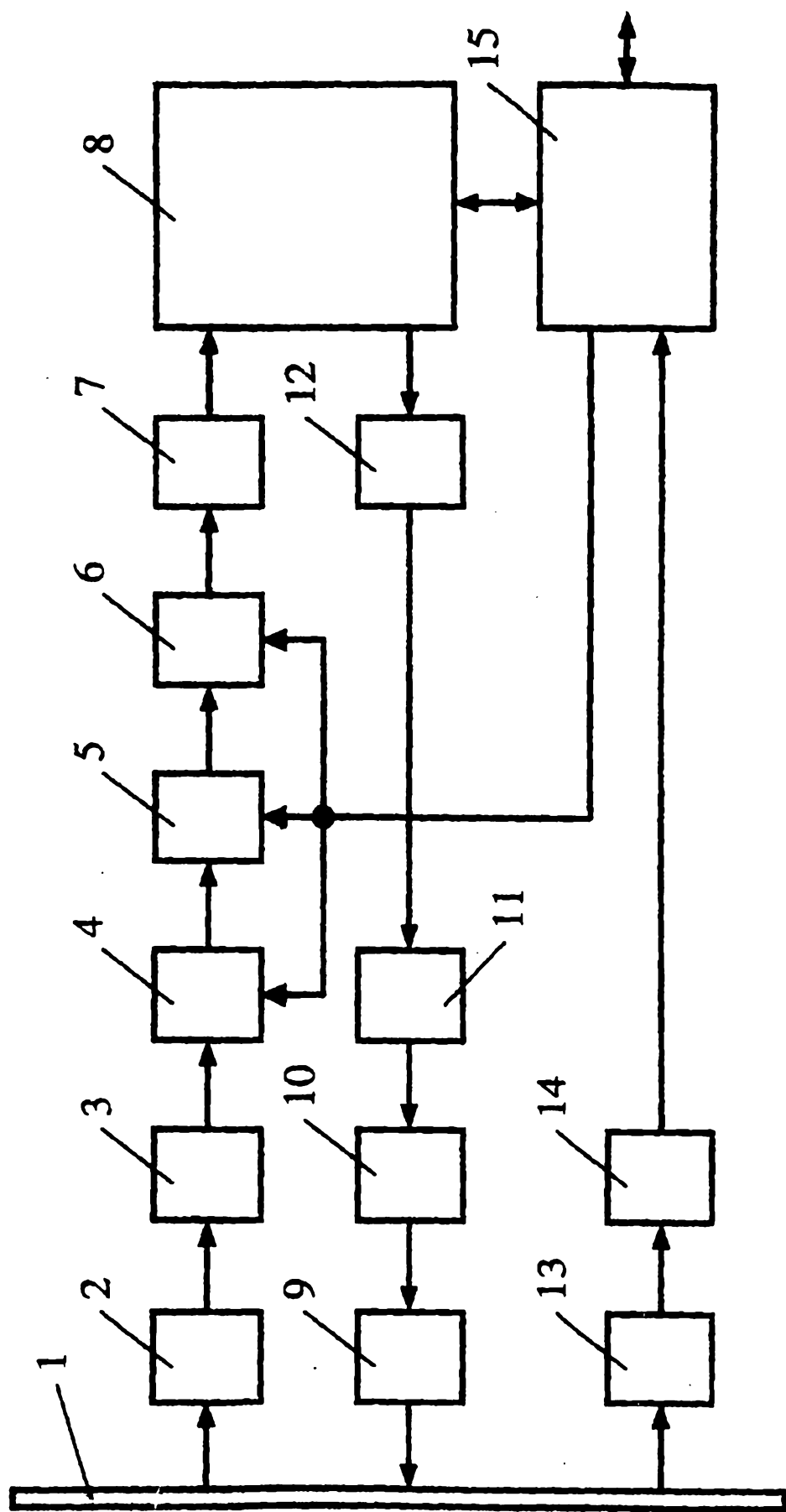


Fig. 1

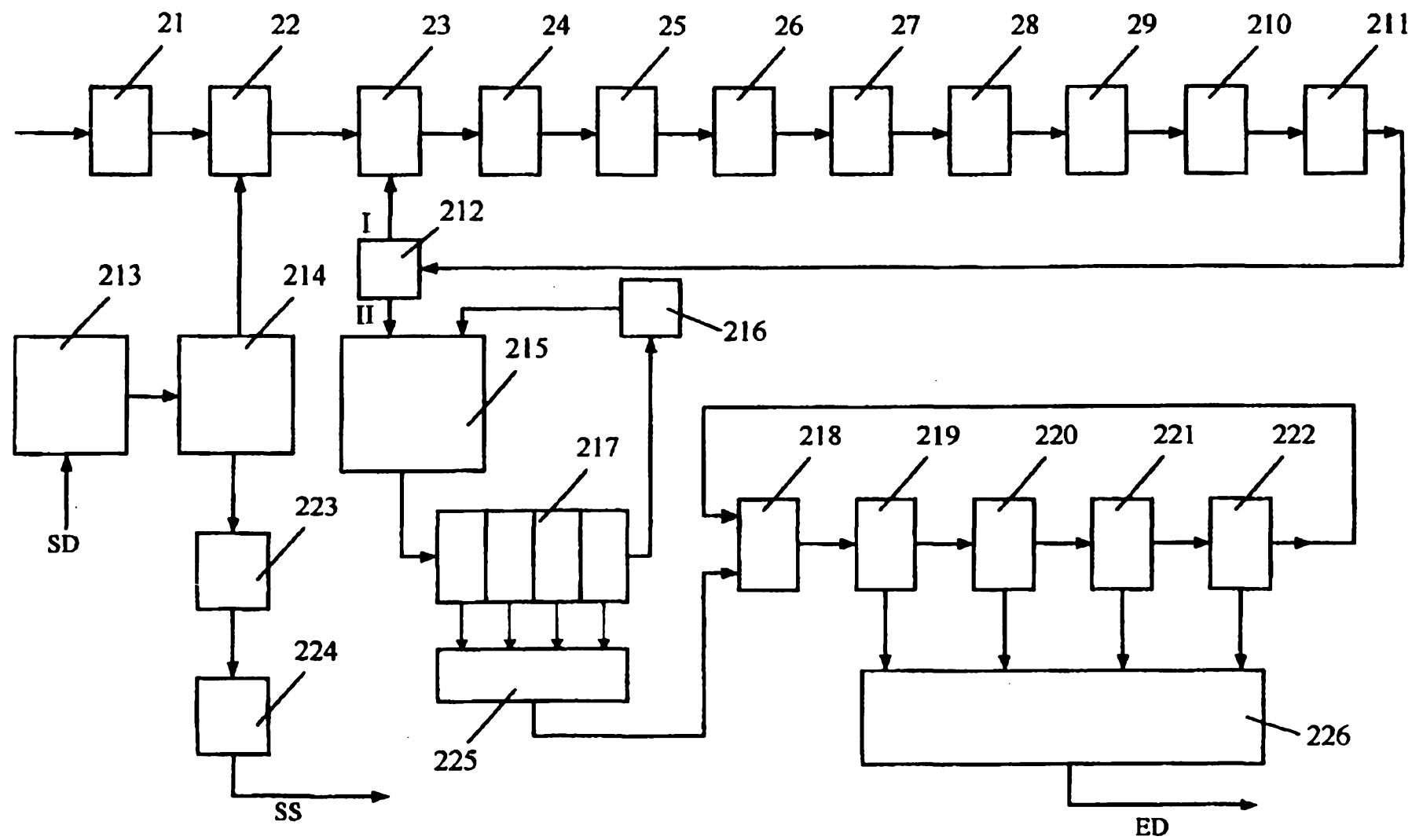


Fig. 2

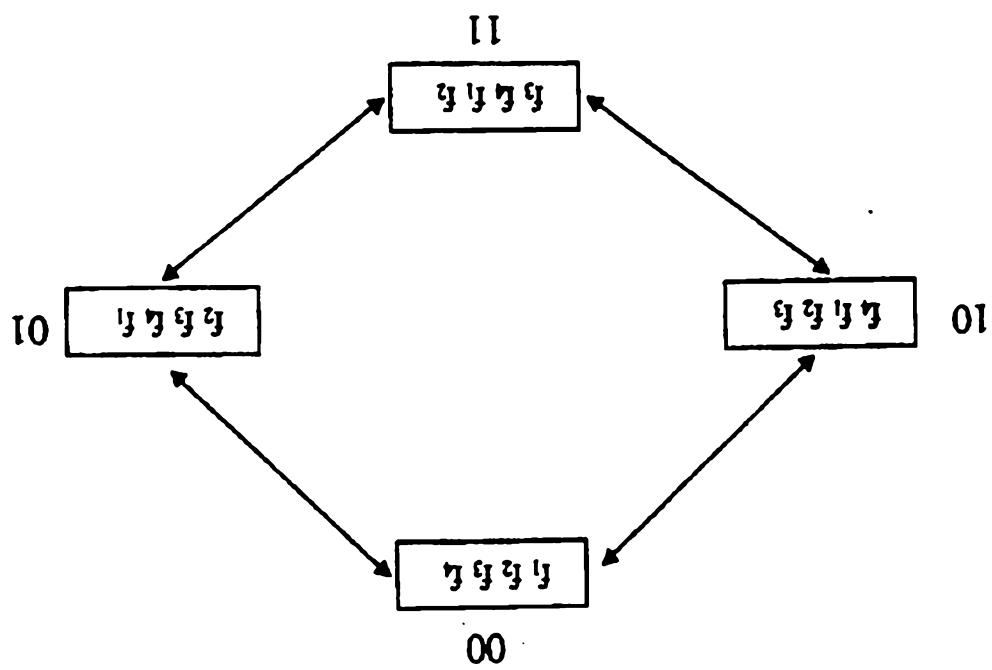


Fig. 3