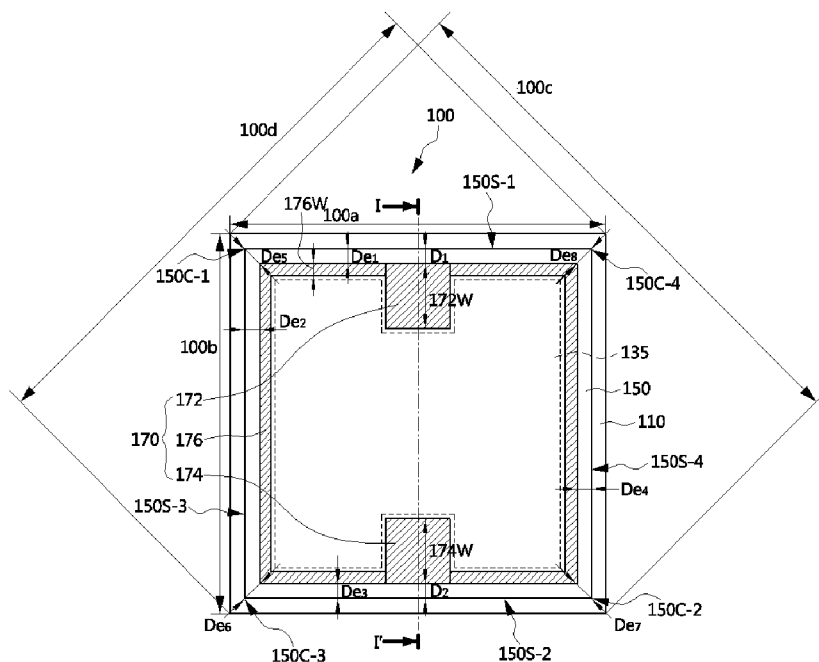




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[Continued on nextpage]

- (54) Title:** LIGHT EMITTING DIODE WITH IMPROVED CURRENT SPREADING



- (57) Abstract:** A light emitting diode is provided. The light emitting diode includes a substrate. A semiconductor structure layer including an active layer is positioned on the substrate. A pad pattern is disposed on an upper surface of the semiconductor structure layer. The pad pattern includes a bonding pad disposed adjacent to a first edge of the upper surface of the semiconductor structure layer, a current distribution pad disposed adjacent to a second edge disposed opposite to the first edge, and extensions configured to electrically connect the bonding pad and the current distribution pad.

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Description

Title of Invention: LIGHT EMITTING DIODE WITH IMPROVED CURRENT SPREADING

Technical Field

- [1] Example embodiments of the present invention relate in general to a semiconductor device, and, more specifically, to a light emitting diode.

Background Art

- [2] A light emitting diode (LED) is basically a PN junction diode formed by combining a P-type semiconductor and an N-type semiconductor.
- [3] In the LED, when a P-type semiconductor and an N-type semiconductor are combined and a voltage is applied to the P-type and N-type semiconductors, an electric current is allowed to flow through the P-type and N-type semiconductors. In this case, holes of the P-type semiconductor move toward the N-type semiconductor, whereas electrons of the N-type semiconductor move toward the P-type semiconductor, which causes the electrons and holes to move to the PN junction.
- [4] The electrons transferred to the PN junction are bound to the holes while falling from a conduction band to a valence band. In this case, the PN junction emits energy corresponding to a difference in height, that is, energy between the conduction band and the valence band. In the process, the energy is emitted in the form of light.
- [5] Such an LED is a semiconductor device that emits light and shows characteristics such as environmental friendliness, low voltage, long lifespan and inexpensiveness. In the prior art, the LED was widely applied to a display lamp or display of simple information such as numbers. With the development of industrial technology, particularly, information display technology and semiconductor technology, however, the LED has been used in a variety of fields such display devices, automobile head lamps, projectors, etc.
- [6] LEDs may include horizontal LEDs and vertical LEDs. In general, vertical LEDs have excellent current distribution performance compared with horizontal LEDs. That is, horizontal LEDs are formed on a growth substrate for growing an epitaxial layer, and vertical LEDs are positioned on a metal substrate. Therefore, vertical LEDs have an advantage of showing excellent thermal emission performance since they are formed using a metal substrate having high thermal conductivity.
- [7] However, vertical LEDs show poor luminous efficiency and short device lifespan because an electric current focuses on a pad region.

Disclosure of Invention

Technical Problem

[8] Accordingly, example embodiments of the present invention are provided to substantially obviate one or more problems due to limitations and disadvantages of the related art.

[9] Example embodiments of the present invention provide a light emitting diode in which an electric current is uniformly distributed throughout a light emitting region.

[10] Example embodiments of the present invention also provide a light emitting diode having improved lifespan due to uniform current distribution.

Solution to Problem

[11] In some example embodiments, a light emitting diode is provided. The light emitting diode includes a substrate. A semiconductor structure layer including an active layer is disposed on the substrate. A pad pattern is disposed on an upper surface of the semiconductor structure layer. The pad pattern includes a bonding pad disposed adjacent to a first edge of the upper surface of the semiconductor structure layer, a current distribution pad disposed adjacent to a second edge disposed opposite to the first edge, and extensions configured to electrically connect the bonding pad and the current distribution pad.

[12] A distance between the bonding pad and the first edge may be the same as a distance between the current distribution pad and the second edge. The distance between the bonding pad and the first edge may be in a range of 0.5 to 5% of widths of the light emitting diodes in the same direction. The distance between the bonding pad and the first edge may be in a range of 5 to 40 μm . The distance between the current distribution pad and the second edge may be in a range of 0.5 to 5% of the widths of the light emitting diodes in the same direction. The distance between the current distribution pad and the second edge may be in a range of 5 to 40 μm .

[13] The first and second edges may be first and second sides of the upper surface of the semiconductor structure layer, respectively. In this case, the bonding pad and the current distribution pad may be disposed at symmetrical positions and formed in the same shape. On the other hand, an overlapping region of the current distribution pad and the second edge may have a higher length than an overlapping region of the bonding pad and the first edge. In addition, the current distribution pad may partially overlap third and fourth edges disposed at both sides of the second edge.

[14] The bonding pad may have the same area as the current distribution pad.

[15] The first and second edges may be first and second corners of the upper surface of semiconductor structure layer, respectively. In this case, the bonding pad and the current distribution pad may be disposed at symmetrical positions and formed in the same shape. On the other hand, the current distribution pad may be a first current distribution pad, and a second current distribution pad may be disposed on at least one of

- third and fourth corners of the upper surface of the semiconductor structure layer.
- [16] The extensions may be disposed adjacent to edges of the upper surface of the semiconductor structure layer. Distance between the extensions and the edges may be in a range of 5 to 40 μm . The distance between the extensions and the edges may be in a range of 0.5 to 5% of widths of the light emitting diodes in the same direction. The extensions may not lie across a central region of the semiconductor structure layer.
- [17] The bonding pad may not protrude outward relative to the extension adjacent to the bonding pad. A distance between the bonding pad and the first edge may be the same as a distance between the extension and the first edge.
- [18] The current distribution pad may not protrude outward relative to the extension adjacent to the current distribution pad. A current distribution pad current distribution pad and the second edge may be the same as a distance between the extension and the second edge.
- [19] In other example embodiment, another example of a light emitting diode is provided. The light emitting diode includes a substrate. A semiconductor structure layer including an active layer is disposed on the substrate. A pad pattern is disposed on an upper surface of the semiconductor structure layer. The pad pattern includes a bonding pad disposed adjacent to a first edge of the upper surface of the semiconductor structure layer, a current distribution pad disposed spaced apart from the bonding pad, and extensions configured to electrically connect the bonding pad and the current distribution pad. In this case, the bonding pad does not protrude in a direction of the edges relative to the extension adjacent to the bonding pad.
- [20] The distance between the bonding pad and the first edge may be in a range of 0.5 to 5% of widths of the light emitting diodes in the same direction. The distance between the bonding pad and the first edge may be the same as the distance between the extension and the first edge.
- [21] The current distribution pad may be disposed adjacent to the other edges other than the first edge of the upper surface of the semiconductor structure layer. A distance between the current distribution pad and an edge adjacent to the current distribution pad may be in a range of 0.5 to 5% of the widths of the light emitting diodes in the same direction. The extensions may be disposed adjacent to the edges of the upper surface of the semiconductor structure layer. Distances between the extensions and the edges may be in a range of 0.5 to 5% of the widths of the light emitting diodes in the same direction. In addition, the extensions may not lie across a central region of the semiconductor structure layer. Meanwhile, the current distribution pad may not protrude outward relative to the extension adjacent to the current distribution pad.

Advantageous Effects of Invention

[22] According to example embodiments of the present invention, a light emitting diode having improved current spreading performance can be obtained by respectively disposing a bonding pad and a current distribution pad adjacent to facing edges of an upper surface of the semiconductor structure layer. Also, a light emitting diode having improved current spreading performance can be obtained by disposing the bonding pad adjacent to one of the edges of the upper surface of the semiconductor structure layer and arranging the bonding pad so that the bonding pad cannot protrude toward the edge relative to the extension adjacent to the bonding pad.

[23] The technical effects of the present invention are not limited to those described above, and other technical effects can be clearly understood by those skilled in the art.

Brief Description of Drawings

[24] Example embodiments of the present invention will become more apparent by describing in detail example embodiments of the present invention with reference to the accompanying drawings, in which:

[25] FIG. 1 is a plane view showing a light emitting diode according to one example embodiment of the present invention.

[26] FIG. 2 is a cross-sectional view taken along line I-I' shown in FIG. 1.

[27] FIG. 3 is a plane view showing a light emitting diode according to another example embodiment of the present invention.

[28] FIG. 4 is a plane view showing a light emitting diode according to still another example embodiment of the present invention.

[29] FIG. 5 is a plane view showing a light emitting diode according to still another example embodiment of the present invention.

[30] FIG. 6 is a plane view showing a light emitting diode according to still another example embodiment of the present invention.

[31] FIG. 7 is a plane view showing a light emitting diode according to still another example embodiment of the present invention.

[32] FIG. 8 is a cross-sectional view taken along line A-A' shown in FIG. 7.

[33] FIG. 9 is a plane view showing a light emitting diode according to still another example embodiment of the present invention.

[34] FIG. 10 is a plane view showing a light emitting diode according to yet another example embodiment of the present invention.

[35] FIGS. 11A to 11D are images taken while allowing an electric current of 350 mA to flow through light emitting diodes according to Experiment Examples 1 to 4, respectively.

[36] FIGS. 12A to 12C are plane views showing light emitting diodes according to Experiment Examples 5 to 7, respectively.

- [37] FIGS. 13A to 13C are images taken while allowing an electric current of 350 mA to flow through the light emitting diodes according to Experiment Examples 5 to 7, respectively.
- [38] FIG. 14 is a schematic plane view showing a light emitting diode according to Experiment Example 15.
- [39] FIGS. 15A to 15D are images taken while allowing an electric current of 350 mA to flow through light emitting diodes according to Experiment Examples 8 to 11, respectively.
- [40] FIG. 16 is a schematic plane view showing a light emitting diode according to Experiment Example 12.
- [41] FIGS. 17A to 17D are images taken while allowing an electric current of 1,000 mA to flow through light emitting diodes according to Experiment Examples 12 and 13, respectively.
- [42] FIGS. 18A and 18B are images taken while allowing an electric current to flow through light emitting diodes according to Experiment Examples 14 and 15, respectively.

Mode for the Invention

- [43] Example embodiments of the present invention are disclosed herein. However, specific structural and functional details disclosed herein are merely representative for purposes of describing example embodiments of the present invention, however, example embodiments of the present invention may be embodied in many alternate forms and should not be construed as limited to example embodiments of the present invention set forth herein.
- [44] Accordingly, while the invention is susceptible to various modifications and alternative forms, specific example embodiments thereof are shown by way of example in the drawings and will herein be described in detail. It should be understood, however, that there is no intent to limit the invention to the particular forms disclosed, but on the contrary, the invention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention. Like numbers refer to like elements throughout the description of the figures.
- [45] It will be understood that, although the terms first, second, etc. may be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another. For example, a first element could be termed a second element, and, similarly, a second element could be termed a first element, without departing from the scope of the present invention. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

- [46] It will be understood that when an element is referred to as being "connected" or "coupled" to another element, it can be directly connected or coupled to the other element or intervening elements may be present. In contrast, when an element is referred to as being "directly connected" or "directly coupled" to another element, there are no intervening elements present. Other words used to describe the relationship between elements should be interpreted in a like fashion (*i.e.*, "between" versus "directly between," "adjacent" versus "directly adjacent," etc.).
- [47] The terminology used herein is for the purpose of describing particular example embodiments only and is not intended to be limiting of the invention. As used herein, the singular forms "a," "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises," "comprising," "includes" and/or "including," when used herein, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.
- [48] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this invention belongs. It will be further understood that terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.
- [49] FIG. 1 is a plane view showing a light emitting diode according to one example embodiment of the present invention, and FIG. 2 is a cross-sectional view taken along line I-I shown in FIG. 1.
- [50] Referring to FIGS. 1 and 2, the light emitting diode 100 includes a semiconductor structure layer 150 disposed on a supporting substrate 110. A bonding metal layer 120 may be disposed between the supporting substrate 110 and the semiconductor structure layer 150. Also, a current spreading inducing layer 130 including a current interrupting pattern 133 and a current transfer pattern 135 may be disposed between the bonding metal layer 120 and the semiconductor structure layer 150. A pad pattern 170 including a bonding pad 172, a current distribution pad 174 and extensions 176 configured to electrically connect the bonding pad 172 and the current distribution pad 174 may be disposed on an upper surface of the semiconductor structure layer 150.
- [51] The semiconductor structure layer 150 may include the first-type semiconductor layer 152, a second-type semiconductor layer 156 and an active layer 154 positioned between the first and second-type semiconductor layers 152 and 156. The first-type semiconductor layer 152 is a nitride-based semiconductor layer that may be doped with

an n-type dopant. By way of example, the first-type semiconductor layer 152 may be a layer in which an $\text{In}_x\text{Al}_y\text{Ga}_{1-x-y}\text{N}$ ($0 < x \leq 1$, $0 < y \leq 1$, and $x+y \leq 1$) layer is doped with Si as the n-type dopant. More particularly, the first-type semiconductor layer 152 may be a GaN layer doped with Si. On the other hand, the first-type semiconductor layer 152 may be provided with a plurality of $\text{In}_x\text{Al}_y\text{Ga}_{1-x-y}\text{N}$ ($0 < x \leq 1$, $0 < y \leq 1$, and $x+y \leq 1$) layers having different compositions.

- [52] The active layer 154 may be an $\text{In}_x\text{Al}_y\text{Ga}_{1-x-y}\text{N}$ ($0 < x < 1$, $0 < y < 1$, and $0 < x+y < 1$) layer, and have a single quantum well (SQW) structure or multiple quantum well (MQW) structure. By way of example, the active layer 154 may have an SQW structure of an InGaN layer or an AlGaIn layer, or a multi-layered structure, that is, an MQW structure, of InGaIn/GaN, AlGaIn/(In)GaIn or InAlGaIn/(In)GaIn.
- [53] Also, the second-type semiconductor layer 156 may be a nitride-based semiconductor layer, and may be a layer doped with a p-type dopant. By way of example, the second-type semiconductor layer 156 may be a layer in which an $\text{In}_x\text{Al}_y\text{Ga}_{1-x-y}\text{N}$ ($0 < x \leq 1$, $0 < y \leq 1$, and $0 \leq x+y < 1$) layer is doped with Mg or Zn as the p-type dopant. More particularly, the second-type semiconductor layer 156 may be a GaN layer doped with Mg. On the other hand, the second-type semiconductor layer 156 may be provided with a plurality of $\text{In}_x\text{Al}_y\text{Ga}_{1-x-y}\text{N}$ ($0 < x \leq 1$, $0 < y \leq 1$, and $0 \leq x+y < 1$) layers having different compositions.
- [54] The supporting substrate 110 may be a semiconductor substrate formed of Si, GaAs, GaP, or InP, or a metal substrate formed of Cu or W. The supporting substrate 110 may function to support the semiconductor structure layer 150, and optionally function as an electrode.
- [55] The bonding metal layer 120 is a layer that functions to couple the semiconductor structure layer 150 to the supporting substrate 110, and may be a thermo-compressive bonding layer or a eutectic bonding layer. The thermo-compressive bonding layer may be an Au layer/Au layer, and the eutectic bonding layer may be an Au:Sn layer or a Pd:In layer.
- [56] As described above, the current spreading inducing layer 130 may include the current interrupting pattern 133 and the current transfer pattern 135. By way of example, these two patterns may be formed adjacent to each other. The current interrupting pattern 133 is a region that functions to prevent an electric current 180 from flowing in a vertical direction of the bonding pad 172, and may be an insulation pattern. By way of example, the current interrupting pattern 133 may be formed of silicon oxide or silicon nitride. The current interrupting pattern 133 may be formed below the bonding pad 172, and also formed below the current distribution pad 174. Further, the current interrupting pattern 133 may be formed below the extensions 176.
- [57] Meanwhile, the current transfer pattern 135 is a region that functions to reflect light

generated from the active layer 154 while coming in ohmic contact with the semiconductor structure layer 150, particularly, the second-type semiconductor layer 156, and may be a metal pattern. The current transfer pattern 135 may be a single metal film or a multiple metal film formed of a material selected from the group consisting of nickel (Ni), platinum (Pt), palladium (Pd), rhodium (Rh), tungsten (W), titanium (Ti), silver (Ag) and gold (Au).

- [58] The bonding pad 172 provided in the pad pattern 170 is disposed adjacent to a first edge of the upper surface of the semiconductor structure layer 150. The current distribution pad 174 is disposed apart from the bonding pad 172, and may be disposed in single or plural number. The bonding pad 172 is a pad to which an electrical interconnection configured to apply an electric source, such as a conductive wire, is connected during packaging of the light emitting diode 100. On the other hand, the current distribution pad 174 is a pad to which no electrical interconnection is connected, and functions to distribute an electric current.
- [59] Also, the first edge may refer to one of sides 150s-1, 150s-2, 150s-3 and 150s-4 of the upper surface of the semiconductor structure layer 150, or one of corners 150c-1, 150c-2, 150c-3 and 150c-4 of the upper surface of the semiconductor structure layer 150. As described in this example embodiment, the bonding pad 172 may be disposed adjacent to the first side 150s-1 of the upper surface of the semiconductor structure layer 150. More particularly, the bonding pad 172 may be disposed adjacent to a central region of the first side 150s-1. Meanwhile, the current distribution pad 174 may be disposed adjacent to a second edge positioned opposite to the first edge, particularly, the second side 150s-2 positioned opposite to the first side 150s-1.
- [60] A distance D1 between the bonding pad 172 and the first edge 150s-1 of the upper surface of the semiconductor structure layer 150 may be in a range of 5 to 40 μm , and may be in a range of 0.5 to 5% of widths 100b of the light emitting diodes 100 in the same direction. Likewise, a distance D2 between the current distribution pad 174 and the second edge 150s-2 of the upper surface of the semiconductor structure layer 150 may be in a range of 5 to 40 μm , and may be in a range of 0.5 to 5% of the widths 100b of the light emitting diodes 100 in the same direction.
- [61] The bonding pad 172 and the current distribution pad 174 may have substantially the same area, and may be formed in the same shape. Also, the bonding pad 172 and the current distribution pad 174 may be disposed at symmetrical positions.
- [62] Widths 176w of the extensions 176 may be 3 to 10% smaller than a width 172w of the bonding pad 172 and a width 174w of the current distribution pad 174. Also, the extensions 176 may be disposed adjacent to the edges of the upper surface of the semiconductor structure layer 150. That is, the extensions 176 may be disposed along the edges of the upper surface of the semiconductor structure layer 150. More particularly,

distances De1, De2, De3, De4, De5, De6, De7 and De8 between the extensions 176 and the edges 150s-1, 150s-3, 150s-2, 150s-4, 150c-1, 150c-3, 150c-2 and 150c-4 of the upper surface of the semiconductor structure layer 150 may be in a range of 5 to 40 μm . In this case, these distances may be in a range of 0.5 to 5% of widths 100a, 100b, 100c and 100d of the light emitting diodes 100 in the same direction.

[63] Meanwhile, the bonding pad 172 may not protrude to an outside direction relative to the extension 176 connected to the bonding pad 172. That is, the distance D1 between the bonding pad 172 and the first edge 150s-1 of the upper surface of the semiconductor structure layer 150 may be substantially the same as a distance De1 between the extension 176 and the first edge 150s-1 of the upper surface of the semiconductor structure layer 150. Also, the current distribution pad 174 may not protrude to an outside direction relative to the extension 176 connected to the current distribution pad 174. That is, the distance D2 between the current distribution pad 174 and the second edge 150s-2 of the upper surface of the semiconductor structure layer 150 may be substantially the same as a distance De3 between the extension 176 and the first edge 150s-2 of the upper surface of the semiconductor structure layer 150.

[64] The pad pattern 170 may not include extensions other than the extension 176, for example, extensions that do not lie across the central region of the upper surface of the semiconductor structure layer 150. That is, all the extensions provided in the pad pattern 170 may be disposed adjacent to the edges of the upper surface of the semiconductor structure layer 150, or disposed along the edges of the upper surface of the semiconductor structure layer 150, as described above.

[65] The semiconductor structure layer 150 is formed by sequentially stacking the first-type semiconductor layer 152, the active layer 154 and the second-type semiconductor layer 156 on a growth substrate (not shown). Thereafter, the current spreading inducing layer 130 and the bonding metal layer 120 are formed on the second-type semiconductor layer 156, and the supporting substrate 110 is then attached to the bonding metal layer 120. Then, the light emitting diode 100 may be manufactured by removing the growth substrate using a lift-off method such as a laser lift-off (LLO) method or a chemical lift-off (CLO) method, followed by forming the pad pattern 170 on the first-type semiconductor layer 152 that is exposed by removal of the growth substrate. The pad pattern 170 may be an Al layer, a Pt layer, a Ni layer, an Au layer, or a composite layer thereof.

[66] FIG. 3 is a plane view showing a light emitting diode according to another example embodiment of the present invention. The light emitting diode according to this example embodiment has a configuration similar to the light emitting diode described with reference to FIGS. 1 and 2, except for the configurations to be described below.

[67] Referring to FIG. 3, a pad pattern 170 includes a bonding pad 172 disposed adjacent

to a first edge of an upper surface of a semiconductor structure layer 150, and at least one current distribution pad 174 spaced apart from the bonding pad 172. The pad pattern 170 may further include extensions 176 configured to electrically connect the bonding pad 172 and the current distribution pad 174.

[68] Also, the first edge may be a first side 150s-1 of the upper surface of the semiconductor structure layer 150. That is, the bonding pad 172 may be disposed adjacent to the first side 150s-1 of the upper surface of the semiconductor structure layer 150. More particularly, the bonding pad 172 may be disposed adjacent to a central region of the first side 150s-1.

[69] Meanwhile, the current distribution pad 174 may be disposed adjacent to a second edge positioned opposite to the first edge, particularly, a second side 150s-2. Unlike the example embodiment described with reference to FIG. 1, however, the current distribution pad 174 may be configured so that an overlapping region of the current distribution pad 174 and the second edge, particularly, the second side 150s-2, can have a higher length than an overlapping region of the bonding pad 172 and the first edge, particularly, the first side 150s-1. In addition, the current distribution pad 174 may extend to partially overlap third and fourth edges disposed at both sides of the second edge, particularly, third and fourth sides 150s-3 and 150s-4. In this case, widths 174w1 and 174w2 of the current distribution pad 174 may be higher than a width 176w of the extension 176. Meanwhile, the current distribution pad 174 may have substantially the same area as the bonding pad 172.

[70] FIG. 4 is a plane view showing a light emitting diode according to still another example embodiment of the present invention. The light emitting diode according to this example embodiment has a configuration similar to the light emitting diode described with reference to FIGS. 1 and 2, except for the configurations to be described below.

[71] Referring to FIG. 4, a pad pattern 170 includes a bonding pad 172 disposed adjacent to a first edge of an upper surface of a semiconductor structure layer 150, and at least one current distribution pad 174 spaced apart from the bonding pad 172. The pad pattern 170 may further include extensions 176 configured to electrically connect the bonding pad 172 and the current distribution pad 174.

[72] The first edge may be a first corner 150c-1 of the upper surface of the semiconductor structure layer 150. That is, the bonding pad 172 may be disposed adjacent to a first corner 150c-1 of the upper surface of the semiconductor structure layer 150. Meanwhile, the current distribution pad 174 may be disposed adjacent to a second edge positioned opposite to the first edge, particularly, a second corner 150s-2.

[73] Also, the bonding pad 172 and the current distribution pad 174 may have substantially the same area, and may be formed in the same shape. Also, the bonding pad

172 and the current distribution pad 174 may be disposed at symmetrical positions.

[74] FIG. 5 is a plane view showing a light emitting diode according to still another example embodiment of the present invention. The light emitting diode according to this example embodiment has a configuration similar to the light emitting diode described with reference to FIGS. 1 and 2, except for the configurations to be described below.

[75] Referring to FIG. 5, a pad pattern 170 includes a bonding pad 172 disposed adjacent to a first edge of an upper surface of a semiconductor structure layer 150, and at least one current distribution pad 174 spaced apart from the bonding pad 172. The pad pattern 170 may further include extensions 176 configured to electrically connect the bonding pad 172 and the current distribution pad 174.

[76] The first edge may be a first corner 150c-1 of the upper surface of the semiconductor structure layer 150. That is, the bonding pad 172 may be disposed adjacent to the first corner 150c-1 of the upper surface of the semiconductor structure layer 150.

[77] Meanwhile, the current distribution pad 174 may include a first current distribution pad 174a disposed adjacent to a second edge positioned opposite to the first edge, particularly, a second corner 150s-2, and second and third current distribution pads 174b and 174c disposed respectively at the other corners 150c-3 and 150c-4 of the upper surface of the semiconductor structure layer 150.

[78] Also, the bonding pad 172 and the first and third current distribution pads 174a, 174b and 174c may be formed in the same shape, and the bonding pad 172 may have substantially the same area as the sum of areas of the first and third current distribution pads 174a, 174b and 174c.

[79] FIG. 6 is a plane view showing a light emitting diode according to still another example embodiment of the present invention. The light emitting diode according to this example embodiment has a configuration similar to the light emitting diode described with reference to FIGS. 1 and 2, except for the configurations to be described below.

[80] As shown in FIG. 1, a ratio of the width 100a of the light emitting diode in the first direction and the width 100b of the light emitting diode in the second direction is close to 1:1, whereas, the light emitting diode as shown in FIG. 6 may be formed to have a higher width 100b in the second direction than a width 100a in the first direction. By way of example, referring to FIG. 6, a ratio of the width 100a in the first direction and the width 100b in the second direction may be in a range of approximately 1:1.5 to 1:2.

[81] FIG. 7 is a plane view showing a light emitting diode according to still another example embodiment of the present invention. FIG. 8 is a cross-sectional view taken along line A-A' as shown in FIG. 7.

[82] Referring to FIGS. 7 and 8, a light emitting diode 100 according to this example em-

bodiment may include a supporting substrate 110, a bonding metal layer 120, a current spreading inducing layer 130, a semiconductor structure layer 150, a passivation layer 160 and a pad pattern 170. The pad pattern 170 may include a bonding pad 172, a current distribution pad 174, and extensions 176 configured to electrically connect the bonding pad 172 and the current distribution pad 174.

[83] The supporting substrate 110 may be a substrate that functions to support the semiconductor structure layer 150, for example, a conductive substrate. Also, the supporting substrate 110 may function to apply an electric source to the light emitting diode 100, particularly, the semiconductor structure layer 150, that is, may act as an electrode of the light emitting diode 100.

[84] The bonding metal layer 120 is interposed between the supporting substrate 110 and a current spreading inducing layer 130 (or a semiconductor structure layer 150) positioned on the supporting substrate 110, and thus functions to couple the supporting substrate 110 and the current spreading inducing layer 130.

[85] The current spreading inducing layer 130 may include a current interrupting pattern 133 and a current transfer pattern 135. In this case, the current interrupting pattern 133 may include an open region, and may be formed in a shape in which the current transfer pattern 135 is filled in the open region of the current interrupting pattern 133.

[86] The current interrupting pattern 133 functions to prevent an electric current 180 supplied from the bonding pad 172, the current distribution pad 174 and the extension 176 from flowing in a vertical direction of the pad pattern 170, thereby allowing the electric current 180 to uniformly flow in the semiconductor structure layer 150, preferably, throughout the active layer 154. That is, the current interrupting pattern 133 functions to sufficiently distribute the electric current 180 supplied to the semiconductor structure layer 150 in the first-type semiconductor layer 152 of the semiconductor structure layer 150 so as to supply the electric current 180 to the active layer 154 provided below the first-type semiconductor layer 152. Also, the current interrupting pattern 133 may function to give information on an etching end point so as to form the semiconductor structure layer 150 during manufacture of the light emitting diode 100. The current interrupting pattern 133 may be formed of an insulating material, and may be composed of a silicon oxide film or a silicon nitride film.

[87] The current transfer pattern 135 may include a material that comes in ohmic contact with the second-type semiconductor layer 156, and reflect light emitted from the active layer 154. The current transfer pattern 135 may be referred to as an ohmic reflective metal pattern. For example, when the second-type semiconductor layer 156 is a P-type semiconductor, the current transfer pattern 135 may be formed of a material such as nickel (Ni), platinum (Pt), palladium (Pd), rhodium (Rh), tungsten (W), titanium (Ti), silver (Ag) or gold (Au), which may come in ohmic contact with the P-type semi-

conductor.

- [88] Meanwhile, the bonding metal layer 120 may function to maintain the reflectivity of the current transfer pattern 135 by preventing metal elements from being distributed from the supporting substrate 110 to the current transfer pattern 135. Also, a Schottky barrier metal layer (not shown) may be disposed between the bonding metal layer 120 and the current interrupting pattern 133.
- [89] The semiconductor structure layer 150 may include a first-type semiconductor layer 152, an active layer 154 and a second-type semiconductor layer 156. Here, the second-type semiconductor layer 156 may be formed on the current spreading inducing layer 130, the active layer 154 may be formed on the second-type semiconductor layer 156, and the first-type semiconductor layer 152 may be formed on the active layer 154. Also, the semiconductor structure layer 150 may further include a superlattice layer (not shown) or an electron blocking layer (not shown). Layers other than the active layer 154 may be omitted in the semiconductor structure layer 150.
- [90] The first-type semiconductor layer 152 may be a III-N-based compound semiconductor doped with first-type impurities, for example, N-type impurities, for example, an (Al, Ga, In) N-based Group III nitride semiconductor layer. The first-type semiconductor layer 152 may be a GaN layer doped with N-type impurities, that is, an N-GaN layer. Also, the first-type semiconductor layer 152 may have a single-layered or multi-layered structure. For example, when the first-type semiconductor layer 152 is formed in a multi-layered structure, the first-type semiconductor layer 152 may have a superlattice structure.
- [91] The active layer 154 may be composed of a III-N-based compound semiconductor, for example, an (Al, Ga, In) N semiconductor layer. Here, the active layer 154 may be formed of a single layer or multiple layers, and thus may emit light of predetermined wavelengths. Also, the active layer 154 may have an SQW structure including one well layer (not shown), and may have an MQW structure in which well layers (not shown) and barrier layers (not shown) are alternately stacked with each other. In this case, one or both of the well layer (not shown) or barrier layer (not shown) may be formed with a superlattice structure.
- [92] The second-type semiconductor layer 156 may be a III-N-based compound semiconductor doped with second-type impurities, for example, P-type impurities, for example, an (Al, In, Ga) N-based Group III nitride semiconductor. The second-type semiconductor layer 156 may be a GaN layer doped with P-type impurities, that is, a P-GaN layer. Also, the second-type semiconductor layer 156 may be formed with a single-layered or multiple-layered structure. For example, the second-type semiconductor layer 156 may be formed with a superlattice structure.
- [93] The superlattice layer (not shown) may be provided between the first type semi-

conductor layer 152 and the active layer 154, and may have a structure including layers formed by stacking a plurality of III-N-based compound semiconductors, for example, (Al, Ga, In) N semiconductor layers, for example, repeatedly stacking InN layers and InGaN layers. In this case, the superlattice layer (not shown) is formed prior to formation of the active layer 154 to prevent dislocations or defects from being transferred to the active layer 154. As a result, the superlattice layer (not shown) may function to reduce formation of the dislocations or defects of the active layer 154 and maintain excellent crystallinity of the active layer 154.

- [94] The electron blocking layer (not shown) may be provided between the active layer 154 and the second-type semiconductor layer 156. In this case, an electron blocking layer (not shown) may be provided to enhance recombination efficiency of electrons and holes and formed of a material having a relatively wide band gap. The electron blocking layer (not shown) may be formed from an (Al, In, Ga) N-based Group III nitride semiconductor, and made of a P-AlGa_N layer doped with Mg.
- [95] The passivation layer 160 may be formed on one surface of the supporting substrate 110 including the semiconductor structure layer 150. In this case, the passivation layer 160 may function to protect the semiconductor structure layer 150 by covering lateral surfaces as well as one surface of the semiconductor structure layer 150 to prevent the semiconductor structure layer 150 from being exposed to the outside. The passivation layer 160 may be made of an insulation film such as a silicon oxide film or a silicon nitride film. Meanwhile, the passivation layer 160 may include an opening 162 configured to expose a certain region of the first conductive semiconductor layer 152.
- [96] The pad pattern 170 may be formed on the passivation layer 160. In this case, FIG. 8 shows that the pad pattern 170 is formed on the passivation layer 160. However, the pad pattern 170 may be provided between the semiconductor structure layer 150 and the passivation layer 160, that is, may be provided so that the passivation layer 160 can cover the pad pattern 170. In this case, the passivation layer 160 may have an opening configured to open the bonding pad 172 of the pad pattern 170.
- [97] The bonding pad 172 of the pad pattern 170 may be formed on a certain region of the passivation layer 160, preferably one edge of a surface of the semiconductor structure layer 150. The bonding pad 172 may be connected with an external device or an external electric source through a wire (not shown). That is, the light emitting diode 100, particularly, the semiconductor structure layer 150, according to one example embodiment of the present invention is connected to an external electric source through the bonding pad 172. The current interrupting pattern 133 may be positioned just under the bonding pad 172.
- [98] In this case, the bonding pad 172 may have a smaller size than the current interrupting pattern 133. That is, the bonding pad 172 may be provided so that a width of

the bonding pad 172 can be smaller than that of the current interrupting pattern 133.

[99] The current distribution pad 174 of the pad pattern 170 is formed in plural number on a certain region of the passivation layer 160. In this case, the current distribution pad 174 may be provided to be spaced apart from the bonding pad 172. The current distribution pad 174 may be formed on one edge of the surface of the semiconductor structure layer 150 other than the one edge of the surface of the semiconductor structure layer 150 on which the bonding pad 172 is positioned. That is, when the bonding pad 172 is positioned on one edge of the surface of the semiconductor structure layer 150 as shown in FIG. 7, the current distribution pad 174 may be formed on the other edge of the surface of the semiconductor structure layer 150 that is positioned opposite the one edge on which the bonding pad 172 is positioned.

[100] Like the bonding pad 172, the current interrupting pattern 133 may be positioned just under the current distribution pad 174. Therefore, the current interrupting pattern 133 may be provided so that an electric current injected from the current distribution pad 174 to the semiconductor structure layer 150 cannot focus in a vertical direction of the current distribution pad 174 but can be spread within the semiconductor structure layer 150. The current distribution pad 174 may have a size identical to or smaller than that of the bonding pad 172. The current distribution pad 174 is formed to a wider width than the extension 176.

[101] The extensions 176 of the pad pattern 170 may be formed on the semiconductor structure layer 150. The extensions 176 may be connected to the bonding pad 172, and may be provided to be uniformly distributed on the semiconductor structure layer 150. That is, the extensions 176 may be arranged along the edges on the surface of the semiconductor structure layer 150 surface, and arranged across the central region.

[102] The extensions 176 are connected to the bonding pad 172 to uniformly distribute an electric source supplied from the outside in the semiconductor structure layer 150, and thus function to inject the electric source into the semiconductor structure layer 150. The extensions 176 function to electrically connect the bonding pad 172 and the current distribution pad 174. Like the bonding pad 172, the extensions 176 may be provided in a shape in which the current interrupting pattern 130 is positioned just under the extensions 17.

[103] In summary, the light emitting diode 100 according to this example embodiment includes a pad pattern 170, which includes the bonding pad 172, the current distribution pad 174 and the extensions 176, all of which are formed on the semiconductor structure layer 150. When the current interrupting pattern 133 is disposed under at least the bonding pad 172 and the current distribution pad 174 of the pad pattern 170, an electric current flowing through the semiconductor structure layer 150 is allowed to uniformly flow by interaction between the bonding pad 172 and current

distribution pad 174 and the current interrupting pattern 133, thereby uniformly emitting light all over the semiconductor structure layer 150.

[104] FIG. 9 is a plane view showing a light emitting diode according to still another example embodiment of the present invention.

[105] Referring to FIG. 9, the light emitting diode 100 according to this example embodiment is different from the light emitting diode 100 described with reference to FIGS. 7 and 8 in that the current distribution pad 174 may be provided on edges other than the one edge of the surface of the semiconductor structure layer 150. That is, the current distribution pad 174 may be disposed on another edge on which the bonding pad 172 is provided among the edges of the semiconductor structure layer 150.

[106] FIG. 10 is a plane view showing a light emitting diode according to yet another example embodiment of the present invention.

[107] Referring to FIG. 10, the light emitting diode 100 according to this example embodiment is different from the light emitting diode 100 described with reference to FIGS. 7 and 8 in that the current distribution pad 174 may be provided on a central region of the surface of the semiconductor structure layer 150. That is, the light emitting diode 100 according to this example embodiment may have a structure in which the current distribution pad 174 is disposed on a certain region on the surface of the semiconductor structure layer 150 other than the edges of the semiconductor structure layer 150.

[108] Hereinafter, experiment examples of the present invention will be described in detail for better understanding of the invention. However, it should be understood that the following examples are only illustrative for better understanding of the invention, and are not intended to limit the scope of the present invention.

[109] Comparison of device performances according to change in area of current distribution pad

[110] In the light emitting diode as shown in FIG. 1, the area of the current distribution pad 174 was set to amount to 60% (Experiment Example 1), 80% (Experiment Example 2), 100% (Experiment Example 3), and 150% (Experiment Example 4) of the bonding pad 172, and the driving voltage and power were measured. The results are listed in the following Table 1. Also, FIGS. 11A to 11D are images taken while applying an electric current of 350 mA to the light emitting diodes according to Experiment Examples 1 to 4, respectively.

[III] Table 1

[Table 1]

	(Area of current distribution pad/area of bonding pad)	light intensity [mW]	Driving voltage (Vf)[V]
Experiment Example 1	60%	<u>445.4</u>	<u>3.81</u>
Experiment Example 2	80%	<u>444.9</u>	<u>3.80</u>
Experiment Example 3	100%	446.0	3.79
Experiment Example 4	150%	<u>443.7</u>	3.78

[112]

[113] As listed in Table 1, it was confirmed that, when the area of the current distribution pad was identical to that of the bonding pad (Experiment Example 3), the light emitting diode showed the most excellent light intensity (or power) and also had a relatively low driving voltage. However, when the area of the current distribution pad was smaller than that of the bonding pad (Experiment Examples 1 and 2), the light emitting diode showed a lower light intensity than that of Experiment Example 3 and also had a relatively high driving voltage. Also, when the area of the current distribution pad was higher than that of the bonding pad (Experiment Example 4), the light emitting diode showed a lower light intensity than that of Experiment Example 3.

[114] Referring to FIGS. 11A to 11D, it was revealed that the light emitting diode had an excellent current spreading effect, for example, showing a higher ratio of a region emitting light more strongly than those of the other experiment examples (i.e., a red region, ER), when the area of the current distribution pad was identical to that of the bonding pad (see Experiment Example 3 and FIG. 11C).

[115] From these results, it could be seen that, when the area of the current distribution pad was identical to that of the bonding pad, the light emitting diode showed better device performance, compared with when the area of the current distribution pad was not identical to that of the bonding pad.

[116] Comparison of device performance according to change in position of extensions

[117] In the light emitting diode as shown in FIG. 1, the distance D1 between the bonding pad 172 and the edge of the upper surface of the semiconductor structure layer 150 and the distance D2 between the current distribution pad 174 and the edge of the upper surface of the semiconductor structure layer 150 were set to a fixed value of 24 μm , and

the distances (De1, De2, De3, and De4) between the extensions and the edges of the upper surface of the semiconductor structure layer 150 were set respectively to 24 μm (Experiment Example 3), 39 μm (Experiment Example 5), 54 μm (Experiment Example 6), and 69 μm (Experiment Example 7). Then, the driving voltage and power were measured. The results are listed in the following Table 2. Also, FIGS. 12A to 12C are plane views showing the light emitting diodes according to Experiment Examples 5 to 7, respectively, and FIGS. 13A to 13C are images taken while applying an electric current of 350 mA to the light emitting diodes according to Experiment Examples 5 to 7, respectively. In Experiment Examples 3 and 5 to 7, the area of the current distribution pad was set to the same area as the bonding pad.

[118] Table 2

[Table 2]

	Distance between bonding pad (or current distribution pad) and edge of upper surface of semiconductor structure layer	Distance between extensions and edges of upper surface of semiconductor structure layer	Light intensity[mW]	Driving voltage (Vf)[V]
Experiment Example 3	24 μm	24 μm	446.0	3.79
Experiment Example 5		39 μm	<u>425.6</u>	3.80
Experiment Example 6		54 μm	<u>420.1</u>	3.79
Experiment Example 7		69 μm	<u>422.9</u>	3.77

[119] As listed in Table 2, it was confirmed that, when the bonding pad or the current distribution pad did not protrude from the light emitting diode relative to the extension (Experiment Example 3), the light emitting diode showed the most excellent light intensity (or power) and also had a relatively low driving voltage. However, when the bonding pad or current distribution pad protruded from the light emitting diode relative to the extension, that is, the extension moved to be disposed to the central direction of the upper surface of the light emitting diode (Experiment Examples 5, 6, and 7), the light emitting diode showed a drastically reduced light intensity, compared with that of Experiment Example 3.

[120] Referring to FIG. 11C (Experiment Example 3), and FIGS. 13A to 13C (Experiment

Examples 5, 6 and 7), it was revealed that, when the bonding pad or the current distribution pad protruded outward relative to the extension (FIGS. 13A to 13C), the light emitting diode had a poor current spreading effect, for example, showing a lower ratio of a region strongly emitting light (i.e., a red region, ER), compared with when the bonding pad or the current distribution pad did not protrude outward relative to the extension (FIG. 11C). In this case, it was confirmed that the ratio of the region strongly emitting light (i.e., a red region, ER) reduced as the bonding pad or the current distribution pad increasingly protruded outward relative to the extension.

[121] From these results, it could be seen that the light emitting diode showed good device performance when the bonding pad or the current distribution pad did not protrude from the light emitting diode relative to the extension, that is, the distance between the bonding pad (or a current distribution pad) and the edge of the upper surface of the semiconductor structure layer was identical to the distance between the extension and the edge of the upper surface of the semiconductor structure layer.

[122] Comparison of device performance according to changes in positions and shapes of bonding pad, current distribution pad and extensions

[123] The driving voltages and powers of the light emitting diodes as shown in FIG. 1 (Experiment Example 1), FIGS. 3 to 5 (Experiment Examples 8, 9 and 10), and FIG. 14 (Experiment Example 11) were measured. The results are listed in the following Table 3. FIGS. 15A to 15D are images taken while applying an electric current of 350 mA to the light emitting diodes according to Experiment Examples 8 to 11, respectively.

[124] Table 3

[Table 3]

	Bonding pad	Current distribution pad	Extensions	Power[mW]	Driving voltage (V _f)[V]
Experiment Example 3(FIG. 1)	Adjacent to one side of upper surface of semiconductor structure	Adjacent to opposite side of bonding pad and formed in same shape	Formed adjacent to edge of upper surface of semiconductor structure	446.0	3.79
Experiment Example 8(FIG. 3)		Adjacent to opposite side of bonding pad, but having higher overlapping length with sides (having same area as bonding pad)		447.1	3.78
Experiment Example 9(FIG. 4)	Adjacent to one corner of upper surface of semiconductor structure	Adjacent to opposite corner of bonding pad and formed in same shape		447.1	<u>3.86</u>
Experiment Example 10(FIG. 5)		Formed in plural number on opposite corner of bonding pad and other corners (having same area as sum of areas of bonding pads)		449.5	<u>3.86</u>
Experiment Example 11(FIG. 14)	Adjacent to one side of upper surface of semiconductor structure	-	Lying across central region of upper surface of semiconductor structure	<u>444.7</u>	3.75

- [125] As listed in Table 3, it was confirmed that the light emitting diode showed high light intensity (or power) and also had a relatively low driving voltage when the bonding pad 172 was disposed adjacent to one side 150s-1 of the upper surface of the semiconductor structure 150, and the current distribution pad 174 was disposed opposite to the bonding pad 172, that is, disposed adjacent to another side 150s-2 of the upper surface of the semiconductor structure 150 and had the same shape as the bonding pad 172 (Experiment Example 3), as shown in FIG. 1.
- [126] As shown in FIG. 3, it was also confirmed that the light emitting diode showed high light intensity (or power) and also had a relatively low driving voltage when the bonding pad 172 was disposed adjacent to one side 150s-1 of the upper surface of the semiconductor structure 150, and the current distribution pad 174 was disposed opposite to the bonding pad 172, that is, disposed adjacent to another side 150s-2 of the upper surface of the semiconductor structure 150 and had a long overlapping length with the side 150s-2 (Experiment Example 8).
- [127] Meanwhile, the light emitting diode showed a relatively high driving voltage when the bonding pad 172 was disposed adjacent to one corner 150c-1 of the upper surface of the semiconductor structure 150 as shown in FIG. 4 or 5 (Experiment Examples 9 and 10).
- [128] Also, the light emitting diode showed a relatively low light intensity (or power) when one extension 176b of the extensions 176 lay across the central region of the upper surface of the semiconductor structure 150 as shown in FIG. 14 (Experiment Example 11).
- [129] Referring to FIG. 11C (Experiment Example 3), and FIGS. 15A to 15D (Experiment Examples 8 to 11), it was revealed that Experiment Example 3 (the light emitting diode having the configuration as shown in FIG. 1) had an excellent current spreading effect, for example, showing a higher ratio of a region emitting light more strongly than those of the other experiment examples (i.e., a red region, ER in FIG. 11C). However, it was also revealed that Experiment Example 8 (the light emitting diode having the configuration as shown in FIG. 3) had an excellent current spreading effect, for example, showing a relatively high ratio of a region emitting light more strongly than those of the other experiment examples (i.e., a red region, ER in FIG. 15A).
- [130] From these results, it could be seen that the light emitting diode showed good device performance when the bonding pad 172 was disposed adjacent to one side 150s-1 of the upper surface of the semiconductor structure 150, and the current distribution pad 174 was disposed opposite to the bonding pad 172, that is, disposed adjacent to another side 150s-2 of the upper surface of the semiconductor structure 150 and also had the same shape as the bonding pad 172 as shown in FIG. 1 (Experiment Example 3), or when the bonding pad 172 was disposed adjacent to one side 150s-1 of the upper

surface of the semiconductor structure 150, and the current distribution pad 174 was disposed opposite to the bonding pad 172, that is, disposed adjacent to another side 150s-2 of the upper surface of the semiconductor structure 150 and had an longer overlapping length with the side 150s-2 (Experiment Example 8) than the bonding pad 172.

[131] Comparison of device performance according to presence/absence of current distribution pad

[132] The driving voltages and powers of the light emitting diodes as shown in FIG. 6 (Experiment Example 12) and FIG. 16 (Experiment Example 13) were measured. The results are listed in the following Table 4. FIG. 16 is a schematic plane view showing the light emitting diode according to Experiment Example 13. Also, FIGS. 17A and 17D are images taken while applying an electric current of 1,000 mA to the light emitting diodes according to Experiment Examples 12 to 13, respectively.

[133] Table 4

[Table 4]

	Bonding pad	Current distribution pad	Power[mW]	Driving voltage (Vf)[V]
Experiment Example 12(FIG. 6)	Adjacent to one side of upper surface of semiconductor structure	Adjacent to opposite side of bonding pad and formed in same shape	426.61	3.57
Experiment Example 13(FIG. 16)		-	433.60	<u>3.67</u>

[134] As shown in Table 4, it was revealed that, when the pad pattern 170 included the current distribution pad 174 facing the bonding pad 172 as shown in FIG. 6, the light emitting diode showed a relatively lower driving voltage, compared with when the pad pattern 170 did not include a current distribution pad as shown in FIG. 16.

[135] Referring to FIG. 17A (Experiment Example 12) and FIG. 17B (Experiment Example 13), when the pad pattern 170 included the current distribution pad 174 facing the bonding pad 172 (Experiment Example 12) as shown in FIG. 6, the light emitting diode had an excellent current spreading effect, for example, showing a lower ratio of a region strongly emitting light(i.e., a red region, ER), compared with when the pad pattern 170 did not include a current distribution pad (Experiment Example 13) as shown in FIG. 16

[136] From these results, it could be seen that, when the pad pattern 170 included the

current distribution pad 174 facing the bonding pad 172 (Experiment Example 12) as shown in FIG. 6, the light emitting diode showed good device performance, compared with when the pad pattern 170 did not include a current distribution pad (Experiment Example 13) as shown in FIG. 16.

[137] FIGS. 18A and 18B are images taken while applying an electric current to the light emitting diode (Experiment Example 14) as shown in FIG. 7 and the light emitting diode (Experiment Example 15) in which a current distribution pad was removed from the light emitting diode as shown in FIG. 7.

[138] Referring FIG. 18B, it could be seen that, in the case of the light emitting diode (Experiment Example 15) from which the current distribution pad was removed, an electric current focused on a certain region, particularly, a region 190 adjacent to the bonding pad 172 (see FIG. 7) so that the region 190 could emit stronger light than other regions.

[139] Referring FIG. 18A, it could be seen that, in the case of the light emitting diode (Experiment Example 14) including the current distribution pad, light was relatively uniformly emitted from a region in which the current distribution pad 174 was disposed, as well as a region in which the bonding pad 172 was disposed, for example, light was relatively uniformly emitted from an entire region of the pad pattern. That is, it could be seen that the light emitting diode including the current distribution pad showed uniform current distribution over the semiconductor structure layer, that is, the entire light emitting region.

[140] While the example embodiments of the present invention and their advantages have been described in detail, it should be understood that various changes, substitutions and alterations may be made herein without departing from the scope of the invention.

Claims

- [Claim 1] A light emitting diode comprising:
a substrate;
a semiconductor structure layer which is positioned on the substrate and includes an active layer; and
a pad pattern including a bonding pad disposed adjacent to a first edge of an upper surface of the semiconductor structure layer, a current distribution pad disposed adjacent to a second edge opposite to the first edge and extensions configured to electrically connect the bonding pad and the current distribution pad.
- [Claim 2] The light emitting diode of claim 1, wherein a distance between the bonding pad and the first edge is the same as a distance between the current distribution pad and the second edge.
- [Claim 3] The light emitting diode of claim 1 or 2, wherein the distance between the bonding pad and the first edge is in a range of 0.5 to 5% of widths of the light emitting diodes in the same direction.
- [Claim 4] The light emitting diode of claim 1 or 2, wherein the distance between the bonding pad and the first edge is in a range of 5 to 40 μm .
- [Claim 5] The light emitting diode of claim 1, wherein the distance between the current distribution pad and the second edge is in a range of 0.5 to 5% of the widths of the light emitting diodes in the same direction.
- [Claim 6] The light emitting diode of claim 1, wherein the distance between the current distribution pad and the second edge is in a range of 5 to 40 μm .
- [Claim 7] The light emitting diode of claim 1, wherein the first and second edges are first and second sides of the upper surface of the semiconductor structure layer, respectively.
- [Claim 8] The light emitting diode of claim 7, wherein the bonding pad and the current distribution pad are disposed at symmetrical positions and formed in the same shape.
- [Claim 9] The light emitting diode of claim 7, wherein an overlapping region of the current distribution pad and the second edge has a higher length than an overlapping region of the bonding pad and the first edge.
- [Claim 10] The light emitting diode of claim 9, wherein the current distribution pad partially overlaps third and fourth edges disposed at both sides of the second edge.
- [Claim 11] The light emitting diode of any one of claims 1 to 9, wherein the bonding pad has the same area as the current distribution pad.

- [Claim 12] The light emitting diode of claim 1, wherein the first and second edges are first and second corners of the upper surface of the semiconductor structure layer, respectively.
- [Claim 13] The light emitting diode of claim 12, wherein the bonding pad and the current distribution pad are disposed at symmetrical positions and formed in the same shape.
- [Claim 14] The light emitting diode of claim 12, wherein the current distribution pad is a first current distribution pad, and which further comprises a second current distribution pad disposed on at least one of third and fourth corners of the upper surface of the semiconductor structure layer.
- [Claim 15] The light emitting diode of claim 1, wherein the extensions are disposed adjacent to the edges of the upper surface of the semiconductor structure layer.
- [Claim 16] The light emitting diode of claim 15, wherein distances between the extensions and the edges are in a range of 5 to 40 μm .
- [Claim 17] The light emitting diode of claim 15, wherein the distances between the extensions and the edges are in a range of 0.5 to 5% of the widths of the light emitting diodes in the same direction.
- [Claim 18] The light emitting diode of claim 15, wherein the extensions do not lie across a central region of the semiconductor structure layer.
- [Claim 19] The light emitting diode of claim 1, wherein the bonding pad does not protrude outward relative to the extension adjacent to the bonding pad.
- [Claim 20] The light emitting diode of claim 19, wherein a distance between the bonding pad and the first edge is the same as a distance between the extension and the first edge.
- [Claim 21] The light emitting diode of claim 1, wherein the current distribution pad does not protrude outward relative to the extension adjacent to the current distribution pad.
- [Claim 22] The light emitting diode of claim 21, wherein a distance between the current distribution pad and the second edge is the same as a distance between the extension and the second edge.
- [Claim 23] A light emitting diode comprising:
a substrate;
a semiconductor structure layer which is positioned on the substrate and includes an active layer; and
a pad pattern including a bonding pad disposed adjacent to a first edge of an upper surface of the semiconductor structure layer, a current dis-

tribution pad disposed apart from the bonding pad and extensions configured to electrically connect the bonding pad and the current distribution pad,

wherein the bonding pad does not protrude in a direction of the edges relative to the extension adjacent to the bonding pad.

[Claim 24] The light emitting diode of claim 23, wherein a distance between the bonding pad and the first edge is in a range of 0.5 to 5% of widths of the light emitting diodes in the same direction.

[Claim 25] The light emitting diode of claim 23 or 24, wherein the distance between the bonding pad and the first edge is the same as a distance between the extension and the first edge.

[Claim 26] The light emitting diode of claim 23, wherein the current distribution pad is disposed adjacent to the other edges other than the first edge of the upper surface of the semiconductor structure layer.

[Claim 27] The light emitting diode of claim 26, wherein a distance between the current distribution pad and an edge adjacent to the current distribution pad is in a range of 0.5 to 5% of the widths of the light emitting diodes in the same direction.

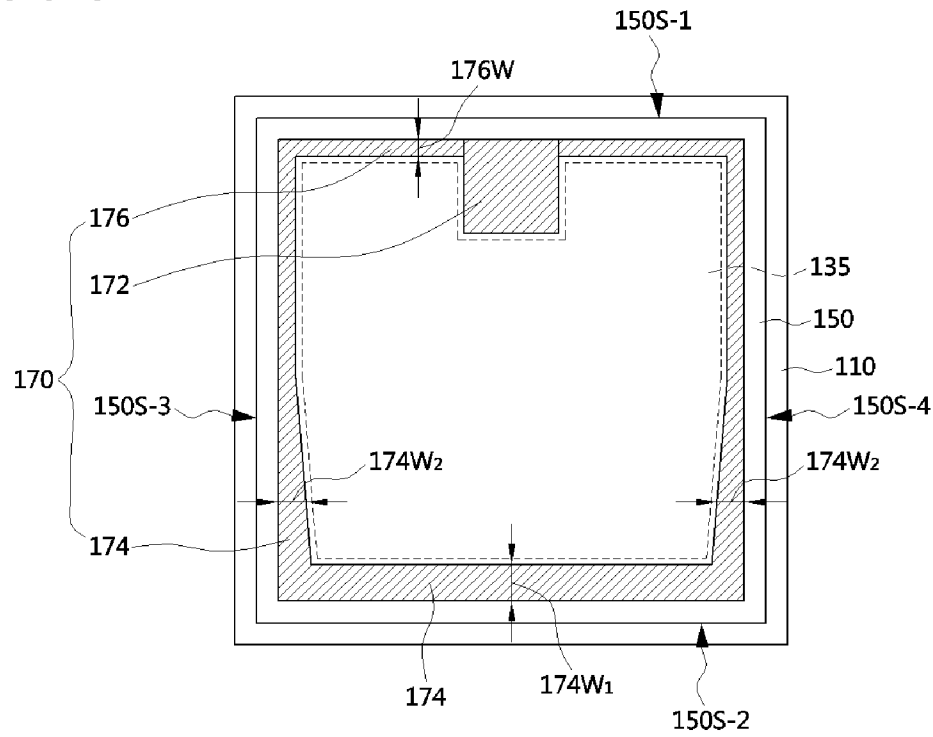
[Claim 28] The light emitting diode of claim 26, wherein the extensions are disposed adjacent to the edges of the upper surface of the semiconductor structure layer.

[Claim 29] The light emitting diode of claim 28, wherein distances between the extensions and the edges are in a range of 0.5 to 5% of the widths of the light emitting diodes in the same direction.

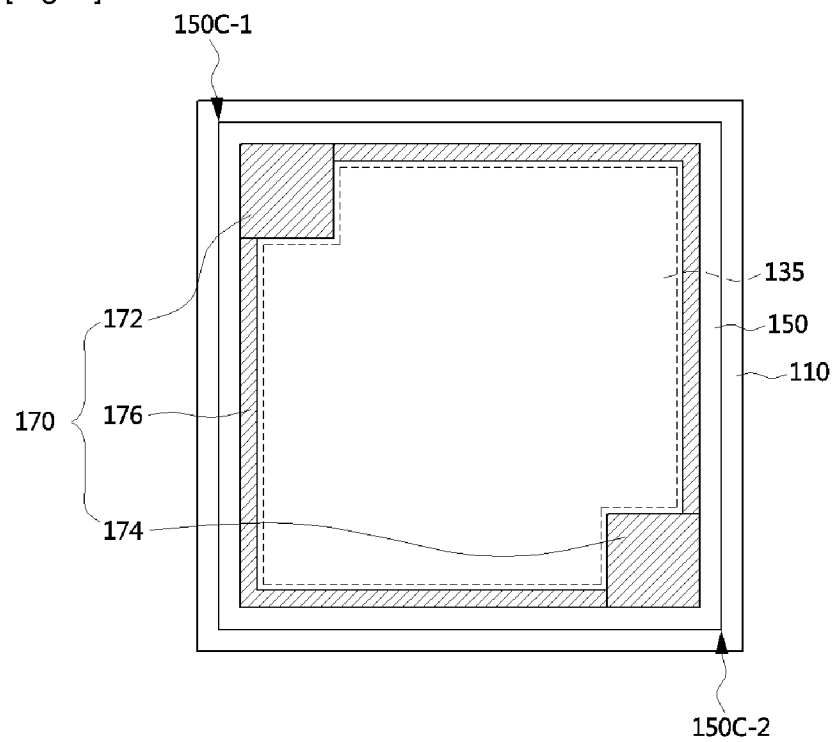
[Claim 30] The light emitting diode of claim 28, wherein the extensions do not lie across a central region of the semiconductor structure layer.

[Claim 31] The light emitting diode of claim 26, wherein the current distribution pad does not protrude outward relative to the extension adjacent to the current distribution pad.

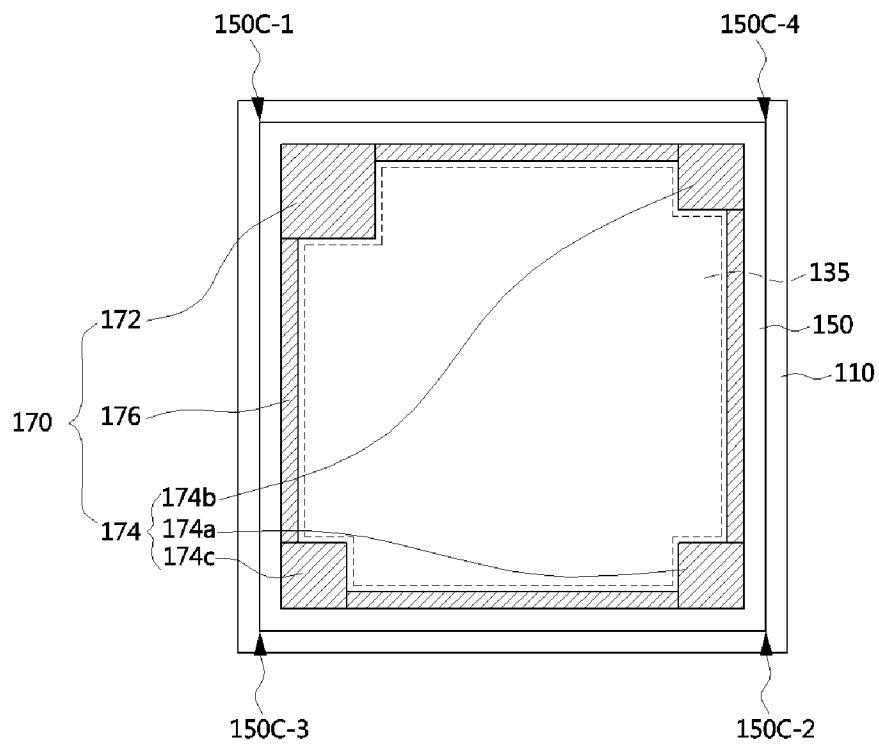
[Fig. 3]



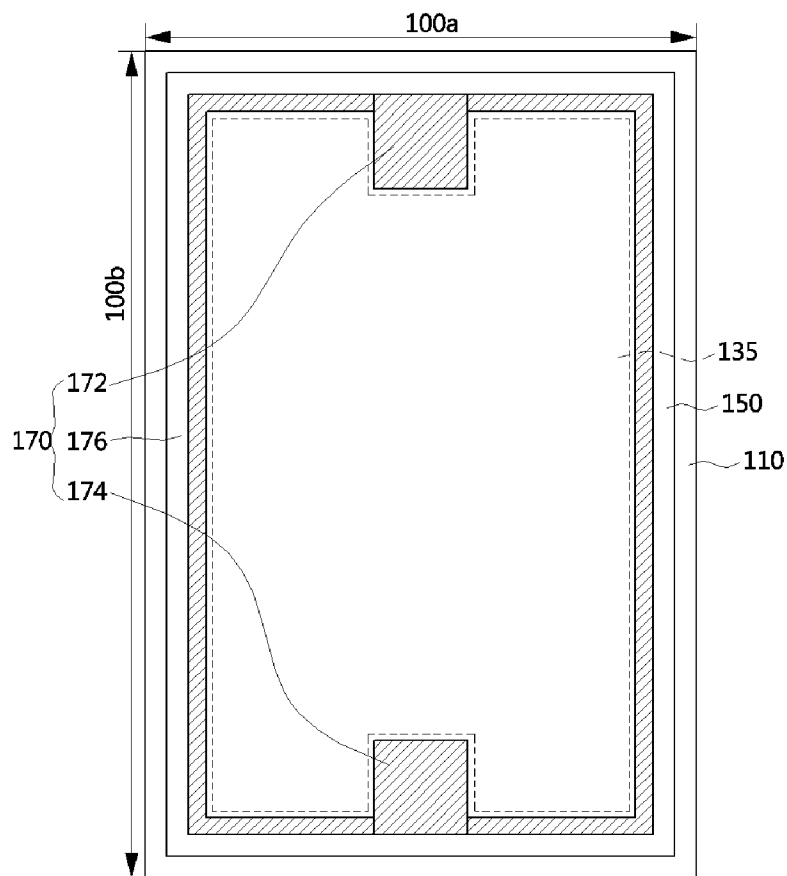
[Fig. 4]



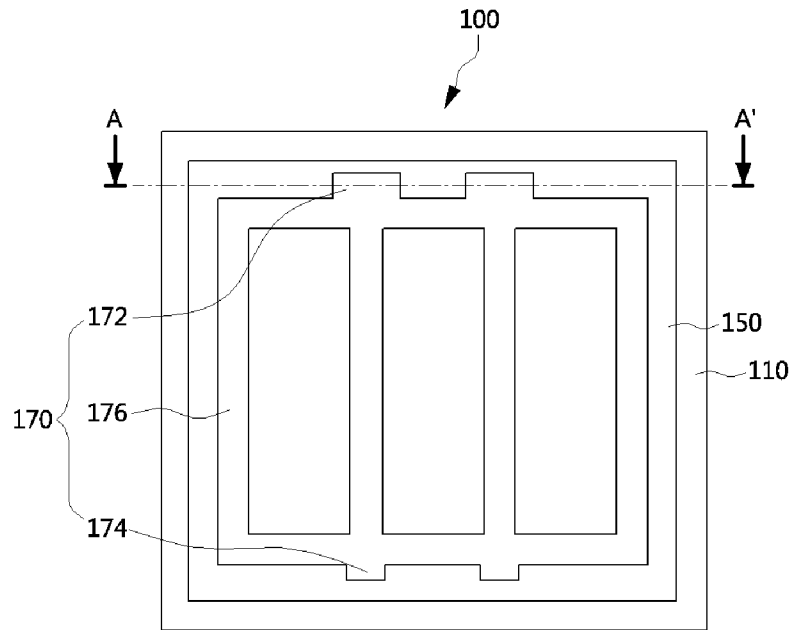
[Fig. 5]



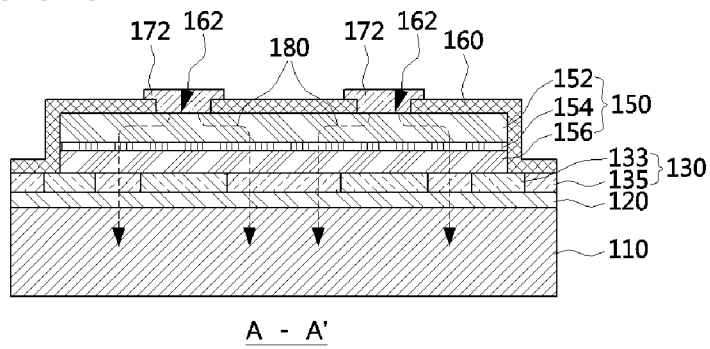
[Fig. 6]



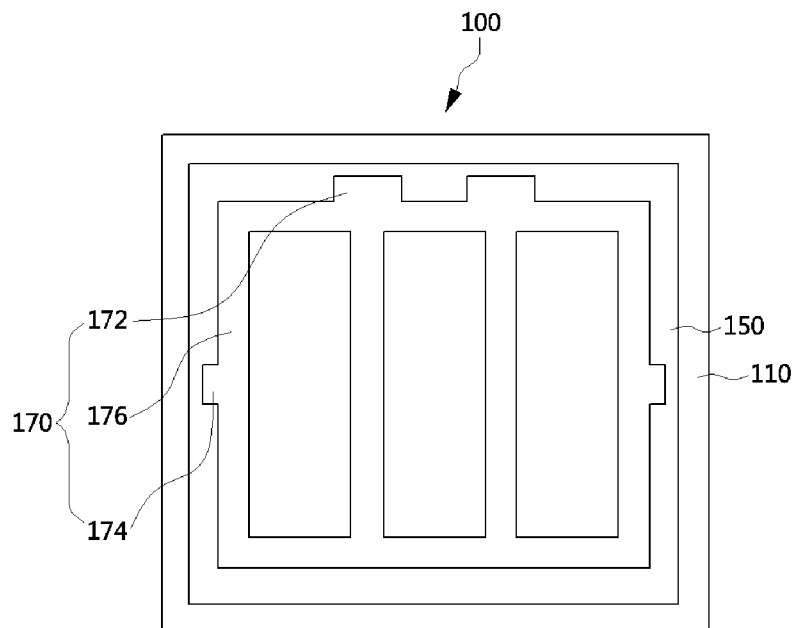
[Fig. 7]



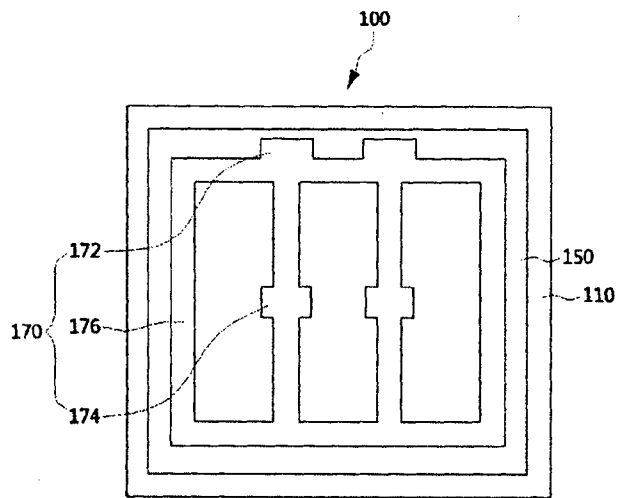
[Fig. 8]



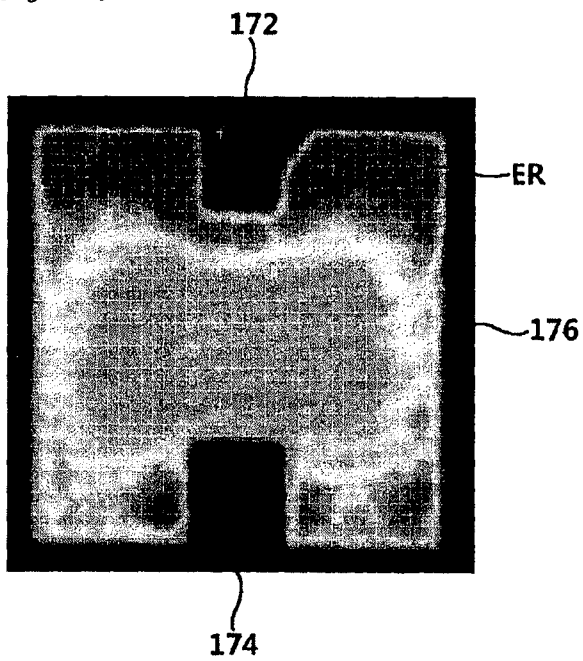
[Fig. 9]



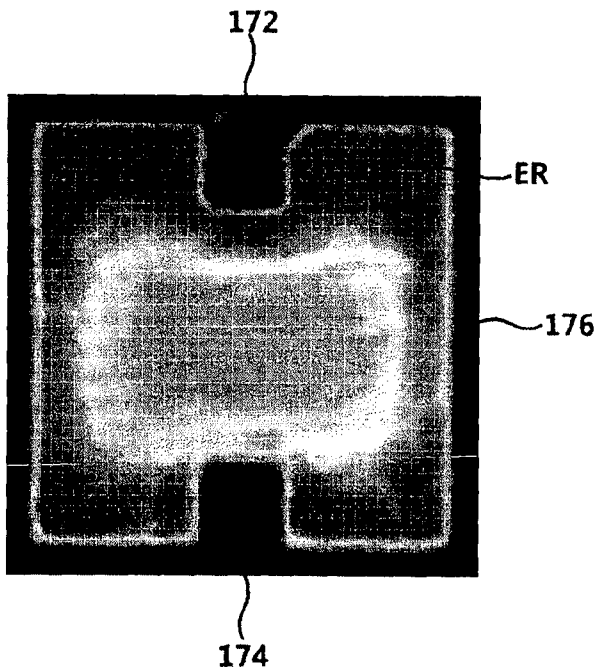
[Fig. 10]



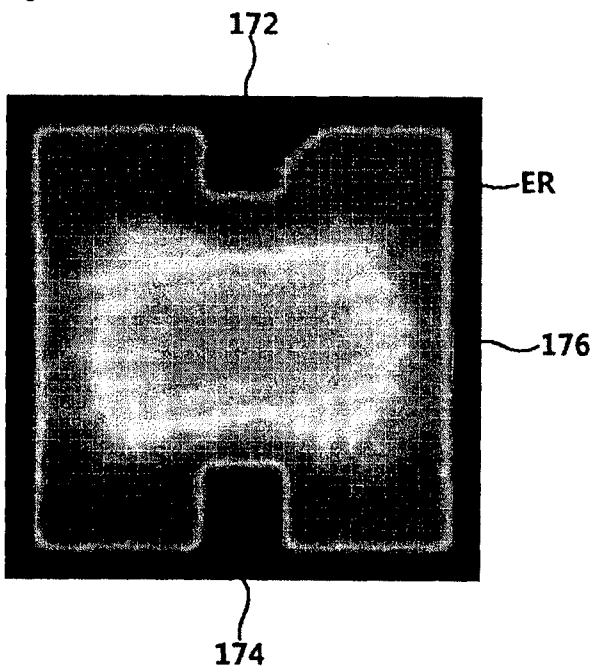
[Fig. 11A]



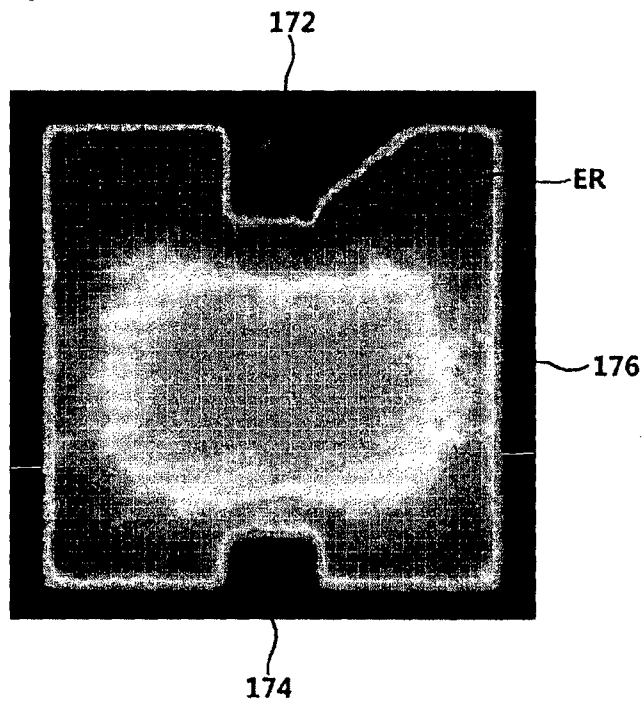
[Fig. 11B]



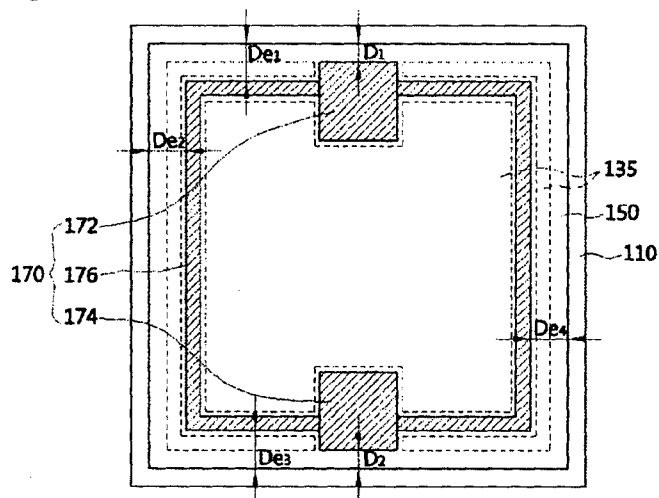
[Fig. 11C]



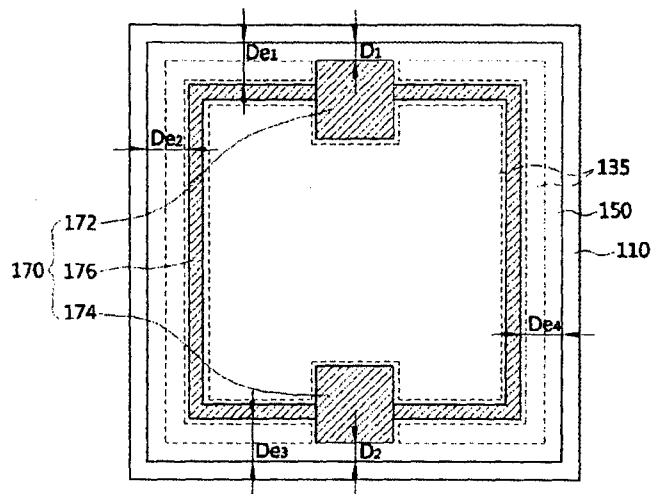
[Fig. 11D]



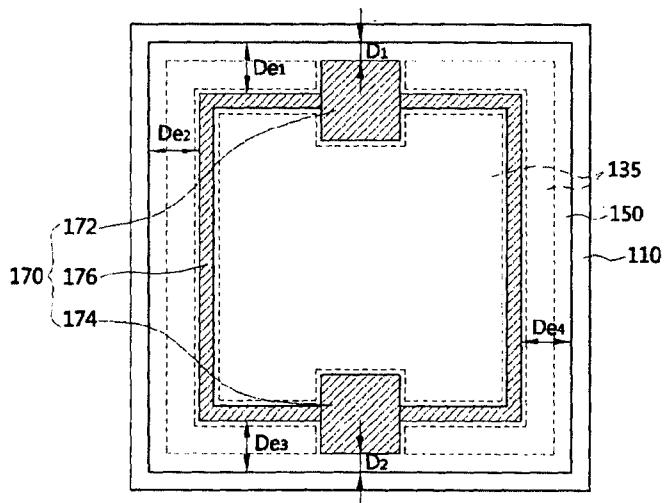
[Fig. 12A]



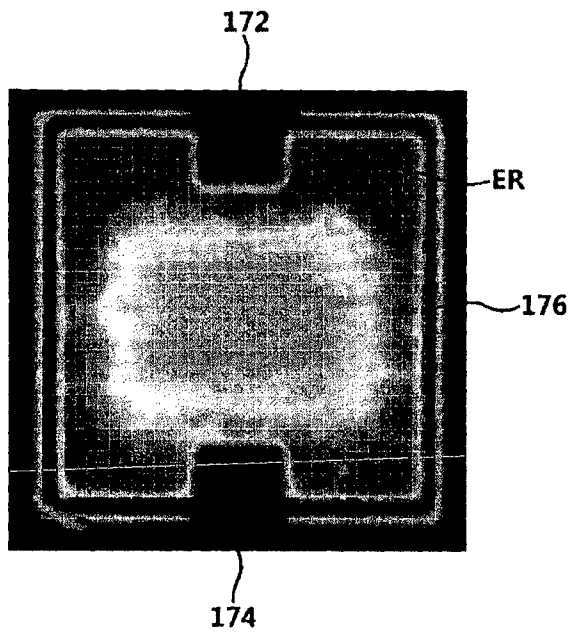
[Fig. 12B]



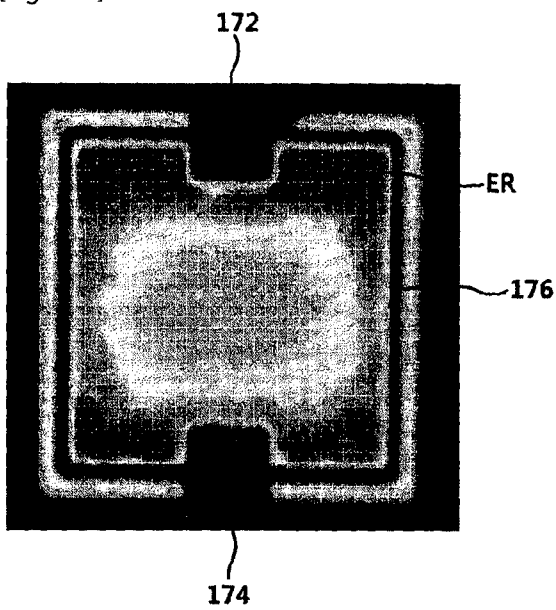
[Fig. 12C]



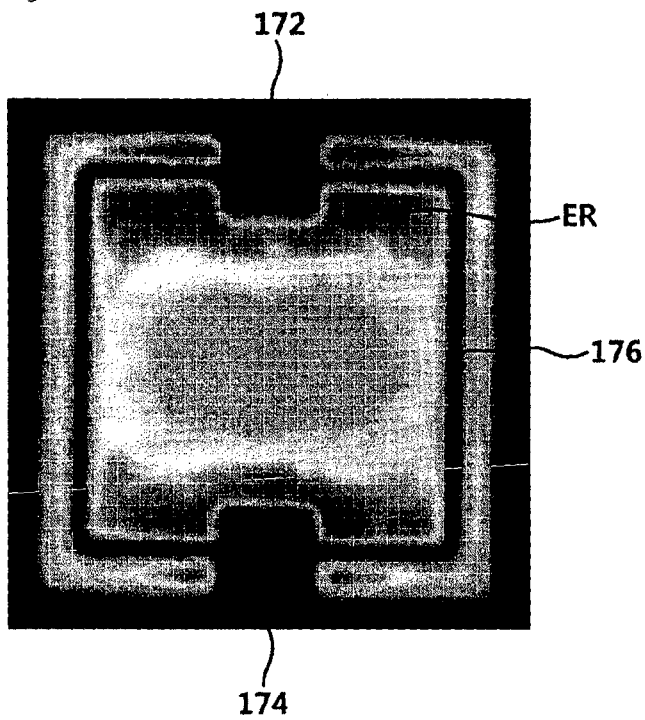
[Fig. 13A]



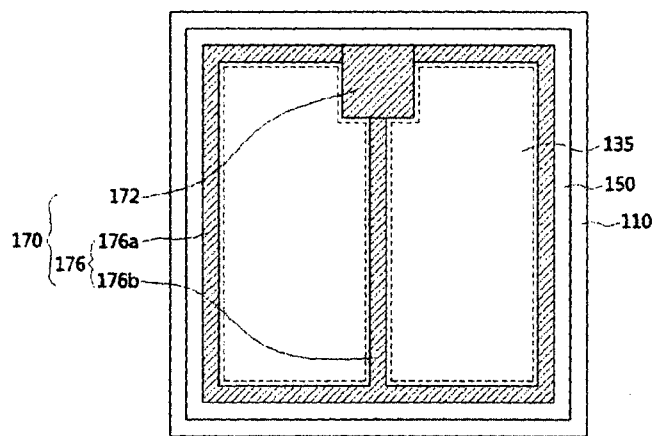
[Fig. 13B]



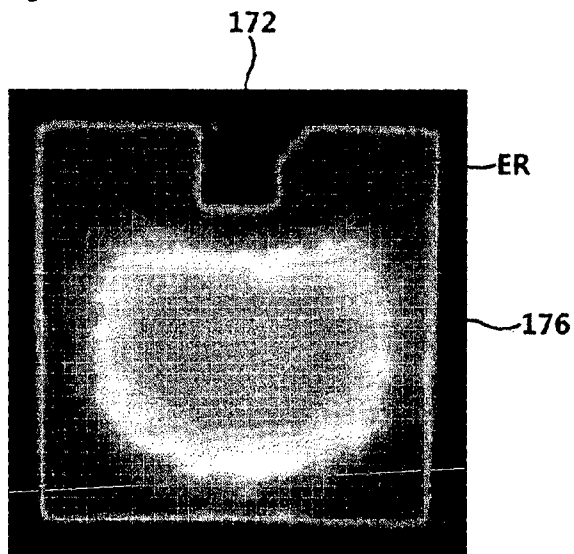
[Fig. 13C]



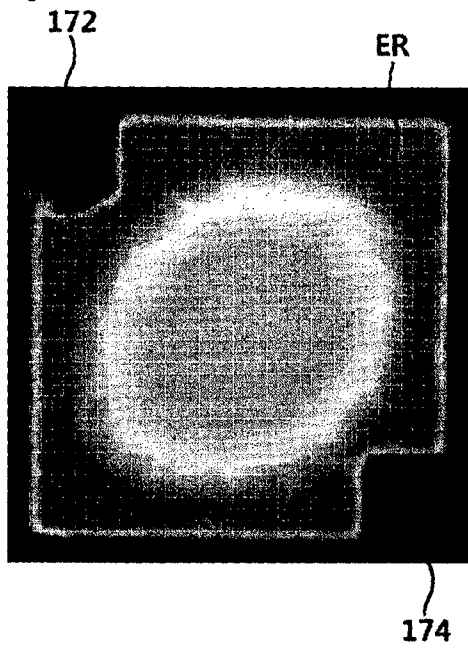
[Fig. 14]



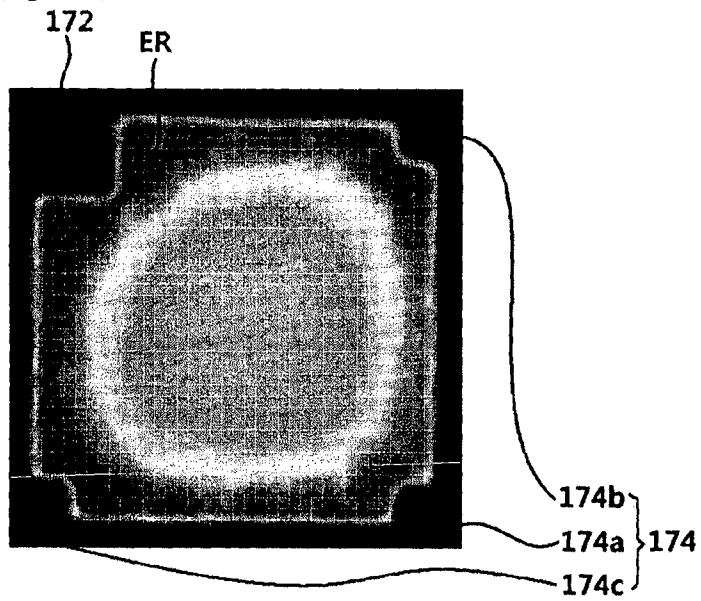
[Fig. 15A]



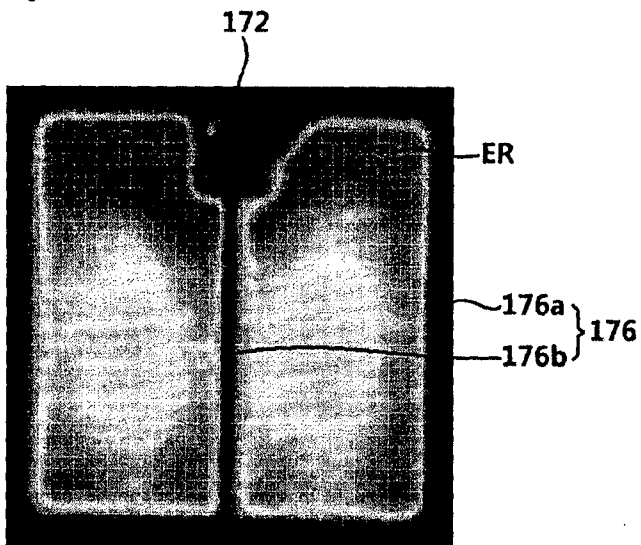
[Fig. 15B]



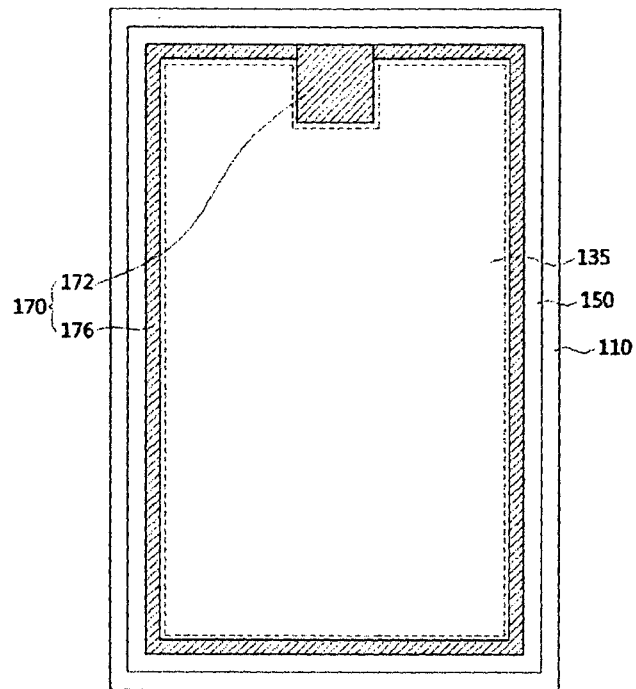
[Fig. 15C]



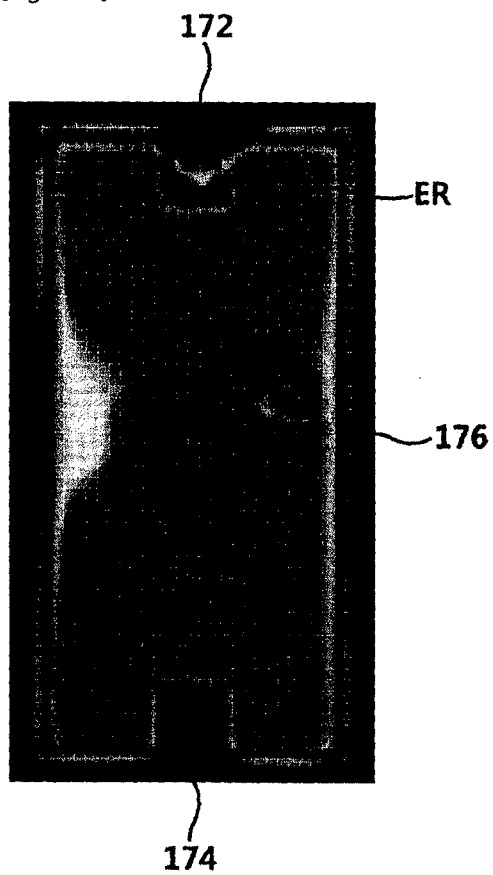
[Fig. 15D]



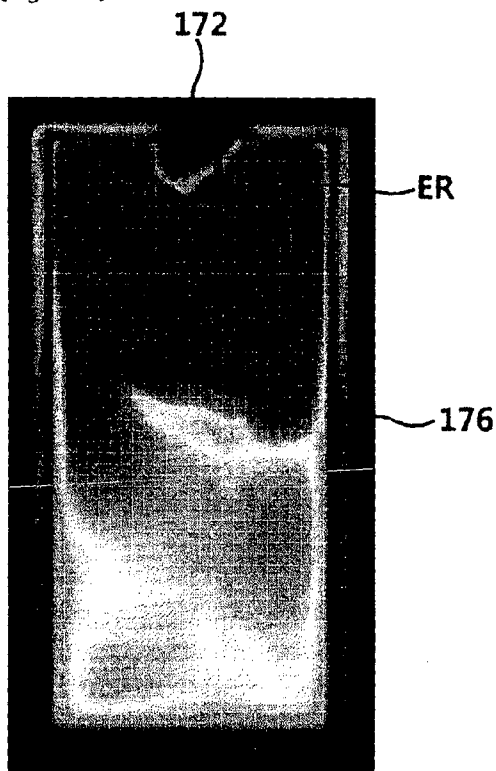
[Fig. 16]



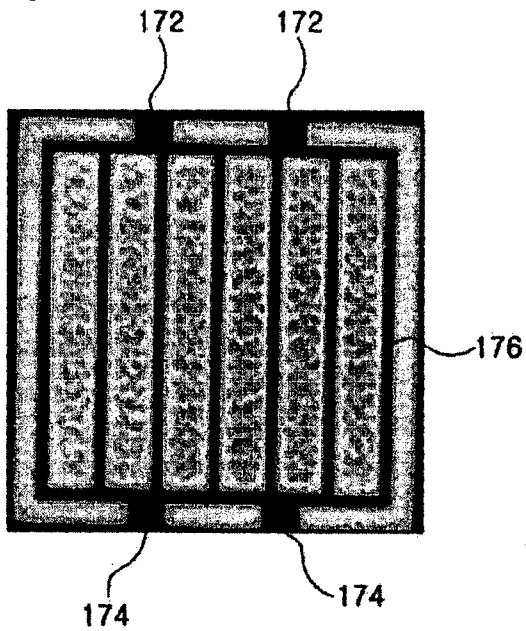
[Fig. 17A]



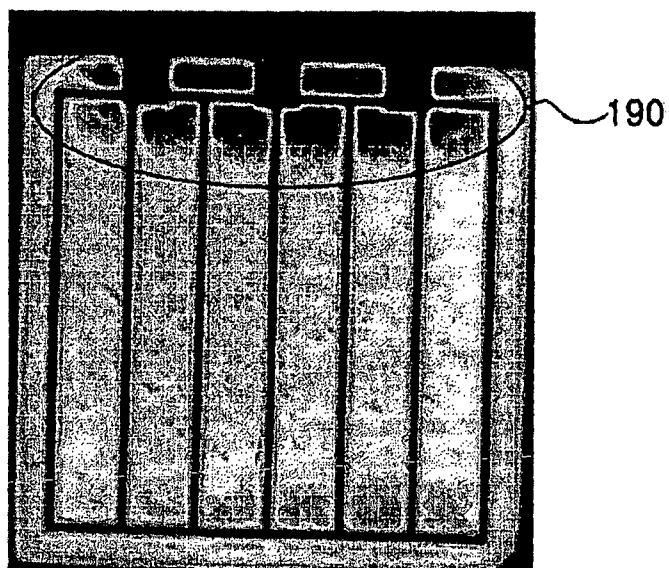
[Fig. 17B]



[Fig. 18A]



[Fig. 18B]



INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR2012/010436**A. CLASSIFICATION OF SUBJECT MATTER****H01L 33/36(2010.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 33/36; H01L 33/00; H01L 33/42; H01L 33/38

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: LED, bonding pad, current distribution pad, extension

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	KR 10-1048912 B1 (THELEDS CO., LTD.) 12 July 2011 See paragraphs [0021], [0026], [0029], claim 1, and figures 1,2.	1-10, 12-14, 21, 22 15-20, 23-31
Y A	KR 10-0665120 B1 (SAMSUNG ELECTRO-MECHANICS CO., LTD.) 09 January 2007 See abstract, pages 4-5, claim 1, and figure 2.	15-20, 23-31 1-10, 12-14, 21, 22
A	KR 10-1012823 B1 (SEMICON LIGHT CO., LTD.) 08 February 2011 See abstract, claim 1, and figure 4b	1-10, 12-31
A	KR 10-2011-0101573 A (LG DISPLAY CO., LTD.) 16 September 2011 See abstract, claim 1, and figure 4.	1-10, 12-31
A	JP 2009-302201 A (TOYODA GOSEI CO., LTD.) 24 December 2009 See abstract, claim 1, and figure 1.	1-10, 12-31

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

27 March 2013 (27.03.2013)

Date of mailing of the international search report

29 March 2013 (29.03.2013)

Name and mailing address of the ISA/KR

Korean Intellectual Property Office
189 Cheongsu-ro, Seo-gu, Daejeon Metropolitan
City, 302-70 1, Republic of Korea

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Authorized officer

PARK, Hye Lyun

Telephone No. 82-42-481-3463



INTERNATIONAL SEARCH REPORT

International application No.

PCT/KR2012/010436

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☒ Claims Nos.: II
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☒ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☒ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☒ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☒ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/KR2012/010436

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
KR 10- 1048912 B1	12 .07 .20 11	None	
KR 10-0665 120 B1	09 .0 1 .2007	JP 2006-245524 A KR 10-2006-0095690 A US 2006-0202227 A1 US 7282741 B2	14. 09 .2006 0 1 .09 .2006 14. 09 .2006 16 . 10 .2007
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JP 2009-30220 1 A	24 .12 .2009	None	