(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
28 March 2019 (28.03.2019)

WIPO | PCT

(10) International Publication Number
WO 2019/057293 A1

(51) International Patent Classification:
G06F 21/86 (2013.01) *H01L 23/00* (2006.01)
G06F 21/79 (2013.01) *H05K 1/02* (2006.01)

(21) International Application Number:
PCT/EP2017/074005

(22) International Filing Date:
22 September 2017 (22.09.2017)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant: **ARCELIK ANONIM SIRKETI** [TR/TR]; E5 Ankara Asfalti Uzeri, Tuzla, 34950 ISTANBUL (TR).

(72) Inventors: **YALCIN, Murat**; E5 Ankara Asflati Uzeri, Tuzla, 34950 ISTANBUL (TR). **CEBECI, Tamer**; E5 Ankara Asfalti Uzeri, Tuzla, 34950 ISTANBUL (TR). **ACAR, Nuri**; E5 Ankara Asfalti Uzeri, Tuzla, 34950 ISTANBUL (TR).

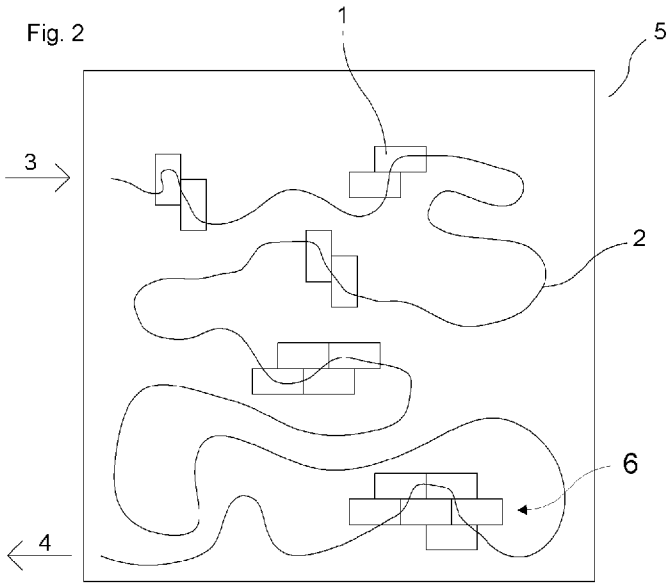
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report (Art. 21(3))*

(54) Title: SYSTEM AND METHOD FOR CONFIGURING AN ELECTROMAGNETIC SECURITY NETWORK FOR MEMORY MODULES OF SALE RECORDING DEVICES

Fig. 2



(57) **Abstract:** The present invention relates to a system and method for designing an electromagnetic security network (5) for memory modules of sale recording devices. The present invention more particularly relates to an electromagnetic security network (5) for detecting and recording any interference to a memory module, said electromagnetic security network (5) comprising openings through which outlet and inlet pins of a memory module processor are attached to signal ends of the electromagnetic security network.

WO 2019/057293 A1

Description

SYSTEM AND METHOD FOR CONFIGURING AN ELECTROMAGNETIC SECURITY NETWORK FOR MEMORY MODULES OF SALE RECORDING DEVICES

[0001] The present invention relates to a system and method for designing an electromagnetic security network for memory modules of sale recording devices.

[0002] It is well-known that one of the components for providing the memory module (MM) of sale recording devices (such as point-of sale (POS) devices) with protection against writing and erasing of data is the electromagnetic security network (ESN). It is necessary for the ESN to be designed in such a random and authentic way that does not contain repetitive structures that can be detected by the naked eye. For this reason, ESN design is a challenging and lengthy process that uses up a lot of resources. Additionally, as ESNs are designed manually, many errors can be made during the design process; which are again cumbersome to detect and correct.

[0003] Put simply, the purpose of the ESN is to detect outside physical and electronic interferences to the MM. In order to achieve this, two lines (two signals) having a thickness of 0.15 mm with a clearance of 0.15 mm therebetween are passed on the ESN. The lines should not be following a pattern that is detectible from the outside. The lines should not be straight over long distances and must contain curves at intervals. It must be ensured that the lines travel in the ESN in as chaotic and random manner as possible to create a complex structure. The physical dimensions of the ESN are determined by the MM and its shape is selected to prevent outside access to the MM.

[0004] When there is outside interference, the ESN is damaged, resulting in two possible scenarios. One possible scenario is that one or both of the signal lines traveling in the ESN are severed, causing an open circuit. In this situation, the signal(s) entering the ESN from the pins at one end of the ESN cannot reach the other end. The other possible scenario is that the signal lines come into contact with each other, causing a short circuit. In

the situation, a signal entering the ESN at one end reached both pins at the other end. Both situations are detected by the processor and recorded onto the MM. In this manner, unauthorized outside interferences to the MM are recorded.

[0005] Among others, a prior art publication in the technical field of the invention may be referred to as WO2005041002, which discloses a device having a circuit board with various exposed components such as an LCD and keys. A circuit is housed within an enclosure formed between the board and a cover. The cover has, on its inside surface, a security track in a dense serpentine pattern. The board has a security track, also in a dense serpentine pattern. The track is linked to covered surface-level tracks. The cover's security track is connected to the board's security tracks via a deformable pad whose conductivity increases with applied compression.

[0006] The present invention, on the other hand, addresses the situation where a modular, complex unit cell structure and its derivatives are used in ESN design. Using said unit cell structure prevents manual design of the ESN which accelerates the design process and prevents unnecessary losses of resources. In addition, as first only one unit cell is designed and only after said unit cell passes the necessary tests the whole of the ESN is designed, errors decrease and security increases. Another advantage is that as the unit cell is modular, even if the physical dimensions of the ESN changes, it would not be necessary to start the ESN design process from scratch. This is especially advantageous for ESNs having large dimensions.

[0007] The present invention provides a system and method for designing an electromagnetic security network for memory modules of sale recording devices, as provided by the characterizing features defined in Claim 1.

[0008] Primary object of the present invention is to provide a system and method for designing an electromagnetic security network for memory modules of sale recording devices using unit cell structures.

[0009] The present invention proposes an electromagnetic security network for a memory module. Said electromagnetic security network comprises a plurality of unit cells with signal inlets and outlets such that a unit cell

group can be organized by unit cells in contact with each other, assembling a number of unit cells with corresponding inlets and outlets in electrical contact with each other. Therefore, said plurality of unit cells and at least one unit cell group in the electromagnetic security network form a signal line between outlet and inlet pins of a memory module processor enclosed by said electromagnetic security network.

[0010] Two subsequent unit cells organized separately or forming part of a unit cell group are connected to each other with respective signal outlets of the first unit cell connected to respective signal inlets of the second unit cell such that one of said first or second unit cells is closer to inlet or outlet pins of the memory module processor on a signal line thereinbetween.

[0011] Accompanying drawings are given solely for the purpose of exemplifying an electromagnetic security network, whose advantages over prior art were outlined above and will be explained in brief hereinafter.

[0012] The drawings are not meant to delimit the scope of protection as identified in the Claims, nor should they be referred to alone in an effort to interpret the scope identified in said Claims without recourse to the technical disclosure in the description of the present invention. The drawings are only exemplary in the sense that they do not necessarily reflect the actual dimensions and relative proportions of the respective components of the system.

[0013] Fig. 1A-C demonstrate schematic diagrams of exemplary unit cell structures according to the present invention.

[0014] Fig. 2 demonstrates a schematic diagram of an electromagnetic security network (ESN) according to the present invention.

[0015] The following numerals are assigned to different part number used in the detailed description:

1. Unit cell
2. Signal line
3. Signal inlet
4. Signal outlet
5. Electromagnetic security network (ESN)
6. Unit cell group

[0016] The present invention proposes an electromagnetic security network ESN (5) serving for the purpose of detecting and recording any interference to a memory module (MM). It is therefore to noted that the ESN (5) is not effective in preventing interferences to the MM by itself.

[0017] According to the present invention, the ESN (5) is preferably configured to avoid obvious repetitions and patterns, empty spaces, and signal lines (2) that are thicker than necessary on the ESN (5) and which is accordingly adapted to be undetected from the outside. For this reason, the signals are configured to travel in the ESN (5) by using thin signal lines (2), in a random fashion and preferably without leaving empty portions.

[0018] To achieve the above-mentioned advantages, the present invention proposes unit cell (1) structures as will be explained hereinafter. The basis when designing a unit cell (1) is that the signals travel in the unit cell (1) in a completely random fashion. The dimensions of unit cell (1) is kept relatively small because large unit cells (1) would appear as a repetition or a pattern on the ESN (5), which would cause security vulnerabilities. On the other hand the dimensions of unit cell (1) cannot be too small; otherwise it would not be possible for the signal lines (2) to travel within unit cell (2) in the random and chaotic manner as desired.

[0019] Additionally, unit cell (1) does not preferably have a definite shape, such as a square or rectangle, which will form a pattern that can easily be detected from the outside. Instead of obvious and common geometric shapes, preferably a design having a structure similar to puzzle or Tetris pieces will prevent detection of a pattern from the outside and allows the unit cells (1) to be compatible with each other.

[0020] Further, the shape of ESN (5) is configured in a way that contains openings through which the pins of the MM can be attached. The structure is completed by attaching the signal ends of the ESN (5) to the processor of the MM. Typically, two signals can enter and two signals can exit the ESN (5); therefore there can be four pins (two inlet and two outlet) in total. The signals sent from the outlet pins of the MM processor enter the ESN (5) through the inlet pins and after travelling in the ESN, the signals exit the ESN through the outlet pins and enter the inlet pins of the MM

processor. In this manner, the ESN (5) is typically periodically electronically monitored.

[0021] According to the present invention, each unit cell (1) comprises signal inlets (3) and signal outlets (4). Unit cells (1) are assembled with each other within the ESN (5) to form a unit cell group (6). A unit cell group (6) comprising at least a first unit cell (1) and at least a second unit cell (1) and preferably a plurality of other isolated unit cells (1) can therefore form a signal line (2) between outlet pins and inlet pins of the MM processor.

[0022] The locations where signal inlets (3) and signal outlets (4) are configured on each unit cell (1) are determined such that two subsequent unit cells (1) in a unit cell group (6) are connected to each other with respective signal outlets (4) of the first unit cell (1) connected to respective signal inlets (3) of the second unit cell (2) to form part of a signal line (2) between outlet pins and inlet pins of the MM processor. To this end, two subsequent unit cells (1) in a unit cell group (6) along the signal line (2) are connected to each other such that one of said first or second unit cells (1) is closer to said outlet pins of the MM processor along said signal line (2) and the other one of said first or second unit cells (1) is closer to inlet pins of the MM processor along said signal line (2).

[0023] According to the present invention, a preferably 90^{o} angle directional change is provided between the directions of signal inlet (3) and signal outlet (4) directly in electrical connection with said MM. This arrangement increases system complexity, and therefore security.

[0024] According to the present invention, all the unit cells (1) in the ESN (5) have the same signal inlet (3) and signal outlet (4) positions as well as internal signal line (2) structures. In order to further increase security, the same unit cell (1) structure and/or one unit cell group (6) structure is used in multiple locations along said signal line (2) in rotated, mirrored, rotated and mirrored or mirrored and rotated images being added to the signal line (2) design. In this case, the places of signal inlet (3) and signal outlet (4) are determined to be compatible with the different versions of unit cell (1). Alternatively, more than one master unit cell (1) structure can be used as shown in Fig. 2. However, a single master unit cell (1) design is more

advantageous for simplicity, without compromising security.

[0025] After the overall configuration is completed, the master unit cell (1) to be used in the ESN (5) is tested before moving on to the design of the ESN (5). In this manner, security is increased, risk is decreased and design flaws are prevented. After the design of the unit cells (1) is finalized, they are used in ESNs (5).

[0026] In order to simplify the design process of ESNs, unit cells (1) are positioned within the ESN (5) in order to fit the maximum amount of unit cells (1). It is noted that if it becomes necessary to make changes in the design, it will be sufficient to add new unit cells (1) to or remove some of the present unit cells (1) from the design. In this context, using unit cells (1) to complete and modify the structure of ESNs (5) accelerates the design process and minimizes possible errors. The ESN (5) is a generally planar structure in the form of a standard PCB with embedded unit cells (1) and unit cell groups (6) typically having copper conductor lines. The finalized ESN (5) is then reshaped to fully enclose the MM in the form of an enclosure.

[0027] In a nutshell, the present invention proposes an electromagnetic security network (5) for detecting and recording any interference to a memory module, said electromagnetic security network (5) comprising openings through which outlet and inlet pins of a memory module processor are attached to signal ends of the electromagnetic security network.

[0028] In one embodiment of the present invention, said electromagnetic security network (5) comprises a plurality of unit cells (1), each one having at least one signal inlet (3) and at least one signal outlet (4).

[0029] In a further embodiment of the present invention, said electromagnetic security network (5) comprises at least one unit cell group (6) comprising at least a first unit cell (1) and at least a second unit cell (1) assembled with each other within said electromagnetic security network (5).

[0030] In a further embodiment of the present invention, said plurality of unit cells (1) and at least one unit cell group (6) form a signal line (2) between the outlet and inlet pins of said memory module processor.

[0031] In a further embodiment of the present invention, each unit cell (1) is

structurally configured in the form of a puzzle or Tetris piece.

[0032] In a further embodiment of the present invention, locations where signal inlets (3) and signal outlets (4) are configured on each unit cell (1) are determined such that two subsequent unit cells (1) in a unit cell group (6) are connected to each other with respective signal outlets (4) of the first unit cell (1) connected to respective signal inlets (3) of the second unit cell (2) to form a signal line (2) between outlet pins and inlet pins of the MM processor.

[0033] In a further embodiment of the present invention, two subsequent unit cells (1) in a unit cell group (6) along the signal line (2) are connected to each other such that one of said first or second unit cells (1) is closer to said outlet pins of the memory module processor along said signal line (2) and the other one of said first or second unit cells (1) is closer to inlet pins of the memory module processor along said signal line (2).

[0034] In a further embodiment of the present invention, a directional change is provided between the directions of signal inlet (3) and signal outlet (4) of the electromagnetic security network (5) forming signal ends thereof directly in electrical connection with said memory module processor.

[0035] In a further embodiment of the present invention, all the unit cells (1) in the electromagnetic security network (5) have the same signal inlet (3) and signal outlet (4) positions as well as internal signal line (2) structures.

[0036] In a further embodiment of the present invention, the same unit cell (1) structure and/or one unit cell group (6) structure is added to the signal line (2) configuration in multiple locations along said signal line (2) in rotated, mirrored, rotated and mirrored or mirrored and rotated images.

[0037] Therefore, the present invention is devised under the recognition that a complex unit cell structure can be created using a modular master unit cell (1) and its derivatives in the ESN (5) design. Such an ESN (5) design prevents manual design and accelerates the process by preventing unnecessary losses of resources. The ESN (5) is priorly known to comply with security requirements and the final product can be swiftly redesigned and adapted to different product generations with specific size requirements due to use of modular units.

Claims

1. An electromagnetic security network (5) for detecting and recording any interference to a memory module, said electromagnetic security network (5) comprising openings through which outlet and inlet pins of a memory module processor are attached to signal ends of the electromagnetic security network **characterized in that**;

   said electromagnetic security network (5) comprises a plurality of unit cells (1), each one having at least one signal inlet (3) and at least one signal outlet (4), said electromagnetic security network (5) comprises at least one unit cell group (6) comprising at least a first unit cell (1) and at least a second unit cell (1) assembled with each other within said electromagnetic security network (5), said plurality of unit cells (1) and at least one unit cell group (6) form a signal line (2) between the outlet and inlet pins of said memory module processor.
2. An electromagnetic security network (5) as in Claim 1, **characterized in that** each unit cell (1) is structurally configured in the form of a puzzle or Tetris piece.
3. An electromagnetic security network (5) as in Claim 1 or 2, **characterized in that** locations where signal inlets (3) and signal outlets (4) are configured on each unit cell (1) are determined such that two subsequent unit cells (1) in a unit cell group (6) are connected to each other with respective signal outlets (4) of the first unit cell (1) connected to respective signal inlets (3) of the second unit cell (2) to form a signal line (2) portion between outlet pins and inlet pins of the memory module processor.
4. An electromagnetic security network (5) as in Claim 3, **characterized in that** two subsequent unit cells (1) in a unit cell group (6) along the signal line (2) are connected to each other such that one of said first or second unit cells (1) is closer to said outlet pins of the memory module processor along said signal line (2) and the other one of said first or second unit cells (1) is closer to inlet pins of the memory module processor along said signal line (2).
5. An electromagnetic security network (5) as in Claim 1, **characterized in that** a directional change is provided between the directions of signal inlet (3) and signal outlet (4) of the electromagnetic security network (5) forming signal ends thereof directly in electrical connection with said memory module processor.

6. An electromagnetic security network (5) as any preceding Claim, **characterized in that** all the unit cells (1) in the electromagnetic security network (5) have the same signal inlet (3) and signal outlet (4) positions as well as internal signal line (2) structures.
7. An electromagnetic security network (5) as in Claim 6, **characterized in that** the same unit cell (1) structure and/or one unit cell group (6) structure is added to the signal line (2) configuration in multiple locations along said signal line (2) in the form of rotated, mirrored, rotated and mirrored or mirrored and rotated images.

Fig. 1A

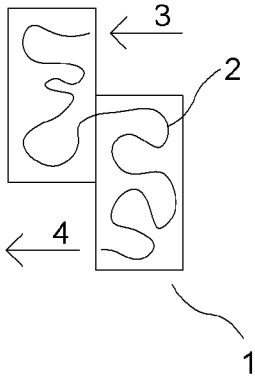


Fig. 1B

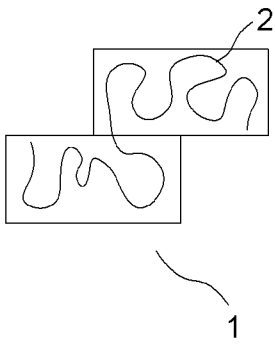


Fig. 1C

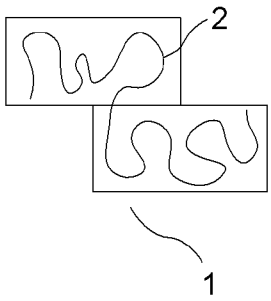
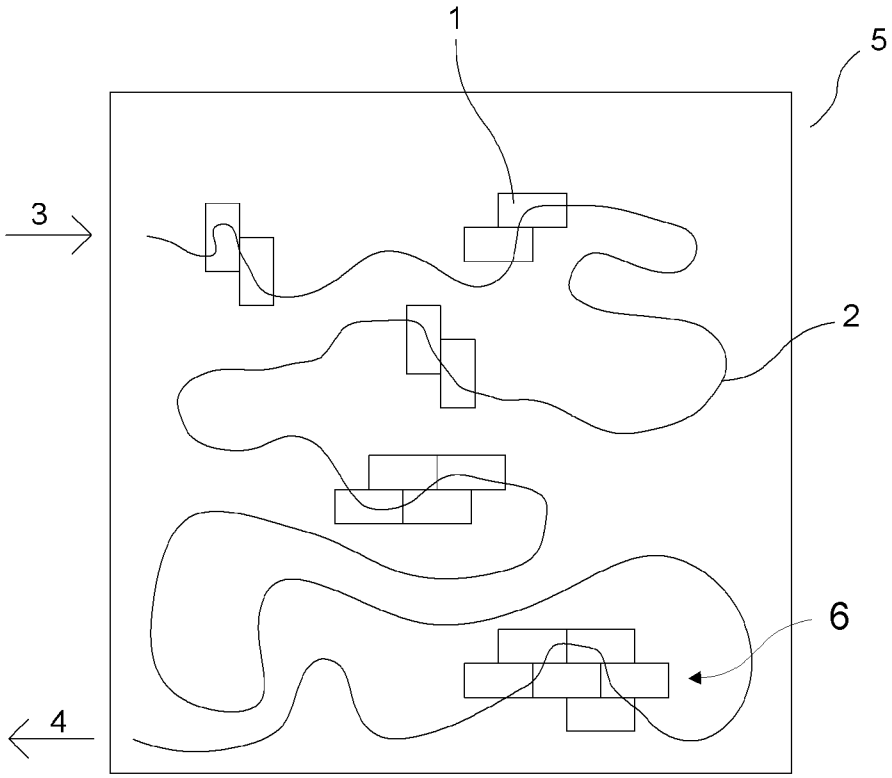


Fig. 2



INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2017/074005

A. CLASSIFICATION OF SUBJECT MATTER
INV. G06F21/86 G06F21/79 H01L23/00 H05K1/02
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06F H01L H05K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2008/036598 A1 (OGGIONI STEFANO S [IT]) 14 February 2008 (2008-02-14) paragraphs [0002], [0013], [0022] - [0027], [0052], [0056] - [0062], [0066], [0074], [0077], [0079], [0094] - [0095]; figures 3-11	1-7
X	EP 3 188 073 A1 (THALES SA [FR]) 5 July 2017 (2017-07-05) paragraphs [0001], [0005], [0011], [0018] - [0019], [0022] - [0023], [0028] - [0035] figures 2, 3, 5-10	1-7

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
23 May 2018	01/06/2018

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Volpato, Gian Luca

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2017/074005

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2008036598 A1	14-02-2008	NONE	
EP 3188073 A1	05-07-2017	EP 3188073 A1	05-07-2017
		FR 3046480 A1	07-07-2017
		SG 10201610911W A	28-07-2017