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Tomisawa et al.

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[54] **ELECTRONIC MUSICAL INSTRUMENT WITH KEY CODING IN A KEY ADDRESS MEMORY**

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[51] **Int. Cl.** **G10h 1/02,** G10h 5/02

[58] **Field of Search** 84/1.01, 1.03, 1.13, 1.24, 84/1.26; 340/172.5

[56] **References Cited**

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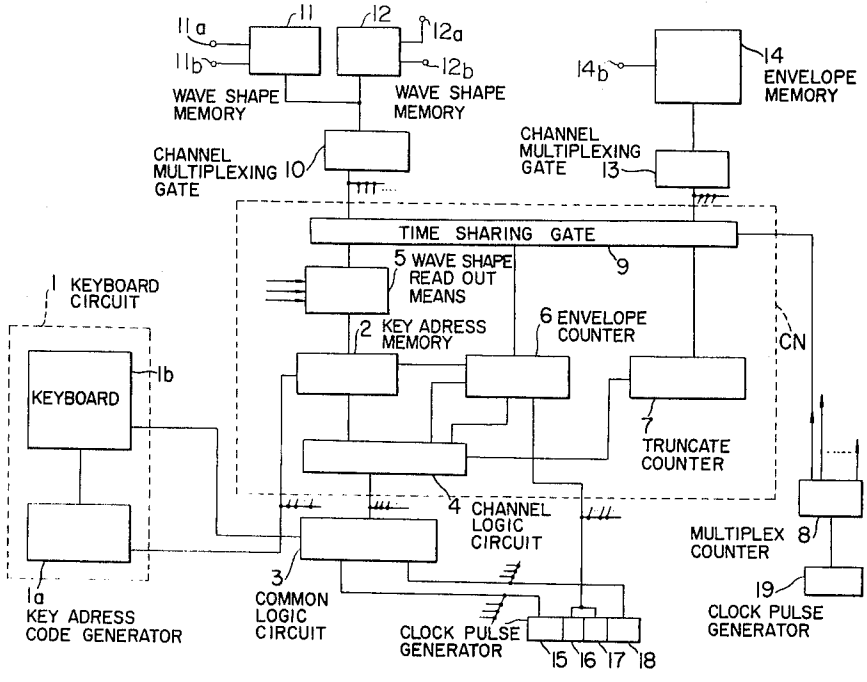
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Assistant Examiner—Stanley J. Witkowski
Attorney, Agent, or Firm—Ladas, Parry, Von Gehr, Goldsmith & Deschamps

[57] **ABSTRACT**

In an electronic musical instrument, an actuation of a key switch produces a key address code corresponding to the key switch. This key address code is stored in a key address memory. A tone clock pulse corresponding to the key address code is selected from among a plurality of tone clock pulses. A musical tone wave shape memory stores in analog a wave shape to be reproduced. The musical tone wave shape is read from this wave shape memory at a reading rate corresponding to the tone clock thus selected. Attack and decay of the musical tone wave shape envelope are stored in analog in an envelope memory. When the key address code is stored by the actuation of the key switch, a clock pulse is selected to read out the attack wave shape portion at a reading rate corresponding to this clock pulse. When the key switch is cut off, another clock pulse is selected to read out the decay wave shape portion at a reading rate corresponding thereto. The read out output of the envelope memory is applied to the voltage control terminal of the musical tone wave shape memory thereby causing the musical tone wave shape memory to produce from the output thereof a musical tone wave shape with the desired envelope.

19 Claims, 18 Drawing Figures



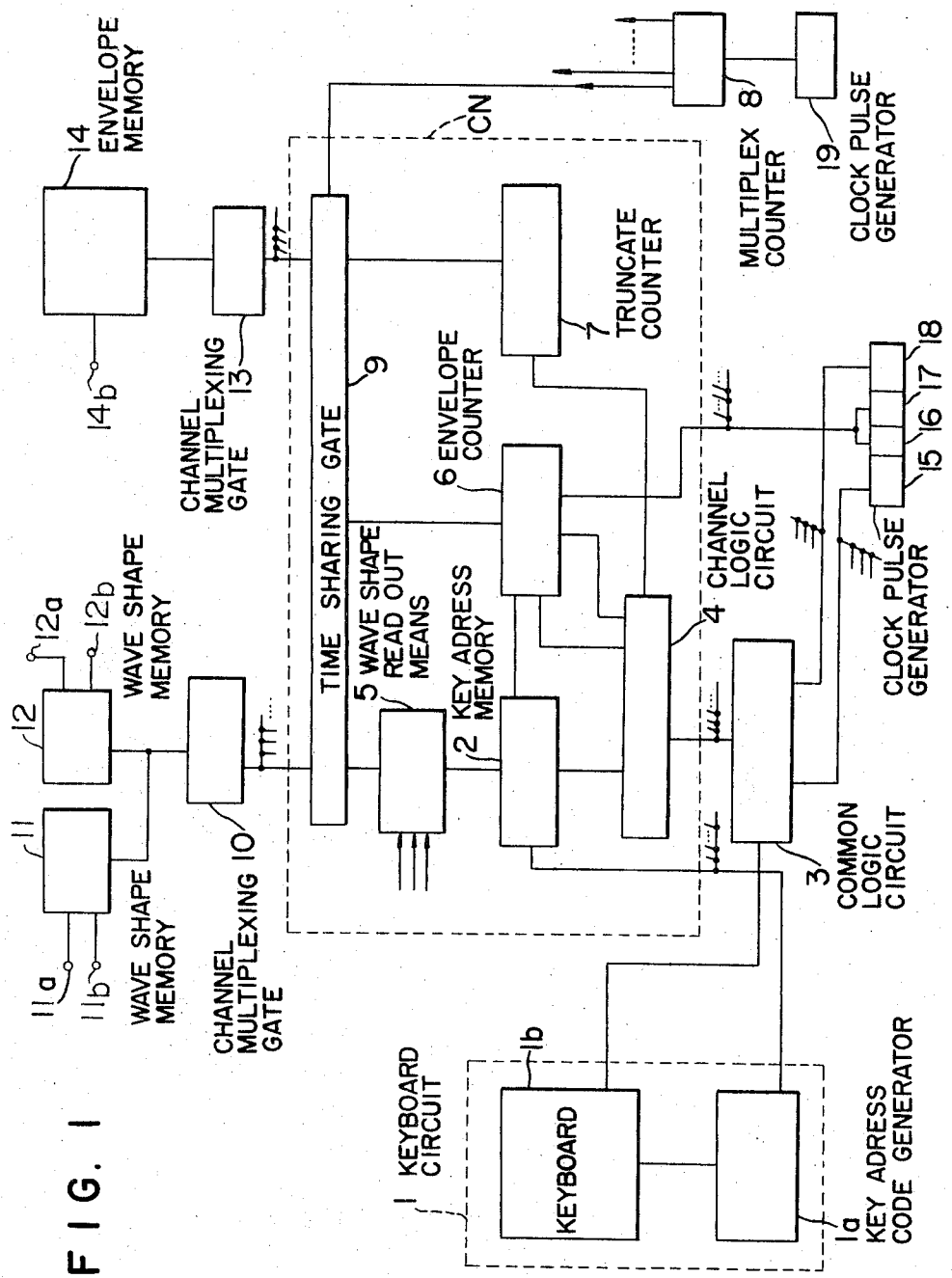
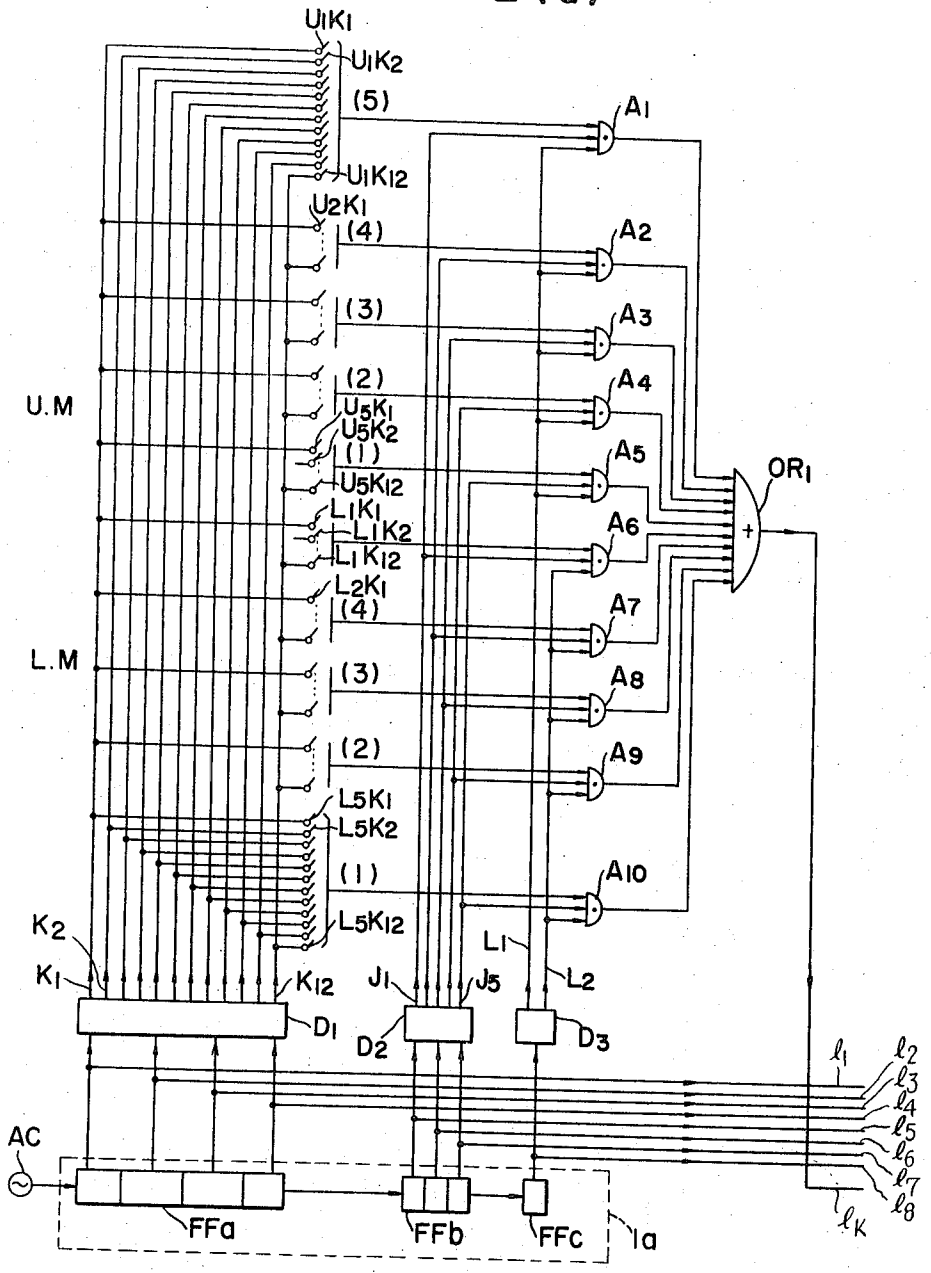

1 KEYBOARD CIRCUIT
1a KEY ADRESS CODE GENERATOR
1b KEYBOARD
2 KEY ADRESS MEMORY
3 COMMON LOGIC CIRCUIT
4 CHANNEL LOGIC CIRCUIT
5 WAVE SHAPE READ OUT MEANS
6 ENVELOPE COUNTER
7 TRUNCATE COUNTER
8 MULTIPLEX COUNTER
9 TIME SHARING GATE
10 CHANNEL MULTIPLEXING GATE
11 WAVE SHAPE MEMORY
11a
11b
12 WAVE SHAPE MEMORY
12a
12b
13 CHANNEL MULTIPLEXING GATE
14 ENVELOPE MEMORY
14b
15
16
17
18
19 CLOCK PULSE GENERATOR
CLOCK PULSE GENERATOR
CN

FIG. 1

FIG. 2(a)


U1K1
U1K2
(5)
U1K12
U2K1
(4)
(3)
(2)
U5K1
U5K2
(1)
U5K12
L1K1
L1K2
L1K12
L2K1
(4)
(3)
(2)
L5K1
L5K2
(1)
L5K12
U.M
L.M
K2
K1
K12
J1
J5
L1
L2
D1
D2
D3
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
OR1
AC
FFa
FFb
FFc
1a
ℓ1
ℓ2
ℓ3
ℓ4
ℓ5
ℓ6
ℓ7
ℓ8
ℓK

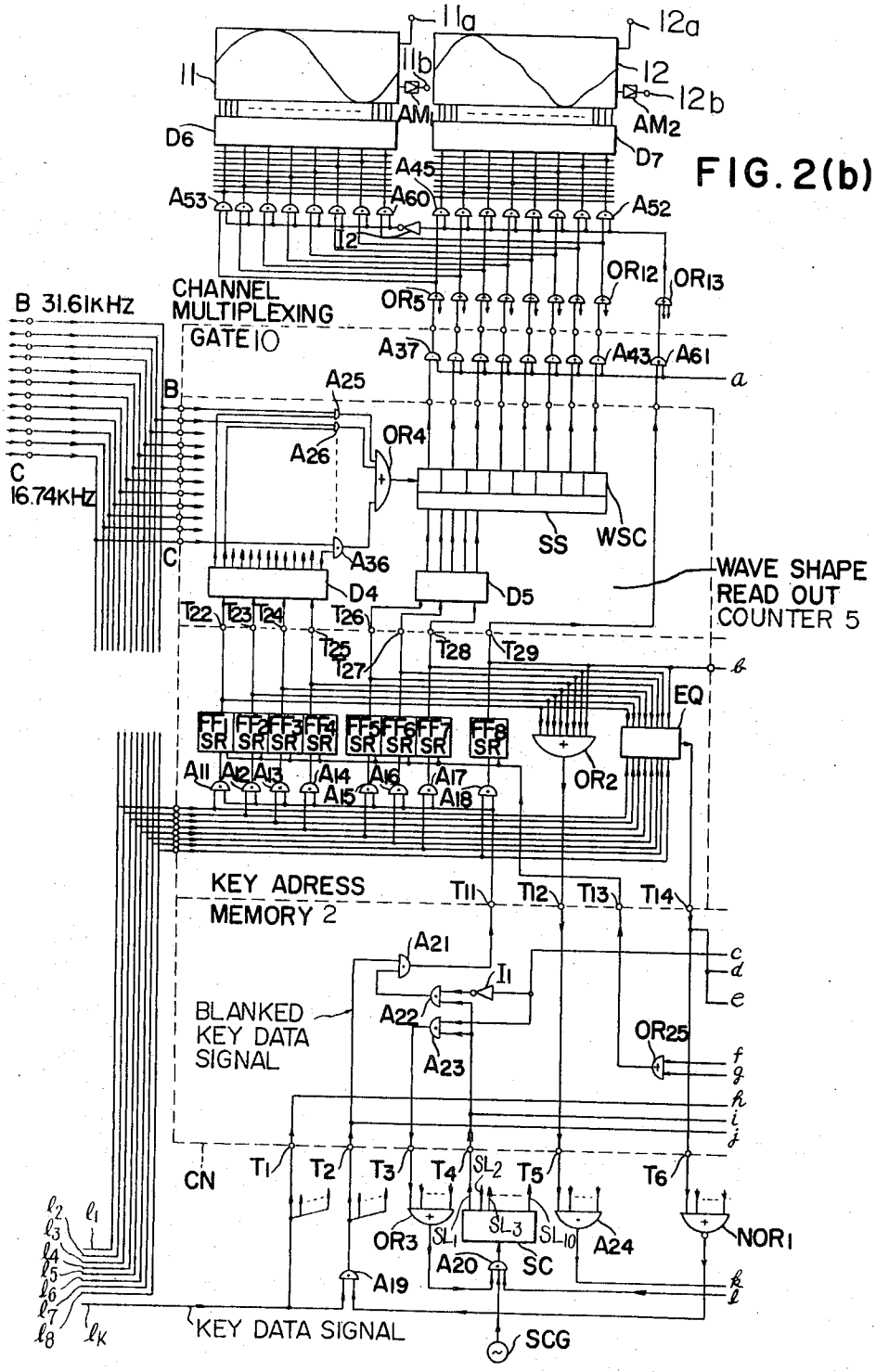

11a
12a
11b
12
12b
11
AM1
AM2
D6
D7
A45
A53
A60
A52
OR12
OR13
CHANNEL MULTIPLEXING GATE 10
B 31.61KHz
OR5
A37
A43
A61
a
B
A25
OR4
A26
C
16.74KHz
SS
WSC
C
A36
WAVE SHAPE READ OUT COUNTER 5
D4
D5
T22
T23
T24
T26
T25
T27
T28
T29
b
EQ
FF1 SR
FF2 SR
FF3 SR
FF4 SR
FF5 SR
FF6 SR
FF7 SR
FF8 SR
A11
A12
A13
A14
A15
A16
A17
A18
OR2
KEY ADRESS MEMORY 2
T11
T12
T13
T14
A21
I1
c
d
e
BLANKED KEY DATA SIGNAL
A22
A23
OR25
f
g
h
i
j
CN
T1
T2
T3
T4
SL2
T5
T6
OR3
SL1
SL3
SL10
A24
NOR1
A20
SC
A19
k
l
KEY DATA SIGNAL
SCG

FIG. 2(b)

FIG. 2(c)

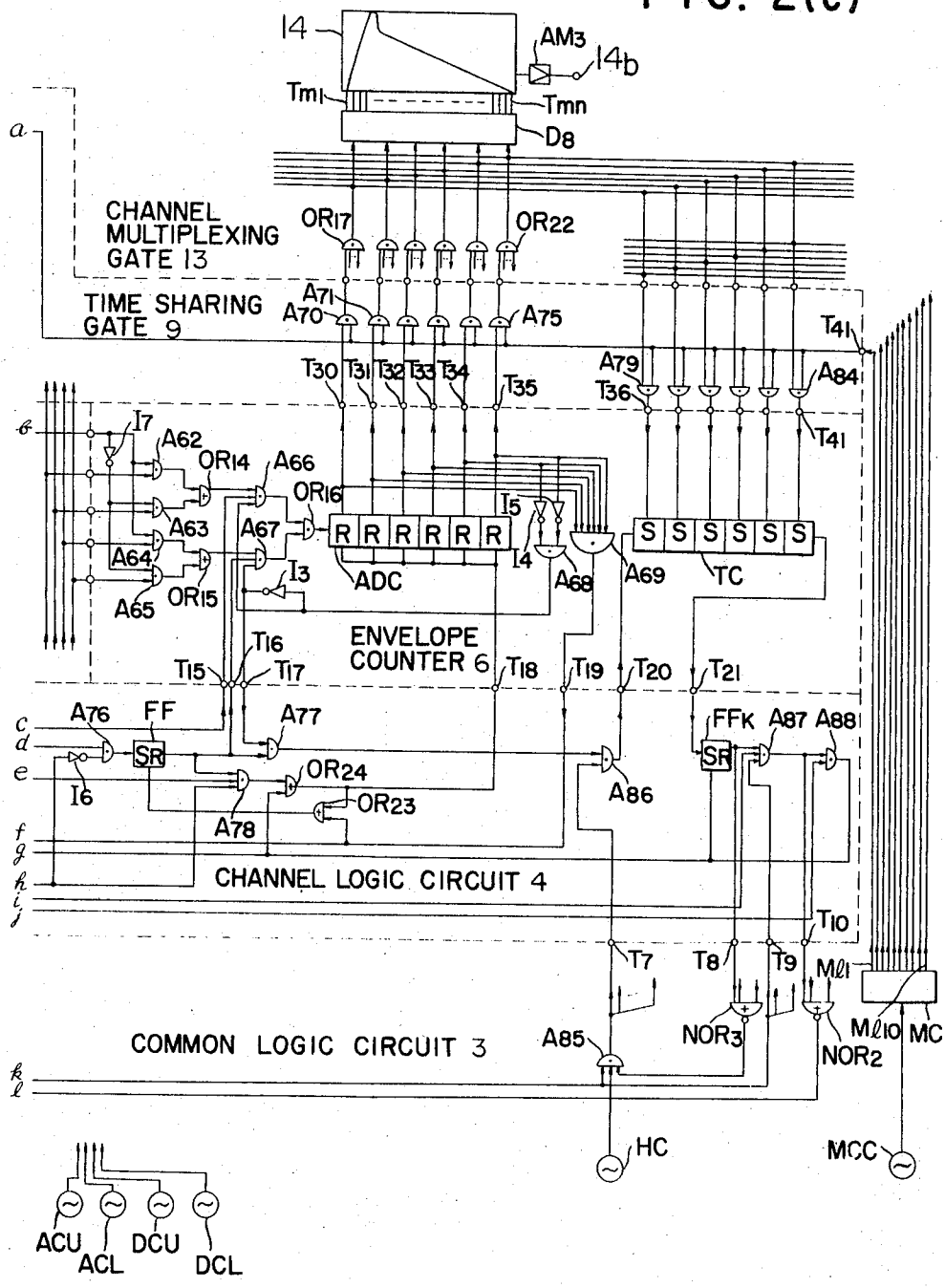

14
AM3
14b
Tm1
Tmn
D8
a
CHANNEL MULTIPLEXING GATE 13
OR17
OR22
TIME SHARING GATE 9
A71
A70
A75
T41
T30 T31 T32 T33 T34
T35
A79
T36
A84
T41
b
I7
A62
OR14
A66
OR16
A63
A67
A64
OR15
A65
I3
R R R R R R
ADC
I5
I4
A68
A69
S S S S S S
TC
ENVELOPE COUNTER 6
T15
T16
T17
T18
T19
T20
T21
c
d
e
A76
FF
SR
I6
A77
OR24
OR23
A78
A86
FFK
A87
A88
SR
f
g
h
i
j
CHANNEL LOGIC CIRCUIT 4
T10
T7
T8
T9
Mℓ1
COMMON LOGIC CIRCUIT 3
A85
NOR3
NOR2
Mℓ10
MC
k
ℓ
HC
MCC
ACU
ACL
DCU
DCL

FIG. 3(a)

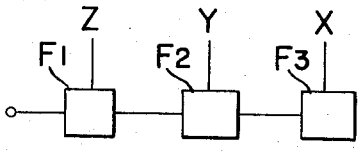


FIG. 3(b)

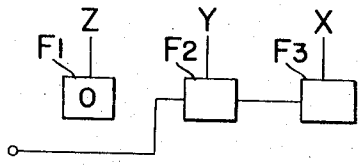


FIG. 3(c)

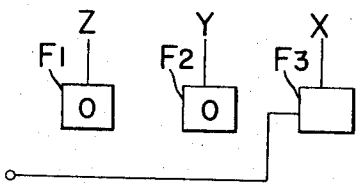


FIG. 5

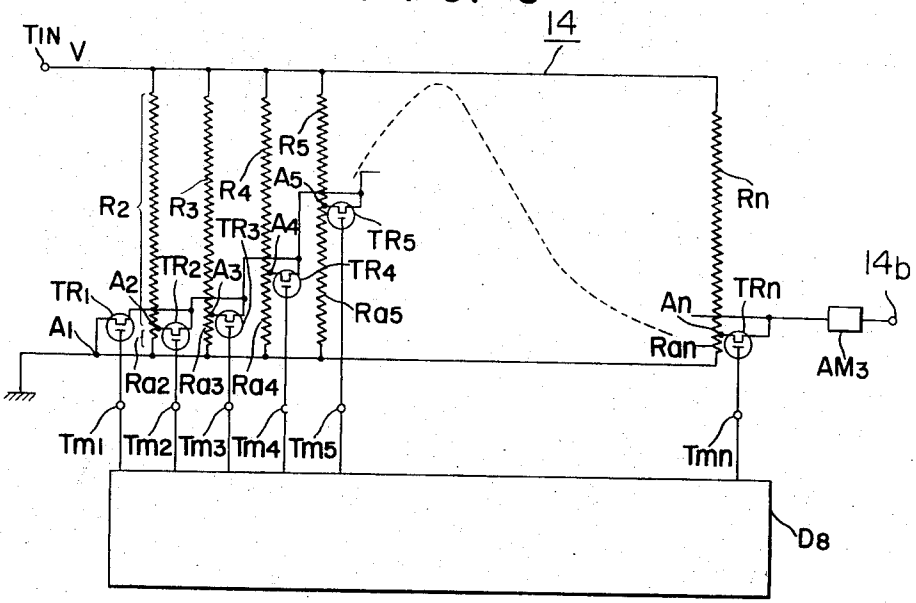


FIG. 4

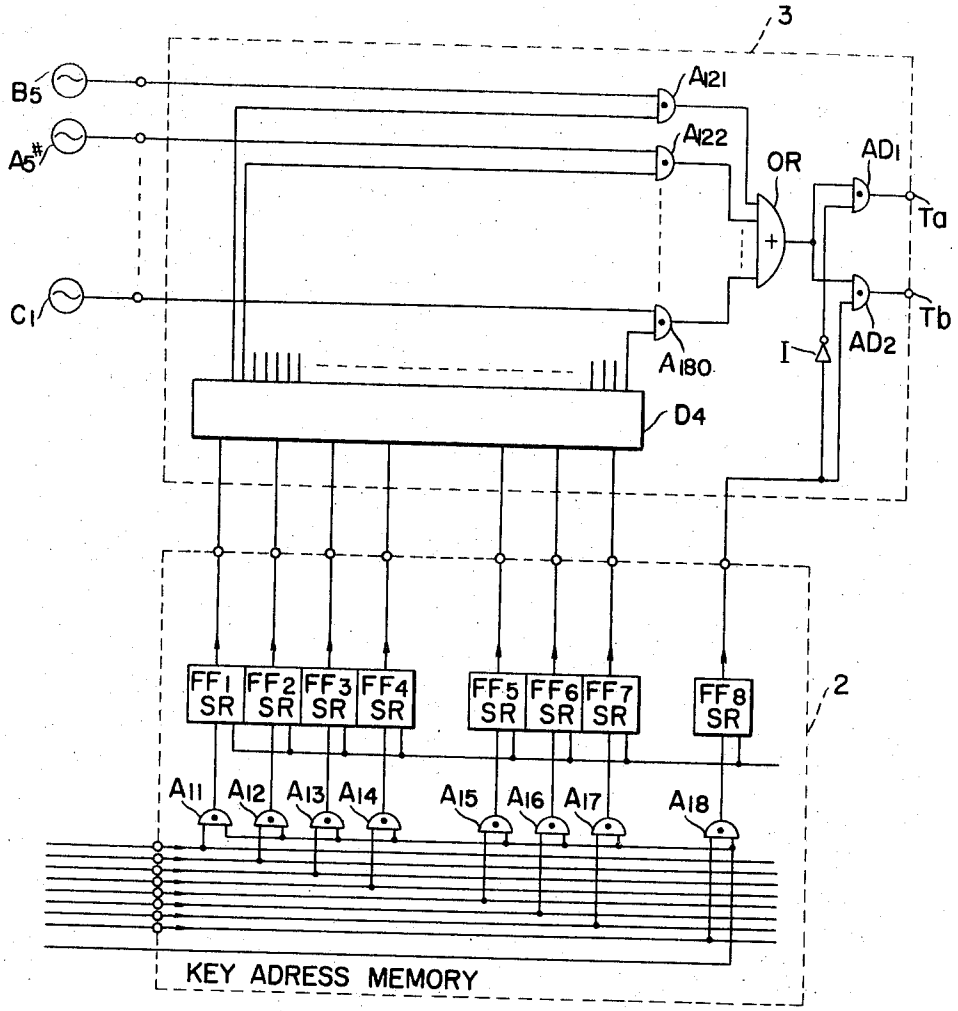

3
B5
A5*
C1
A121
A122
A180
OR
AD1
AD2
Ta
Tb
I
D4
FF1 SR
FF2 SR
FF3 SR
FF4 SR
FF5 SR
FF6 SR
FF7 SR
FF8 SR
2
A11
A12
A13
A14
A15
A16
A17
A18
KEY ADRESS MEMORY

FIG. 6

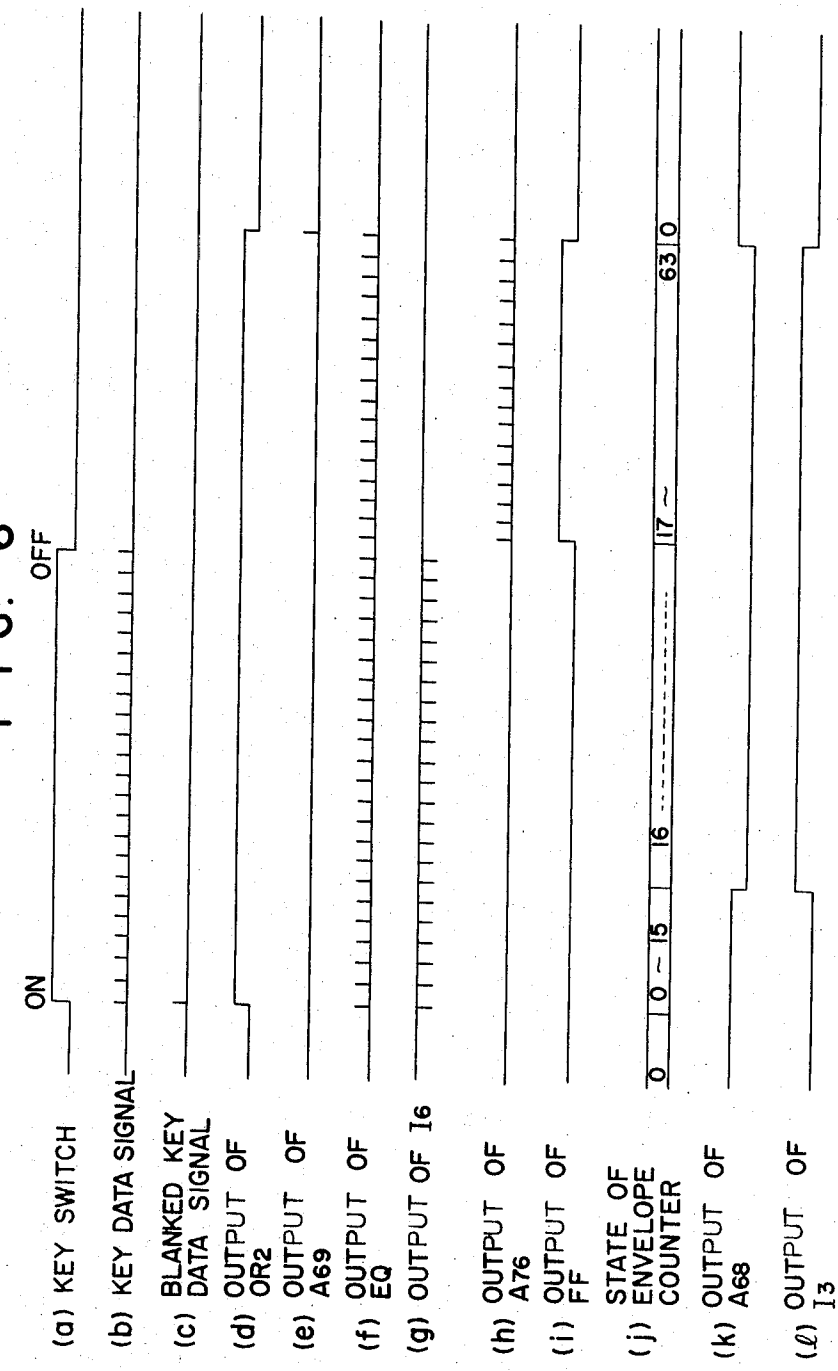

ON
OFF
(a) KEY SWITCH
(b) KEY DATA SIGNAL
(c) BLANKED KEY DATA SIGNAL
(d) OUTPUT OF OR2
(e) OUTPUT OF A69
(f) OUTPUT OF EQ
(g) OUTPUT OF I6
(h) OUTPUT OF A76
(i) OUTPUT OF FF
(j) STATE OF ENVELOPE COUNTER
0
0 ~ 15
16
17 ~
63
0
(k) OUTPUT OF A68
(ℓ) OUTPUT OF I3

FIG. 7

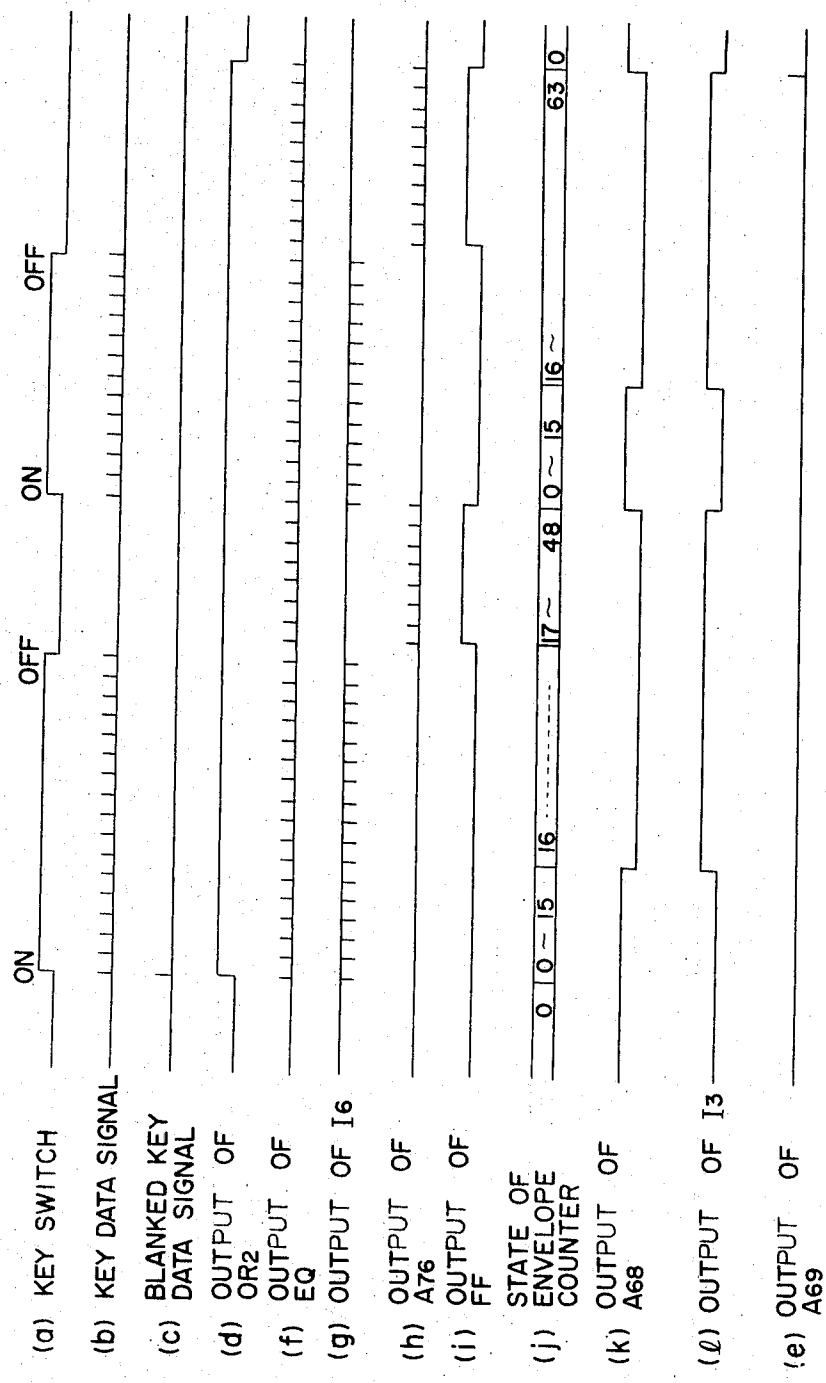

ON
OFF
ON
OFF
(a) KEY SWITCH
(b) KEY DATA SIGNAL
(c) BLANKED KEY DATA SIGNAL
(d) OUTPUT OF OR2
(f) OUTPUT OF EQ
(g) OUTPUT OF I6
(h) OUTPUT OF A76
(i) OUTPUT OF FF
(j) STATE OF ENVELOPE COUNTER
0 | 0 ~ 15 | 16 ..... | 17 ~ 48 | 0 ~ 15 | 16 ~ | 63 | 0
(k) OUTPUT OF A68
(ℓ) OUTPUT OF I3
(e) OUTPUT OF A69

FIG. 8

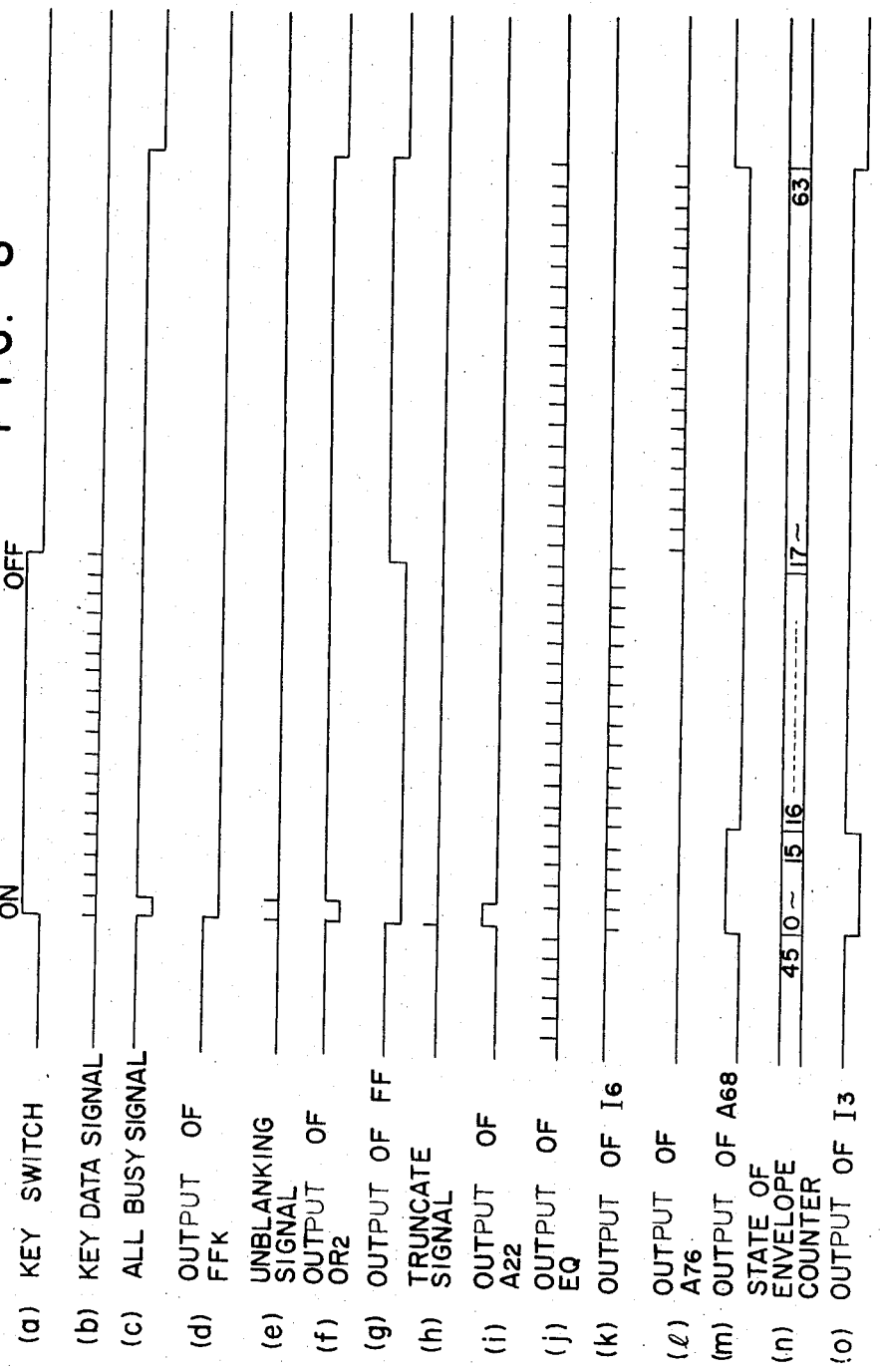

(a) KEY SWITCH
ON
OFF
(b) KEY DATA SIGNAL
(c) ALL BUSY SIGNAL
(d) OUTPUT OF FFK
(e) UNBLANKING SIGNAL
(f) OUTPUT OF OR2
(g) OUTPUT OF FF
(h) TRUNCATE SIGNAL
(i) OUTPUT OF A22
(j) OUTPUT OF EQ
(k) OUTPUT OF I6
(ℓ) OUTPUT OF A76
(m) OUTPUT OF A68
(n) STATE OF ENVELOPE COUNTER
45
0 ~ 15
16 ---- 17 ~ 63
(o) OUTPUT OF I3

FIG. 9

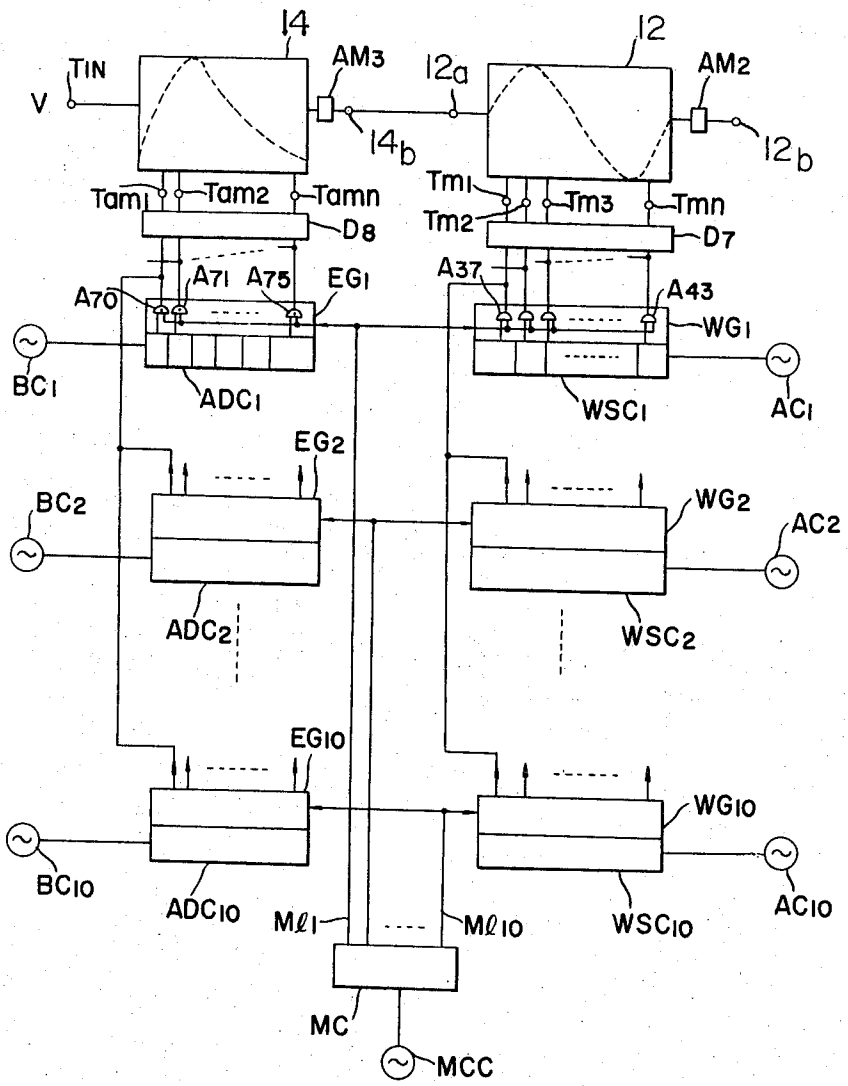

14
12
TIN
V
AM3
12a
AM2
14b
12b
Tam1
Tam2
Tamn
D8
Tm1
Tm2
Tm3
Tmn
D7
A71
A75
EG1
A70
A37
A43
WG1
BC1
ADC1
WSC1
AC1
EG2
BC2
WG2
AC2
ADC2
WSC2
EG10
WG10
BC10
ADC10
Mℓ1
Mℓ10
WSC10
AC10
MC
MCC

FIG. 10(a)

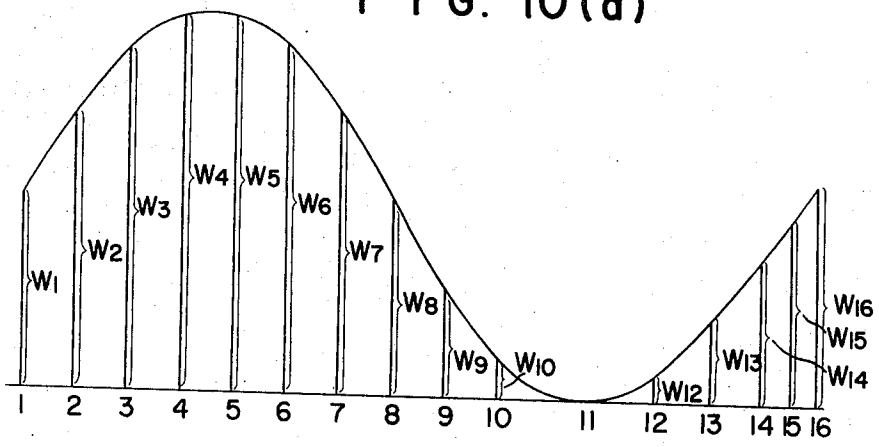


FIG. 10(b)

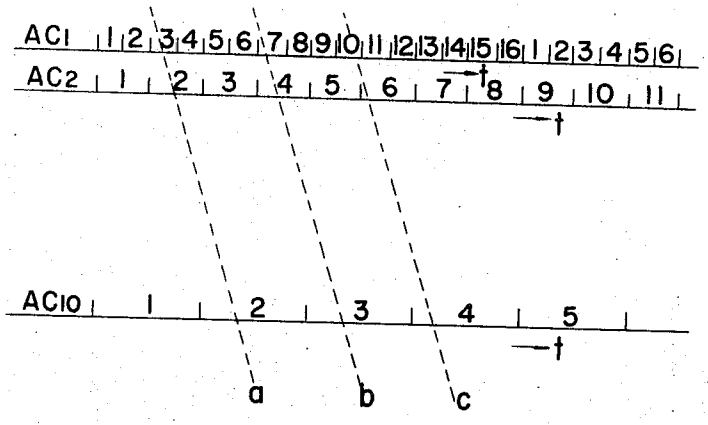


FIG. 11(a)

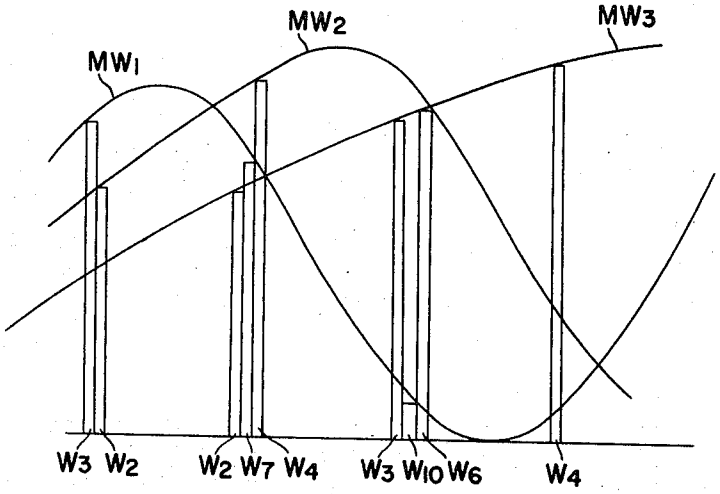


FIG. 11(b)

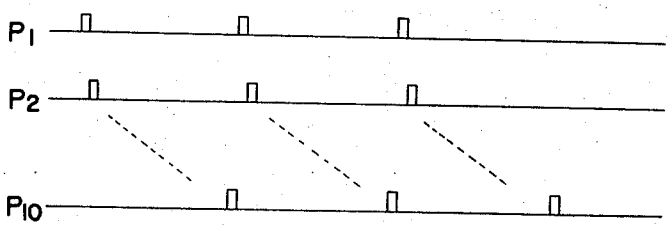
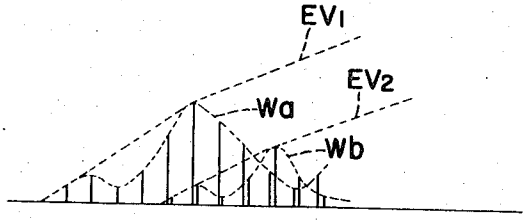


FIG. 12



ELECTRONIC MUSICAL INSTRUMENT WITH KEY CODING IN A KEY ADDRESS MEMORY

This invention relates to an electronic musical instrument and, more particularly, to an electronic musical instrument capable of producing a musical tone signal corresponding to an address code which is produced by depression of a selected key.

Electronic musical instruments of conventional types employ a plurality of oscillators or frequency dividers for providing sound source signals from their outputs. These sound source signals are supplied to a tone-color circuit through key switches by closing thereof, whereupon desired musical tone signals are obtained. The prior art electronic musical instruments therefore require a large number of oscillators or frequency dividers. Besides, the tone-color circuit has an extremely complicated construction. As a result, the musical instrument generally has a complicated and large system for producing required musical tone signals.

Moreover, it was impossible in the prior art electronic musical instruments to obtain musical tone signals having the same wave shapes as those of natural musical instruments. The musical tones reproduced from the prior art electronic musical instruments therefore only had resemblance to natural musical tones to a degree which is far from being satisfactory.

The prior art electronic musical instruments require a large amount of electrical wiring because each tone generator and key switch need to be connected to each other. Besides, the arrangement by which the sound source signals are obtained through the key switches is subject to the occurrence of switch chatterings and key clicks caused by making and breaking of the key switches.

Again, in the prior art electronic musical instruments, an envelope of a musical tone signal which determines the rise of the musical tone when a selected key is depressed, sustain of the tone and attenuation of the tone after the key is released has been provided by a switching circuit utilizing charging and discharging characteristics of a capacitor.

A musical tone signal having a predetermined envelope has thus been obtained from the output terminal of the switching circuit by applying thereto a signal having a predetermined amplitude and operating a switch provided in the charging and discharging circuit in response to the operation of a key switch.

However, the above described device which utilizes charging and discharging characteristics of a capacitor for obtaining a musical tone signal is incapable of producing a complicated envelope of a natural musical tone which, for example, rises abruptly, then falls somewhat rapidly to a certain level and maintains this level for a certain length of time and falls gradually thereafter. The envelope characteristic of the musical tone signal obtained by the above described prior art system is at best a rough simulation of that of a natural musical tone. Further, the prior art system is incapable of changing at will the time length of the rise portion of the envelope which is formed immediately after depression of a key (hereinafter referred to as "attack") and that of the fall portion which is formed after releasing of the key (hereinafter referred to as "decay").

According to the present invention, an electronic musical instrument for obtaining a musical tone which is equivalent to a musical tone of a natural musical instrument or a musical tone having any desired wave shape is disclosed. The invention utilizes a wave shape memory which stores in an analog form the wave shape of a desired musical tone to be reproduced as well as an envelope memory which stores in an analog form the attack and decay shapes of the musical tone to be reproduced.

For generating a musical tone, a selected manual or pedal key is depressed. When the key is depressed, a key data signal is produced if a key address code provided from a key address code generator is one which corresponds to the depressed key. Controlled by this key data signal, the key address code corresponding to the depressed key is stored in a key address code memory. A tone clock pulse is thereby selected to operate a wave shape readout counter which reads out the wave shape from the wave shape memory at the clock rate of the tone clock pulse. Simultaneously, an envelope counter is operated by another selected clock pulse to read out a desired envelope from the envelope memory at the clock rate of the selected clock pulse. The output of the envelope memory is applied to a voltage control terminal of the wave shape memory whereby the desired musical tone wave shape accompanied by the desired envelope is read from the wave shape memory.

If two or more keys are simultaneously depressed, key address codes each corresponding to the respective depressed keys are stored in separate key address code memories to operate the respective wave shape readout counters. The outputs of the respective counters are applied in a time-sharing manner to the wave shape memories to read out a plurality of wave shapes. Simultaneously, each of the envelope counters provided in correspondence to the respective key address memories is operated to supply its output in a time-sharing manner to each of the envelope memories for producing a plurality of envelope wave shapes. Thus, a plurality of musical tones are produced at one time.

In order to effect time control of attack and decay, the counting speed of the envelope counter is varied by selecting a clock pulse in accordance with the contents of a key address code stored in the key address memory.

If a new key is depressed while the maximum number of musical tones to be reproduced at a time are being reproduced, the musical tone which has been attenuated to the greatest degree is cancelled and the musical tone corresponding to the new key is reproduced.

It is therefore a general object of the invention to provide an electronic musical instrument which is capable of producing musical tones of various musical notes.

It is another object of the invention to provide an electronic musical instrument which is capable of producing a musical tone of a desired tone-color and note with a desired envelope by storing the wave shape of the musical tone and that of the envelope in an analog manner, reading out the wave shape of the musical tone periodically and simultaneously reading out the wave shape of the envelope and multiplying it with the wave shape of the musical tone.

It is another object of the invention to provide an electronic organ in which a key address code corresponding to a manual or pedal key is produced and the wave shape of a musical tone is read out from a memory at a clock speed corresponding to the key address code.

It is another object of the invention to provide an electronic musical instrument capable of producing a musical tone which is free from switch chatterings and key clicks by selectively controlling a clock pulse for reading out the stored wave shape of the musical tone by means of a key address code.

It is another object of the invention to provide an electronic musical instrument capable of simultaneously producing a plurality of musical tones which differ from each other.

It is another object of the invention to provide an electronic musical instrument in which a key address code memory is provided in each of a plurality of channels and a new key address code which is different from codes already stored is stored in a not-busy channel whereby the memory can operate effectively.

It is another object of the invention to provide an electronic musical instrument wherein when a new key is depressed while the maximum number of musical tones to be reproduced at a time are being produced, one of the musical tones which has been attenuated to the greatest degree is cancelled and the new musical tone corresponding to the depressed key is produced.

It is another object of the invention to provide an electronic musical instrument which is capable of reading out a wave shape of a complicated envelope from a memory by a single counter and controlling the time lengths of the attack and decay wave shape portions.

It is another object of the invention to provide an electronic musical instrument which is capable of accomplishing, in a time-sharing manner, a multiplexed readout of a plurality of musical tone wave shapes having frequencies different from each other from a single wave shape memory.

It is still another object of the invention to provide an electronic musical instrument which is capable of effecting a time-sharing multiplexed readout from an envelope memory and a musical tone wave shape memory which are in synchronization with each other and thereby producing a plurality of musical tones with a desired envelope.

These and other objects and features of the invention will become apparent from the description made hereinbelow with reference to the accompanying drawings in which:

FIG. **1** is a simplified block diagram showing one embodiment of the electronic musical instrument according to the invention: FIGS. **2** (*a*) (*b*) and (*c*) are circuit diagrams showing in detail the construction of each part of the system. Only one channel among a plurality of channels of the same construction is illustrated in the figure. Lines designated by reference characters a through *l* in FIG. **2**(*b*) continue to lines designated by the same reference characters in FIG. **2**(*c*); FIGS. **3** (*a*) (*b*) and (*c*) are respectively block diagrams showing a principle of operation of a counter WSC and a switch SS; FIG. **4** is a circuit diagram of a modified example of the circuit for selecting one tone clock pulse from among a plurality of tone clock pulses in response to a key address code stored in the key address memory; FIG. **5** is a circuit diagram showing the construction of the envelope memory; FIGS. **6** (*a*) through (*e*) depict wave shapes of signals appearing in some parts of the circuit shown in FIG. **2** when a selected key is depressed; FIGS. **7** (*a*) through **7** (*e*) depict wave shapes of signals appearing in the same parts of the circuit as shown in FIGS. **6** (*a*) through (*e*) when the same key as the one corresponding to a decaying musical tone is depressed again; FIGS. **8** (*a*) through (*o*) depict wave shapes of signals appearing in some parts of the circuit shown in FIG. **2** when the eleventh key is depressed while the ten musical tones are being reproduced and the channel CN_1 is in a state of decay; FIG. **9** is a block diagram showing pertinent parts only in FIG. **2** for explaining that a musical tone wave shape with an envelope is obtained in a multiplexed form; FIG. **10** (*a*) is a diagram showing one example of a wave shape stored in the wave shape memory; FIG. **10** (*b*) is a graphical diagram showing a time relation between clock pulses AC_1, AC_2 and AC_{10} applied to counters WSC_1, WSC_2 and WSC_{10} shown in FIG. **9** and output pulses from a multiplexing ring counter MC; FIG. **11** (*a*) is a graphical diagram showing one example of a wave shape read from a wave shape memory M_2: FIG. **11** (*b*) is a diagram showing the output pulses from the multiplexing ring counter MC; and FIG. **12** is a diagram showing musical tone wave shapes W_a and W_b each having an envelope.

Referring first to FIG. **1**, reference numeral **1** designates a keyboard circuit. An address code generator **1***a* is provided for generating key address codes representing the respective keys one after another in time sequence. Each key address code consists of a note code portion (four digits), an octave code portion (three digits) and an upper-lower keyboard code portion (one digit). The sequentially generated key address codes are supplied to a key address memory **2.** The key address codes are also supplied to a keyboard **1***b*. If a selected key on the keyboard **1***b* is depressed, a key data signal is applied from the keyboard **1***b* to a common logic circuit **3** when the key address code coincides with the code corresponding to the depressed key. The common logic circuit **3** which receives the key data signal transmits it to a channel logic circuit **4** of a channel CN when a logic condition to be described later is satisfied. The channel CN, which is indicated by the large dotted rectangle in FIG. **1,** is necessarily duplicated for each numerical tone of a maximum number of musical tones to be reproduced at a time, e.g., **10.** The channel logic circuit **4** transmits the key data signal to the key address memory **2** only when a logic condition to be described later is satisifed.

The key address memory **2** stores the key address code from the address code generator **1**a only when it receives the key data signal. Hence, if a key data signal is applied to the key address memory **2,** the key address code received by and stored in the memory **2** represents the depressed key. The key address code is applied from the key address memory **2** to a wave shape readout counter **5.** The wave shape readout counter **5** receives tone clock signals respectively corresponding to frequencies of twelve notes of a predetermined octave (e.g., the clock pulse frequency is sixteen times tone frequency in the highest octave), and selects one of the twelve tone clock signals corresponding to the note code portion in the key address code. The octave code of the key address code serves to switch a connection of the counter stages and thereby obtain a readout control signal for reading out a frequency which is one to four octaves lower than the above described tone clock signal. The readout control signal from the wave shape readout counter **5** is applied through a time-sharing gate **9** and a channel multiplexing gate **10** to a

wave shape memory **11** or **12** from which a musical tone signal having a predetermined wave shape is read out. The time-sharing gate **9** and the channel multiplexing gate **10** will be described more in detail later.

An envelope counter **6** supplies a readout control signal to an envelope memory **14** for producing an attack and decay envelope of a musical tone to be obtained. The envelope counter **6** receives an upper-lower keyboard code from the key address memory **2** and a condition signal to be described later from the channel logic circuit **4** and makes a counting operation during the attack time by means of clock pulses applied from an attack clock pulse generator **16.** The readout control signal thus produced by the envelope counter **6** is applied through a channel multiplexing gate **13** to the envelope memory **14,** whereupon an attack wave shape portion stored therein is read out. The read out wave shape is applied to the input terminal **11***a* or **12***a* of the wave shape memory **11** or **12,** and hence a musical tone signal with an attack envelope is produced from the output terminal of the memory **11** or **12.** When the attack time elapses, the counter **6** is caused to cease its counting operation by a signal applied from the channel logic circuit **4.** When the key is released, the envelope counter **6** receives a key off signal from the channel logic circuit **4** and resumes its counting operation by clock pulses supplied from a decay clock pulse generator **17.** Thus, a decay wave shape portion is read from the envelope memory **14** in the same manner as in the case of reading out the attack wave shape. When this reading out of the decay wave shape portion is completed, a finish signal is applied from the counter **6** to the logic circuit **4,** whereupon each flip-flop in the key address memory **2** is reset.

While a key address code is being stored in the key address memory **2,** a signal representing this state (hereinafter called "busy signal") is provided. In case no key address code is stored in the memory **2,** this state is hereinafter called "not-busy."

The common logic circuit **3** operates in such a manner as to always detect whether each channel is busy or not busy and apply a new key address code to a not-busy channel.

If all of the channels (ten channels) are occupied by key address codes respectively corresponding to depressed keys and a new key (an eleventh key) is depressed, there is no channel available for the key address code corresponding to the new key. In order to cope with this situation, that one of the envelope counters **6** in the respective channels which has been most advanced in the decay operation is selected for stopping the operation of its channel and applying the new key address code to the now blank channel. More specifically, the contents of the envelope counter **6** in this channel are previously applied to a truncate counter **7.** When all of the channels are in operation, clock pulses are applied at a very high speed from a clock pulse generator **18** to the truncate counter **7** of each channel for causing it to make a counting operation at a high speed. Hence, the channel having the counter **7** which has first produced an overflow output is recognized to be the channel which has been most advanced in the decay operation. The overflow output of the counter **7** is converted to a truncate signal when the key data signal is applied to the common logic circuit **3.** This truncate signal is used for resetting the key address memory **2** and the envelope counter **6** and causing the key address memory **2** to store the new key address code, thus causing the channel to operate in the foregoing manner.

A multiplexing counter **8** is provided for transmitting readout control signals from all of the channels in a time-sharing manner. Receiving pulses from clock pulse generator **19,** the counter **8** makes a high speed counting operation and successively supplies pulses for opening the time-sharing gate **9** to each channel.

FIG. **2** is a circuit diagram showing in detail one preferred embodiment of the electronic musical instrument according to the invention. In FIG. **2,** a key address code generator **1***a* comprises a flip-flop circuit FF*a* having four stages, (four binary digits to distinguish twelve different notes), a flip-flop circuit FFb having three stages (three binary digits to distinguish five different octaves) and a flip-flop circuit FF*c* having one stage (one binary digit to distinguish two different keyboards) connected in series. Clock pulses having a predetermined frequency, e.g., 60 kHz, generated from an address clock pulse oscillator AC are successively applied to these flip-flop circuits. Each bit output of the flip-flop circuit FFa is applied to a decoder D_1 which converts the four-digit binary code into twelve individual outputs, each bit output of the flip-flop FF*b* to a decoder D_2 converting the three-digit binary code into five individual output, and each bit output of the flip-flop FFc to a decoder D_3 converting the one-digit binary code into two individual output, respectively.

The outputs of the flip-flop FFa make note codes each one of which represents either one of the twelve notes (C, C #,.... B) within an octave. The outputs of the flip-flop circuit FFb make octave codes each one of which represents either one of the octaves (**1, 2 .... 5**) of the upper and lower keyboards. The outputs of the flip-flop FF*c* make upper-lower keyboard codes each one of which represents either the upper keyboard or the lower keyboard.

The decoder D_1 receives the note codes from the flip-flop FFa and successively produces an output at one of twelve output terminals thereof in accordance with the contents (binary notations) of the code. An output line K_1 is connected to one terminal of key switches U_1K_1, U_2K_1, ... U_5K_1, L_1K_1, L_2K_1 ... L_5K_1 which correspond to the highest note (e.g. B) of each octave. Similarly, an output line K_2 is connected to one terminal of key switches U_1K_2 .... U_5K_2, L_1K_2 .... L_5K_2 which correspond to a next note A #. Other output lines are connected in a similar manner to key switches respectively corresponding to subsequent notes, and an output line K_{12} is connected to one terminal of key switches U_1K_{12} .... U_5K_{12}, L_1K_{12} ..... L_5K_{12} corresponding to the lowest note C of each octave.

The other terminal of each key switch for each octave is connected in common to the input terminal of respective AND circuits A_1 through A_{10}.

The decoder D_2 receives the octave code from the flip-flop FFb and successively produces an output at one of five output terminals thereof in accordance with the contents of the code. An output line J_1 is connected to the input terminals of AND circuits A_1 and A_6 corresponding to the highest octave (**5**) of the upper and lower keyboards. An output line J_2 is connected to the input terminals of AND circuits A_2 and A_7 corresponding to an octave (**4**) next to the highest one. Output lines J_3, J_4 and J_5 are connected in a similar manner to AND circuits A_3 and A_8, A_4 and A_9, and A_5 and A_{10}, respectively.

The decoder D_3 receives the upper-lower keyboard code from the flip-flop FFc and produces an output at one of two output terminals thereof in accordance with the content (zero or one) of the code. An output line L_1 is connected to the input terminals of AND circuits A_1 through A_5 corresponding to the upper keyboard and an output line L_2 to the input terminals of AND circuits A_6 through A_{10}, respectively. The output terminals of these AND circuits A_1 through A_{10} are respectively connected to the input terminals of an OR circuit OR_1.

The contents of the key address code generated in the flip-flop circuits FF*a*, FF*b* and FF*c* successively change as these flip-flops receive the address clock pulses. When a predetermined number (in this case: **256**) of clock pulses are applied, the key address code generator returns to its initial state and the flip-flop circuits FFa through FFc successively and cyclically repeat production of the codes in the same manner.

If a particular key is depressed, an output is produced from either one of the AND circuits A_1 through A_{10} at the moment the key address code exhibits the code notation of the depressed key. Hence, the OR circuit OR_1 now produces an output.

The key address code coming out at the time when the output is produced from the OR circuit OR_1 therefore represents the depressed key by its note, octave and keyboard.

Assume now that the key switch L_5K_1 (corresponding to B_2 in the lower keyboard) is closed. When the flip-flop circuit FFa exhibits **0001**, an output is produced at the output line K_1 of the decoder D_1. This output is applied to one of the input terminals of the AND circuit A_{10} through the now closed key switch L_5K_1. When the flip-flop circuit FFb exhibits **101**, an output is produced at the output line J_5 of the decoder D_2, which output is applied to another input terminal of the AND circuit A_{10}. Further, when the flip-flop circuit FFc is **1**, an output is produced at the output line L_2 of the decoder D_3, which output is applied to the remaining input terminal of the AND circuit A_{10}. Thus, the output of the AND circuit A_{10} is provided through an OR circuit OR_1 on a line l_k at the moment the above mentioned three conditions occur simultaneously. At this time, the contents of the flip-flop circuits FFa, FFb and FFc are **00011011** (in this order from left to right). Accordingly, the key address code on lines l_1 through l_8 represent the depressed key. Since the contents of each flip-flop circuit successively and cyclically change and return to **0** after a predetermined number (**256**, in this case) of pulses have been counted, an output is provided on the line l_k at a certain interval of time at the moment the key address code appearing on the lines l_1 through l_8 represents the depressed key, as long as the key remains depressed.

In the following description, the output of the OR circuit OR_1 is referred to as a key data signal. The output lines l_1 through l_8 of the flip-flop FFa through FFc are respectively connected to the input terminals of AND circuits A_{11} through A_{18} which in turn are respectively connected to the set input terminals of eight flip-flop circuits FF_1 through FF_8 constituting the key address memory **2**.

The key data signal is applied to one of the input terminals of an AND circuit A_{19}. The other input terminal of the AND circuit A_{19} is connected to the output terminal of a NOR circuit NOR_1, and the AND circuit A_{19} can produce an output upon receipt of the key data signal only while an unblanking signal to be described later from the NOR circuit NOR_1 is applied thereto. This output of the AND circuit A_{19} is hereinafter referred to as a blanked key data signal. The output terminal of the AND circuit A_{19} is connected to one of the input terminals of an AND circuit A_{21}. The other input terminal of the AND circuit A_{21} is connected to the output terminal of an AND circuit A_{22}. Hence the blanked key data signal can come out at the output terminal of the AND circuit A_{21} only while an output 1 is produced from the AND circuit A_{22}. This blanked key data signal is applied to the remaining input terminals of the AND circuits A_{11} through A_{18}. Accordingly, the key address code produced at the moment the key data signal exists is stored in the flip-flops FF_1 through FF_8.

An OR circuit OR_2 is connected to each of the bit output terminals of the key address memory **2** comprising the flip-flops FF_1 through FF_8. This OR circuit OR_2 is provided for discriminating whether or not a key address code is stored in the key address memory **2**. When the key address code is stored therein, the OR circuit OR_2 produces an output 1 (hereinafter referred to as "busy signal"). When, on the contrary, no key address code is stored, it produces an output 0 (hereinafter referred to as "not-busy signal").

A terminal T_{12} of the key address memory **2** is connected to one of the input terminals of an AND circuit A_{24}. The AND circuit A_{24} produces an output 1 only when all of the channels are busy, i.e., all the OR_2's in the respective channels are busy. This output is hereinafter referred to as an "all busy signal."

The output terminals of the flip-flops FF_1 through FF_8 are connected to the input terminals on one side of a coincidence circuit or identity logic EQ. The input terminals on the other side of the coincidence circuit EQ receive the key address codes. The coincidence circuit EQ detects coincidence of the key address code already stored in the flip-flops FF_1 through FF_8 with the incoming key address code and produces a coincidence signal 1 at its output when it has detected the coincidence. When there is no coincidence, the output of the coincidence circuit EQ is 0. This coincidence signal is applied to one of the input terminals of the NOR circuit NOR_1 via terminals T_{14} and T_6. The same is the case with all the other channels.

Accordingly, if, when the key is depressed and the key data signal is supplied from the OR circuit OR_1 to one of the input terminals of the AND circuit A_{19}, the key address code applied from he key address code generator to the coincidence circuit EQ coincides with the key address code already stored in the memory **2** of one of the channels, the coincidence signal is applied to the input terminal of the NOR circuit NOR_1 and the NOR circuit NOR_1 produces an output 0. Hence, the other input of the AND circuit A_{19} is 0 so that the key data signal does not pass through the AND circuit A_{19}. Therefore, a key address code which is the same as that already stored in one channel is prevented from being stored in any other channel.

Again, if any key address code is already stored in the particular channel, e.g., CN_1, and, accordingly, the above described busy signal is being produced from the OR circuit OR_2, no new key address code is stored in the same channel. The construction for effecting this will be described hereinbelow.

When a key address code which is different from that already stored in the channel CN_1 is applied to the coincidence circuit EQ simultaneously with a key data signal, the NOR circuit NOR_1 produces an output 1 and the blanked key data signal is applied to one of the input terminals of the AND circuit A_{21} through the AND circuit A_{19}. In the meantime the busy signal from the OR circuit OR_2 is inverted by an inverter I_1 and applied to one of the inputs of an AND circuit A_{22} as an input 0. Accordingly, the output of the AND circuit A_{22} is 0 and the above described blanked key data signal is not applied to the other input terminals of the AND circuits A_{11} through A_{18}. Thus no key address code is applied to the key address memory **2**.

According to the invention, a search is always made to find out whether each channel is busy or not busy so that a new key address code may be stored in a channel which is not busy.

Assume that the channel CN_1 is busy and the output **1** of a search counter SC is provided on a line SL_1. A busy signal is applied to one of the input terminals of an AND circuits A_{23} and the output 1 on the line SL_1 is applied to the other input terminal thereof. Accordingly, the AND circuit A_{23} produces an output 1. This output is applied to one of the input terminals of an AND circuit A_{20} via an OR circuit OR_3. A search clock pulse generated in a search clock generator SCG passes through the AND circuit A_{20} and is applied to the search counter SC. Hence, the search counter SC counts one and produces an output 1 on an output line SL_2. If a busy signal is applied from a channel CN_2, the search counter SC further counts one. If a not-busy signal is applied to one of the input terminals of the AND circuit A_{23} in a channel CN_3, the output of the OR circuit OR_3 is 0 and, accordingly, the search counter SC does not count further and remains in a state in which the output 1 is provided on an output line SL_3. Thus, the AND circuit A_{22} receives the input signal 1 from the search counter SC and the input signal 1 which is produced by inverting the not-busy signal in the inverter **1**, and produces an output 1. The channel CN_3 is now in a standby condition to receive a blanked key data signal to be transmitted from the AND circuit A_{19}.

As described in the foregoing, the search counter SC is always searching to determine whether each channel is busy or not busy and stops its counting operation when it has found a not-busy channel so that a new key address code may be stored in the not-busy channel.

Accordingly, if a key address code corresponding to a key data signal produced by depression of a selected key is not already stored in any channel it will be stored in the not-busy channel when the key data signal passes through the AND circuit A_{19} and is applied to the input terminals of the AND circuits A_{11} through A_{18}, i.e., when the blanked key data signal is applied to the inputs of the AND circuits A_{11} through A_{18}.

The outputs of the flip-flops FF_1 through FF_4 are applied to the input terminals of a decoder D_4 via terminals T_{22} through T_{25}. The outputs of the flip-flops FF_5 through FF_7 are applied to the input terminals of a decoder D_5 via terminals T_{26} through T_{28}. The decoder D_4 has twelve output lines and produces an output 1 only on an output line which corresponds to the note code applied to the input terminal thereof. Each of the output lines of the decoder D_4 is connected to one input terminal of each of AND circuits A_{25} through A_{36}. The AND gates A_{25} through A_{36} receive at the other input terminals respective tone clock pulses at frequencies corresponding to those of the twelve notes of the lowest octave of the upper and lower keyboards. Accordingly, when the output **1** is produced from the decoder D_4, a tone clock pulse is selected by the AND circuit to which the output from the decoder D_4 is applied. This tone clock pulse is applied through an OR circuit OR_4 to the input terminal of a counter WSC consisting of eight cascade connected flip-flops, in this case. The decoder D_5 has five output lines and produces an output 1 only on an output line which corresponds to the octave code applied to the input terminal thereof. The five output lines are respectively connected to a select switch SS. The select switch SS is provided for switching the connection of the output from the OR logic OR_4 and the respective flip-flop stages of the counter WSC in accordance with the octave code selected. The detailed construction of a select switch for such switching has been described in a copending U.S. Pat. application Ser. No. 276,103, filed July 28, 1972.

The rate of reading out the wave shape memory **11** or **12** by a readout control signal obtained by decoding the output of the counter WSC by means of decoders D_6 or D_7 can be changed by operation of the aforementioned select switch SS. The principle of the foregoing arrangement will be described with reference to FIG. **3** in which the counter WSC has three flip-flop stages.

If three stages of flip-flops F_1 through F_3 are connected in series as shown in FIG. **3**(*a*), the output X, Y and Z of the respective flip-flops produced by application of the clock input thereto are as shown in Table **1**(*a*). If these outputs are decoded by a binary input-to-individual output decoder, the outputs of the decoder become **0, 1, 2, ... 7** successively.

Table 1

(*a*)		(*b*)	
X Y Z	Decoded output	X Y Z	Decoded output
0 0 0	0	0 0 0	0
0 0 1	1	0 1 0	2
0 1 0	2	1 0 0	4
0 1 1	3	1 1 0	6
1 0 0	4	0 0 0	0
1 0 1	5	0 1 0	2
1 1 0	6	1 0 0	4
1 1 1	7	1 1 0	6

If, as shown in FIG. **3**(*b*), the flip-flop F_1 is separated from the rest of flip-flops and fixed at **0** and a clock input is applied to the flip-flop F_2, the outputs X, Y and Z are as shown in Table **1**(*b*). If these outputs are decoded by a decoder, the decoded outputs become **0, 2, 4, 6, 0 .... 6.** If the decoded outputs shown in Table **1**(*b*) are used for reading out a wave shape stored in the wave shape memory, the readout rate or speed will be double that obtained when the decoded outputs shown in Table **1**(*a*) are used. If the flip-flops F_1 and F_2 are separated from the flip-flop F_3 as shown in FIG. **3**(*c*), the readout rate or speed will become four times that obtained when the outputs shown in Table **1**(*a*) are used. It will be understood from the foregoing description that the select switch SS switches the connection of the flip-flop stages in the counter WSC in accordance with the octave code thereby changing the rate of reading out the wave shape stored in the wave shape memory.

The output signals of the counter WSC pass through AND circuits A_{37} through A_{44} and OR circuits OR_5 through OR_{12}. In case the depressed key belongs to the upper keyboard, the output signals are applied through AND circuits A_{45} through A_{52} to the decoder D_7 where they are decoded and used to successively read out a wave shape stored in the wave shape memory **12.** The read out wave shape is amplified in an amplifier AM_2 and is taken out at a terminal **12***b*. The wave shape memory **12** stores the wave shape in the form of resistance values. Thus a musical note signal corresponding to the decoding rate is obtained at the terminal **12***b*. In case the depressed key belongs to the lower keyboard, the output signals of the OR circuit OR_5 through OR_{12} are applied through AND circuits A_{53} through A_{60} to the decoder D_6. These output signals are decoded in the decoder D_6 and used to read out a wave shape stored in the wave shape memory **11.** The read out wave shape is amplified in an amplifier AM_1 and a musical tone signal is taken out at a terminal **11**b.

Since the output of the flip-flop FF_8 of the key address memory **2** is 1 when a key on the lower keyboard is depressed, the output 1 is applied to one input terminal of each of the AND circuits A_{45} through A_{52} via an AND circuit A_{61} and an OR circuit OR_{13}. Therefore, the outputs of the counter WSC are applied to the decoder D_7. Whereas, the output of the flip-flop FF_8 is 0 when a key on the upper keyboard is depressed, so that the output 1 is applied to one input terminal of each of the AND circuits A_{53} through A_{60} through the AND circuit A_{61}, the OR circuit OR_{13} and an inverter I_2. Therefore, the outputs of the counter WSC are applied to the decoder D_6.

The musical tone signals obtained at the terminal T_{01} and T_{02} should have an envelope which includes an attack characteristic lasting for a certain length of time after depression of the key and a decay characteristic lasting for a certain length of time after the key is released. In order to provide this envelope for the musical tone signals, the output of the envelope memory **14** is applied to terminals **11***a* and **12***a* of the wave shape memories **11** and **12.**

In the foregoing example, a tone clock pulse corresponding to a selected note code is selected from among tone clock pulses at frequencies corresponding to the twelve notes of the lowest octave and is applied to a wave shape readout counter. The connection of each stage of the wave shape readout counter is switched for changing the rate of reading out the wave shape stored in the wave shape memory **11** or **12** in accordance with the depressed key.

Referring to FIG. **4,** a modified example will now be described. In this example, tone clock pulse corresponding in number to keys on each of the upper and lower keyboards are provided. A tone clock pulse is directly selected from among these tone clock pulses in accordance with the note code and the octave code, and the tone clock pulses is directed to operate, in response to the upper-lower keyboard code, one of the wave shape readout counters associated respectively with the to wave shape memories provided for the upper and lower keyboards.

The outputs of flip-flops FF_1 through FF_7 are applied to a decoder D_4. The decoder D_4 receives selected note and octave codes and produces an output at one of a plurality of outputs, e.g., **60,** in response to the note and octave codes. Each output line of the decoder D_4 is connected to one input terminal of each of AND circuits A_{121} through A_{180}. The other input terminal of each of the AND circuits A_{121} through A_{180} receives each corresponding tone clock signal. The tone clock signals are signals at frequencies corresponding to notes C_1 through B_5.

When an output is produced on one of the output lines of the decoder D_4, the AND circuit to which this output line is connected conducts and passes a tone clock signal which is applied to this AND circuit. This tone clock signal is applied through an OR circuit OR to the inputs of AND circuits AD_1 and AD_2. In the meanwhile, the flip-flop FF_8 stores either the upper keyboard code or the lower keyboard code and its output is either 0 or 1. If, for example, the output 0 is produced in response to the upper keyboard code, this output 0 is inverted by an inverter I and a signal 1 is applied to one of the input terminals of the AND circuit AD_1. This causes the AND circuit AD_1 to conduct and the tone clock signal is transmitted to a terminal T*a*. Similarly, if the lower keyboard signal is applied to the flip-flop FF_8, the AND circuit AD_2 conducts and the tone clock signal is transmitted to a terminal Tb.

Thus, when a selected key is depressed, a key address code corresponding to the depressed key is stored in the key address memory **2** and a tone clock signal corresponding to the key address code is selected and transmitted to the output terminal by a tone clock signal selection circuit **3.**

In the foregoing example, the number of keys of the upper and lower keyboards is **60** each. This number may of course vary. Further, if a single keyboard is used instead of the upper and lower keyboards, the flip-flop FFc and the decoder D_3 shown in FIG. **2** and the AND circuit A_{18}, flip-flop FF_8, inverter I and the AND circuits AD_1 and AD_2 will be omitted.

Referring again to FIG. **2,** the reading out of the attack and decay envelope wave shape from the memory **14** will now be described.

An envelope wave shape is sampled *n* times and an amplitude of the envelope wave shape at each sample time is respectively stored in an envelope memory **14.** In the memory **14,** the attack portion of the envelope wave shape is stored at addresses **1** through a predetermined one, e.g. **16.** The decay portion is stored at the subsequent addresses to the last one, e.g., **63.**

T_{m1} through T_{mn} designate readout control terminals of the envelope memory **14.** When readout control signals which are the outputs of a decoder D_8 are applied to these terminals as will be described later, the wave shape amplitudes at the address corresponding to these terminals are read out.

When the key address code is stored in the key address memory **2,** the output 1 of the flip-flop FF_8 is applied to one of the input terminals of an AND circuit A_{62} in case the depressed key belongs to the lower keyboard. Accordingly, clock pulses applied to the other input terminal of the AND circuit A_{62} from an attack clock generator ACU pass through the AND circuit A_{62} and are applied to one of the input terminals of an AND circuit A_{66} via an OR circuit OR_{14}. Another input terminal of the AND circuit A_{66} receives the busy signal from the terminal T_{12}. The remaining input terminal of the AND circuit A_{66} receives a signal 1 from an AND circuit A_{68}. Hence, the attack clock pulses are provided at the output terminal of the AND circuit A_{66} and applied through an OR circuit OR_{16} to the input terminal

of an envelope counter ADC which consists, for example, of six flip-flop stages. The envelope counter ADC starts counting upon receipt of these attack clock pulses. While the counter ADC counts **0** through **16**, the outputs thereof are applied to the decoder D_8 via terminals T_{30} through T_{35}, AND circuits A_{70} through A_{75} and OR circuits OR_{17} through OR_{22}. The decoder D_8 operates to decode the binary notations to individual outputs which successively come out one after another similar to outputs from a ring counter thereby producing readout control signals, on one of a plurality of output lines H_1 through H_n in response to counting of the counter ADC. When the counter ADC counts **1**, a readout control signal is produced on the output line H_1. As the counter ADC continues counting, readout control signals are successively produced on the output lines H_2 ..... toward H_n. Accordingly, the decoder D_8 decodes the output of the counter ADC and applies the readout control signals from **0** to **16** to the envelope memory **14** thereby causing the attack wave shape to be provided at a terminal **14**b through an amplifier AM_3.

Since the output of the flip-flop stage of the most significant digit and the flip-flop stage next thereto of the counter ADC are respectively 0 while the counter ADC counts from **1** through **16**, the outputs of inverters I_4 and I_5 are respectively 1 and, accordingly, the AND circuit A_{68} produces an output 1. This output of the AND circuit A_{68} continues to be applied to the AND circuit A_{66}, and hence the attack clock pulses continue to be applied to the counter ADC via the AND circuit A_{66} and the OR circuit OR_{16}. When the counter ADC counts up to **16**, either of the outputs of the flip-flop stage of the most significant digit and the flip-flop stage next thereto is 1. Hence, the output of the AND circuit A_{68} is 0 and the attack clock pulses do not pass through the AND circuit A_{66}. The counter ADC therefore ceases counting. The output 0 of the AND circuit A_{68} is inverted to 1 by an inverter I_3 and applied to the input terminal of the AND circuit A_{67}.

When the key is released and the key switch is off, the key data signal becomes 0. This signal 0 is inverted to 1 by an inverter I_6 and thereafter is applied to one of the input terminals of an AND circuit A_{76}. The other input terminal of the AND circuit A_{76} receives the coincidence signal from the terminal T_{14}. The key address code is successively supplied from the key address code generator **1***a* to the coincidence circuit EQ even after the key is released. Accordingly, the coincidence signal is produced at a predetermined time interval even after the key is released. When this coincidence signal is applied to the other input terminal of the AND circuit A_{76}, the AND circuit A_{76} produces an output 1. This output 1 represents a key-switch-off state and is applied to the set input terminal of a flip-flop FF to set the flip-flop FF. The set output 1 of the flip-flop FF is applied as a key-off signal to the input terminal of the AND circuit A_{67}.

Decay clock pulses from a decay clock generator DCU are applied to one of the input terminals of the AND circuit A_{67} via an AND circuit A_{64} and an OR circuit OR_{15}. Accordingly, when the key-off signal is applied to the AND circuit A_{67}, the decay clock pulses are provided at the output terminal thereof and applied to the input terminal of the envelope counter ADC through the OR circuit OR_{16}. The counter ADC resumes counting from **17** upon receipt of the decay clock pulses. The decoder D_8 supplies readout control signals (No. **17** and thereafter) to the memory **14** thereby causing the decay envelope wave shape to be produced at the terminal T_{03}. The envelope wave shapes read out in the above described manner are applied to the terminals **11**a and **12**a of the wave shape memories **11** and **12**.

When the envelope counter ADC has counted **63**, the states of all the flip-flop stages become 1 and an AND circuit A_{69} produces an output 1. This output signal is applied to the reset input terminal of the flip-flop FF via a terminal T_{19} and an OR circuit OR_{23}. This causes the flip-flop FF to be reset and the key-off signal from the flip-flop FF becomes 0. Hence, the decay clock pulses cease to pass through the AND circuit A_{67}.

In the meantime, the signal from the terminal T_{19} is applied to the reset input terminal of each of the flip-flops FF_1 through FF_8 via an OR circuit OR_{25} and resets all of these flip-flops.

Thus, reading out of the envelope wave shape from the envelope memory **14** has been completed.

FIG. **5** shows an example of the envelope memory **14**. An envelope wave shape to be stored is sampled n time (e.g., **64**). The amplitude of the wave shape at each sample time is stored by means of resistance in accordance with a voltage dividing ratio. A constant voltage V is applied between the terminal T_{IN} and the ground. If a connecting point with the ground is designated as A_1, a connecting point of resistances R_2 and R'_2 as A_2 .... and a connecting point of resistances Rn and R'n as An, voltages at the connecting points A_1 through A_n are **0**, $R'_2V/R_2+R'_2$, ... $R'_nV/R_n+R'_n$ respectively. These voltages respectively correspond to the amplitudes of the envelope wave shape to be stored. The drains of transistors TR_1 through TR_n are respectively connected to the connecting points A_1 through An. The sources of the transistors TR_1 through TR_n are successively connected to each other and connected through an amplifier AM_3 to the output terminal **14***b*. The gates of these transistors are respectively connected to readout control terminals T_{m1} through T_{mn}. The drain of the transistor TR_1 is connected to the ground, its source to the source of the transistor TR_2 and its gate to the readout control terminal T_{m1} respectively.

When the readout control signal is applied from the decoder D_8 to one of the readout control terminals T_{m1} through T_{mn}, the transistor connected to the terminal conducts and the corresponding voltage is supplied to the terminal **14***b* after being amplified in the amplifier AM_3. It will be understood from the foregoing description that a musical tone signal with the attack and decay envelope is provided at the terminal **12***b*.

The time lengths of the read out attack and decay wave shape portions can be varied by employing attack and decay clock generators of a variable type and thereby varying the frequencies of the clock pulses generated by these clock generators.

The reading out of the attack and decay envelope from the envelope memory has been described hereinafter with regard to the case wherein the key on the lower keyboard was depressed. In case a key on the upper keyboard is depressed, the output 0 of the flip-flop FF_8 is inverted to 1 by an inverter I_7 and applied to the AND circuits A_{63} and A_{65}. Hence, attack clock pulses from the attack clock generator ACL pass through the AND circuit A_{63} during the attack time and

decay clock pulses from the decay clock generator DCL pass through the AND circuit A_{65} during the decay time. The reading out operation is the same as in the case of the lower keyboard in all other respects.

While the envelope counter ADC counts **17** and subsequent numbers, the output 1 of the inverter I_3 is applied to one of the input terminals of an AND circuit A_{77}. The other input terminal of the AND circuit A_{77} receives the key-off signal 1, and hence the AND circuit A_{77} produces an output 1. This output signal indicates that the decay operation is proceeding (hereinafter referred to as a "decay signal"). This signal will be described more in detail later.

If the same key is depressed again during this decay operation, the key data signal is applied to one of the input terminals of an AND circuit A_{78}. The other input terminals of the AND circuit A_{78} receive the key-off signal from the flip-flop FF and the coincidence signal from the terminal T_{14}, and hence the AND circuit A_{78} produces an output 1 upon receipt of the key data signal. This output signal is applied to the reset input terminal of the counter ADC via the OR circuit OR_{24} and the terminal T_{18}. The counter ADC is reset and returns to **0**, and starts again to read out the attack wave shape in the above described manner. After keying off, the counter ADC reads out the decay wave shape.

If the eleventh key is depressed while all of the ten channels are busy, a search is made for determining the channel in which the decay operation is most advanced and the key address memory of this channel is reset for receiving the key address code of the eleventh key.

Assume that the ten channels are all busy and the decay operation is most advanced in the channel CN_1. The contents of the envelope counter ADC are periodically transferred to a truncate counter TC via the AND circuits A_{70} through A_{75}, the OR circuits OR_{19} through OR_{22} and the AND circuits A_{79} through A_{84}. An AND circuit A_{85} receives an all-busy signal 1 and a signal 1 from NOR circuit NOR_3, and hence clock pulses from a high frequency clock generator HC pass through the AND circuit A_{85} and is applied to one of the input terminals of the AND circuit A_{86}. The other input terminal of the AND circuit A_{86} receives the above described decay signal, and hence the clock pulses are applied to the input terminal of the truncate counter TC via a terminal T_{20}. Accordingly, each counter TC makes a high speed counting operation starting from the transferred count and that counter TC among those of the ten channels in which the largest count has been transferred produces an overflow output 1. This overflow output 1 sets a flip-flop FFk. The set output 1 of this flip-flop FFk is applied to one of the input terminals of the AND circuit A_{87}. The AND circuit A_{87} further receives the all-busy signal and the output appearing on the output line SL_1 of the search counter SC which is transmitted through the terminal T_4. Since all of the channels are busy, the search counter SC repeats counting and successively provides the signal 1 on the output line SL_1 .... SL_{10}, SL_1. If the counter TC of the channel CN_1 produces the overflow output, the AND circuit A_{87} of the channel CN_1 produces the output 1 when the output 1 is produced on the output SL_1. This output is inverted to 0 by a NOR circuit NOR_2 and thereafter is applied to the AND circuit A_{20}. This causes the search counter SC to stop its counting operation, maintaining the output 1 on the output line SL_1. The set output of the flip-flop FFk is inverted to 0 by the NOR circuit NOR_3 and applied to the AND circuit A_{85}. Hence, the high rate clock pulses are prevented from passing through the AND circuit A_{85} and the truncate counter TC ceases its counting operation immediately upon producing the overflow output.

In the state described above, if the eleventh key is depressed, a blanked key data signal is applied to one of the input terminals of the AND circuit A_{88}, and hence the AND circuit A_{88} produces an output 1 which becomes a truncate signal. This truncate signal is applied to the reset input terminal of each stage of the envelope counter ADC via the OR circuit OR_{24} to reset the counter ADC. Simultaneously, the truncate signal is applied to the reset input terminal of each flip-flop stage FF_1 through FF_8 of the key address memory **2** via the OR circuit OR_{25} to reset these flip-flop stages. Thus, the eleventh key address code is stored in the memory **2** whereby the eleventh musical tone signal is obtained.

FIG. **6** shows wave shapes at some parts of the circuit shown in FIG. **2**. During a period between ON and OFF of the key switch shown in FIG. **6**(*a*) the key data signal is produced as shown in FIG. **6**(*b*). The blanked key data signal which is the output of the AND circuit A_{19} is a pulse corresponding to the first pulse of the key data signal as shown in FIG. **6**(*c*). Since the coincidence signal is produced from the coincidence circuit EQ at the second and subsequent pulses of the key data signal and this coincidence signal is applied through the NOR circuit NOR_1 to the AND circuit A_{19} as an input 0, the AND circuit A_{19} does not produce an output. A new key address code is stored in the key address memory by means of this blanked key data signal and the OR circuit OR_2 produces a busy signal. This memory returns to **0** as shown in FIG. **6**(*d*) upon receipt of the output of the AND circuit A_{69}(FIG. **6**(*e*)). FIG. **6**(*f*) shows the coincidence signal from the coincidence circuit EQ. The coincidence signal is produced at a predetermined interval during storage of the key address code in the key address memory. FIG. **6**(*g*) shows the output of the inverter I_6 which is obtained by inverting the key data signal. The AND circuit A_{76} receives the coincidence signal shown in FIG. **6**(*f*) and the signal shown in FIG. **6**(*g*) and produces the output as shown in FIG. **6**(*h*). Accordingly, the flip-flop FF is set as shown in FIG. **6**(*i*) at the first pulse of the signal shown in FIG. **6**(*h*) until it is reset by the output of the AND circuit A_{69}. FIG. **6**(*j*) shows the states of the envelope counter ADC. The envelope counter ADC starts counting at the rise of the busy signal and counts to **16.** The counter ADC thereafter suspends its counting operation until the key switch becomes OFF. When the key switch becomes OFF, the counter ADC resumes counting and counts to **63.** FIGS. **6**(*k*) and (*l*) show the output of the AND circuit A_{68} and the inverter I_3 respectively.

FIG. **7** shows the wave shapes at the parts of the circuits shown in FIG. **2** when the same key is depressed again during the decay of the musical tone signal. The reference characters (*a*), (*b*) ... (*l*) in FIG. **7** correspond to those used in FIG. **6.** The wave shape at each part before the key switch becomes ON again is the same as the one shown in FIG. **6.** When the key switch becomes ON again, a key data signal is produced as shown in FIG. **7**(*b*). At the first pulse of this key data signal, the flip-flop FF is reset and its state is inverted as shown in FIG. **7**(*i*). Simultaneously, the counter

ADC is reset as shown in FIG. 7(*i*) and starts counting from **0.** FIG. **8** shows wave shapes at some parts of the circuit shown in FIG. **2** when the eleventh key is depressed while the ten channels are busy and the decay operation is most advanced in the channel CN_1. FIG. **8**(*a*) shows the ON-OFF state of the key switch. FIG. **8**(*b*) shows the new key data signal corresponding to the eleventh key. The first pulse of this key data signal passes through the AND circuit A_{19} and becomes a blanked key data signal as shown in FIG. **8**(*e*). The AND circuit A_{88} produces a truncate pulse as shown in FIG. **8**(*h*) upon receipt of the blanked key data signal. This truncate pulse resets the key address memory, whereby the busy signal of the channel CN_1 becomes 0 as shown in FIG. **8**(*f*) and the flip-flop FF is reset as shown in FIG. **8**(*g*). The second key data signal from the time when the key switch has become ON passes through the AND circuit A_{19} and is applied to the key address memory of the channel CN_1 as a blanked key data signal. Hence, the eleventh key address codes are stored in this memory and the busy signal becomes 1 as shown in FIG. **8**(*f*). From this time on, the coincidence signal is produced at a constant interval as shown in FIG. **8**(*j*). FIG. **8**(*k*) shows the output of the inverter I_6, FIG. **8**(*l*) the output of the AND circuit A_{76}, FIG. **8**(*m*) the output of the AND circuit A_{68}, FIG. **8**(*n*) the states of the envelope counter ADC and FIG. **8**(*o*) the output of the inverter I_3 respectively.

Receiving clock pulses from a multiplexing clock generator MCC, a multiplexing counter MC makes a counting operation at a high rate and produces an output successively on output lines Ml_1, through Ml_{10}. Each output of the multiplexing counter MC is successively applied to the AND circuits A_{37} through A_{44}, A_{61}, A_{70} through A_{75}, and A_{79} through A_{84} of the respective channels. Thus, the output for each channel is applied in a time sharing manner to the wave shape memory **11** or **12,** the envelope memory **14** and the truncate counter TC.

FIG. **9** is a block diagram showing essential parts of the circuit shown in FIG. **2** for explaining that a musical tone wave shape with an envelope can be obtained in a multiplexed form from the wave shape memory **12** and the envelope memory **14.**

In FIG. **9,** a gate circuit EG_1 consisting of the AND circuits A_{70} through A_{75} controls the output of the envelope counter ADC_1 of the first channel. A gate circuit WG_1 consisting of the AND circuits A_{37} through A_{44}, controls the output of the wave shape readout counter WSC_1 of the first channel. Gate circuit EG_2 through EG_{10} and WG_2 through WG_{10} which are respectively of the same construction as the gate circuit EG_1 and WG_1 are provided for the second through tenth channels. The input to the envelope counter ADC in FIG. **2** is the output of the OR circuit OR_{16}. In FIG. **9,** however, the output of a clock pulse generator BC_1 is applied to the envelope counter ADC_1 for convenience of explanation. The other envelope counters ADC_2 through ADC_{10} likewise receive clock pulses from clock pulses generators BC_2 through BC_{10}. Again, the wave shape readout counter WSC_1 receives the output of a clock pulse generator AC_1 instead of the output of the OR circuit OR_4 shown in FIG. **2.** Likewise, the other wave shape readout counters WSC_2 through WSC_{10} receive clock pulses from clock pulse generator AC_2 through AC_{10}. It is assumed that the clock pulse generators BC_1 through BC_{10} generate the clock pulses having much lower frequencies than the clock pulses generated by the clock pulse generators AC_1 through AC_{10}. The constructions of the wave shape memory **12** and the envelope memory **14** are the same as those shown in FIG. **5.**

The multiplexing counter MC receives the pulses from the clock pulse generator MCC and makes a high rate counting operation. The counter MC produces its output successively and cyclicly on the output lines Ml_1 through Ml_{10}. The output line Ml_1 is connected to the gate circuit EG_1 and WG_1 The other output lines Ml_2 through Ml_{10} are respectively connected to the gate circuit EG_2, WG_2, .. EG_{10} and WG_{10}. When the pulse is applied from the multiplexing counter MC to the gate circuits WG_1 and EG_1, the output of each stage of the wave shape counter WC_1 and the output of each stage of the envelope counter EG_1 are applied respectively to the decoders D_7 and D_8 in synchronization with each other. Thus, the decoder D_7 produces an output on its output line corresponding to the count of the counter WSC_1 and applies this output to a corresponding one of the readout control terminals T_{m1} through T_{mn}. In the meanwhile, the decoder D_2 produces an output on its output line corresponding to the count of the counter ADC_1 and applies this output to a corresponding one of the readout control terminals T_{m1}' through T_{mn}'.

The amplitude of the envelope wave shape stored at the address in the envelope memory **14** corresponding to the readout control terminal to which the output of the decoder D_8 is applied is readout in the form of a voltage value and applied to the terminal **12***a* of the wave shape memory **12.** Again, when the output of the decoder D_7 is applied to one of the readout control terminals of the wave shape memory **12,** a voltage which is a product of the voltage corresponding to the wave shape amplitude stored at the address corresponding to the particular readout control terminal and the voltage applied to the terminal **12***a* is read out at the terminal **12***b* via the amplifier AM_2.

Thus, the output pulse of the multiplexing counter MC is successively applied to the gate circuits EG_2 and WG_2, ..., EG_{10} and WG_{10} and the output of each wave shape counter and each envelope counter corresponding thereto are successively applied in a time-sharing manner to the decoders D_8 and D_7 to read out wave shape amplitude with a desired envelope.

The multiplexing readout of a musical tone wave shape will be described more in detail hereinbelow. For convenience of explanation, it is assumed that a constant voltage is provided at the output terminal **14**b of the envelope memory **14,** that the number of sample points of the wave shape memory **12** is **16,** that wave shape amplitudes W_1 through W_{16} at these sample points are stored in the memory **12** as shown in FIG. **10**(*a*) and that clock pulses AC_1, AC_2 and AC_{10} as shown in FIG. **10**(*b*) are successively applied to the wave shape readout counters WSC_1, WSC_2 and WSC_{10}. The ring counter MC produces its pulse outputs P_1, P_2, ... P_{10}, P_1 successively at a high rate on the output lines Ml_1 through Ml_{10} as shown in FIG. **11**(*b*). Hence, each time the output of the ring counter MC is applied to each of the gate circuits WG_1 through WG_{10}, each gate circuit WG_1, WG_2 .... WG_{10} gates out the output of each of the counters WSC_1 through WSC_{10} to apply it through the decoder D_7 to the wave shape memory as the readout control signal.

The crossing points of a dotted line and the pulses AC_1, AC_2 and AC_{10} in FIG. **10**(*b*) respectively represent time at which the corresponding pulses P_1, P_2 and P_{10} are applied from the ring counter. Dotted lines *b* and *c* indicate the same thing.

In FIG. **10**(*b*), the pulses P_1, P_2 and P_{10} are applied to the gate circuits WG_1, WG_2 and WG_{10} at the time when the dotted line *a* crosses each read out pulse. Since the count of the counter WSC_1 is **3**, a pulse is applied from the decoder D_7 to the readout control terminal T_{m3} to read out the wave shape amplitude W_3. The count of the counter WSC_2 is **2** and hence the wave shape amplitude W_2 is read out. The count of the counter WSC_{10} is **2**, and hence the wave shape amplitude W_2 is read out.

Nextly, as the pulses P_1, P_2 and P_{10} are applied at the time when the dotted line *b* crosses each read out pulse, the count of the counter WSC_1 is **7**, that of the counter WSC_2 is **4** and that of the counter WSC_{10} is **3**. Accordingly, the wave shape amplitudes W_7, W_4 and W_3 are respectively read out.

As the ring counter MC repeats the counting, the wave shape amplitude W_{10} is read out with respect to the counter WSC_1, the wave shape amplitude W_6 with respect to the counter WSC_2 and the wave shape amplitude W_4 with respect to the counter WSC_{10}.

FIG. **11**(*a*) shows a wave shape read from the wave shape memory **12**. Wave shapes MW_1, MW_2 and MW_3 are respectively wave shapes read out by readout control signals from the counters WSC_1, WSC_2 and WSC_3.

Thus, a plurality of wave shapes are read out in a multiplexed form in accordance with the counting speeds of the counters. It will be noted that time relation is shown in an enlarged form in FIGS. **11**(*a*) and (*b*) for convenience of explanation. Further, the actual sampling number of the wave shape memory is very large, e.g., more than **128**.

In the foregoing description, the output of the terminal T_{03} is assumed to be a constant voltage. Actually, however, an envelope wave shape amplitude corresponding to the count of each of the envelope counter ADC_1 through ADC_{10} is produced from the envelope memory **14**. Accordingly, a voltage which is a product of the wave shape amplitude stored in the memory **14** and the envelope wave shape amplitude is read from the wave shape memory **12**.

Thus pairs of outputs of the wave shape counter and the envelope counter are successively applied in a time-sharing manner to the readout terminals of the wave shape memory and the envelope memory through the decoders D_7 and D_8 whereby musical tone wave shapes each corresponding to the pair of outputs are obtained. FIG. **12** illustrates examples of the read out musical tone wave shape with a desired envelope. A musical tone wave shape W_a has an envelope wave shape EV_1 and a musical tone wave shape Wb has an envelope wave shape EV_2.

What we claim is:

1. An electronic musical instrument comprising, in combination:

a. a preloaded wave shape memory in which a multiplicity of amplitude samples of at least one period of a complex musical tone wave shape have been stored in analog representation, said wave shape memory having for each sample a respective readout control terminal whose energization causes the respective sample to be read out of said memory and

b. read out means coupled to the read out control terminals of said wave shape memory for repetitively reading out in succession the stored samples of the wave shape in said memory at a selectable rate and producing therefrom repeated cycles of voltage, each cycle having a wave shape matching that of said stored wave shape and a period determined by the selected rate of readout, said read out means comprising a key address memory for storing a key address code consisting of a note code, an octave code and a keyboard code, a selecting circuit for selecting a tone clock pulse from among a plurality of tone clock pulses at frequencies corresponding to respective keys in response to note and octave codes stored in said key address memory, a wave shape readout counter receiving said selected tone clock pulse, and gate circuitry for receiving the output of each stage of said wave shape readout counter and successively applying an energizing output corresponding to the count of said counter to each readout control terminal of said wave shape memory.

2. An electronic musical instrument according to claim **1**, wherein said read out means is adapted to simultaneously repetitively read out in succession the stored samples in said wave shape memory at a plurality of selectable rates and to simultaneously produce therefrom a like plurality of groups of repeated cycles of voltage, each cycle of each group having a wave shape matching that of said stored wave shape and a period determined by the selected rate of readout for the respective group.

3. An electronic musical instrument comprising, in combination:

a. a preloaded wave shape memory in which a multiplicity of amplitude samples of at least one period of a complex musical tone wave shape have been stored in analog representation, said wave shape memory having for each sample a respective readout control terminal whose energization causes the respective sample to be read out of said memory and

b. read out means coupled to the read out control terminals of said wave shape memory for repetitively reading out in succession the stored samples of the wave shape in said memory at a selectable rate and producing therefrom repeated cycles of voltage, each cycle having a wave shape matching that of said stored wave shape and a period determined by the selected rate of readout, said read out means comprising a key address memory for storing a key address code consisting of a note code, an octave code and a keyboard code corresponding to a depressed key, a selecting circuit for selecting a tone clock pulse from among a plurality of tone clock pulses having frequencies respectively corresponding to twelve note-identifying keys of the highest octave of several encoded octaves in response to the note code stored in said key address memory, a wave shape readout counter receiving said selected tone clock pulse, a select switch for switching the connection of each stage of said wave shape readout counter in response to the octave code stored in said key address memory, and gate circuitry for receiving the output of each stage of said

wave shape readout counter and successively applying an energizing output corresponding to the count of said counter to each readout control terminal of said wave shape memory.

4. An electronic musical instrument as defined in claim **3** which further comprises an additional preloaded wave shape memory similar in construction and content to the first-mentioned wave shape memory, and means for interchanging said wave shape memories in response to the keyboard code stored in said key address memory.

5. An electronic musical instrument comprising, in combination:

a. a preloaded wave shape memory in which a multiplicity of amplitude samples of at least one period of a complex musical tone wave shape have been stored in analog representation, said wave shape memory having for each sample a respective readout control terminal whose energization causes the respective sample to be read out of said memory;

b. read out means coupled to the read out control terminals of said wave shape memory for repetitively reading out in succession the stored samples of the wave shape in said memory at a selectable rate and producing therefrom repeated cycles of voltage, each cycle having a wave shape matching that of said stored wave shape and a period determined by the selected rate of readout;

c. a preloaded envelope memory in which an analog representation of an envelope wave shape for said musical tone is stored;

d. second read out means for reading said analog representation from said envelope memory at a selectable rate;

e. means for feeding the output of said envelope memory to an input terminal of said wave shape memory; and

f. means in said wave shape memory for multiplying the output of said envelope memory and the output of said wave shape memory, thereby producing a wave shape of said musical tone with an envelope.

6. An electronic musical instrument as defined in claim **5** in which said envelope memory stores amplitude samples of an attack portion and a subsequent decay portion of said envelope wave shape.

7. An electronic musical instrument as defined in claim **6** wherein said second readout means is capable of reading out said attack portion and said decay portion independently at a selectable rate.

8. An electronic musical instrument comprising a keyboard, means coupled to said keyboard for providing in a time-sharing manner a key address code and a key data signal synchronized with each other, said key data signal being produced when a selected key of said keyboard is depressed, a plurality of key address memories, means for searching for an unloaded memory among said plurality of key address memories, means for searching whether said key address code synchronized with said key data signal is already stored in a key address memory, means for applying a key address code which is not already stored to said unloaded memory, a wave shape memory for storing analog samples of a musical tone wave shape, means for selecting a tone clock pulse from among a plurality of tone clock pulses in response to the key address code stored in said key address memory and applying it to a wave shape readout counter connected to said wave shape memory thereby causing the wave shape of said musical tone to be read from said wave shape memory.

9. An electronic musical instrument as defined in claim **8** in which said means for providing a synchronized key address code and key data signal comprise a key address generator which receives clock pulses from a clock generator and produces successively changing key address code each consisting of a note code, an octave code and and a keyboard code, a first decoder which receives the note code from said key address generator and produces an output successively on a plurality of output lines, a second decoder which receives the octave code from said key address generator and produces an output successively on a plurality of output lines, a third decoder which receives the keyboard code from said key address generator and produces an output successively on a plurality of output lines, AND circuits each having three input terminals and being provided for each octave of a key switch and means for producing the key data signal from the output of the AND circuit corresponding to the octave to which the depressed key belongs by connecting the outputs of said first, second and third decoders to the input terminals of said AND circuit when the key address code corresponding to the depressed key is produced by said key address generator, whereby the key address code in synchronization with said key data signal is the key address code representing the depressed key.

10. An electronic musical instrument as defined in claim **8** in which said means for searching whether said key address code synchronized with said key data signal is already stored comprise a plurality of coincidence circuits which compare the contents of said key address code with those stored already in said key address memories and produce identical binary outputs when these contents coincide with each other, and OR gates which receive the binary outputs of said coincidence circuits.

11. An electronic musical instrument as defined in claim **8** in which said means for searching for an unloaded key address memory comprise a detection circuit for detecting whether said memory is loaded or unloaded, a search counter having a plurality of output lines and producing an output on either one of said output lines, a search clock pulse generator and a logic circuit for passing a search clock pulse to said search counter; when said memory is loaded and blocking the search clock pulse when said memory is unloaded, thereby causing said search counter to stop its counting operation when the output of said detection circuit indicates an unloaded key address memory.

12. An electronic musical instrument as defined in claim **8** in which said means for applying a key address code to a unloaded key address memory comprise, blanking means for passing said key data signal synchronized with said key address code only when said coincidence circuit does not produce an output, and a gate circuit which is controlled by a specific output of said search counter produced when it is suspending its counting operation and which passes the key data signal provided from said blanking means thereby causing said key address codes to be applied to said unloaded key address memory.

13. An electronic musical instrument as defined in claim 8 which further comprises an envelope memory for storing analog samples of an envelope wave shape, an envelope clock pulse generator, and detection means for detecting the storage of said key address code in said address code memory and applying an envelope clock pulse from said pulse generator to said envelope counter thereby causing the envelope to be read from said envelope memory, a modulated musical tone signal being obtained from a product of the musical tone wave shape and the wave shape of said envelope.

14. An electronic musical instrument as defined in claim 13 in which said detection means comprise an envelope counter for applying a readout control signal successively to readout control terminals of said envelope memory through a decoder, means for applying an attack clock pulse to said envelope counter upon depression of the key until said envelope counter has counted a predetermined count thereby reading an attack wave shape portion and thereafter reading a constant amplitude wave shape portion by stopping the counting operation of said envelope counter, and means for applying a decay clock pulse to said envelope counter upon release of the key thereby causing said envelope counter to resume its counting operation and to read the decay wave shape portion, the application of the decay clock pulses being stopped when the reading out of said decay wave shape portion is completed.

15. An electronic musical instrument as defined in claim 14 in which the frequencies of said attack clock pulses and decay clock pulses are selectable.

16. An electronic musical instrument as defined in claim 13 comprising means for detecting, while key address codes are stored in all of the key address memories, an envelope counter among all the envelope counters which is most advanced in its counting operation over a predetermined count, means for stopping said detected envelope counter so as to designate the gate circuit of the key address memory corresponding to the detected envelope counter and means for clearing the detected key address memory and envelope counter upon receipt of the key data signal and thereafter causing a key address code synchronized with said key data signal to be stored in said key address memory.

17. An electronic musical instrument as defined in claim 16 in which said detecting means comprise a truncate counter for each key address memory to which the count of each envelope counter is transferred and means for applying a clock pulse to said truncate counter at a high rate thereby causing said truncate counter to count at a corresponding high rate, whereby the envelope counter which is most advanced in its counting operation is detected by the truncate counter first producing an overflow output.

18. An electronic musical instrument comprising a wave shape memory for storing at least one period of wave shape, a plurality of readout counters which respectively receive a readout pulse having a selected frequency, a plurality of gate circuits provided at the output terminals of said readout counters, a decoder connected to the readout control terminals of said wave shape memory, a ring counter which operates at a high counting rate and provides time-sharing control pulses to each of said gate circuits, and means for applying the output of each readout counter in a time-sharing manner to the readout control terminals of said wave shape memory through said decoder, thus producing a plurality of musical tone wave shapes having frequencies different from each other.

19. An electronic musical instrument comprising a wave shape memory in which sample amplitudes of at least one period of a musical tone wave shape are stored, an envelope memory in which sample amplitudes of an envelope wave shape are stored, a plurality of wave shape readout counters which respectively receive clock pulses having a selected frequency, a plurality of envelope readout counters which respectively receive clock pulses having a selected frequency, and means for applying the outputs of corresponding wave shape readout envelope and readout counters in synchronization with each other and in a time-sharing manner to decoders connected respectively to the readout control terminals of said wave shape memory and said envelope memory and producing at the output terminal of said wave shape memory a voltage representing a product of the wave shape amplitude stored in said wave shape memory and the wave shape amplitude stored in said envelope memory, thereby producing a plurality of musical tone wave shapes with an envelope in a multiplexed form.

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