

[54] **WATCHMAN'S TOUR RECORDING SYSTEM**

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 3,736,561 5/1973 Rumpel 340/147

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[57] **ABSTRACT**

[52] U.S. Cl. **340/173 R**; 340/306; 340/309.1;
 346/59

A watchman's tour recording system which includes a watchman's unit having a clock and a clock signal producing means, a station identification signal producing means, a signal memory and means for directing associated clock and station identification signals to corresponding locations in the signal memory when a watchman connects the unit to each check station along a predetermined tour route. At the end of the tour the unit is connected to a computer terminal and its signal memory is read out into the computer. In this way errors made during the tour, such as stations checked too early, too late, in improper order, or not checked at all, are noted.

[51] Int. Cl.² **G11C 13/00**

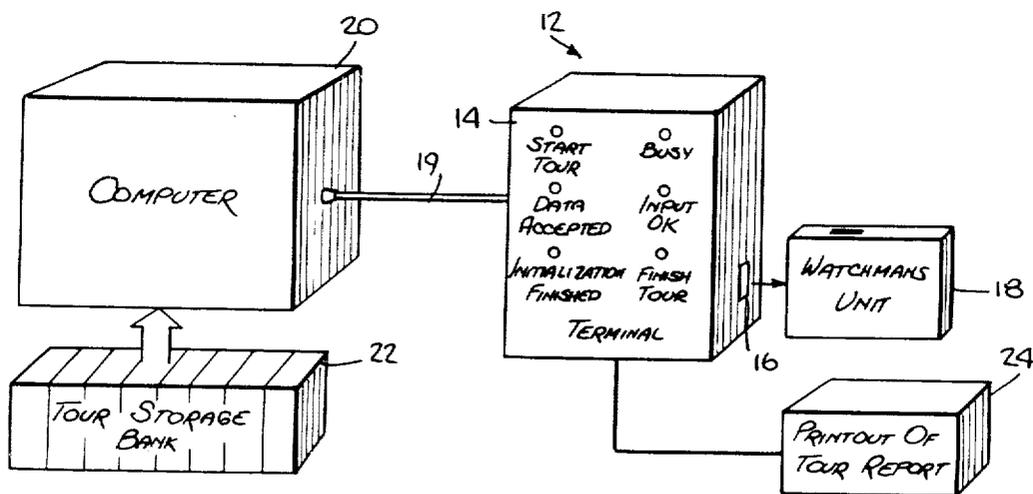
[58] Field of Search 340/173 R, 306, 309.1;
 346/59, 60

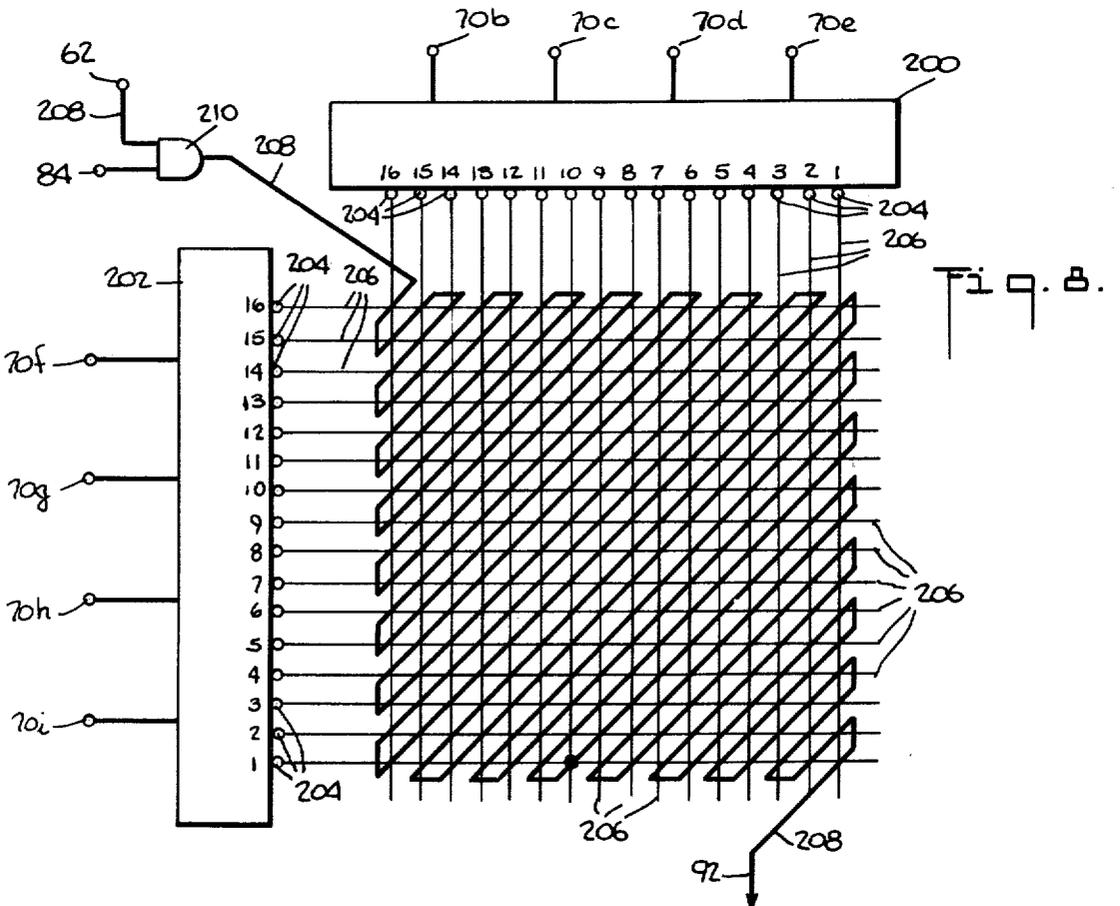
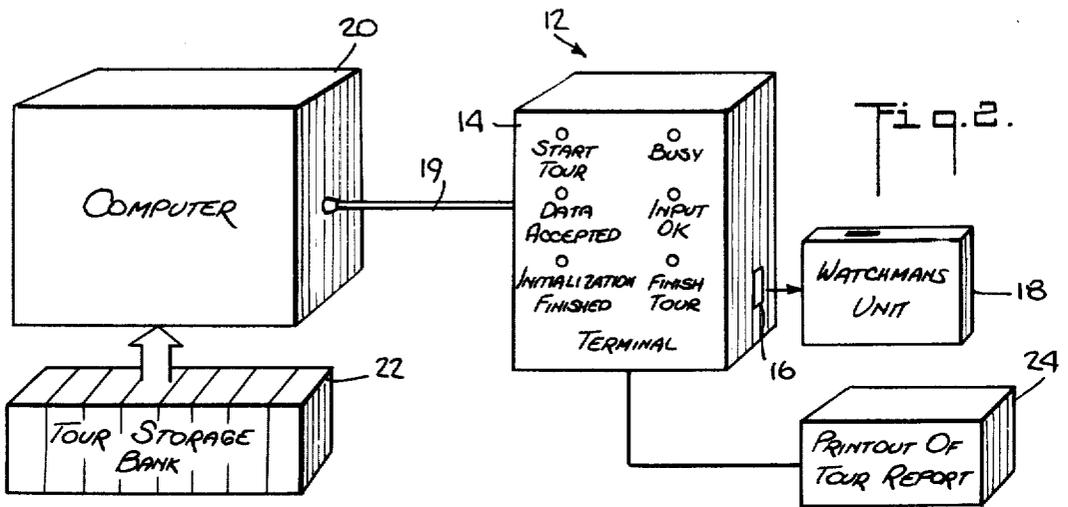
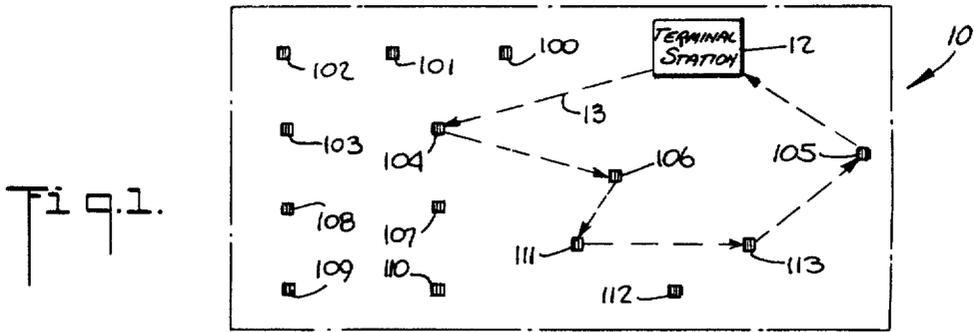
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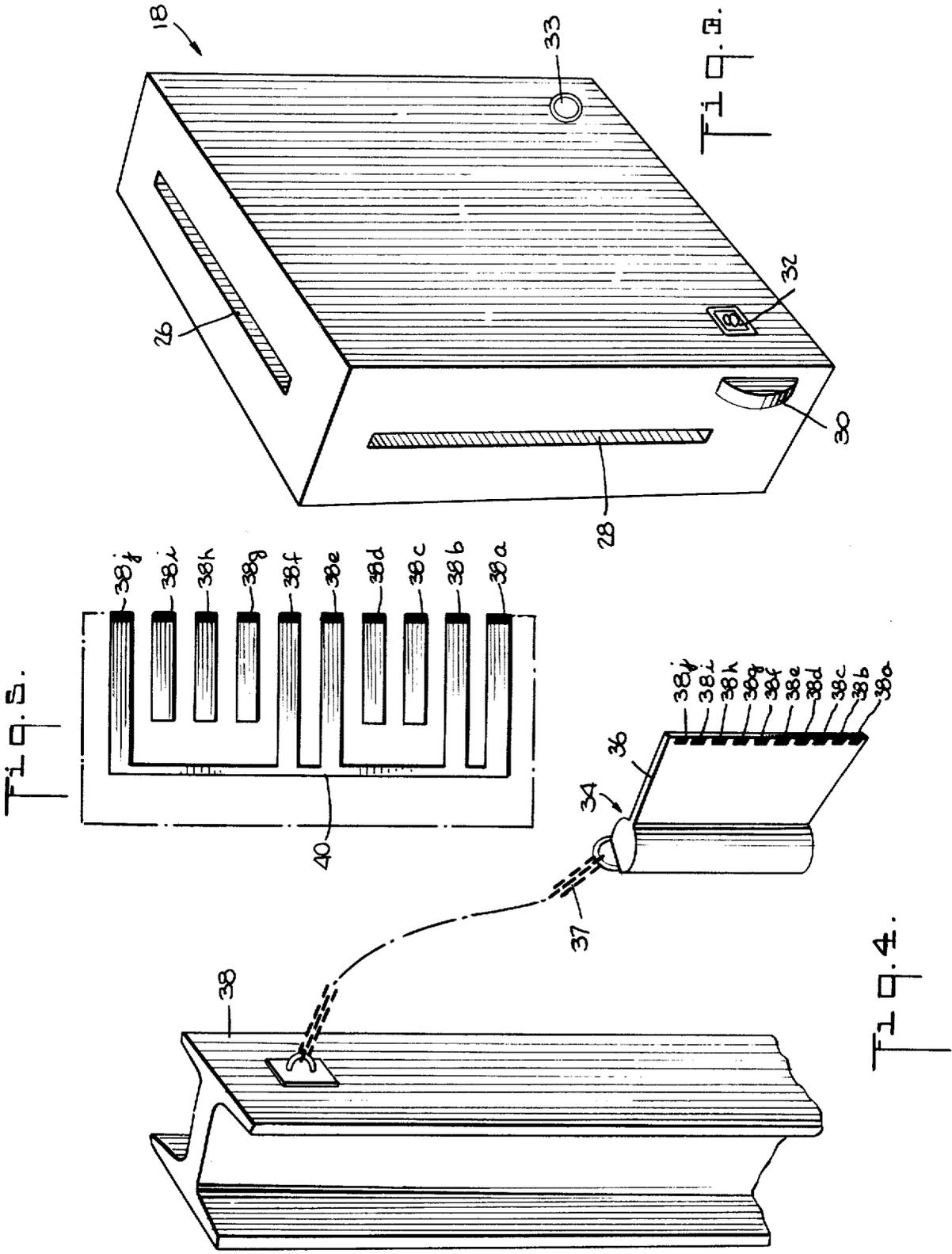
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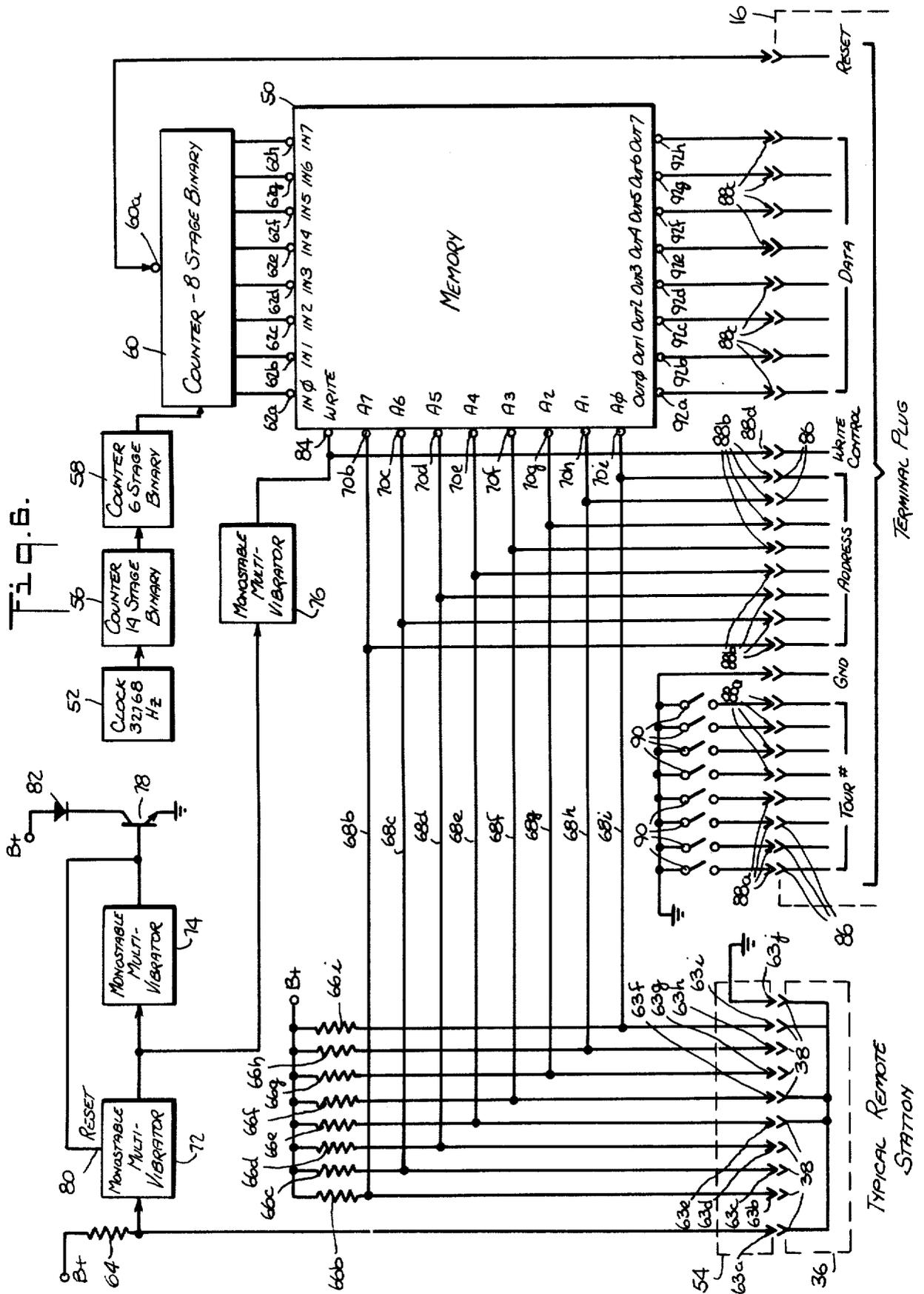
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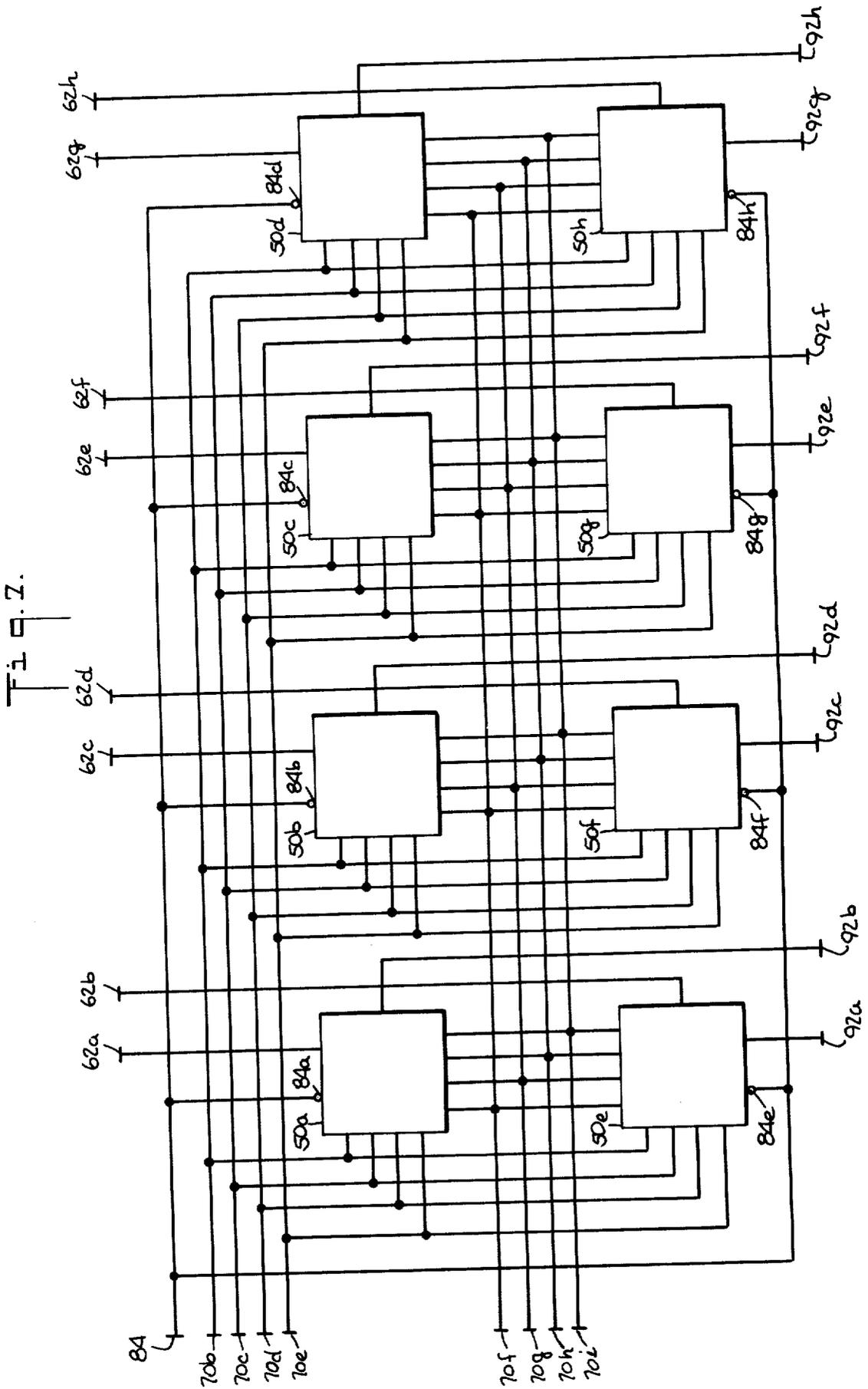
24 Claims, 13 Drawing Figures

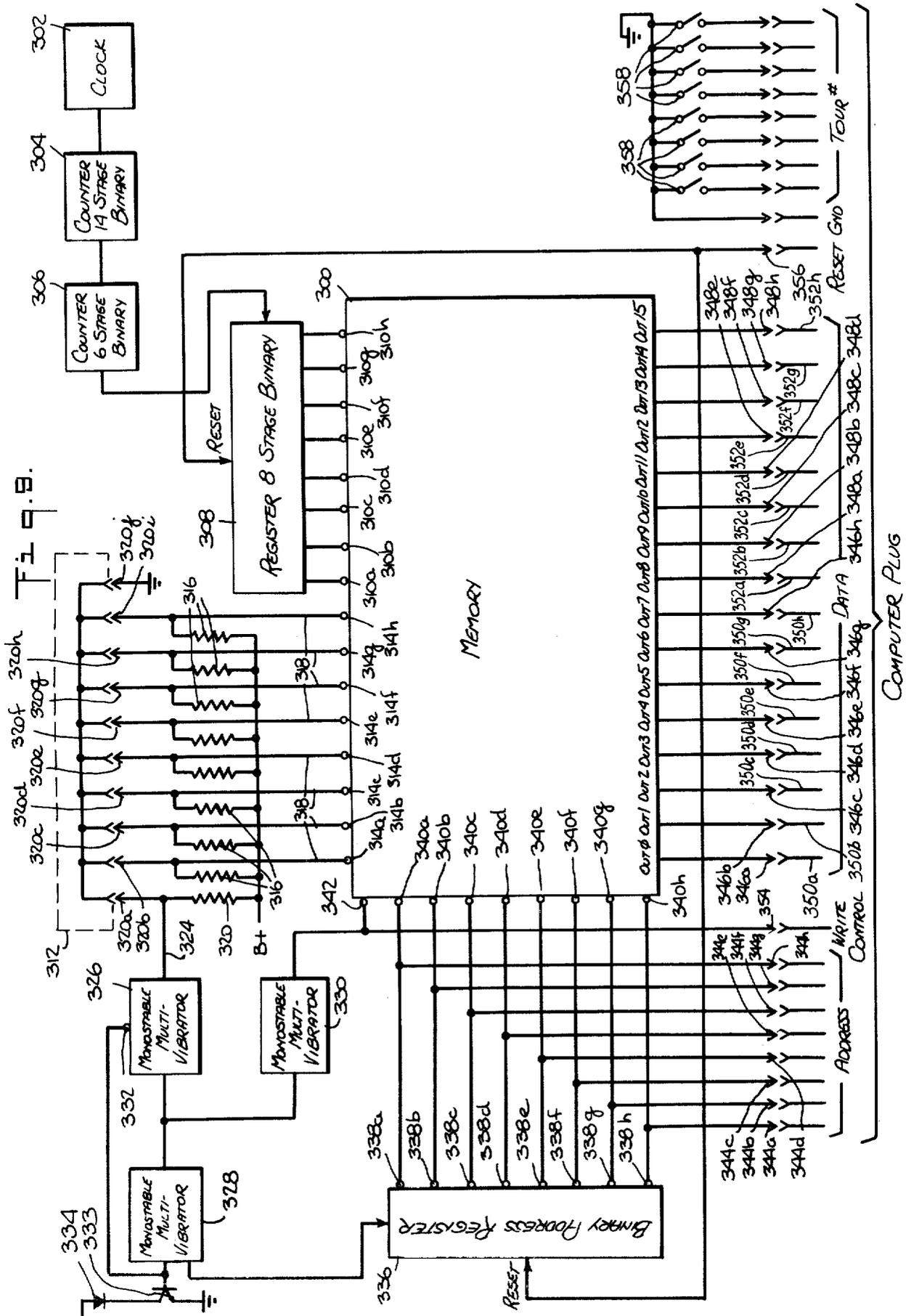












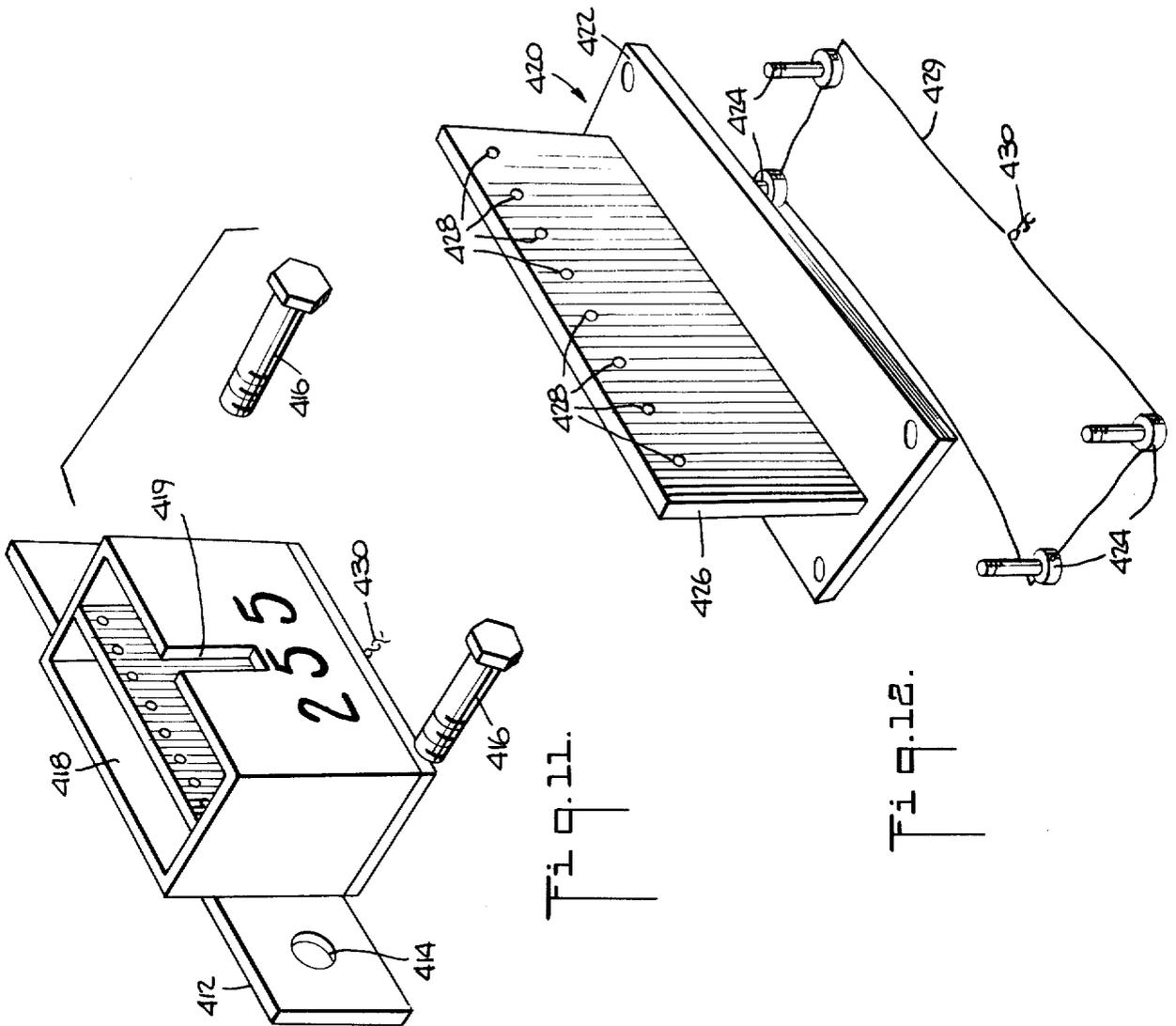


Fig. 11.

Fig. 12.

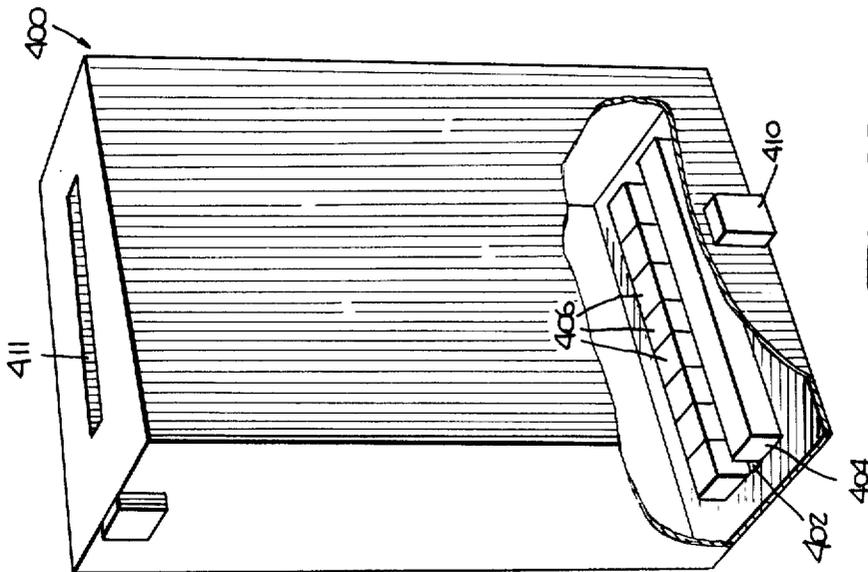
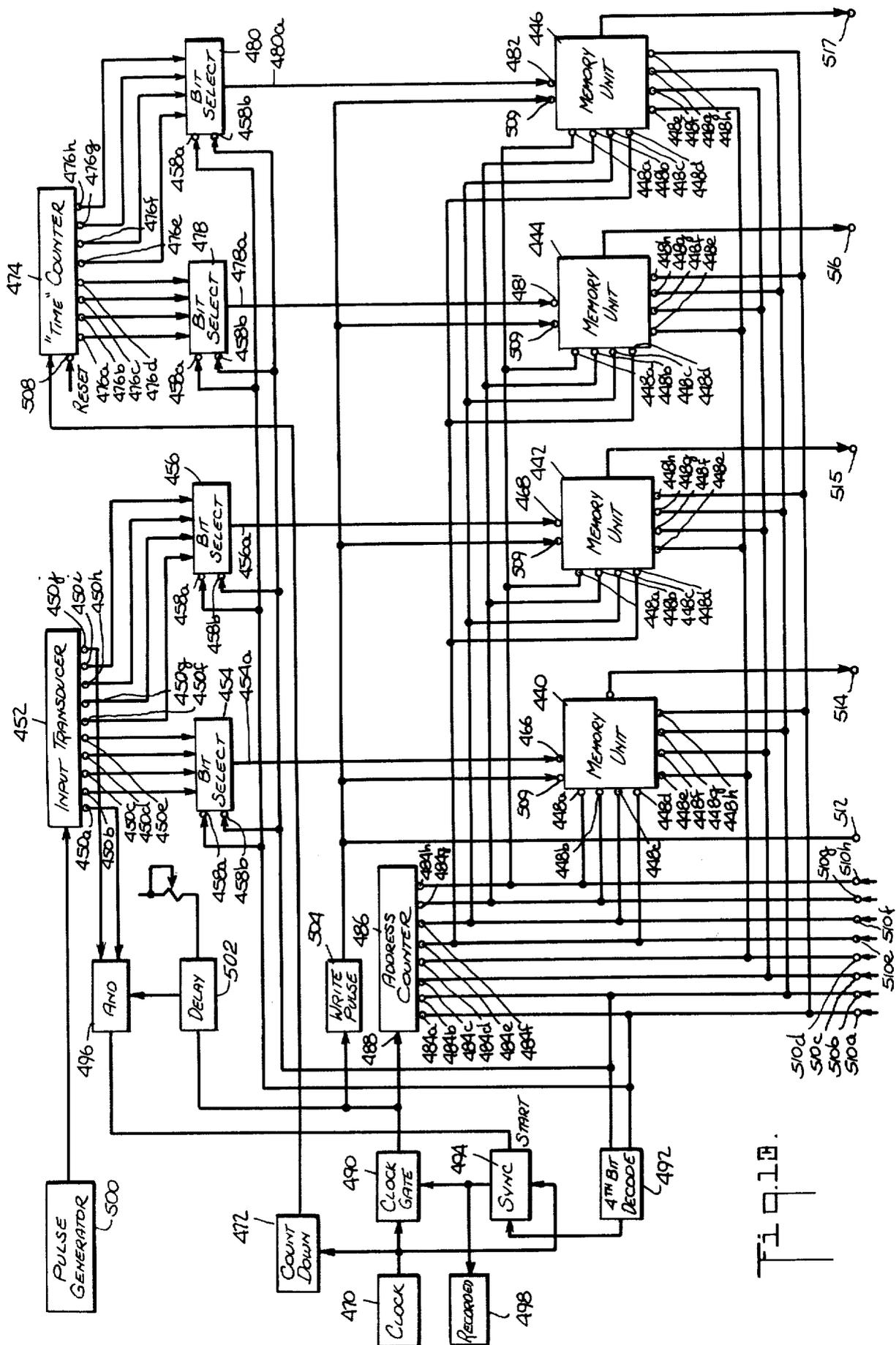


Fig. 10.



WATCHMAN'S TOUR RECORDING SYSTEM**BACKGROUND OF THE INVENTION****1. Field of the Invention**

This invention relates to security systems and more particularly it concerns novel arrangements for recording and checking security tours made by watchman.

2. Description of the Prior Art

In carrying out security checking operations in factories or other commercial establishments, watchmen usually follow a prearranged tour so that critical areas are checked at predetermined intervals and so that a complete coverage of the premises can be ensured. It is important for insurance and other purposes to have a record made of the watchman's tour. In the past this was obtained by providing the watchman with a self-contained recording unit which included a clock and a disk shaped paper which was rotated by the clock. The recording unit was "punched" or connected to special station keys at preselected locations along the watchman's tour. As each punch was made, the key would make an impression on the paper disk. This impression was in the form of a symbol which corresponded to the identity of the station; and the location of the symbol on the disk, which was rotated by the clock, would correspond to the time that station was checked. After the tour had been completed, the paper disk would be removed from the unit and replaced by a new one. By noting the symbols and their locations on the disk, it was possible to ascertain what stations were checked and at what times and in what order they were checked.

While this system provided a permanent record of the watchman's tour, it was limited, from a practical standpoint, to relatively simple tours involving a small number of stations. Where a greater number of stations are involved the process of checking the recorded disks becomes very time consuming and subject to error. Also, the system does not lend itself to the checking of multiple tours, nor is it readily adaptable to tour modifications.

It has been proposed to utilize electronic means and a computer system to overcome the above described limitations of the conventional watchman's clock system. Such proposals are found, for example, in U.S. Pat. Nos. 1,919,007; 2,275,981; 2,308,198; 2,734,791; 3,237,183; 3,371,349 and 3,736,561. These electronic means, however, involved the wiring of each station to be checked to a central computer. While these electronic systems would produce an instantaneous computer readable indication of each station check made by a watchman, they suffer from the disadvantage that the wiring involved makes them quite expensive. Also, a wired system does not lend itself to that type of tour modification which involves relocation of check stations.

SUMMARY OF THE INVENTION

The present invention overcomes these difficulties of the prior art. With the present invention it is possible to provide one or several tours covering a great number of stations; and these tours may be reported and checked accurately and rapidly with computer means. Moreover, with the present invention no special wiring is required between the individual stations and a central location. It is also possible with the present invention to relocate check stations with a minimum of difficulty.

According to the present invention there is provided a tour recording arrangement which is carried in a watchman's unit. This tour recording arrangement includes a clock signal producing means, a station identification signal producing means, a signal storage or memory device and means for directing corresponding clock and station identification signals to particular locations in the memory device each time the watchman connects the unit to a station being checked. Unlike the clock rotated paper disc units of the prior art, the clock signals in the present invention are recorded as actual data in predetermined locations in the memory device. Thereafter, at the end of a tour the watchman's unit may simply be plugged into a terminal and the data stored in its memory device can be read out to provide a complete, accurate and instantaneous report of the tour along with an indication of missed or improperly checked stations or stations checked at the wrong time.

According to one embodiment, the station identification signals direct the clock signals to corresponding locations in the memory device. In another embodiment, the memory device is of sufficient capacity to receive and store both clock signals and station identification signals. In this second embodiment there are provided sequencing means which, upon each station check, directs the station identification and clock signals to corresponding locations in the memory device. It will be appreciated that this arrangement requires no special wiring between the stations and a separate computer. Further, this arrangement allows tour changes to be made without adjustments either to the stations themselves or to the watchman's unit. Also, if desired, individual check stations can be relocated with a minimum of difficulty since no rewiring is necessary.

In a preferred embodiment, signals representative of station identification and time data are supplied to various memory units in a manner which permits maximum use of the storage capacity of the units. More particularly the storage unit address means are scanned in synchronism with registers containing station identification and time data words; and means are provided to continue the storage scan while the registers are scanned repeatedly as successive station checks are made.

There has thus been outlined rather broadly the more important features of the invention in order that the detailed description thereof that follows may be better understood, and in order that the present contribution to the art may better be appreciated. There are, of course, additional features of the invention that will be described more fully hereinafter. Those skilled in the art will appreciate that the conception on which this disclosure is based may readily be utilized as the basis of the designing of other methods and structures for carrying out the purposes of this invention. It is important, therefore, that this disclosure be regarded as including such equivalent constructions as do not depart from the spirit and scope of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Several embodiments of the invention have been chosen for purposes of illustration and description, and are shown in the accompanying drawings forming a part of the specification, wherein;

FIG. 1 is a diagrammatic representation of a watchman's tour route in which the present invention is utilized;

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FIG. 2 is a block diagram showing a computer, computer terminal and watchman's unit in which the present invention is embodied;

FIG. 3 is an enlarged perspective view of the exterior of the watchman's unit of FIG. 2;

FIG. 4 is a fragmentary perspective view showing a check station along the tour route of FIG. 1;

FIG. 5 is a cutaway view showing the interior configuration of a station key forming one portion of the check station of FIG. 4;

FIG. 6 is a schematic and block diagram showing the various interior components of the watchman's unit of FIG. 3;

FIG. 7 is a further schematic and block diagram illustrating in greater detail a memory or storage arrangement forming one of the interior components of the watchman's unit of FIG. 6;

FIG. 8 is a diagrammatic representation of a memory unit forming one portion of the diagram of FIG. 7;

FIG. 9 is a view similar to FIG. 6 but showing an alternate internal configuration of a watchman's unit according to the present invention;

FIG. 10 is a perspective view of a watchman's unit for use with the present invention and employing photoelectric station identifying means;

FIG. 11 is a partially exposed perspective view showing the exterior of a station to be checked by the watchman's unit of FIG. 10;

FIG. 12 is a partially exploded perspective view showing the interior of the station of FIG. 11; and

FIG. 13 is a block diagram showing the interior arrangement of components in the watchman's unit of FIG. 10.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

In FIG. 1, a premises to be protected is indicated schematically by an outline 10. Within the premises there is provided a terminal station 12 from which various guard tours start and end. Also within the premises are several check stations 100-113. The number and location of these stations is preselected in accordance with the particular security requirements of the premises.

In conducting a tour, a watchman begins at the terminal station 12; and then he walks along a preassigned route, as indicated by the dashed lines 13, to preselected check stations. At each station the watchman connects a station key to a watchman's unit which he carries with him. This provides a recording in the watchman's unit of the time of each check which he makes, along with a corresponding identification of the station checked.

The number of stations to be checked in each tour, the order in which stations are checked and the times they are to be checked is established before the watchman's tour begins. For the purpose of maximizing security within the premises, the tour routes are changed periodically. It is the ability to adapt to various tour changes which constitutes one important feature of the present invention.

Upon completion of his tour the watchman returns to the terminal station 12 where, as shown in FIG. 2, there is provided a terminal board 14 having a connector plug 16 thereon. A watchman's unit 18 is shown connected to the terminal board 14 via the connector plug 16. When the watchman completes his tour he connects his unit 18 to the terminal board 14; and the data

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representative of the stations checked and the time of each check made during the tour is fed from the watchman's unit 18 into the terminal board 14. The terminal board 14 is shown to be connected via a cable 19 to a central computer 20. This computer may be remotely located or it may be located at the terminal station 12. A tour storage bank 22 is provided in association with the computer 20. The tour storage bank 22 contains information representative of the stations to be checked for each of several predetermined tours. The tour storage bank 22 may form an integral part of the computer 20 itself. When a watchman's unit 18 is connected to the terminal board 14 to feed actual tour data through the board into the computer 20, ideal data for that particular tour is also fed into the computer from the tour storage bank 22. The actual tour data and the ideal tour data are compared in the computer and any discrepancies which exist are noted and reported. This report may take the form of a printout at the terminal board 14 as indicated at 24 in FIG. 2.

The watchman's unit 18 is a small electronic device which, as shown in FIG. 3, externally resembles a small portable radio. The unit is provided with a terminal connector slot 26 and a station connector slot 28 into which various plugs, such as the connector plug 16 on the terminal board 14 and corresponding plugs at the various stations 100-113 are inserted for reading data into and out from the unit. The unit 18 is also provided with a switch dial 30 which may be turned to any of several positions corresponding to different tours to which the unit may be assigned. A tour identification number, corresponding to the setting of the dial switch 30 appears at a window 32 at the side of the unit. An operation light 33 is also provided on one side of the unit 18 to indicate when data transferred into or out from the unit is complete.

In carrying out a tour, a watchman proceeds from the terminal station 12 and follows a route corresponding to the tour to which his unit 18 has been set. This tour requires that the watchman be present at particular ones of the check stations 100-113 at predetermined times. The presence of the watchman at each station is recorded in his unit when he inserts a station plug into the station connector slot 28 of the unit 18.

A typical check station arrangement is shown in FIG. 4. The check station is provided with a station plug 34 which is anchored, by means of a chain 37 to a post 38 or other structural member on the premises. The station plug 34 includes a projecting card like connector member 36 along one edge of which are provided a plurality of electrical contacts 38a-38j. When the connector member 36 is inserted into the station connector slot 28 of the watchman's unit 18, the contacts 38 make connection to corresponding contacts (not shown) located within the unit. Inside the connector member 36, various ones of the electrical contacts 38 are connected to each other while other contacts have no connection. This provides a code which identifies the particular station. As can be seen in the cutaway view of FIG. 5, the outermost contacts 38a and 38j are connected to a common base strip 40. These outer contacts provide no part of the station code but instead they provide battery connections as will be described more fully hereinafter. As shown, selected ones of the other contacts, namely the second, 38b, the fifth, 38e, and the sixth, 38f, are each connected to the base strip 40. These contacts represent, respectively, a binary 1, a binary 8 and a binary 16, so that together they represent the binary form

of the number 25 which constitutes the identification of the station. Other stations, of course, will have other groups of their contacts **38** connected to the base strip **40**. With the eight contacts **38b** . . . **38i**, being available for binary coding, a total of **256** different station codes are available. A greater number may be provided by increasing the number of contacts. It should be noted that other means of producing coded signals may be substituted; for example the connector member **38** may be provided with spaced apart segments of magnetic material and the watchman's unit may be provided with magnetic sensing means.

As indicated above, the watchman's unit **18** records the time of checking of each station along the watchman's tour. Data representative of the time of checking is provided by means of a clock arrangement carried in the watchman's unit.

The general interior composition and arrangement of the watchman's unit **18** is illustrated schematically in FIG. 6. As can be seen, the unit includes a memory **50**, a clock **52** for supplying time data to the memory and a station signal receiving means **54** for supplying station identification data to the memory. Electrical power is supplied by a self contained battery (not shown) to which various B⁺ and ground connections are made.

The clock **52** is a crystal controlled oscillator which operates at a frequency of 32,768 Hz. The clock output is connected to a fourteen stage binary counter **56** which divides down the clock frequency to 1 Hz, i.e., one pulse per second. The output of the counter **56** is supplied to a six stage second binary counter **58** which divides the clock frequency down even further to one pulse each 2.12 minutes. These pulses are supplied to an eight stage binary register **60**. The stages of this register are connected to eight corresponding time data input terminals **62a**–**62h** of the memory **50**. The count condition of the register **60** changes each 2.12 minutes; and since an eight stage binary register is capable of accumulating a total of 256 counts, the clock and memory system is capable of providing time data to the memory **50** in 2.12 minute increments over a total duration of approximately nine hours. The number of increments and the total duration may be increased by increasing the size of the memory and by decreasing the number of counter stages.

The clock arrangement measures elapsed time from a given point, usually the start of a tour. This point in time is established by having the binary register cleared at the start of the tour. A "clear" signal is applied from the terminal board **14** to a reset terminal **60a** to hold the register cleared until the unit is removed from the terminal board to start the tour.

The station signal receiving means **54** includes a plurality of electrical contacts **63a** . . . **63j**, which, when a station connector member **36** (FIG. 4) is inserted into the station connector slot **28** (FIG. 3) of the unit, make contact with corresponding ones of the connector contacts **38a** . . . **38j**. The outermost contacts **63a** and **63j** are connected, respectively, through a first resistor **64** to B⁺, and to ground. The intermediate contacts **63b** . . . **63i** are connected through associated voltage control resistors **66b** . . . **66i** to B⁺. Each of the intermediate contacts **63b** . . . **63i** is also connected via associated station address lines **68b** . . . **68i** to corresponding station address input terminals **70b** . . . **70i** of the memory **50**.

The outermost contact **63a** is also connected to the input of a first monostable multivibrator **72**. The output

of this multivibrator in turn is connected to the inputs of second and third monostable multivibrators **74** and **76**. The output of the second multivibrator **74** is connected both to the base of a control transistor **78** and to a reset terminal **80** of the first monostable multivibrator. A light emitting diode **82** is connected in series with the emitter and collector terminals of the control transistor **78** between B⁺ and ground. The light emitting diode forms the operation light **33** (FIG. 3) of the watchman's unit. The third monostable multivibrator **76** is connected to a write input terminal **84** of the memory **50**.

The first monostable multivibrator **72** responds to a decrease in voltage at the first contact **63a**, which occurs upon connection to a station connector **36**, to produce a rather short output pulse, e.g., of 10–15 milliseconds. The purpose for this pulse is to cause a time delay sufficient to allow settlement of all transients which occur upon making connection to the station connector **36**. The second and third monostable multivibrators **74** and **76** both respond to the trailing edge of the pulse produced by the first monostable multivibrator **72**. The output of the second monostable multivibrator **74** is also in the form of a pulse but this pulse lasts for a much larger period of time, e.g., 15 seconds. This pulse maintains the first monostable multivibrator **72** in its reset condition so that a double reading will not be fed into the memory **50** if the connector contact is broken and reestablished more than once while a station is being checked. In normal use the connector **36** will be removed well in advance of the 15 second delay interval; and yet this delay interval should expire long before the watchman reaches a subsequent station for taking a new reading.

During the pulse output interval of the terminal monostable multivibrator **74** the control transistor **78** is maintained conductive so that current flows through it and through the light emitting diode **82** causing it to illuminate and signal the entry of data into the memory **50**.

The trailing edge of the output pulse from the first monostable multivibrator **72** also triggers the third monostable multivibrator so that it produces a short gating pulse which is applied to the memory **50**. This pulse allows information which is present at the time data input terminals **62a** . . . **62h** to be fed into the memory at locations corresponding to the data present at the station address input terminals **70b** . . . **70i** of the memory **50**.

In summary, it will be seen that with the trigger arrangement described above, a reading is taken by inserting a connector **36** into the unit to trigger the monostable multivibrators **72**, **74** and **76** in a particular sequence so that a write input terminal **84** of the memory **50** is energized a short time following insertion of the connector. Also, during this time the light emitting diode is illuminated to show that the reading is being taken.

During the taking of each reading, a different combination of time signals and station signals is present at the terminals **62** and **70** of the memory **50**. These time signals are directed into the memory in accordance with their associated station signals, so that the time each station was checked can be read out after completion of a tour. Thus, at the end of a tour there will be stored in the memory **50** as many time signals as the number of stations checked in a tour. The memory **50**, having eight address input terminals **70b** . . . **70i**, is ca-

pable of accepting as many as 256 different binary signal combinations which corresponds to a total of 256 different stations. In an actual tour, substantially less than this number of stations would be checked.

At the end of the tour, the watchman's unit 18 is returned to the terminal station 12 and is connected to the terminal board 14 by inserting its connector plug 16 into the terminal connector slot 26 of the unit. The terminal connector plug 16, which is represented schematically in FIG. 6 has terminal connectors 86 which contact corresponding connectors 88 in the unit. A first group of these connectors 88a are connected via switches 90 which are opened and closed by operation of the switch dial 30. The particular combination of these switches which are closed corresponds to the identification number of the tour just completed; and this information is read into the terminal board 14 and the computer 20 so that a corresponding ideal tour will be selected from the tour storage bank 22 for comparison in the computer with the data to be read out from the watchman's unit. A second group of connectors, 88b, is connected to the station address input terminals 70b . . . 70i of the memory 50 to apply interrogation signals from the computer to the memory 50 for reading its contents in prescribed fashion into the computer. A third group of connectors 88c is connected to time data output terminals 92a . . . 92h of the memory 50. These last mentioned terminals correspond respectively, to the time data input terminals 62a . . . 62h of the memory and they become energized in accordance with the energization of their respective data input terminals when interrogation addresses from the terminal board are applied in the same manner as the station address signals when the unit was connected to a particular station. A writeout connector 88d is connected to the write input terminal 84 to receive signals from the computer which cause writeouts from the memory to be transferred to the computer at proper times.

The computer 20 is set up using known techniques to interrogate the memory 50. In doing this the computer presents in succession signals corresponding to the identification of the different stations along the tour which has been completed. These signals are applied to the address input terminals 70b . . . 70i. A writeout signal is also applied via the contact 88d and the write input terminal 84 and the memory 50 then presents the stored time data corresponding to each identified station. This information, which appears at the data output terminals 92a . . . 92h is then compared in the computer with corresponding information supplied from the tour storage bank 22. Any discrepancies noted by the computer are then identified and reported on a printout or in any other desired manner.

In the arrangement of FIG. 6, the station identification signals supplied to the terminals 70 of the memory 50 serve to direct the time data signals present at the terminals 62 to particular locations in the memory. This may be carried out with the arrangements shown in FIGS. 7 and 8. As shown in FIG. 7, the memory 50 includes eight memory units 50a . . . 50h. Each of the station address input terminals 70b . . . 70i is connected to a corresponding location on each of the memory units 50a . . . 50h. Thus, whenever a station identification code is present on the station address lines 68b . . . 68i (FIG. 6) this same code is applied in the same manner to each of the memory units 50a . . . 50h.

Each of the memory units 50a . . . 50h is also connected to a different one of the time data input termi-

nals 62a . . . 62h. Thus while each of the memory units 50a . . . 50h receive the same station identification signals they each receive a different portion of the time signals.

The write input terminal 84 is also connected to write terminals 84a . . . 84h on each of the memory units 50a . . . 50h. Also each of the memory units 50a . . . 50h is connected to a different one of the time data output terminals 92a . . . 92h for readout to the computer.

FIG. 8 shows, by way of example, one form of memory unit which may serve as one of the memory units 50a . . . 50h. As shown in FIG. 8 there are provided first and second four stage binary decoders 200, 202. The first four station address input terminals 70b, 70c, 70d and 70e are connected as inputs to the first decoder 200 while the second four station address input terminals 70f, 70g, 70h and 70i are connected as inputs to the second decoder 202. Each decoder is capable of responding to each possible combination of binary input signals at its input terminals to energize a different one of sixteen output terminals 204. Memory lines 206 extend in parallel fashion from each of the terminals 204, with those from the first decoder 200 being arranged at right angles to those of the second decoder 202. This arrangement provides a matrix of 256 different line intersections; and for each overall combination of binary signals applied to the two decoders 200, 202 a particular one of the horizontal lines and a particular one of the vertical lines 206 are energized and their mutual intersection is made receptive to retention or memory of applied input signals. A read-write line 208 extends diagonally over the memory matrix crossing each of the 256 intersections in succession. This read-write line is connected both to one of the time data input terminals 62 and the one of the data output terminals 92. A gate 210 is interposed in the read-write line 208. This gate has one input connected to the write input terminal 84 to prevent time signals from being applied to the memory unit until a write signal is applied.

Memory means (not shown), such as magnetic ferrite cores having high hysteresis characteristics, are provided at each intersection defined by two of the memory lines 206 and the read-write line 208. Whenever the three lines defining an intersection are simultaneously energized, the memory means changes its state or condition; and it retains its new state or condition after any or all of the memory lines and read-write line are deenergized. Additional means (not shown) may be provided for deenergizing the memory means to clear the unit between uses.

It is to be understood that the particular memory arrangement illustrated in FIG. 8 is shown only by way of example only and that other units capable of storing bit data at various locations therein, can be substituted.

With the memory arrangement of FIG. 7 it will be seen that as each station is checked, the station identification signals produced by the station connector serves to direct the time signals then occurring to particular locations within the group of memory units 50a . . . 50h. The same memory unit may also store time signals for each of the other stations. Since each unit is provided with 256 different locations for receiving time signals a total of 256 different station checks may be recorded in the eight memory units.

Upon completion of a tour the watchman's unit is read out into the computer by applying different station signal codes successively to each of the memory units 50a . . . 50h; and, during the application of each station

signal code, applying a signal to the write input terminal **84**. If one or more of the memory units **50a . . . 50h** has an energized memory element at the intersection or bit location therein corresponding to the applied station signal code, a signal will be produced at the data output terminals **92** of that particular unit. Meanwhile no signal will be produced at the corresponding data output terminals of the other units. Thus by successively applying interrogation signals corresponding to all of the stations, the particular stations which were checked and the time of each such check will be identified by the computer.

It will be appreciated that the system of FIGS. 6-8 makes use of station identification signals as address means to direct the time signals into different locations in the memory. For some applications it may be preferable to provide a memory into which the time signals and the corresponding station identification signals are both supplied to a memory as stored data. In such case each station's identification signal would be stored in the memory alongside a corresponding time data signal which occurred when the station was checked.

FIG. 9 shows an arrangement for storing both time and station identification signals as data into a memory. As shown in FIG. 9, there is provided a two hundred fifty six by sixteen bit memory **300**. This memory is similar to that of FIG. 8 except that it comprises sixteen memory units each having eight address terminals. Eight of the memory units store the different bits of eight bit time data words while the other eight units store the different bits of eight bit station identification data words. Time data word signals are provided by a clock **302** whose output pulses are divided by first and second binary counters **304** and **306**. The divided pulses from these counters are supplied to an eight stage binary register **308** as in the preceding embodiment; and the outputs from each stage are supplied to corresponding time input data terminals **310a . . . 310h**, shown on the upper right hand side of the memory **300**. These terminals are connected as data inputs to eight memory units similar to the memory units of the preceding embodiment.

Station identification signals are applied from a station key **312**, as in the preceding embodiment and these signals, which are also in binary digital form, are applied to corresponding station identification input terminals **314a . . . 314h**, shown on the upper left hand side of the memory **300**. The station identification signals may be generated as in the preceding embodiment. Thus as shown in FIG. 9 there is provided a common B⁺ connection via individual resistors **316** to corresponding lines **318** interconnecting the various terminals **314a . . . 314h** to associated station key contacts **320b . . . 320i**.

Address signals are produced each time a connection is made to a station key. These address signals serve to direct both the time data input signals and the associated station input signals to corresponding locations in the memory **300**. As shown in FIG. 9, an additional resistor **320** is connected between B⁺ and a station key contact **320a**. A trigger line **324** extends from a junction between the resistor **320** and the contact **320a**, to a first monostable multivibrator **326**. The first monostable multivibrator is connected to second and third monostable multivibrators **328** and **330**. As in the preceding embodiment the first monostable multivibrator **326** provides a short delay so that electrical transients, which occur when a station key is connected to the

unit, can expire. Thereafter, the trailing leg of the output signal of the first monostable multivibrator **326** triggers both the second and third multivibrators **328** and **330**. The second multivibrator **328** produces a first output which lasts for about fifteen seconds, and thereafter it produces a second output. The first output is fed back to a reset terminal **332** of the first multivibrator **326** to hold that multivibrator in its reset condition thereby preventing it from responding to subsequent inputs during the fifteen second interval. The first output from the second multivibrator **328** is also applied to the base terminal of a control transistor **333** connected in series with a light emitting diode **334** between B⁺ and ground. This causes the light emitting diode to illuminate while the time data and station identification signals are being entered into the memory. At the end of the fifteen second interval, i.e., after data has entered the memory **300**, a second output from the second monostable multivibrator **328** is applied to a binary address register **336**. This register has a plurality of stages each connected via an address control line **338a . . . 338h** to a corresponding address input terminal **340a . . . 340h** of the memory **300**. Upon completion of time and station data entry into the memory **300**, the second output from the second monostable multivibrator **328** causes the binary address register to energize a new combination of its address control lines **338a . . . 338h**. These signals control the address portion of the memory **300** so that the next subsequently applied data input signals will be directed to different locations in the memory.

The actual application of data input to the memory **300** is controlled by the third monostable multivibrator **330** which applies a "write" pulse of short duration to a write input terminal **342** of the memory in response to the trailing edge of the pulse from the first multivibrator **326**.

It will be appreciated from the foregoing that while a larger number of memory units is employed in the arrangement of FIG. 9 than is required in the arrangement of FIGS. 6 and 7 for a corresponding number of time and station possibilities, it is possible with the arrangement of FIG. 9 to use memory units of smaller capacity. This is because in most situations a watchman would be expected to make much less than 256 different station checks during a tour. In the more usual situation, where less than 64 different checks are to be made, the sixteen memory units of the memory **300** would only need to have bit capacities of 64. In such case the binary address register would have to have only six different stages rather than the eight stages indicated in FIG. 9.

A further feature of the memory arrangement of FIG. 9 is that it permits the unit to record successive checks of the same station at different times during the course of a tour. This is achieved by virtue of the fact that each check made opens a different location in the memory for receipt of both station identification and time data; and identical station identification data can therefore be accommodated in the different locations of the memory.

The arrangement of FIG. 9 is accommodated for reading recorded data into the terminal board **14** (FIG. 2) in the same manner as in the preceding embodiment. Thus there is provided a plurality of address interrogation contacts **344a . . . 344h** connected, respectively, to the address input terminals **340a . . . 340h** to receive interrogation signals from the computer. There is

also provided a plurality of station data output terminals 346a . . . 346h and a plurality of time data output terminals 348a . . . 348h connected, respectively, to corresponding contacts 350a . . . 350h and 352a . . . 352h for transferring recorded time and station identification data into the computer from those locations in the memory corresponding to the particular address interrogation signals applied to the memory from the computer. The actual readout of data is controlled by a "write" signal from the computer applied through a write input terminal 354 to the write input terminal 342 of the memory.

Reset pulses are applied from the terminal board 14 (FIG. 2) through a reset terminal 356 to both the binary register 308 and the binary address register 336. These pulses are applied to the unit upon the start of each tour so that the production of elapsed time signals will coincide with the start of the tour and so that the address portion of the unit will be set to insert the data from the first station check into the first memory location.

The unit of FIG. 9 is also provided with tour indication switches 358 which are set in accordance with an assigned tour and which, when connected to the terminal board 14, serve to provide signals to the computer for indentifying the tour plan for which the data in the memory should correspond.

FIGS. 10-13 show a modified version of a watchman's unit and check station which has been designed for commercial application. This modified version, which is described and claimed in a copending application, Ser. No. 504,764 filed Sept. 10, 1974 in the name of W. G. Lawrence, et al, differs from the above described versions, firstly in that it employs photoelectric means for generating station identification signals, and secondly, in that it employs memory units in a novel arrangement so that for certain applications their storage capabilities may be utilized more fully and more efficiently than in the preceding embodiments.

In FIG. 10 there is shown a watchman's unit 400 whose external configuration is similar to that of the preceding embodiment. In the present embodiment however there is provided a station key slot 402 at the lower end with a light source 404 extending along one side of the slot and a plurality of photocells 406 distributed along the other side. A switch (not shown) is arranged near the bottom of the slot to turn on the light source 404 when a station key is inserted into the slot 402. A guide lug 410 is also provided near the lower edge of the unit to prevent improper placement of station keys in the slot.

A similar key slot 411 is provided at the upper end of the device for connection to a terminal board at the end of each tour.

FIG. 11 shows a station key arrangement for checking by the watchman's unit 400. This station key arrangement comprises a base plate 412 having holes 414 near each end through which bolts or rivets 416 pass to anchor the arrangement to a structural member or other solid anchor means at a predetermined location in the premises to be checked. A box-like housing 418 is attached to the base plate 412. This housing is opened at the top and is shaped to allow the lower end of the watchman's unit 400 to fit down into it. The front side of the housing 418 is notched at 419 to accommodate the guide lug 410 of the watchman's unit. An identification numeral may be printed on the front of the housing for visual identification of the station.

FIG. 12 shows a station connector assembly 420 which fits into the bottom of the box-like housing 418 of FIG. 11. The connector assembly 420 includes a horizontal bottom plate 422 which fits up against and closes the bottom of the housing 418. The bottom plate 422 is held in place by means of screws 424.

A card like connector element 426 extends upwardly from the center of the bottom plate 422 within the housing 418. As shown in FIG. 12 this connector element is provided with a series of spaced apart holes 428, some of which are filled with a light transparent substance and others of which are filled with a light opaque substance. The particular arrangement of light transparent and light opaque holes forms a binary coding arrangement which identifies the station.

The coding arrangement of the connector element 426 is not readily visible so that it is not susceptible to counterfeiting should a watchman wish to enter false data into the recorder unit. In addition the particular code for the station may be changed by removing the bottom plate and connector unit and replacing it with a new one. A wire 429 may be passed through holes in the screws 424 and fastened with a seal 430 to prevent surreptitious removal of the bottom plate and connector element.

In making a station check, the watchman's unit 400 is fitted into the box-like housing 418 at the station so that the connector element 426 fits into the station key slot 402. When this occurs, the light source 404 is switched on. Light from the source 404 passes through those holes 428 of the connector element which are selectively fitted with a light transparent substance to energize the photocells 406 which are adjacent the light transparent holes. Those photocells which are adjacent the light opaque holes do not become energized. The pattern or arrangement of electrical outputs from the energized and non energized photocells corresponds to the station code; and this output is used for data recording in the watchman's unit.

FIG. 13 shows in block diagram form an alternate arrangement of components within the watchman's unit. In the arrangement of FIG. 13 both station identification and time data signals are inserted into particular memory locations; however the full capacity of only four 256 bit memories is utilized in the recording of 64 station checks. Also with the arrangement of FIG. 13, the same station may be rechecked at different times during a tour and each check will be properly and unambiguously recorded in the storage means.

As shown in FIG. 13, there are provided four 256 bit memory units 440, 442, 444 and 446. Each memory unit includes eight address terminals 448a . . . 448h which control, according to the arrangement of signals applied thereto, the locations within the unit where data information is stored.

Station identification information is generated in binary coded digital form upon the connection of the watchman's unit to check station as described above. This information is presented in binary digital form at various outputs 450b . . . 450i of an input transducer 452. This transducer may, for example, include the photocells 406 of FIG. 10. The outputs from the transducer 452 are arranged into two groups 450b . . . 450e and 450f . . . 450i and are supplied, respectively, to bit select units 454 and 456. These bit select units each have two address terminals 458a and 458b; and, depending on the particular arrangement of binary signals applied to these address terminals, the bit selection

units 454 and 456 will permit a different one of the applied outputs 450 to pass through to a single data input line 454a and 456a respectively. Actually, as will be seen, the binary signals are binary forms of successive counts from one to four so that the bit selections scan the outputs 450 and successively pass each of them through the selectors to their single output. The data input lines 454a and 456a are connected to data input terminals 466 and 468 of the two memory units 440 and 442.

Time data information is generated by means of a clock 470 which generates a continuous series of accurately spaced impulses. A binary counter or "Count Down Circuit" 472 receives these pulses and produces a predetermined submultiple thereof. These divided down pulses are applied to a time counter 474, which may be a multiple stage binary register or accumulator having a plurality of output terminals 476a . . . 476h. The pattern of energization of these terminals, as in the preceding embodiments, represents the total accumulated pulse count from the divider 472; and this in turn corresponds to the elapsed time since the clearing of the time counter 474. The first four terminals 476a . . . 476d are connected to a third bit select unit 478 while the second four terminals 476e . . . 476h are connected to a fourth bit selector unit 480. These two bit selector units operate in the same manner to direct different ones of their applied signals through them to single output data lines 478a and 480a in accordance with binary signals applied to address terminals 458a and 458b thereon. These data lines are connected respectively to data input terminals 481 and 482 of the memory units 444 and 446.

The eight address terminals 448a . . . 448h of the memory units 440, 442, 444 and 446 serve to direct data signals from the bit selection units 454, 456, 478 and 480 to particular ones of the 256 different locations within the memory units.

Corresponding ones of the address terminals of each of the memory units are connected to an associated output terminal 484a . . . 484h of an address counter 486. This address counter has an input terminal 488 connected through a clock gate 490 to the clock 470. As clock signals pass through the gate 490 they are accumulated in the address counter 486 and cause its output terminals 484a . . . 484h successively to change the pattern of their energization, thereby successively changing the bit locations within the memory 440, 442, 444 and 446 which can receive and store data input signals. The address counter 486 is arranged to count in conventional binary form with the first terminals 484a corresponding to the least significant digit and the last terminal 484h corresponding to the most significant digit. The two least significant digit output terminals 484a and 484b of the address counter 486 are connected to corresponding address terminals 458a and 458b of each of the four bit selector units 454, 456, 478 and 480. It will be appreciated that as successive pulses are applied to the address counter 486 to step it through a complete address count sequence, the bit selectors, which are of a much smaller count capacity, recycle, i.e., scan through their selection range successively a number of times. It will further be appreciated that the address counter with its eight output terminals can produce a total of 256 different addresses, corresponding to the number of bit locations in each of the memory units 440, 442, 444 and 446. The bit selector units 454, 456, 478 and 480, on the other hand, are ca-

pable of accumulating only four counts, to direct their four applied inputs in succession to their single output. Thus, as 256 clock pulses are applied successively to the address counter 486, 64 four bit words are successively transferred from the station identification input transducer 452 and the time counter 474 into each of the various memory units. Actually, the two memory units 440 and 442 cooperate by storing different halves of the eight bit words constituting each complete station identification data signal, while the other two memory units 444 and 446 cooperate by storing different halves of the eight bit words constituting each complete time data signal.

The two least significant bit output terminals 484a and 484b of the address counter 486 are also connected to a fourth bit decode counter 492 which produces a stop pulse for application to a SYNCH circuit 494 each time the address counter 486 has been stepped through four address changes. Signals from the clock 470 are also applied to the "SYNCH" circuit 494 and are used to control the clock gate 490.

The station input transducer 452 is provided with output terminals 450a and 450j connected to a start AND gate 496. Outputs from this gate are also applied through the SYNCH circuit 494 to the clock gate 490. A "Recorded" indicator light 498 is connected to the output of the SYNCH circuit 494 to record the insertion of data from the station input transducer 454 and the time counter 474 into their respective memory units 440, 442, 444 and 446. A pulse generator 500 is provided at the station input transducer to produce the signals applied to the AND gate 496. A delay circuit 502 is connected to the output of the clock gate 490; and this circuit serves to close the AND gate 496 for a duration at least as long as necessary to complete a station check. This serves to prevent anomalous readings from transients or other extraneous effects which might cause different signals to be applied through the station input transducer 454 while a station reading is being taken.

The output of the clock gate 490 is also applied to a "WRITE PULSE" circuit 504 which in turn is connected to a write input terminal 509 of each of the memory units 440, 442, 444 and 446.

In operation of the above described system a reset pulse is applied to a reset terminal 508 of the time counter 474 to clear that counter at the start of a watchman's tour. As the watchman proceeds along his tour, the clock produces a continuous series of accurately time pulses, and these pulses, as divided down by the "COUNT DOWN" circuit 472 are accumulated in the time counter 474. The pattern of energization of the time counter output terminals 476a . . . 476h, which corresponds to elapsed time, is applied to the third and fourth bit select units 478 and 480.

When the watchman connects his unit to the first station to be checked, a pulse is generated by the pulse generator 500 and the station input transducer 452 is caused to energize its station identification terminals 450b . . . 450i in accordance with a binary digital code representative of the station identity. This code is applied to the terminals of the first and second bit select units 454 and 456.

The station input transducer also produces a signal via the AND gate 496 to a START terminal of the SYNCH circuit 494. This allows the next subsequent clock signal to pass through the SYNCH circuit and open the clock gate 490. The following clock signals

then pass through the clock gate and step the address counter 486 along so that it successively addresses different storage locations in the four memory units 440, 442, 444 and 446. At the same time, and in synchronism with this address stepping, the signals from the least significant digit outputs 484a and 484b of the address counter 486 are applied to the four bit select units 454, 456, 478 and 480 causing them successively to transmit the signals present on each of their four inputs to different locations within the associated memory units 440, 442, 444 and 446.

When four clock pulses have occurred, the bit select units will have scanned each of their four inputs. Also at this time, the fourth bit decode counter 492 will produce a signal at the STOP terminal of the SYNCH circuit 494 so that no further stepping of either the address counter or the bit select units will take place. During the stepping of these units, the clock pulses which pass through the clock gate 490 also activate the WRITE PULSE circuit 504. This circuit supplies pulses to write input terminals 509 at each of the memory units 440, 442, 444 and 446 to allow those units to accept information present on their respective data input terminals 466, 468, 481 and 482, and to store that data in locations corresponding to the signal pattern at their address terminals 448a . . . 448h.

It will be appreciated from the foregoing that it is possible with the system described herein to store correlated time and station identification data, each having eight bit word lengths, into 256 bit memory units in such a manner that the memory units are used in a most efficient manner for maximum data storage capacity.

Information may be read out of the memory units when the watchman's unit is connected to a computer terminal board as in the case of the preceding embodiments. In such case address interrogation signals are applied from the computer terminal board to address interrogation terminals 510a . . . 510h connected, respectively, to each of the memory unit address terminals. Write signals are also applied from the computer terminal board through a write input terminal 512 to the write input terminals 509 of the memory unit. Data outputs from the memory units is supplied via station identification and time data output terminals 514, 515, 516 and 517 respectively.

Having thus described the invention with particular reference to the preferred forms thereof, it will be obvious to those skilled in the art to which the invention pertains, after understanding the invention, that various changes and modifications may be made therein without departing from the spirit and scope of the invention as defined by the claims appended hereto.

What is claimed and desired to be secured by letters patent is:

1. A watchman's unit for recording the checking of stations by a watchman, said unit comprising, memory means having a plurality of locations therein for storing signals applied thereto, clock means for generating time signals corresponding to elapsed time following an applied reset signal, station detector means for producing station signals corresponding to the identity of a station upon connection of the unit to a station being checked, and address means operative in response to the production of station signals to direct the time signals being generated to a particular location in said memory means.

whereby each location in said memory means which receives a time signal corresponds to the particular station which was being checked during the occurrence of said time signal.

2. A watchman's unit according to claim 1 wherein said memory is a digital bit storage device and wherein said clock means is operative to produce said time signals in binary coded digital form.

3. A watchman's unit according to claim 1 wherein said station detector means is operative to produce said station signals in binary coded digital form.

4. A watchman's unit according to claim 1 wherein said clock means comprises, an oscillator for producing a continuous series of pulses,

binary counter means connected to the output of the oscillator for dividing down the number of pulses and a multiple stage binary register having outputs at each stage, the condition of said outputs corresponding to a binary coded digital representation of said elapsed time.

5. A watchman's unit according to claim 1 wherein said unit includes data entry means comprising means for generating a write pulse duration at a predetermined time following connection of said unit to a check station and means for applying said pulse to a write input terminal of said memory means.

6. A watchman's unit according to claim 5 wherein said means for generating a write pulse comprises first and second monostable multivibrators, said first monostable multivibrator being connected to be actuated upon connection of said watchman's unit to a check station

and said second monostable multivibrator being connected to be energized by the resetting of said first monostable multivibrator and means applying the output of said second monostable multivibrator to said write input terminal.

7. A watchman's unit according to claim 6 wherein said unit includes

a third monostable multivibrator connected to be actuated by said resetting of said first monostable multivibrator

and an indicator connected to be actuated by said third monostable multivibrator.

8. A watchman's unit according to claim 7 wherein said first monostable multivibrator is connected to be held in reset condition by said third monostable multivibrator.

9. A watchman's unit according to claim 1 wherein said address means is operative to direct said time signals being generated to locations in said memory means which correspond to the station signals.

10. A watchman's unit according to claim 9 wherein said clock means includes

a multistage binary register

a means for setting the various stages of said register in accordance with a binary code representative of elapsed time,

and wherein said memory means includes a plurality of memory units, each having several binary code bit memory locations therein, each binary register stage being connected to a different one of said memory units.

11. A watchman's unit according to claim 9 wherein said address means comprises

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means for directing the outputs from said binary register stages to corresponding memory locations in said memory units in accordance with a station identification code.

12. A watchman's unit according to claim 9 wherein said memory is a digital bit storage device having at each of several bit locations a bit memory capable, when activated, of retaining bit information supplied thereto

and wherein said address means comprises decoding means for activating different ones of said bit storage devices according to said station signals.

13. A watchman's unit according to claim 9 wherein said station detector means comprises

a plurality of terminals and means for producing digital signals on various ones of said terminals in accordance with a binary digital representation of the identity of a station.

14. A watchman's unit according to claim 10 wherein the memory comprises

a plurality of memory units corresponding in number to the number of stages of said binary register, each unit being connected to receive the binary output of a different one of said stages,

and wherein said address means is operative to direct the binary outputs produced at a given time to corresponding locations in said memory units.

15. A watchman's unit according to claim 9 wherein each memory unit is a digital bit storage device having at each of several bit locations a bit memory capable, when activated, of retaining bit information supplied thereto.

16. A watchman's unit according to claim 1 wherein said memory means further includes

a second plurality of locations therein for storing station signals, each of said second plurality of locations corresponding to a different one of the first mentioned plurality of locations,

and wherein said address means is operative in response to the production of station signals to direct the station signals and the simultaneously produced time signals to corresponding ones of said second and first plurality of locations.

17. A watchman's unit according to claim 16 wherein said memory is a digital bit storage device

and wherein said clock means is operative to produce said time signals in binary coded digital form.

18. A watchman's unit according to claim 16 wherein said station detector means is operative to produce said station signals in binary coded digital form.

19. A watchman's unit according to claim 16 wherein said clock means comprises

an oscillator means for producing a continuous series of pulses,

and a multiple stage binary register for receiving and accumulating said pulse

and having plural outputs whose pattern of energization corresponds to the accumulated number of pulses therein.

20. A watchman's unit for recording the checking of stations by a watchman, said unit comprising,

memory means having a plurality of data input terminals for receiving digitally coded data and a plurality of address terminals for directing received data to different locations therein corresponding to received address signals,

time signal data producing means comprising pulse generator means for producing a continuous suc-

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cession of pulses and multiple stage digital register for accumulating said pulses and attaining different states in its various stages corresponding to the number of accumulated pulses,

means connecting the various stages of said register to said data input terminals of said memory means,

station signal identification means for producing digitally coded station identification signals corresponding to a station key when applied thereto,

and means directing said station identification signals to said address terminals of said memory means.

21. A watchman's unit according to claim 20 wherein said memory means has

a plurality of data output terminals for connection to a terminal board

and a plurality of address interrogation terminals for connection to a terminal board,

said data output terminals and said address interrogation terminals being connected to said memory

means in a manner such that interrogation signals applied in various patterns to said address interrogation terminals will cause said data output terminals to produce signals representative of the data in the memory locations corresponding to said patterns.

22. A watchman's unit for recording the checking of stations by a watchman, said unit comprising

memory means having a first plurality of data input terminals for receiving digitally coded time data

and a second plurality of data input terminals for receiving digitally coded station identification data,

time signal data producing means comprising pulse generator means for producing a continuous suc-

cession of pulses and a multiple stage digital register for accumulating said pulse and energizing a

plurality of time data terminals according to patterns representative of the number of accumulated

pulses, said time data terminals being connected to corresponding ones of said first plurality of data

input terminals,

station signal identification means for producing digitally coded station identification signals at a plural-

ity of station identification terminals with the pattern of said signals corresponding to the identity of

a station key applied to said unit said station identification terminals connected to corresponding ones

of said second plurality of data input terminals,

a common address means comprising a register having a plurality of output terminals, said register

being responsive to the application of a station key to said watchman's unit to change the pattern of

energization of its output terminals according to a predetermined sequence,

said output terminals each being connected to corresponding address terminals of said memory means,

said memory means being responsive to the application of address signals to said address terminals to

direct data at said first and second data input terminals to corresponding locations therein.

23. A watchman's unit according to claim 22 wherein said memory means comprises

a first signal storage unit having said first plurality of data input terminals and a first set of address terminals

and a second signal storage unit having said second plurality of data input terminals and a second set of

address terminals.

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and wherein said common address means output terminals are connected to corresponding ones of both said first and second sets of address terminals.

24. A security system comprising
a plurality of station connectors distributed about a premises to be checked,
at least one watchman's unit,
station identification signal producing means in said unit and operative to generate, in digital code format, station identification signals corresponding to the identification of different ones of said stations upon connection of said unit to said stations,

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clock means in said watchman's unit for generating in digital code format time data signals representative of elapsed time from a given point in time,
correlation means and memory means in said watchman's unit to record therein, in correlated arrangement, the digitally coded station identification and time data signals produced when said unit is connected to one of said station connectors,
and computer terminal means operative when connected to a watchman's unit, to read out the signals stored therein.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 3,922,649
DATED : November 25, 1975
INVENTOR(S) : Richard J. Thome

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

- Column 6, line 35 - After the words "of the", delete [terminal] and in its place insert second.
- Column 9, line 6 - After the word "output", delete [terminals] and in its place insert terminal.
- Column 13, line 36 - After the word "bit", delete [selection] and in its place insert select.
- Column 14, lines 25 & 27 - The word "SYNCH" should be set off in quotation marks.
- Column 14, lines 66, 67 & 68 - The words "START" and "SYNCH" should be set off in quotation marks.
- Column 15, lines 15 & 20 - The words "STOP", "SYNCH" and "WRITE PULSE" should be set off in quotation marks.
- Column 16, line 59 - Delete the "a" appearing at the beginning of the line and insert "and".
- Column 18, line 1 - After the word "and", insert "a".
- Column 18, line 36 - Delete the word [pulse] and insert in its place pulses.

Signed and Sealed this

first Day of June 1976

[SEAL]

Attest:

RUTH C. MASON
Attesting Officer

C. MARSHALL DANN
Commissioner of Patents and Trademarks