United States
Luce

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[54] **DECODER AND DRIVER CIRCUITS PARTICULARLY ADAPTED FOR USE WITH LIQUID CRYSTAL DISPLAYS**

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[73] Assignee: **Optel Corporation,** Middlesex, N.J.

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[52] **U.S. Cl.** ..... **340/336,** 350/160 LC
[51] **Int. Cl.** **G09f 9/30**
[58] **Field of Search** ... 340/324 R, 336, 334, 324 M; 350/160 LC

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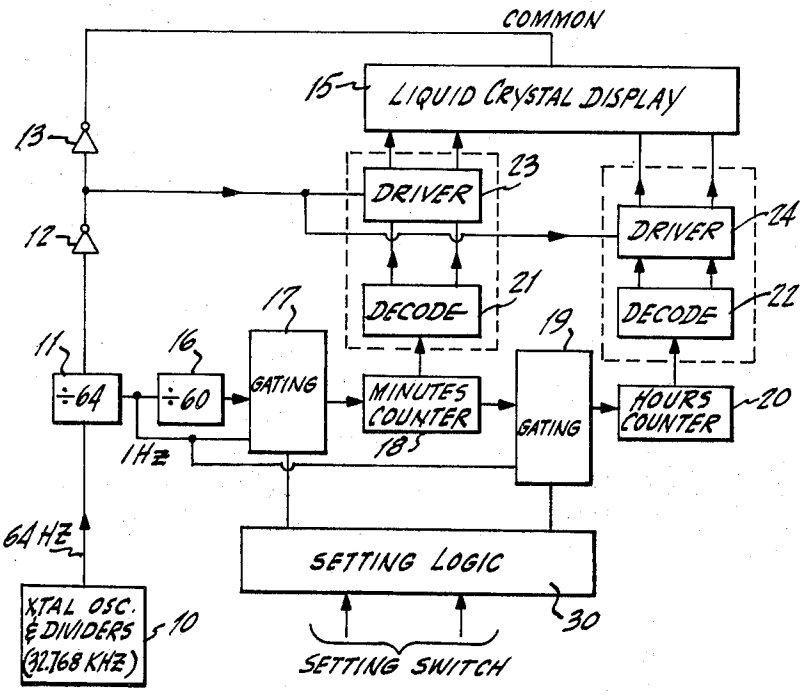
[57] **ABSTRACT**

A decoder-driver network for energizing a liquid crystal display used in a timepiece to cause the same to provide any one of a plurality of presentations according to any one of a number of coded formats. The decoder-driver circuit uses bidirectional devices arranged in series paths to minimize components and increase reliability.

10 Claims, 5 Drawing Figures



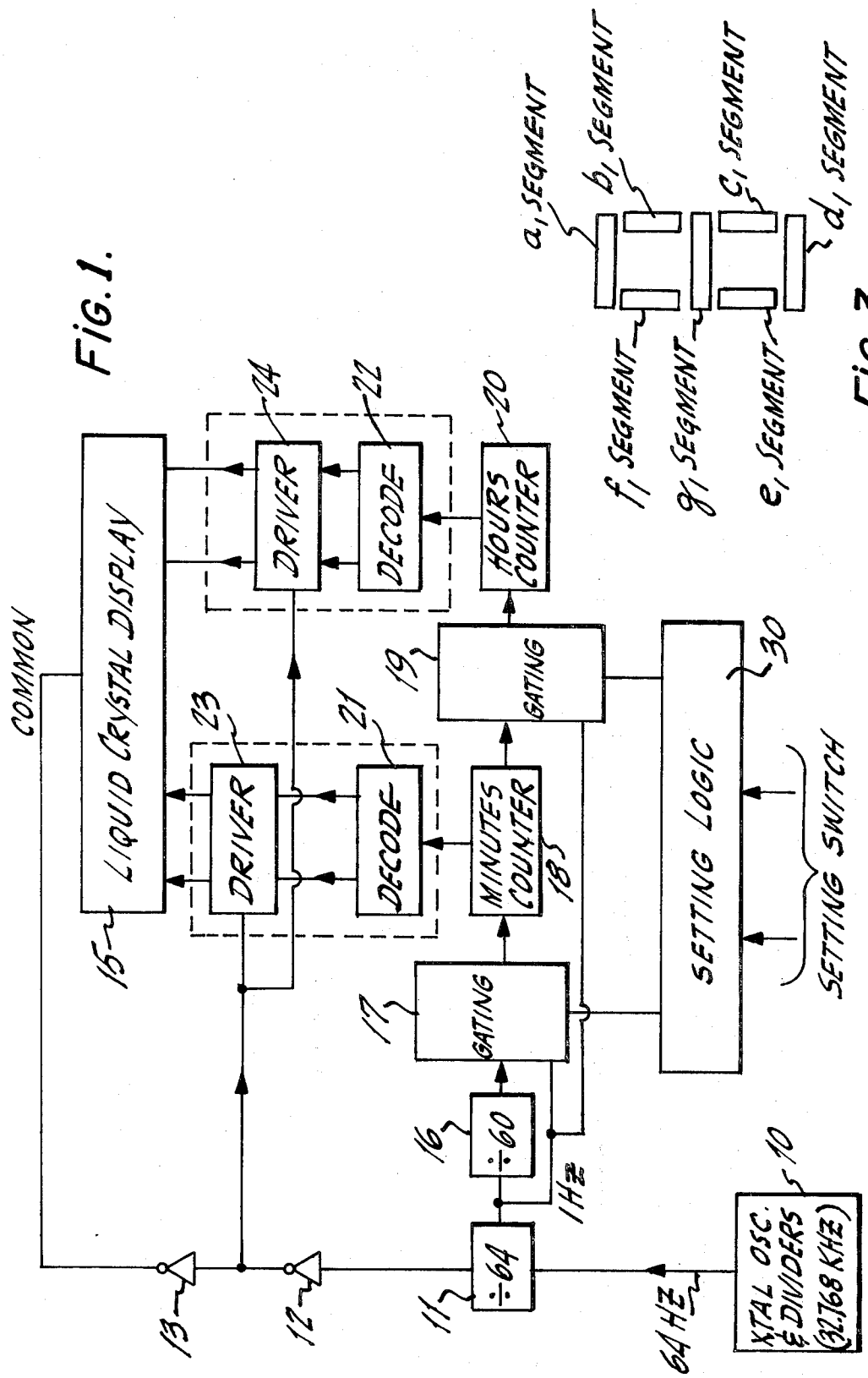

XTAL OSC. & DIVIDERS (32.768 KHZ)
10
64 HZ
÷64
11
÷60
16
1HZ
GATING
17
MINUTES COUNTER
18
GATING
19
HOURS COUNTER
20
DECODE
21
DRIVER
23
DECODE
22
DRIVER
24
LIQUID CRYSTAL DISPLAY
15
COMMON
12
13
SETTING LOGIC
30
SETTING SWITCH

Fig. 1.

a, SEGMENT
b, SEGMENT
c, SEGMENT
d, SEGMENT
f, SEGMENT
g, SEGMENT
e, SEGMENT

Fig. 3.

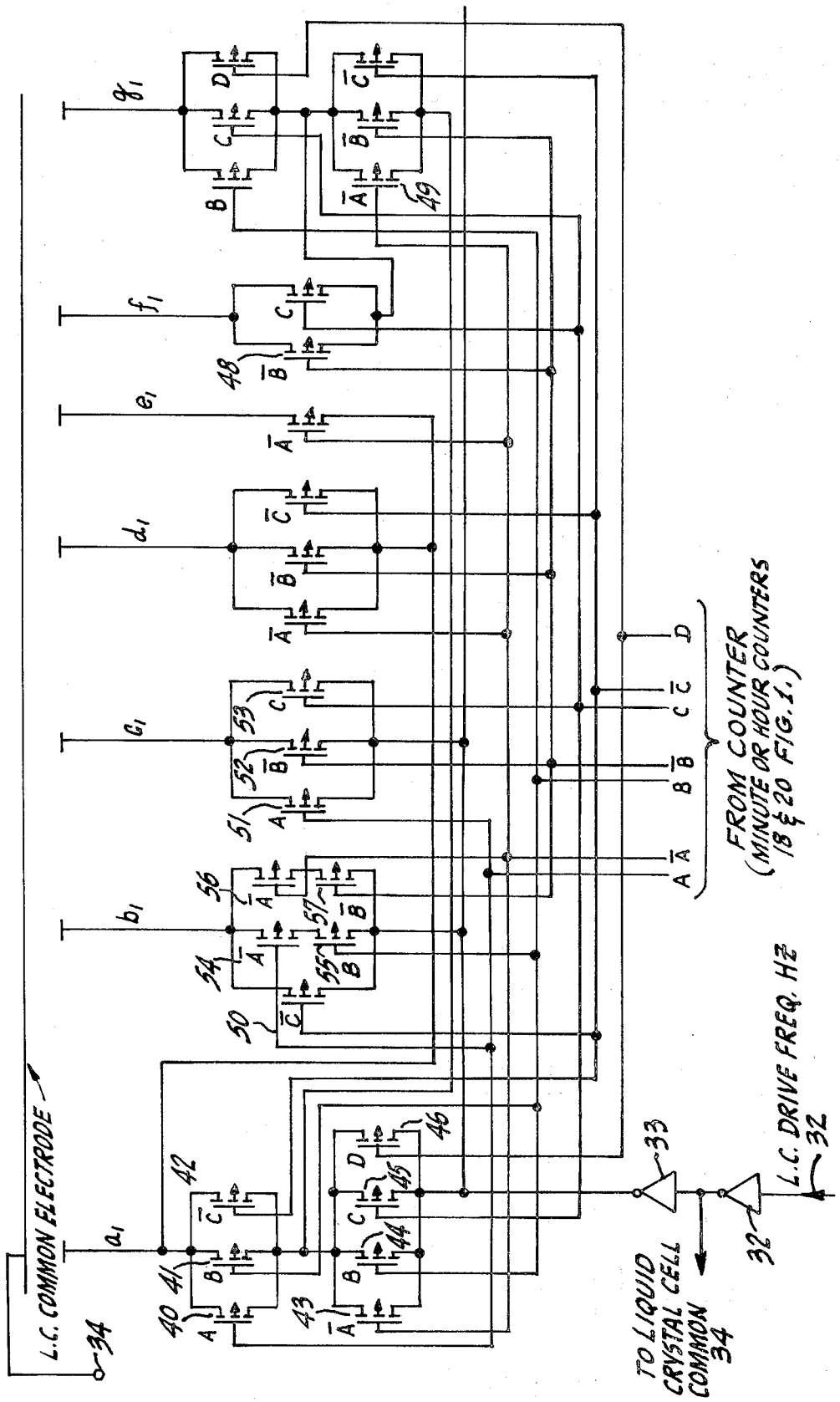

L.C. COMMON ELECTRODE
34
FROM COUNTER
(MINUTE OR HOUR COUNTERS
18 & 20 FIG. 1.)
TO LIQUID
CRYSTAL CELL
COMMON
34
L.C. DRIVE FREQ. HZ
32

Fig. 2.

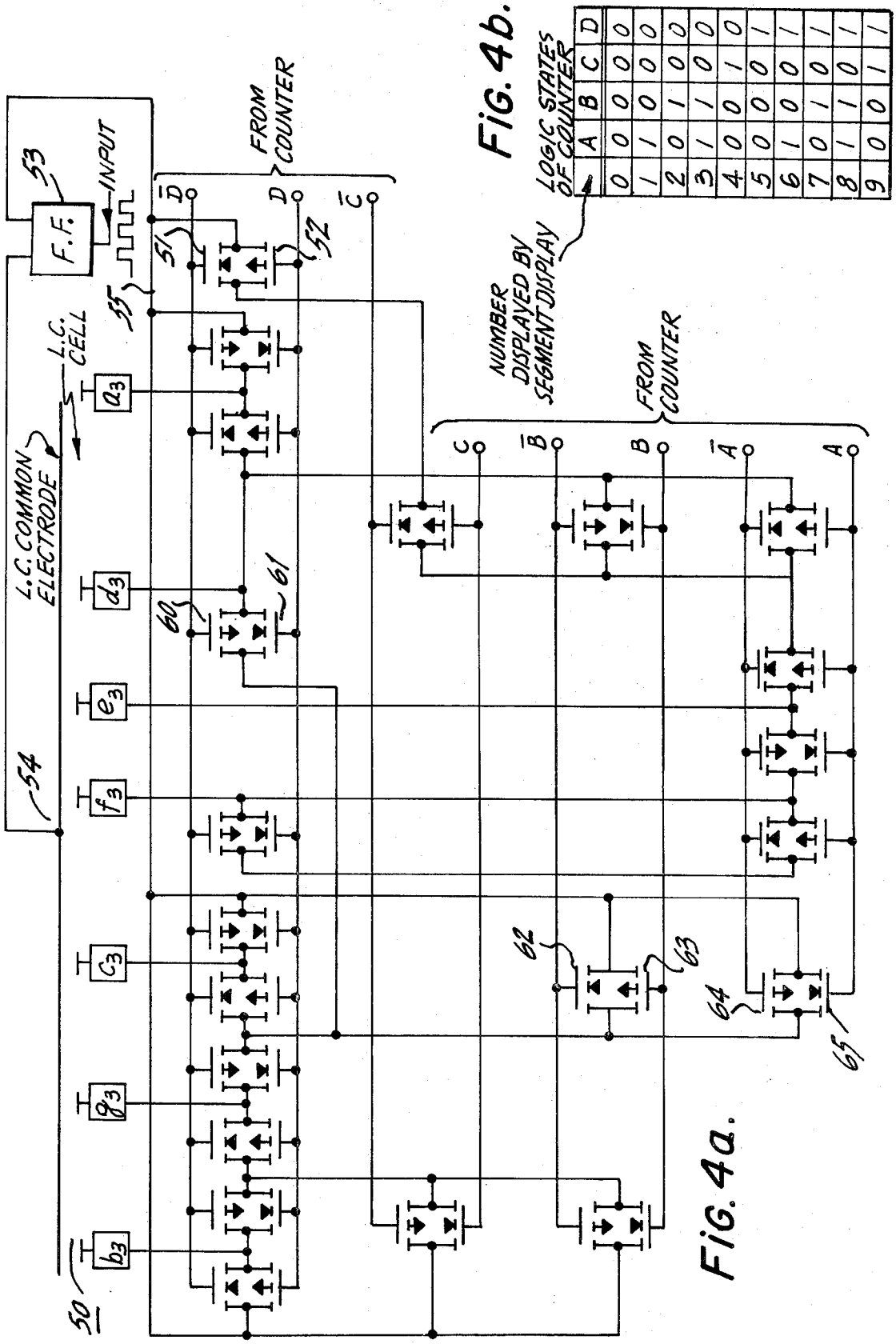

F.F.
53
INPUT
FROM COUNTER
L.C. CELL
L.C. COMMON ELECTRODE
NUMBER DISPLAYED BY SEGMENT DISPLAY
LOGIC STATES OF COUNTER
A B C D
0 0 0 0 0
1 1 0 0 0
2 0 1 0 0
3 1 1 0 0
4 0 0 1 0
5 0 0 0 1
6 1 0 0 1
7 0 1 0 1
8 1 1 0 1
9 0 0 1 1
50
51
52
54
55
60
61
62
63
64
65

Fig. 4b.

Fig. 4a.

DECODER AND DRIVER CIRCUITS PARTICULARLY ADAPTED FOR USE WITH LIQUID CRYSTAL DISPLAYS

This invention relates to decoding and driving circuitry and more particularly to such circuitry for utilization with liquid crystal displays.

BACKGROUND OF INVENTION

Recently, liquid crystal displays in conjunction with integrated circuits have been widely utilized as a valuable combination in digital equipment. Such combined devices especially offer great advantages in the field of timepieces. For example, the digital electronic wrist watch is now a reality. As is well known certain watches which are electronic in nature are available to the consumer. The design and fabrication of a wrist watch using a liquid crystal display and suitable integrated circuitry has been discussed in various articles and other prior art. In any event, in any consumer product there is a desire to build as a reliable device as possible, while maintaining an economical product.

In regard to any electronic product a portion of the cost is directed towards the amount of circuitry utilized and the complexity of the circuitry. Basically, it is safe to say that as the complexity of the circuitry decreases and as the number of components decreases so does the cost. A decreasing component number is further evidenced by an overall increase in the reliability of the product.

Due to the nature of operation of an electronic timepiece one desires a relatively stable oscillator. Such an oscillator may utilize a crystal device which can provide a frequency stability within a few parts per million per year. In general, the higher the frequency of the oscillator the more accurate the timekeeping of the watch will be.

Naturally there is a trade-off in regard to cost in determining the frequency. In any event, the frequency of the oscillator is much higher than the normal repetition rates which are utilized in present timepieces. The output frequency of the oscillator must be divided down in order to produce a pulse train of a 1 Hz. rate to provide the timekeeping function. Again for economical reasons, one must utilize cascaded counters. These counters of course operate according to binary formats. The outputs eventually have to be decoded in order to drive a suitable display. Due to such considerations an integral part of such a timepiece must be a decoding matrix whose function is to convert the counter outputs into suitable signals for driving a display. Usually such a decoder has to be isolated from the display elements, or additional power is necessary to drive the display elements. This therefore requires driver circuitry, which circuitry exists separate and apart from the decoding circuitry. As indicated above, it is desirable to reduce the amount of circuitry in order to reduce cost and increase reliability.

It is therefore an object of the present invention to provide novel decoder and driver circuits which can be used to directly operate a display, and particularly adapted as a decoder-driver for a liquid crystal display utilizing common circuit components.

DESCRIPTION OF PREFERRED EMBODIMENT

A decoder driving apparatus to be used in conjunction with a display, said display being of the type including a first common electrode and a plurality of display electrodes, the electrodes being adapted to be activated by a source of bidirectional potential having first and second terminals for being connected across a display with said first terminal connected to said common electrode of said display and said second terminal connected to any desired one of said plurality of display electrodes, said display capable of indicating a different one of a plurality of presentations according to which of said display electrodes are connected to said second terminal of said source, the decoder driver apparatus comprising a plurality of bidirectional active devices each having an input, output and common electrode, means for coupling a first plurality of said devices in a series path between one of said display electrodes and a circuit terminal adapted to be coupled to said second terminal of said source of energizing potential, and means coupled to said input electrodes of said first plurality of devices to cause a low impedance path to appear between said output and common electrodes of said active devices, to cause said series path to provide a low impedance return path to said second terminal thereby activating said display electrode.

BRIEF DESCRIPTION OF DRAWINGS

FIG. **1** is a block diagram of an electronic timepiece useful in explaining the operation of this invention.

FIG. **2** is a circuit schematic of a decoder driver network according to this invention using bidirectional field effect devices.

FIG. **3** is a front plan presentation of a seven segment display useful in explaining the operation of this invention.

FIG. **4a** is a detailed schematic diagram of an alternate embodiment of a decoder driver circuit according to this invention employing complimentary symmetry devices.

FIG. **4*b*** is a table showing outputs states of the counter for application to the decoder.

DETAILED DESCRIPTION OF FIGURES

Referring to FIG. **1** there is shown a block diagram of a digital timepiece. Numeral **10** references a crystal oscillator and divider module. For purposes of explaining the operation of the system let us assume that the crystal oscillator operates at a frequency of 32,768 Hz. Therefore, in order to obtain an output frequency of, for example, 64 Hz. one would have to divide the above noted frequency by 512. It is also noted that 512 is a binary number and therefore the dividing chain incorporated in module **10** can consist of a conventional binary counter comprising a plurality of cascaded bistable multivibrators. Such counting stages exist either in the form of monolithic integrated circuits or as MOS devices and are easily obtainable and readily available.

The output of the counter is a signal having a repetition rate of 64 Hz. This is applied to another divider **11** which divides the 64 Hz. signal by a factor of **64** to obtain at an output thereof a 1 Hz. signal. This of course is indicative of seconds and can be utilized in conjunction with additional circuitry to perform timekeeping. A 32 Hz. signal is also provided in counter **11** and is applied via inverters **12** and **13** to a common terminal of a segmented liquid crystal display **15.** Basically, the liquid crystal and the principles of operation of the same

have been discussed in detail in various papers. However, a brief description will be given.

Nematic liquid crystals are organic materials made up of rod-like molecules. The term liquid is utilized because of the physical characteristics of the material. These materials are capable of being poured while further possessing the optical properties of a crystalline solid. The nematic materials are temperature sensitive. Accordingly, at low temperatures the material is a solid and at high temperatures it is an isotropic liquid. The transitiitions to the isotropic state are sharp, reversable and reproduceable. Liquid crystal display **15** can be fabricated to operate according to the principles of dynamic scattering. A basic liquid crystal cell consists of a liquid crystal material sandwiched between two pieces of transparent conductive coated glass. The liquid crystal molecules are highly birefringent and are in an ordered structure. The operation is relatively simple. With no voltage applied across the glass plates the cell is transparent. When a voltage is applied a resultant current causes turbulence which is a disruption of the ordered structure. This disruption causes the cell to appear milky white, and hence light reflective. The change in appearance is due to light scattering caused by changes in the index of refraction in the material about the region of disruption. In order to utilize a liquid crystal display in a timepiece the following characteristics are desirable:

1. Must be capable of operating at relatively low power;
2. Have a relatively long life;
3. Have an attractive physical appearance;
4. Be capable of operating for wide temperature ranges.

Liquid crystals in general are sensitive to both moisture and oxygen and in order to accomplish long life the liquid crystal material is preferably packaged in a hermetically sealed unit. Such materials have been developed and are presently available. The liquid crystal display **15** as indicated is segmented. The display has one common terminal and a plurality of segmented terminals in order to provide the requisite number of digits for displaying time. For example, the display may be a seven segment 3½ digit unit with a colon. The digits should be relatively small and still present good overall appearance. To achieve this a display which is approximately .123 inch by .184 inch is available with an active display length of .8 inch. The display can operate at 15 volts and has a nominal power dissipation of 15 microwatts with a contrast ratio that is greater than 10 to one. Such displays are available from Optel Corporation, Princeton, New Jersey, the assignee herein.

As will be described subsequently the common terminal of the liquid crystal display **15** is driven via a flip-flop stage in divider **64** via inverters **12** and **13** at a frequency of 32 Hz. The one cycle output from divider **11** is applied to a divider **16** which performs a division by 60 to obtain at the output of divider **16** a pulse train having a repetition rate of 1/60 a second. The 1 Hz. signal is applied to a gating circuit **17** which receives the 1 Hz. signal and the 1/60th Hz. signal to provide at an output a signal indicative of minutes. This signal is applied to a minutes counter **18** which advances its count by one for each pulse applied via a gating circuit **17.** The output of the minutes counter is applied to a gating circuit **19** which also receives the 1 Hz. signal. The gating circuit **19** produces a pulse for every 60 pulses accumulated by the minutes counter **18.** This output pulse is of course synchronous to the 1 Hz. signal. Therefore, the output of the gating circuit **19** consists of one pulse per hour and this pulse is applied to an hours counter **20.** As previously indicated both the minute counter and the hour counter are digital devices and operate according to a binary or binary coded decimal format. Hence, these binary formats have to be decoded to provide compatability with normal time indications.

There is shown a decoder **21** and a decoder **22** each respectively associated with the minutes counter **18** and the hours counter **20.** The outputs of these decoders **21** and **22** are applied to respective driver circuits **23** and **24** which are in turn coupled to the segment electrodes of the liquid crystal display **15** in order to provide a proper digital display. As seen from FIG. **1** a conventional approach would be to use a separate decoder module such as **21** and **22** to drive a separate driver circuit such as **23** and **24.** The dashed lines surrounding the two modules are included to indicate the structure to be covered by this invention. This structure namely is a combined decoder-driver assembly useful to reduce the number of components and circuit complexity, therefore achieving an increased reliability of the final timepiece.

Numeral **30** represents setting logic circuitry which basically is used to set the timepiece for different times or for initial adjustment. The function of the setting logic **30** is to apply higher frequency pulses to the minute and hour counters **18** and **20** in order to provide easy setability without using excessive time.

Referring to FIG. **2** there is shown a decoder driver circuit according to this invention utilizing P channel MOS devices. Reference numerals **32** and **33** represent two inverting circuits which may be ordinary amplifiers or operational devices which in essence serve to invert the polarity of the liquid crystal drive signal which, as indicated in FIG. **1,** is 32 Hz. The output of inverter **32** is coupled to the liquid crystal common electrode **34,** while the output of inverter **33** is applied to the MOS decoding and driver circuitry. The MOS devices shown are P channel devices. The liquid crystal display **15** requires an alternating current driving source and hence the P channel devices are bidirectional switches. The outputs of the circuits as will be explained are connected to the appropriate segments of the display each separately indicated as a_1, b_1, c_1, d_1, e_1, f_1 and g_1. These circuits serve to swtich between the common electrode **34** and the various segments in a bidirectional manner. When a P channel switch device is turned on the current flows through the liquid crystal in one direction for one half cycle and the reverse direction for the other half cycle. Since the P channel device is symmetrical there is relatively little DC offset on the display. In any of these bidirectional switching circuits one desires to have the leakage current of the switch in the off state as small as possible because of the relatively high impedance associated with the display segments. Such P channel devices can be designed to have leakage currents of 10 nanoamps or less for relatively large temperature variations and hence more than adequately serve to perform the necessary switching. If the leakage current of the P channel device becomes a problem, one can further assure reliable operation by shunting the device with another device by applying approxi-

mately phased signals from a driving source to assure adequate on-off display operation.

The circuit operates as follows: The outputs from a binary or other coded counter are applied to the terminals designated as A, $\overline{A}$, B, $\overline{B}$, C, $\overline{C}$, and D. Segments as a_1 to g_1 are represented by their own binary code. Assume that the a_1 segment of the liquid crystal display is to be activated. As can be seen this segment terminal a_1 is coupled to the MOS devices **40, 41** and **42.** These devices have their output terminals connection in shunt. Since each device **40, 41** and **42** is symmetrical the conventional drain and source electrodes can be interchanged. As indicated the gate electrodes of devices **40, 41** and **42** are respectively connected to the inputs A, B, and $\overline{C}$ from the binary type counter. The upper common electrode of the three devices is coupled directly to the segmented electrode a_1 while the bottom common electrode is coupled to the common electrode connection of the P channel devices **43, 44, 45** and **46.** The other common electrode of these devices being coupled directly to the inverted **32** Hz. drive frequency available at the output of inverter **33.** Assume now that the counter provides a count where the A and B leads are at a logical one. Further assume that the $\overline{C}$ lead is also at logical one indicating a logical zero for C and further assume that the D signal is also logical zero. In this manner the MOS devices **40, 41** and **42** are on or exhibit a low impedance bidirectional path between their common electrodes. It is also noted that device **44** is also on due to the fact that its gate is also coupled to the B output of the counter. This therefore provides a current return path between the a_1 segment and the output terminal of inverter amplifier **33.** It is also noted that device **44** is in cascode with devices **40, 41** and **42.** Hence, the cascode configuration permits higher voltage drive and serves to allow the sharing of dissipation between the devices, therefore reducing the normal power dissipation in any one device. This cascode configuration thereby permits the segment designated as a_1 to be energized. The path is through the P channel devices **40, 41** and **42** and device **44.**

The common electrode of the liquid crystal receives a 34 Hz. clock at one phase and the a_1 segment receives a 34 Hz. at opposite polarity via the above noted P channel devices. The clock alternates polarity every half cycle, but since the devices are symmetrical, they conduct for either polarity and hence maintain the a_1 segment of the liquid crystal display activated.

Referring to FIG. **3** there is shown a seven segment display arrangement of a similar format to that utilized in conjunction with the liquid crystal display herein. Each segment has been designed according to the format specified in FIG. **2.** For example for the above description, the a_1 segment of the display shown in FIG. **3** would be energized by the circuit of FIG. **2.**

The tabulation below indicates the segments which are activated according to the states of the counter respectively designated as A, $\overline{A}$, B, $\overline{B}$, C, $\overline{C}$, and D.

LIQUID CRYSTAL DISPLAY SEGMENT ACTIVATION

SEGMENTS	D	C	B	A	$\overline{C}$	$\overline{B}$	$\overline{A}$
$a_1, b_1, c_1, d_1, e_1, f_1$	0	0	0	0	1	1	1
b_1, c_1	0	0	0	1	1	1	0
a_1, b_1, d_1, e_1, g_1	0	0	1	0	1	0	1
a_1, b_1, c_1, d_1, g_1	0	0	1	1	1	0	0
b_1, c_1, f_1, g_1	0	1	0	0	0	1	1
a_1, c_1, d_1, f_1, g_1	0	1	0	1	0	1	0
$a_1, c_1, d_1, e_1, f_1, g_1$	0	1	1	0	0	0	1
a_1, b_1, c_1	0	1	1	1	0	0	0
$a_1, b_1, c_1, d_1, e_1, f_1, g_1$	1	0	0	0	1	1	1
$a_1, b_1, c_1, d_1, f_1, g_1$	1	0	0	1	1	1	0
This State Not Permitted by Counter	1	0	1	0	1	0	1
do.	1	0	1	1	1	0	0
do.	1	1	0	0	0	1	1
do.	1	1	0	1	0	1	0
do.	1	1	1	0	0	0	1
do.	1	1	1	1	0	0	0

From the above table it can be seen that all digits from 0 through 9 can be displayed by the segmented configuration of FIG. **3.**

While there are 16 possible states evidenced by a four stage counter, it is well known to confine the count to ten, and to eliminate the counts representative of 11 to 16 or binary 1010 to 1111.

It can also be seen from the above tabulation that in the majority of instances the return current path for each segment is through a series path provided by more than one P channel device.

For example, segment f_1 may be activated via P channel device **48** and thence through P channel device **49,** and then through P channel device **43, 44, 45** or **46.** This, of course, specifies at least three devices in cascode, providing the above described advantages in voltage breakdown and power sharing.

The only instances where this does not actually hold true involve segments b_1 and c_1. However, this is no problem as one can design the four P channel devices **50, 51, 52** and **53** with this operation in mind, as these devices are only four out of 27. In any event, the output of inverter **33** can be fabricated as a P channel device which would appear in cascode with all devices in the above described decoder-driver circuit.

In this manner the circuit of FIG. **2** can be used as both the decoder matrix for the counter and the driver circuit for the segments. The series parallel configuration serving to greatly reduce device tolerance and breakdown ratings in regard to both current and voltage. For example, even in regard to devices **50, 51** and **52,** there are conditions where device **51** conducts indicative of $\overline{C}$ and this is shunted by devices **54** and **55;** or the only time device **50** is solely conducting is for the conditions when A and B are not both at logical one or $\overline{A}$ and $\overline{B}$ are not both at logical one. At all other times the $\overline{C}$ condition assures that device **50** is shunted by at

least one additional path, thus serving to share current. The same conditions are applicable to devices **51, 52** and **53.**

Referring to FIG. **4** there is shown a decoder-driver arrangement using complimentary MOS devices or a CMOS configuration.

Due to the fact that the liquid crystal display **50** requires an AC driving source, as previously indicated, bidirectional switches are necessary.

This decoder driver comprises a plurality of paired field effect transistors as **51** and **52.** The devices **51** and **52** are respectively a N channel device and a P channel device, connected in shunt. The plurality of devices are activated by the outputs of a counter (four stage) indicated by the A, $\overline{A}$, B, $\overline{B}$, C, $\overline{C}$, and D, $\overline{D}$ inputs.

A flip-flop or bistable multivibrator **53** is shown. The input of the flip-flop **53** is coupled to a source of pulses such as may be derived from the divider **11** of FIG. **1.** Since a bistable performs a division of two, one may use the 64 Hz. signal directly as a trigger to then obtain 32 Hz. opposite polarity output signals at the two output electrodes of the flip-flop **53.** One output terminal of the flip-flop **53** is connected to the common terminal **54** of the liquid crystal display **50.** The other output terminal of the flip-flop **53** is connected to a drive line **55** associated with the decoder-driver array.

The liquid crystal display **50** is again a seven segment display, wherein the segment electrodes are respectively designated as a_3, b_3, c_3, d_3, e_3, f_3 and g_3. Each of these segment electrodes is connected to a designated point in the decoder-driver matrix and are activated according to a decoding format, similar to that used in conjunction with FIG. **2,** and as shown from the logic table of FIG. **4.**

It can be seen from FIG. **4** that each pair of field effect transistors as **51** and **52** have their gate electrodes returned to opposite sides of a counter flip-flop output. For example the gate electrode of transistor **51** is coupled to the $\overline{D}$ output of the counter circuit, while the gate electrode of transistor **52** is coupled to the D output of the counter. Hence, when D is one and $\overline{D}$ is zero, transistors **51** and **52** are both conducting. The P channel device will conduct on the negative clock cycle, while the N channel device conducts on the positive half clock cycle. Since the transistors are designed to be symmetrical, there is no apparent DC offset on the display.

In a similar manner each count obtained from the counter is represented by a unique activation of a seven segment display, as previously described. There are also multiple series paths provided in the operation of this decoder driver matrix and thus the advantages of power sharing occur in this configuration as well.

The decoder-driver network serves to provide a bidirectional current return path from the liquid crystal common electrode **54** to the network common electrode **55.**

Let us assume that it is desired to access the d_3 segment of the display for the following condition of the counter, $A = 1$, $\overline{A} = 0$, $B = 1$, $\overline{B} = 0$, $C = 0$, $\overline{C} = 1$, and $D = 0$, $\overline{D} = 1$. Proceeding with the D and $\overline{D}$ input lines from the counter, it is seen that transistors **60** and **61** are both activated. This is due to the gate electrode of transistor **60** connected to the $\overline{D}$ line which is at one, and the gate electrode of transistor **61** connected to the D line which is at zero. Hence, there is a first bidirectional path from d_3 via transistors **60** and **61.**

Transistors **62** and **63** are also activated because $\overline{B}$ is at zero and B is at one. Thus, there is a second low impedance path via transistors **62** and **63** to the common return line **55.** Hence, segment d_3 is activated.

It can also be seen that because A is logical one, and $\overline{A}$ is zero transistors **64** and **65** are both biased off, thereby blocking this path to common. But if A was zero and $\overline{A}$ was one, these transistors **64** and **65** would also provide a return for the d_3 segment even if B was at zero.

It is of course understood that the counter inputs can accommodate a number of useful counting formats, such as divide by 12, 10, six, five, two and so on. They can be straight binary devices or binary coded devices. The important factor being that a different number of display segments be activated for each unique count to enable proper time display.

Such counting arrangements are well known in the art, as is the formation of truth tables to enable proper decoding.

The novel aspects of this invention residing in the unique presentation of decoder driver circuits to networks to enable dual operation.

I claim:

1. Apparatus used for driving a display, said display being of the type including a first common electrode and a plurality of display electrodes, said display adapted to be activated by a source of bidirectional potential having first and second terminals for being connected across said display with said first terminal connected to said common electrode of said display, said display capable of indicating any different one of a plurality of presentations according to which of said display electrodes are connected to said second terminal of said source, in combination therewith apparatus for selectively connecting said second terminal to any desired ones of said display electrodes, comprising:

a. a plurality of bidirectional field effect transistors each having a source electrode, a drain electrode and a gate electrode, said field effect devices operative in a first state to provide a low impedance bidirectional current conducting path between said source and drain electrodes when said gate electrode is biased by a first operating potential and in a second state to provide a high impedance between said source and drain electrode when said gate is biased by a second operating potential,

b. means for coupling said second terminal of said source to any desired one of said display electrodes including a series path formed by at least two of said field effect transistors having the source electrode of one directly connected to said desired one of said display electrodes and the drain electrode of said one directly connected to the source electrode of said other, with the drain electrode of said other directly connected to said second terminal of said source,

c. a code generator capable of providing a series of codes each manifesting a different indication capable of selecting a different display presentation, said codes defined by two potential levels which correspond to either said first operating or said second operating potential dependent upon the code provided, said code generator having a plurality of output terminals each providing either of said operating potentials dependent upon said code provided, and

d. means coupling a predetermined one of said output terminals of said code generator to said gate electrode of said one transistor and another predetermined one of said output terminals to said gate electrode of said other transistor, whereby when said code generator is providing said first operating potential at said predetermined output terminals, said display electrode is connected to said second terminal of said source through said low impedance path provided by said at least two field effect transistors both operating in said first state and to provide said high impedance path between said display electrode and said second source terminal when either of said predetermined code generator output terminals is providing said second operating potential.

2. The apparatus according to claim **1** wherein said display comprises a liquid crystal display having a first common electrode and a plurality of segment electrodes.

3. The apparatus according to claim **1** wherein said plurality of bidirectional field effect transistors are a plurality of MOS devices each having a drain output electrode, a source common electrode and a gate input electrode and fabricated for bidirectional conduction between said source and drain electrodes.

4. The apparatus according to claim **1** wherein each of said plurality of transistors includes a first N channel MOS device and a second P channel MOS device each having a common connected source electrode and a common connected drain electrode, respectively corresponding to said common and output electrodes, with a separate gate input electrode, associated with each of said devices.

5. In a liquid crystal display of the type having a common electrode and a series of segment electrodes, said display adapted to be energized by a source of bidirectional potential, said source having a first terminal connected to said common electrode and a second terminal to be connected to any desired one of said segment electrodes, in combination therewith apparatus for selectively connecting said second terminal of said source to a desired one of said segment electrodes, according to a predetermined code format, comprising:

a. a plurality of bidirectional field effect transistor devices, each having a gate input electrode, a source electrode and a drain electrode, and operative to provide in a first operating mode a low impedance bidirectional path between said source and drain electrode upon application of a first biasing potential to said gate electrode, and operative in a second mode presenting a high impedance between said source and drain electrodes upon application of a second biasing potential to said gate electrode,

b. means for coupling at least two of said plurality of devices in a series path between a selected one of said segments and said second terminal of said bidirectional potential source, said remaining devices of said plurality being coupled in a similar series path between said other segments, each of said paths including at least two of said devices arranged with the source electrode of one of said devices connected to said selected segment, the drain of said device connected to the source of the other device and said drain of said other device connected to said second terminal of said bidirectional source,

c. code generating means having a number of individual output terminals, each terminal capable of providing a first state corresponding to said first biasing potential a second state corresponding to said second biasing potential, and

d. means coupling said gate electrode of said one device to a selected one of said output terminals and said gate electrode of said other device to another one of said output terminals, whereby each device has coupled to the associated gate electrode one of said output terminals of said code generating means, whereby when said code generating means is providing said first biasing potential, said selected segment is connected to said second terminal of said bidirectional source through said series low impedance path and when one of said output terminals of said code generating means is providing said second biasing potential, said selected segment is isolated from said second terminal of said bidirectional source by said high impedance.

6. The apparatus according to claim **5,** wherein said plurality of bidirectional devices comprises a plurality of MOS devices each having an output drain electrode, a common source electrode and an input gate electrode.

7. The apparatus according to claim **6,** wherein said plurality of MOS devices are P channel MOS devices.

8. The apparatus according to claim **5,** wherein said code generating means comprises a binary counting chain.

9. The apparatus according to claim **5** wherein said liquid crystal display has seven of said segment electrodes and one common electrode.

10. In a liquid crystal display of the type having a common electrode and a series of segment electrodes, said display adapted to be energized by a source of AC potential connected between said common electrode and any selected one of said segment electrodes, in combination therewith apparatus for selectively activating any segment according to a predetermined code format comprising:

a. a plurality of MOS devices each having a gate, source and drain electrode, and operative to provide a low impedance bidirectional current conducting path between said source and drain electrodes, when said gate electrode is biased by a suitable operating potential, said devices arranged in a plurality of current conducting series path with at least a source electrode of a first MOS device connected to a drain electrode of another MOS device and said source electrode of said other connected to a drain electrode of a last MOS device, said series path formed between said segment electrodes and a suitable terminal associated with said source of AC potential, to provide a series of paths enabling a selected plurality of said segment electrodes to be connected to said source upon activation of said gate electrodes of said MOS devices;

b. a code generator capable of providing a series of codes each manifesting a different indication capable of selecting a plurality of different segment connections to said source of AC potential; and

c. means coupling certain preselected ones of said gate electrodes of said MOS devices to said code generator to cause certain of said series paths to provide said low impedance bidirectional paths for each one of said series of codes.

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